1.25 GHZ FULLY INTEGRATED DC-DC CONVERTER USING ELECTROMAGNETICALLY COUPLED CLASS-D LC OSCILLATORS

[Ph.D student update Work presented at ISSCC 2021]

Alessandro Novello
Ph.D Student at ETH Zurich

alessandro.novello@iis.ee.ethz.ch

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About Alessandro Novello

ETH zürich

1. 2016, B.S degree in electronic engineering from Polytechnic University of Turin

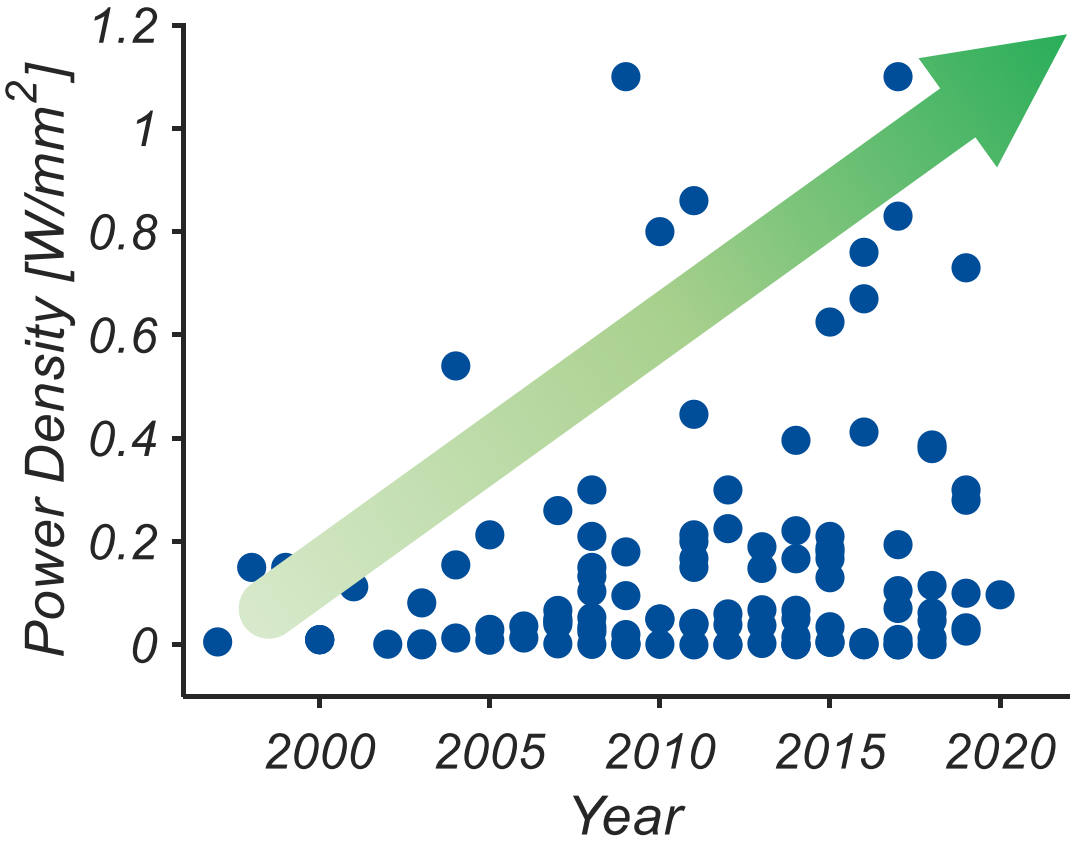
2. 2018, M.S degrees in Micro and Nanotechnologies for Integrated Systems (EPFL/Poly Torino/INP Grenoble)

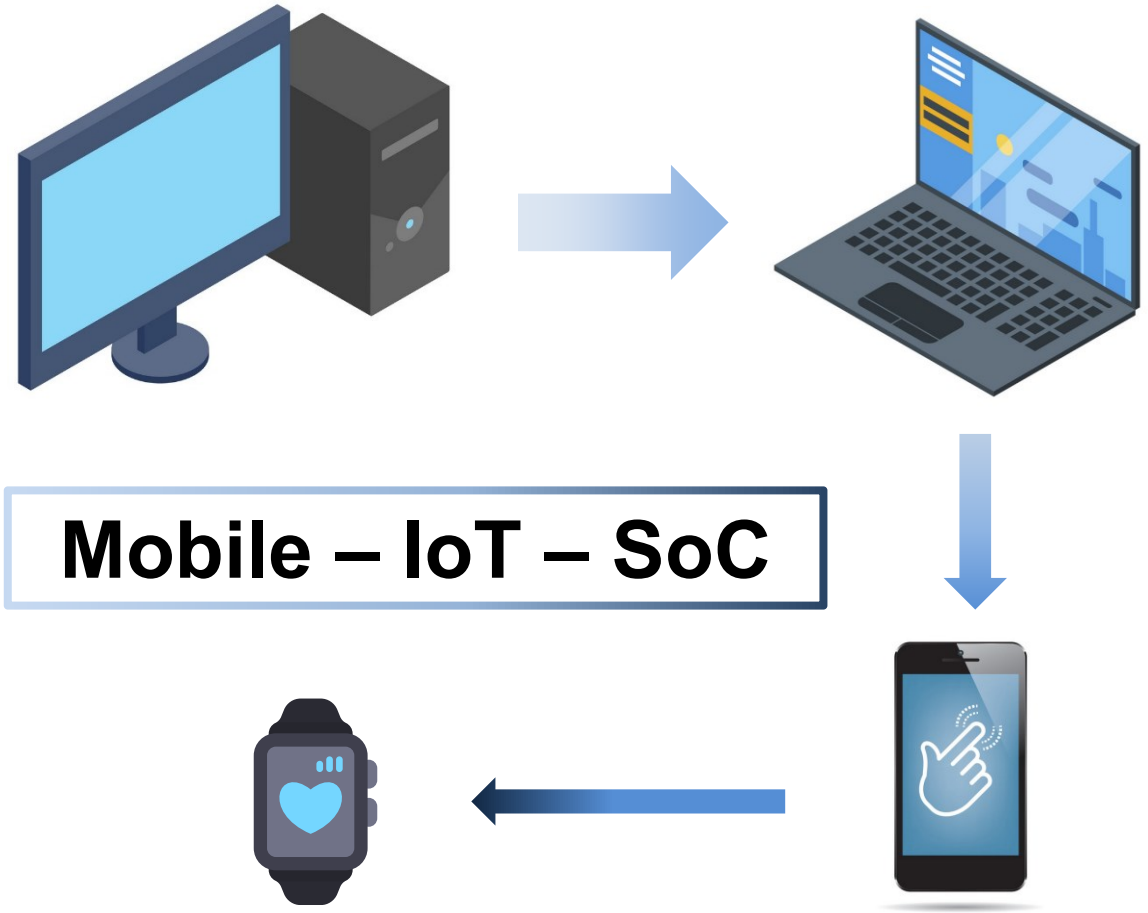
3. Currently pursuing Ph.D in the Energy Efficient Circuits and IoT Systems at ETH. Main research interests include Power Management IC design and Energy Harvesting circuits for ultra-low power

4. Distinguished contribution to SSCs conferences in 2020 and 2021

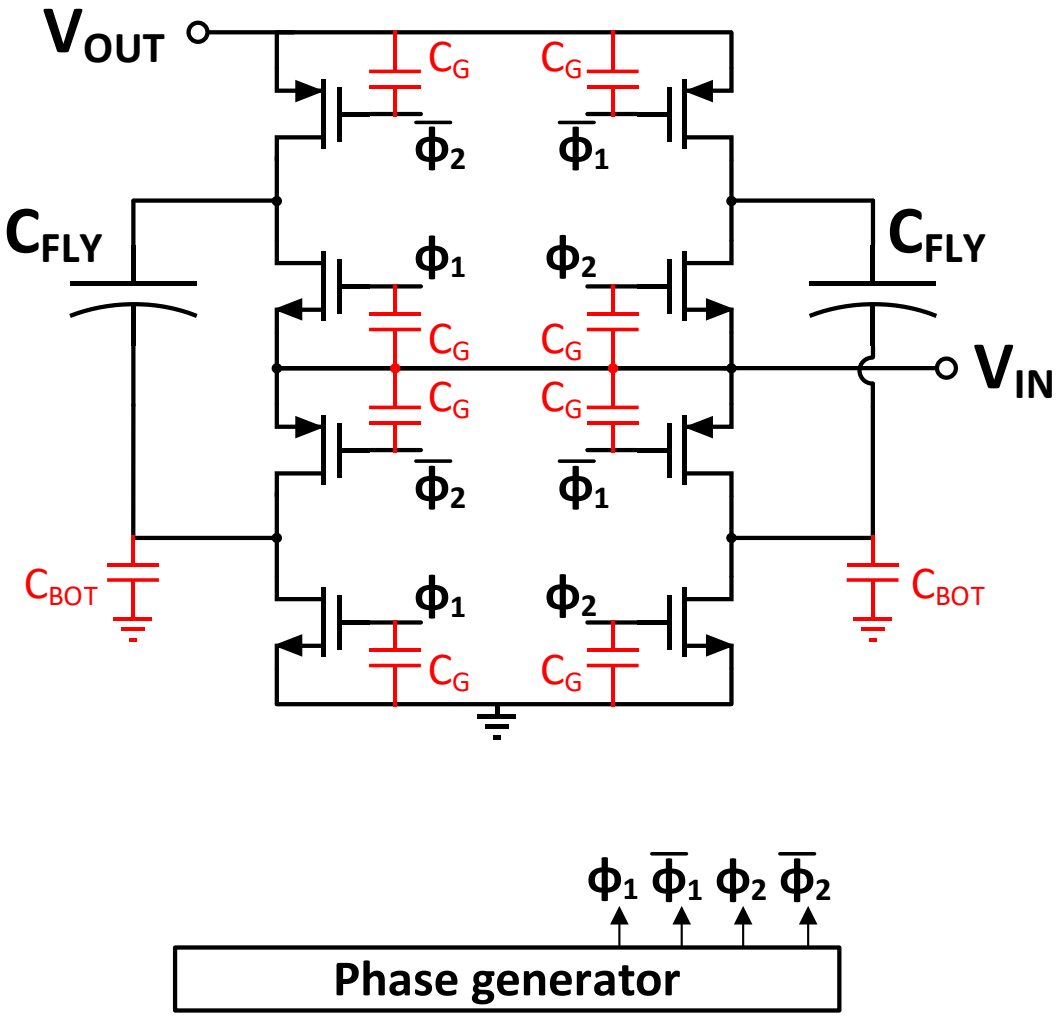
Background and Motivations

Fully integrated DC-DC converter publications



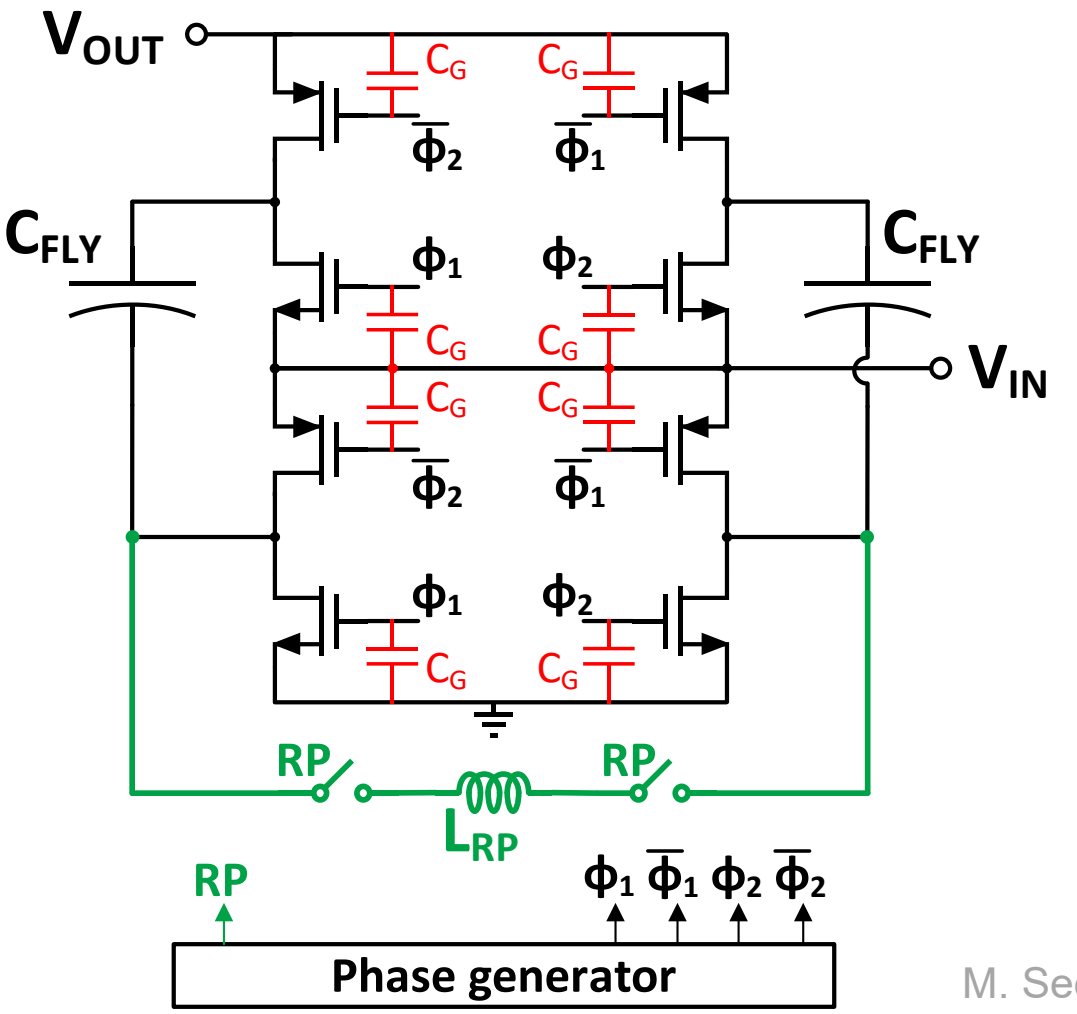


Conventional Switched Capacitor (SC)



- C_{BOT} switching loss
- C_G switching loss
- Low power density
- Auxiliary circuitry
- Large load capacitor

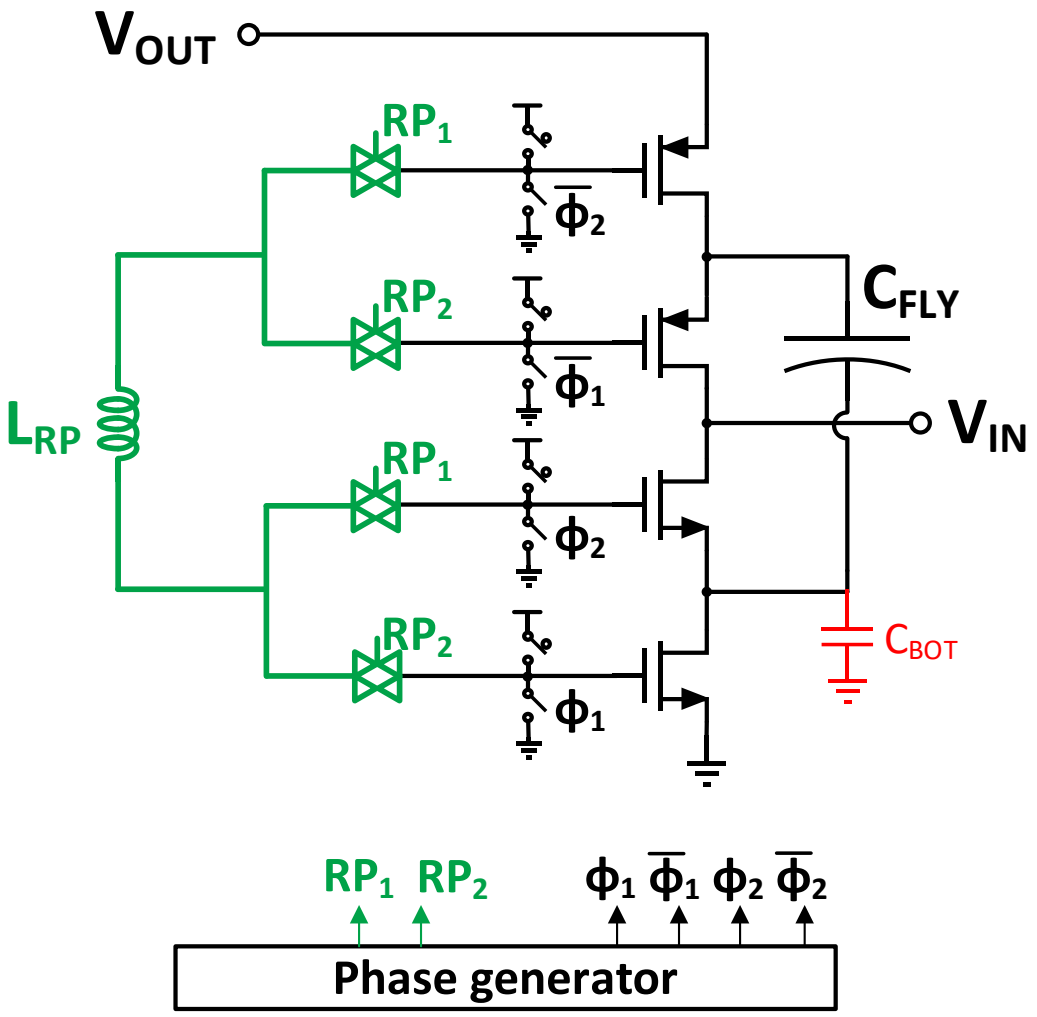
Resonant Drain SC



- ☺ **C_{BOT} switching loss**
- ☹ C_G switching loss
- ☹ Low power density
- ☹ Auxiliary circuitry
- ☹ Large load capacitor

M. Seeman, PhD dissertation, 2009

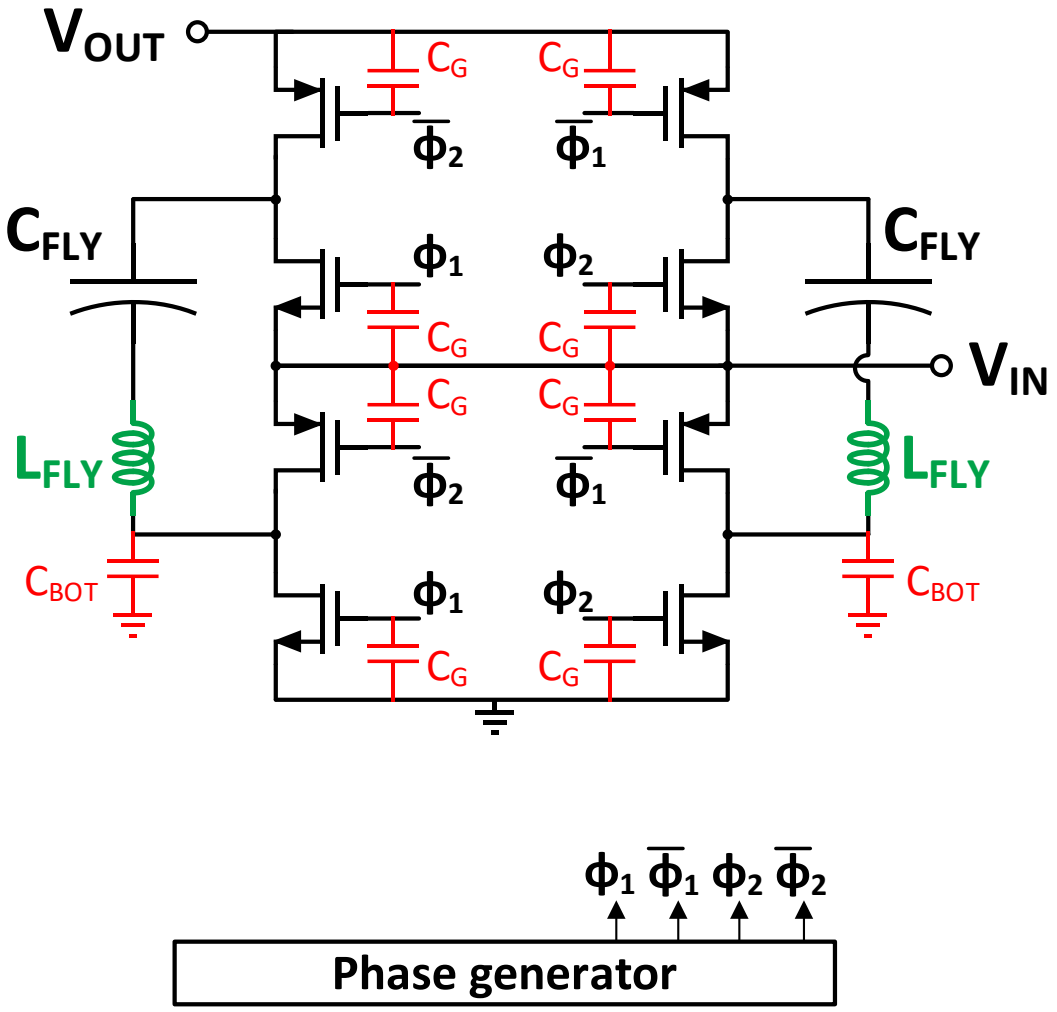
Resonant Gate SC



- ☹ C_{BOT} switching loss
- ☺ **C_G switching loss**
- ☹ Low power density
- ☹ Auxiliary circuitry
- ☹ Large load capacitor

M. Abdelfattah, ISSCC18'

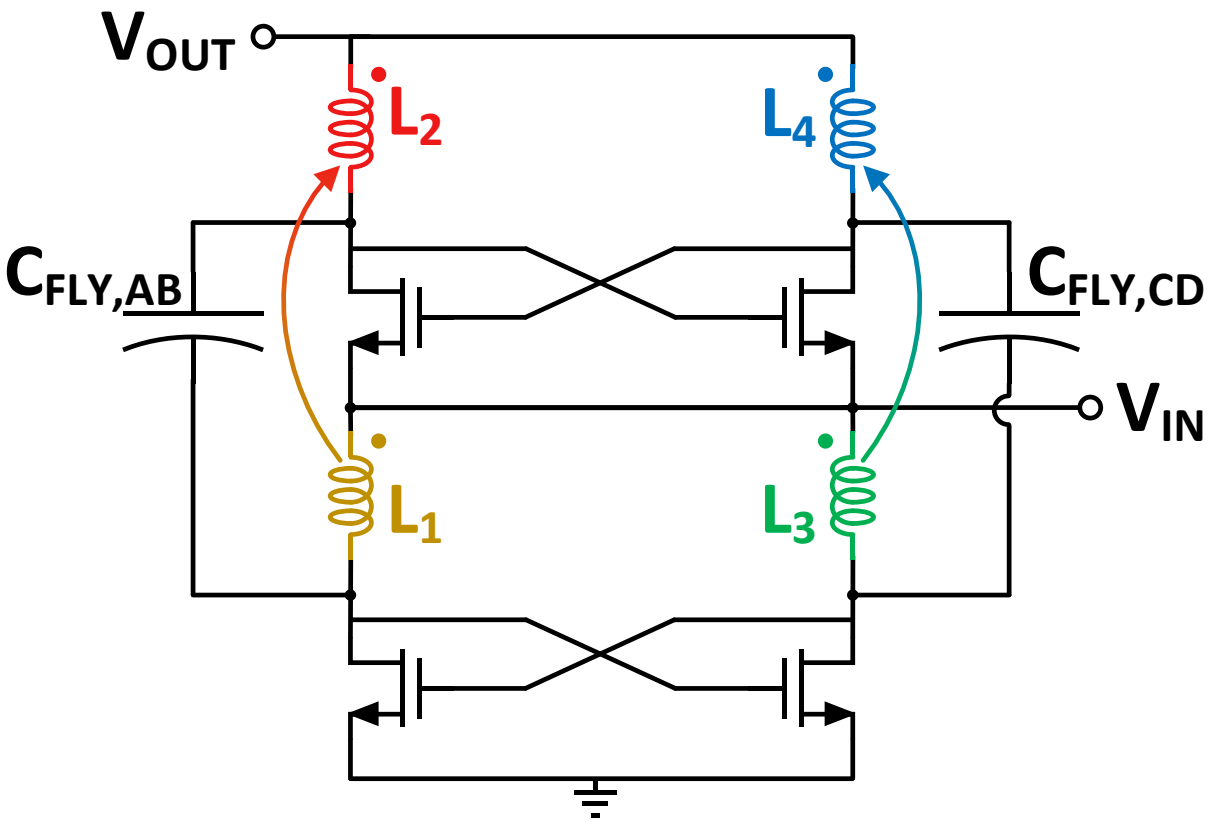
Hybrid-Resonant SC



- 😐 C_{BOT} switching loss
- 😐 C_G switching loss
- 🙂 **High power density**
- ☹ Auxiliary circuitry
- ☹ Large load capacitor

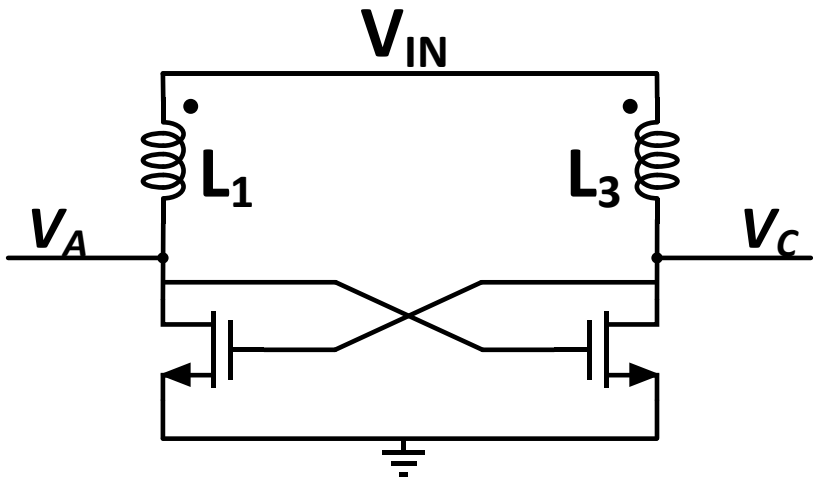
K. Kesarwani, ISSCC14'

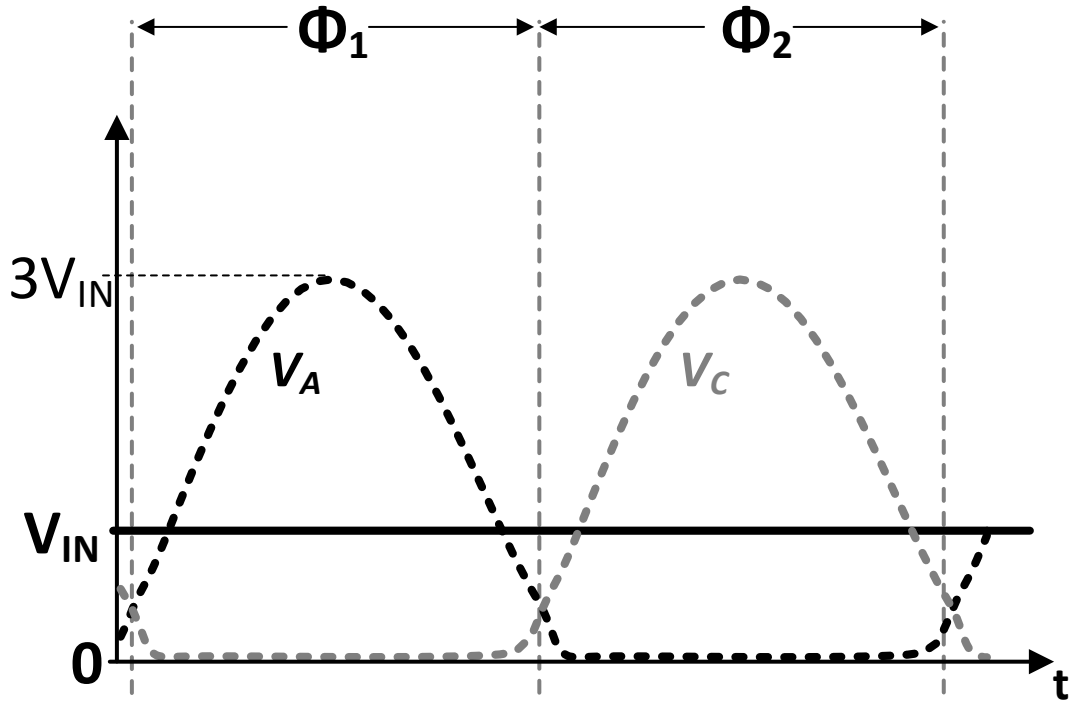
Proposed EM coupled class-D LC 1:2



- C_{BOT} switching loss
- C_G switching loss
- High power density
- No auxiliary circuitry
- No large load capacitor

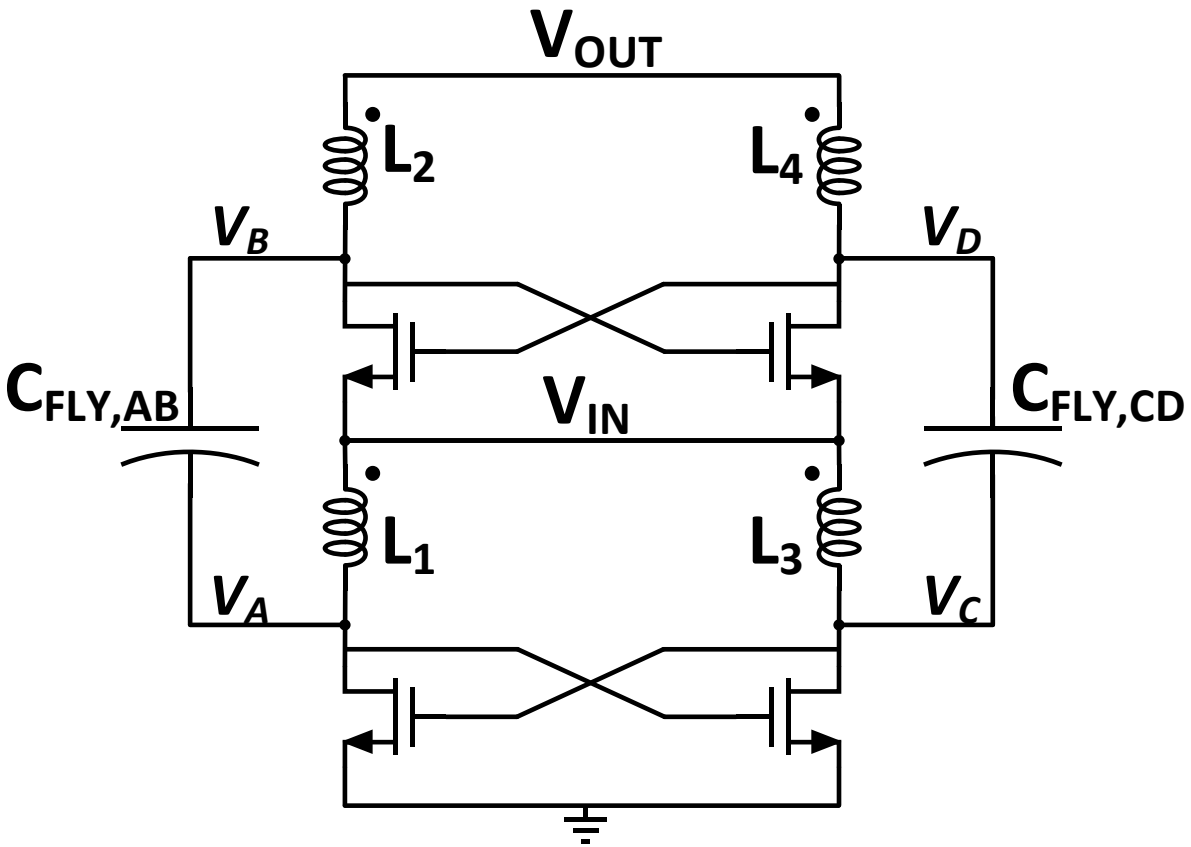
Operating Principles

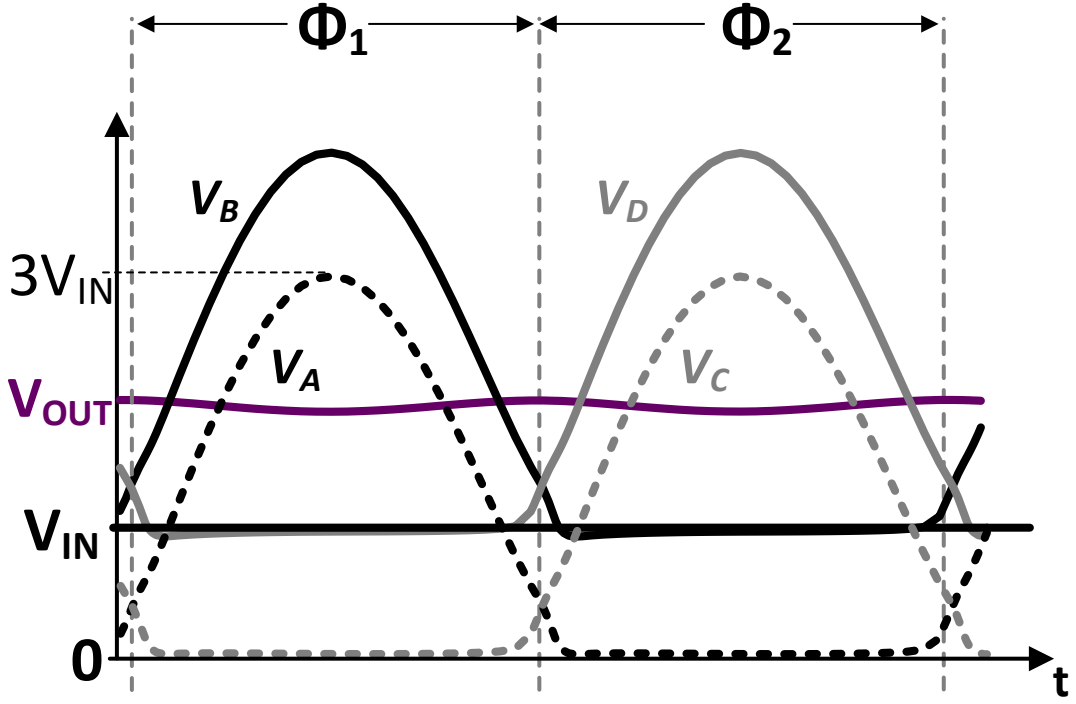




- V_{IN} starts the oscillation on the nodes V_A and V_C

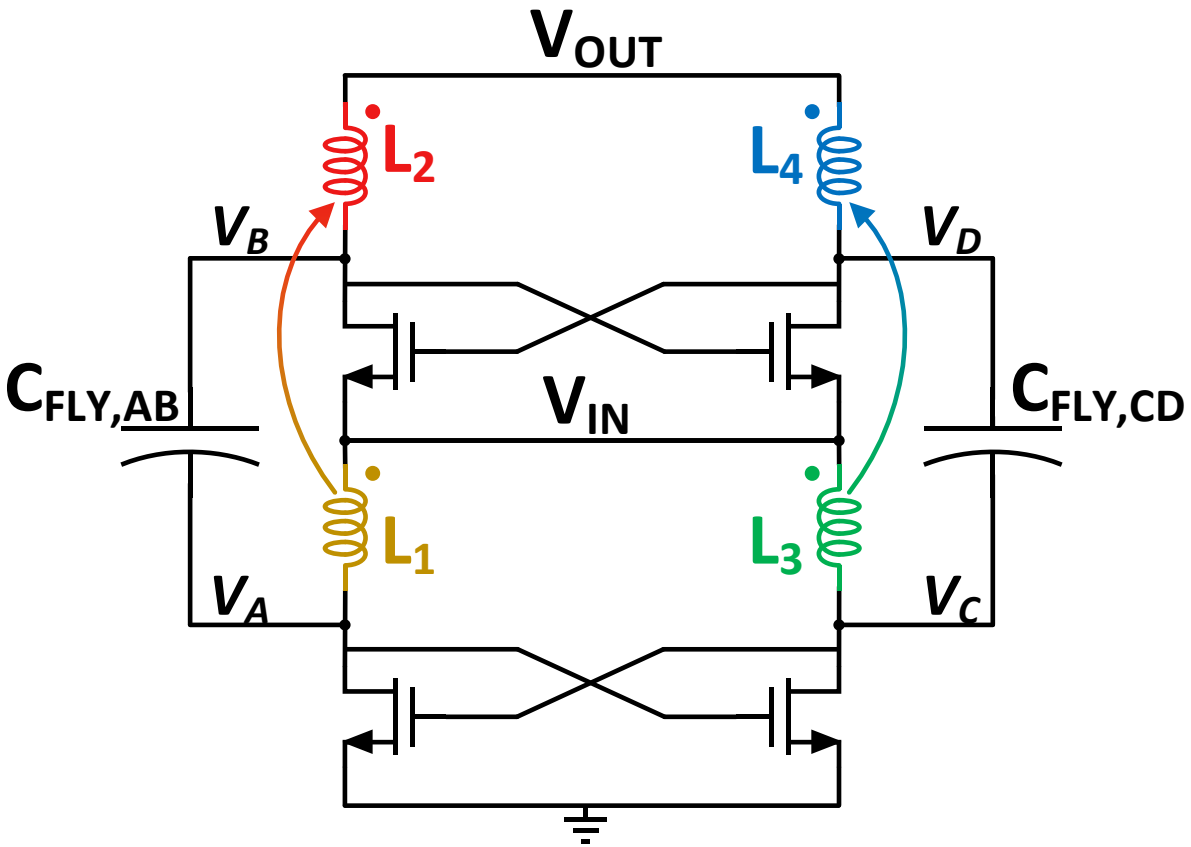
Operating Principles

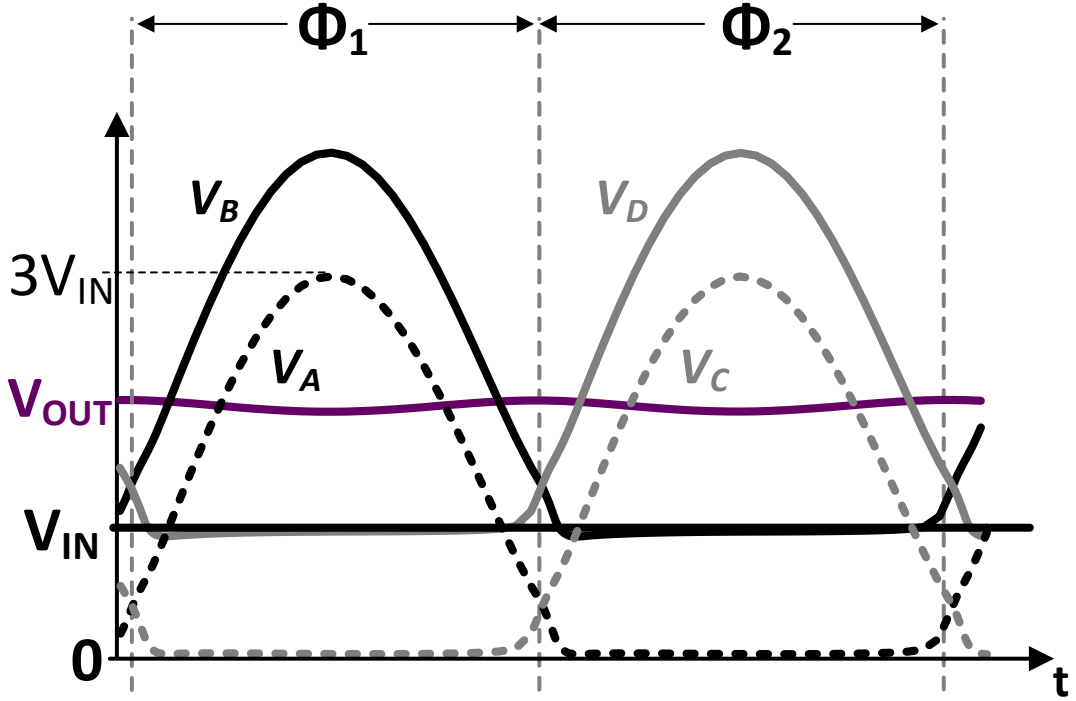




- V_B and V_D follow V_A and V_C thanks to the vertical electric coupling

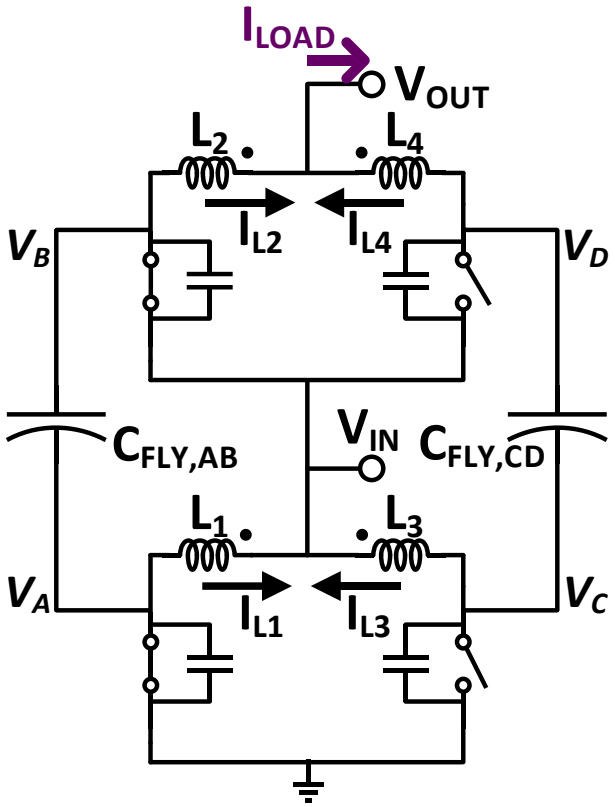
Operating Principles

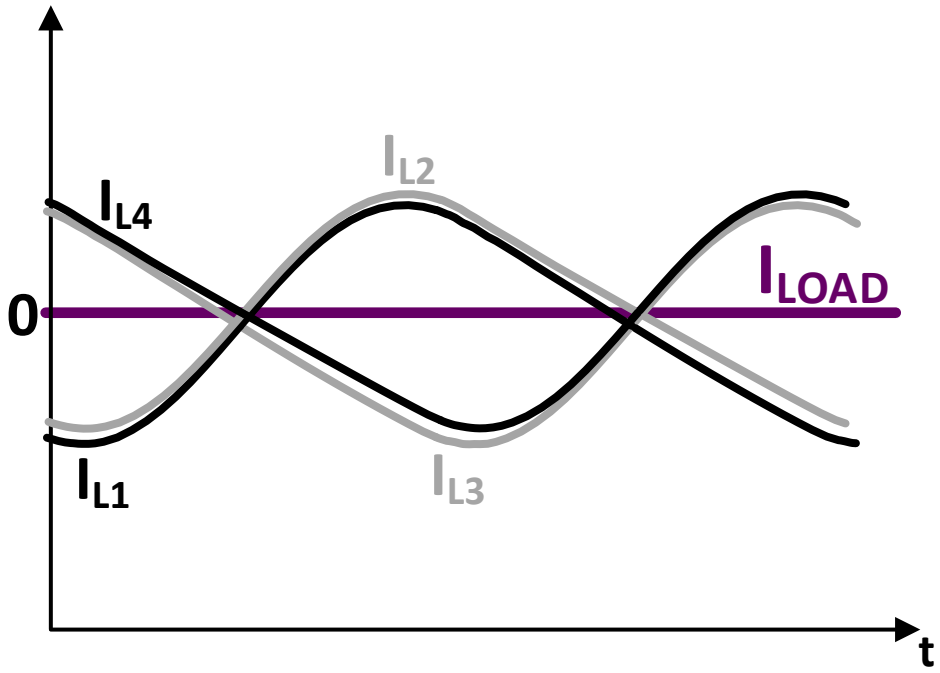




- Vertical magnetic coupling introduces current coupling
- V_{OUT} is built in between L_2 and L_4

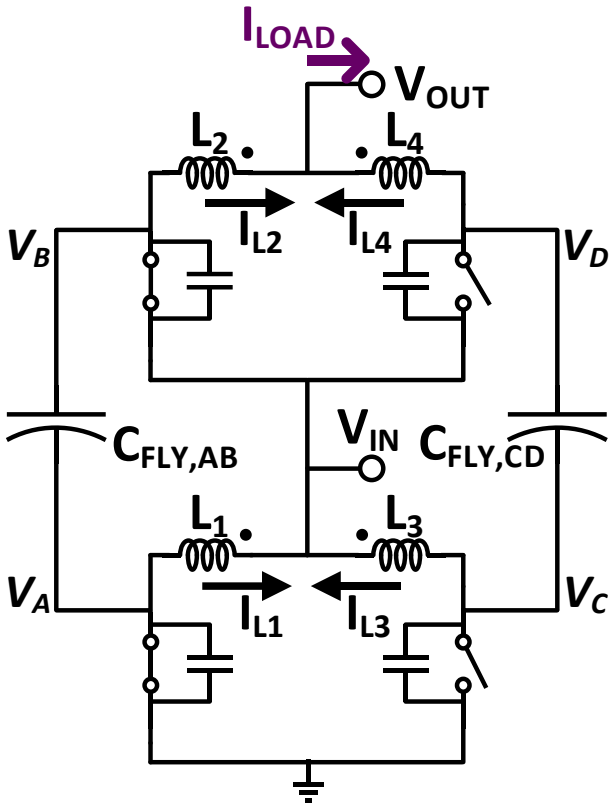
Operating Principles

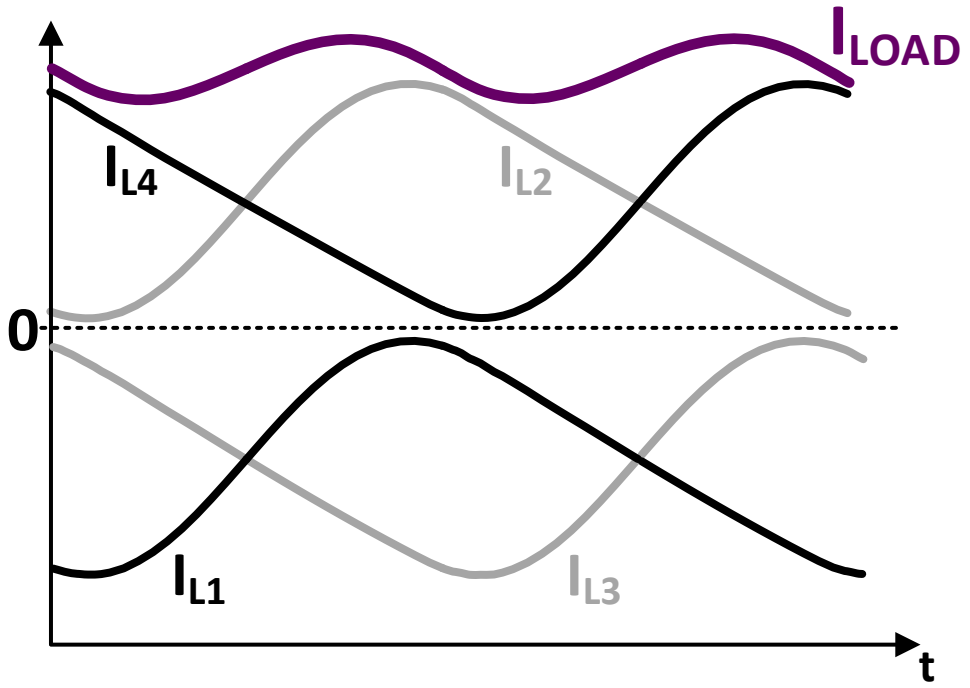




- $\mathbf{I_{LOAD} = 0}$: inductor currents oscillating close to 0

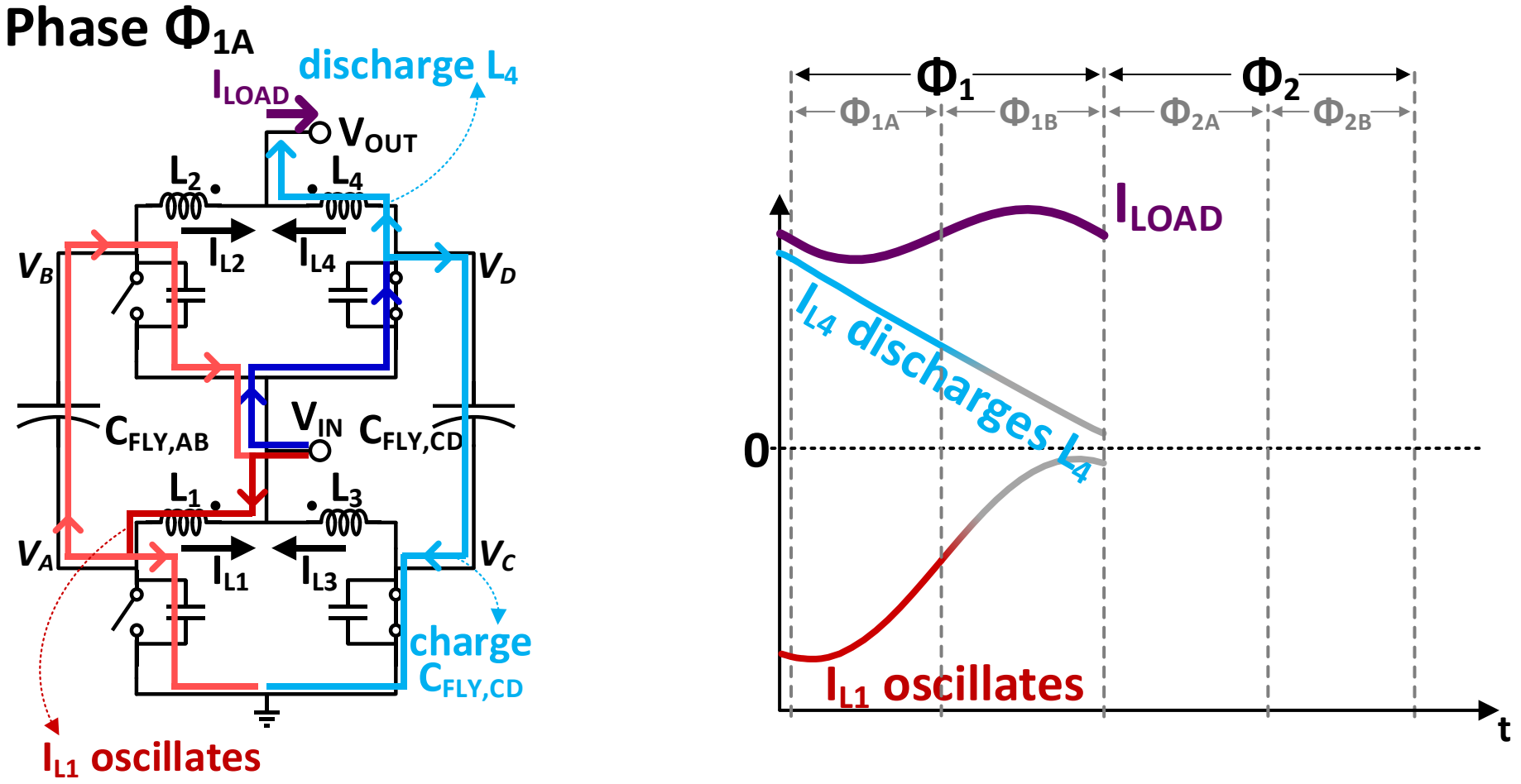
Operating Principles





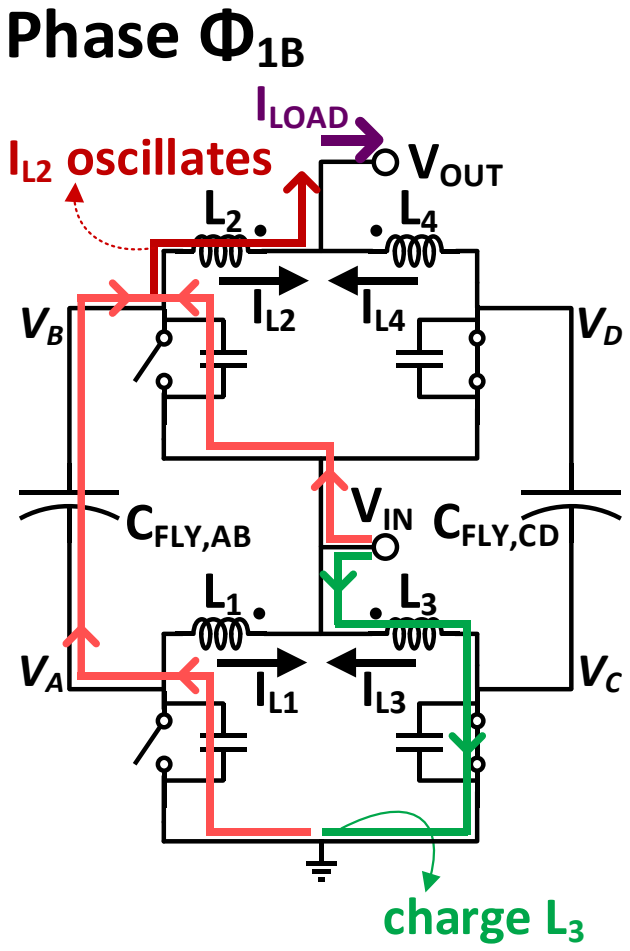
- $\mathbf{I_{LOAD} > 0}$: inductor currents DC component shifted

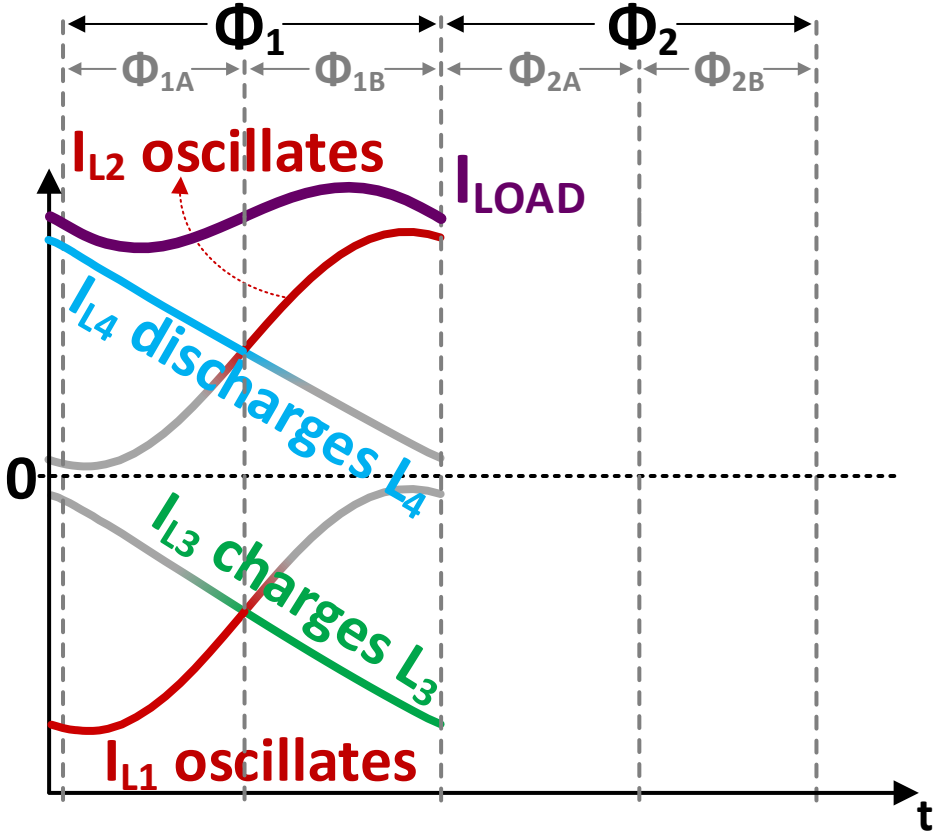
Operating Principles



- **Φ_{1A}:** L_1 energizing both oscillators, L_4 delivering I_{LOAD}

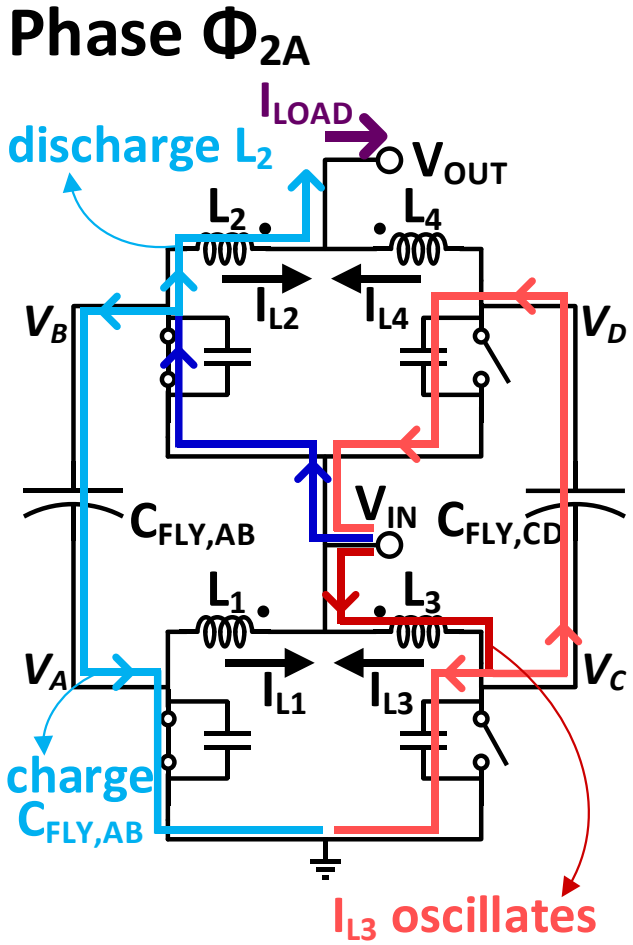
Operating Principles

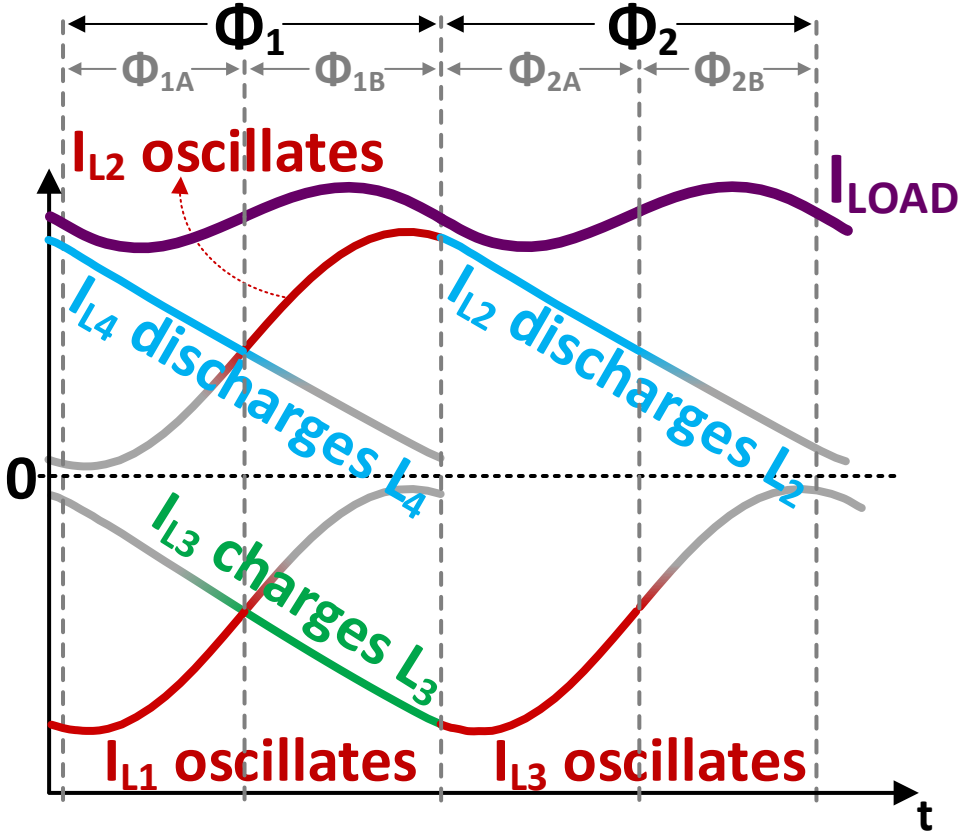




- **Φ1B:** L_3 charging, L_2 delivering I_{LOAD}

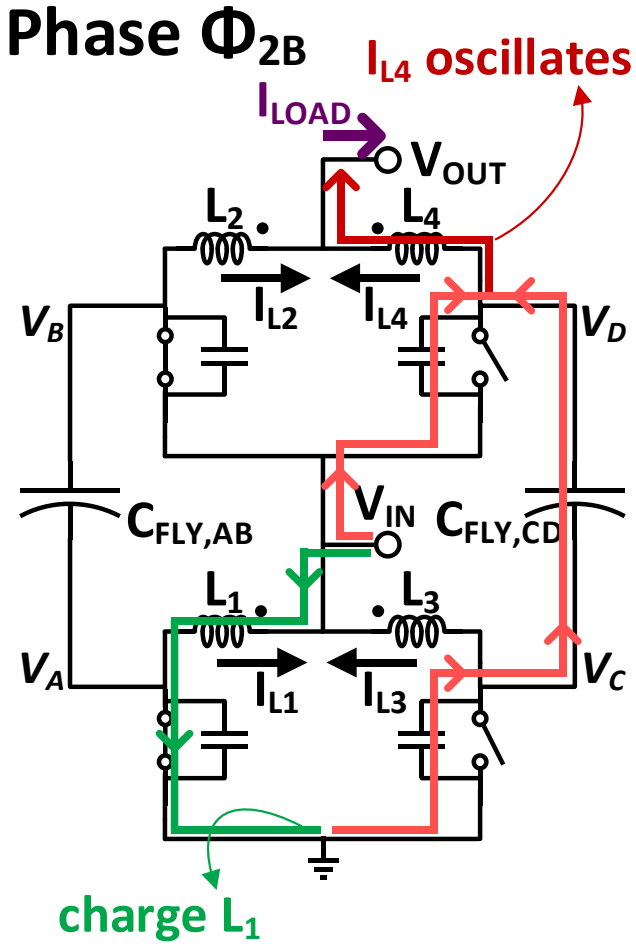
Operating Principles

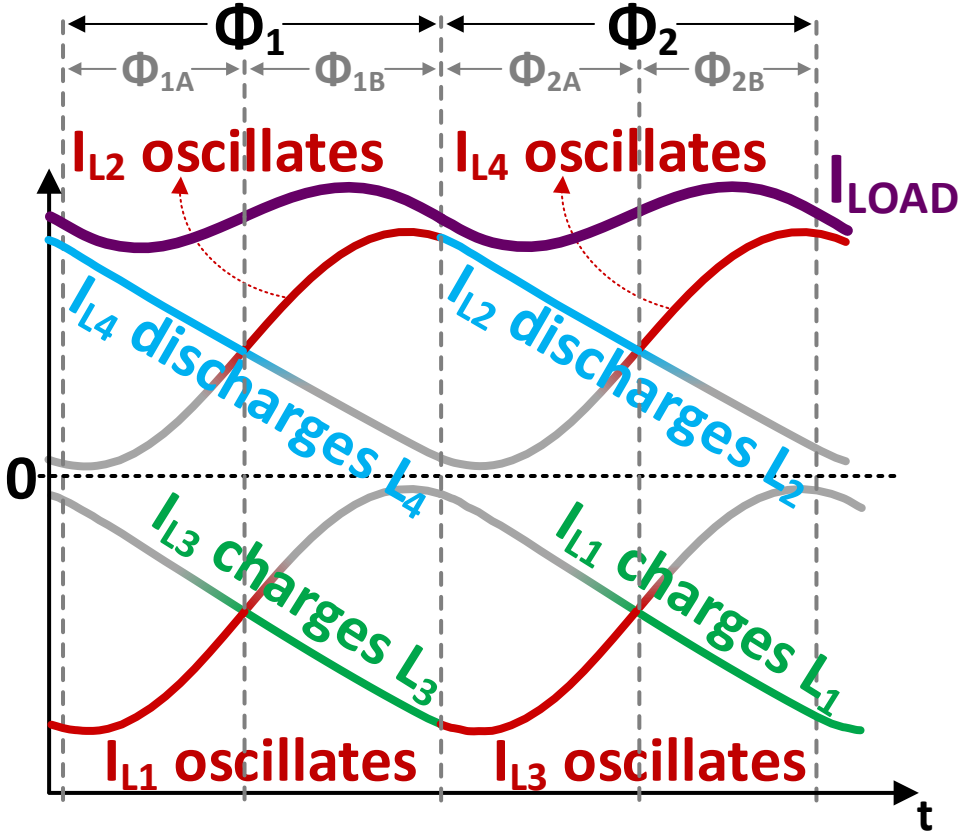




- **Φ_{2A}:** L_3 energizing both oscillators, L_2 delivering I_{LOAD}

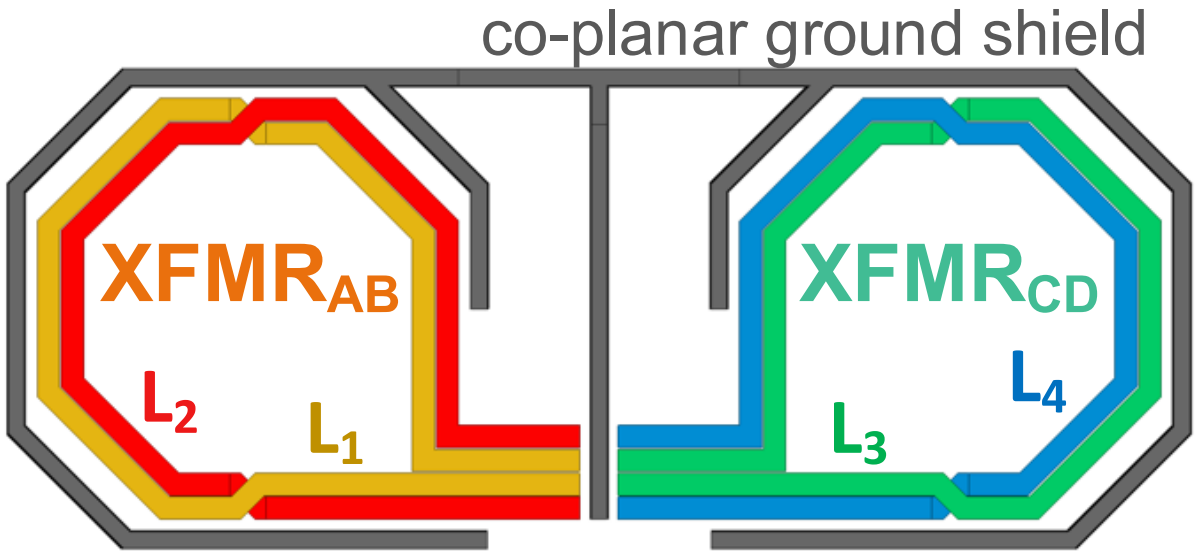
Operating Principles

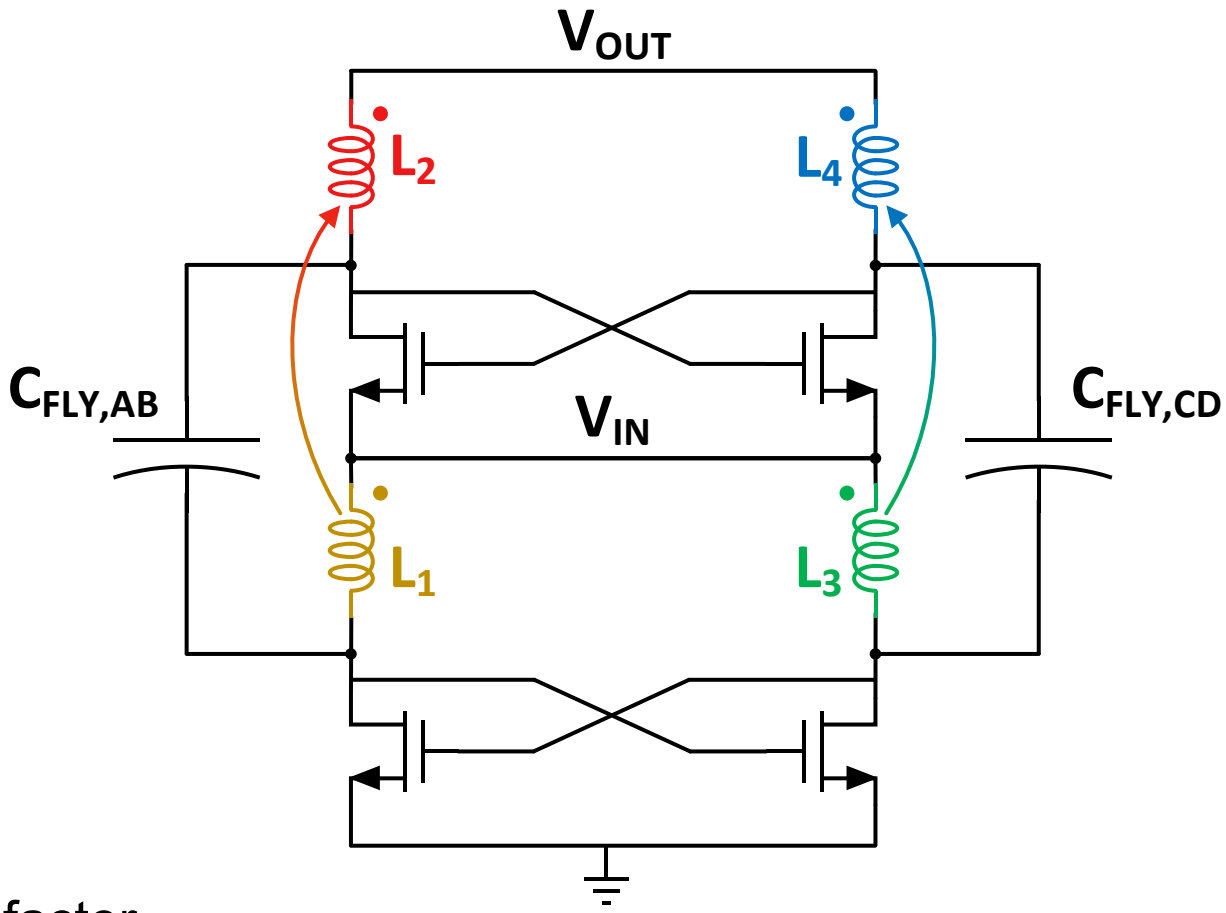




- **Φ2B:** L_1 charging, L_4 delivering I_{LOAD}

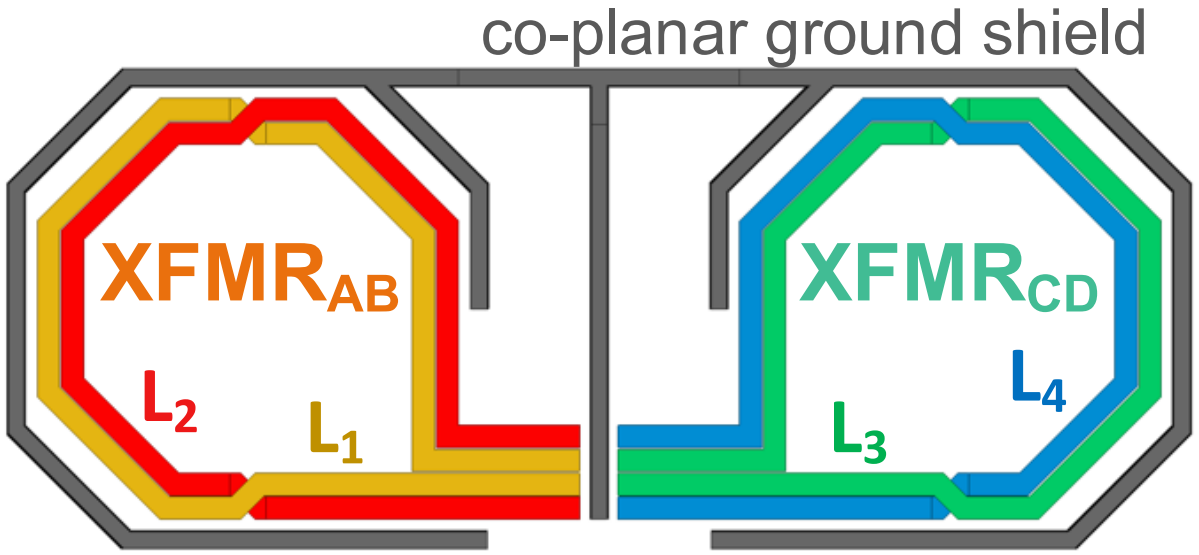
On-chip Transformer Design

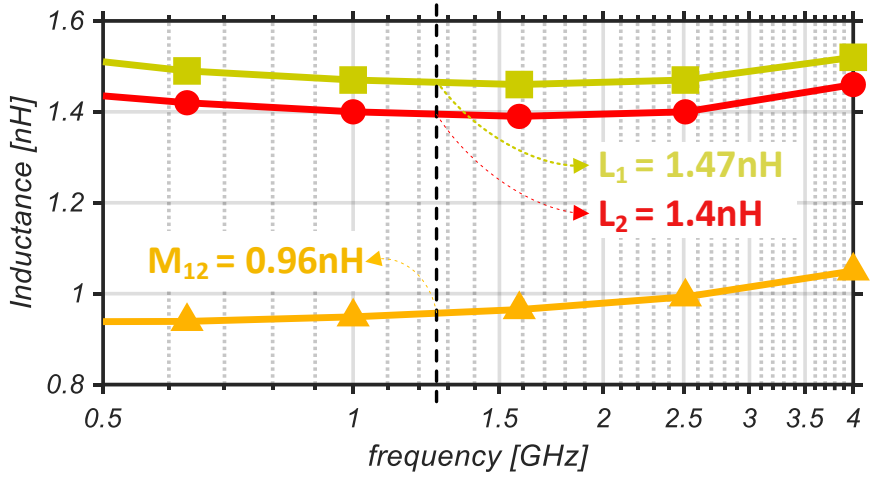


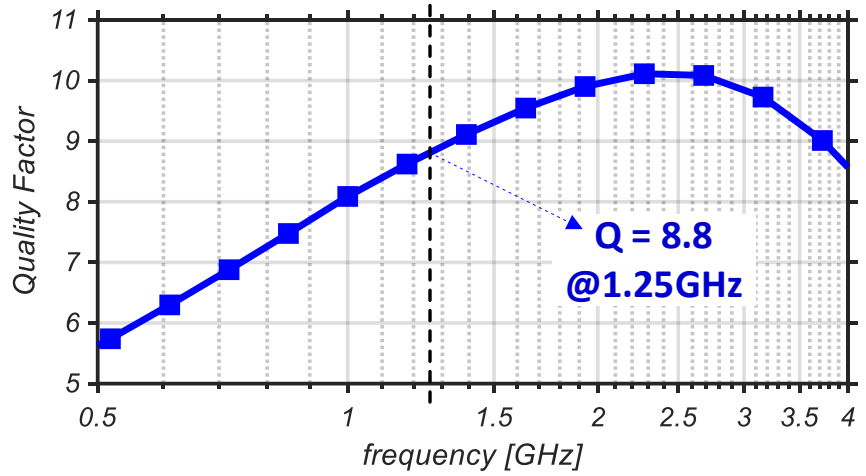


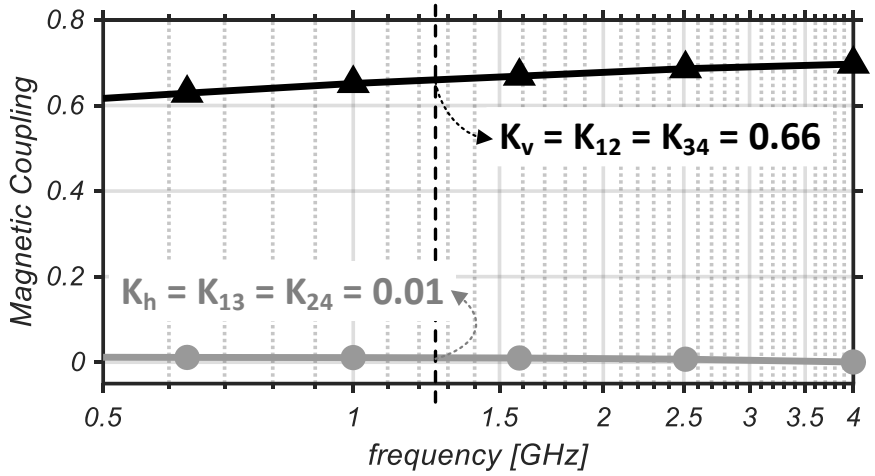
- Interleaved loop structure
- Maximize $K_v = K_{12} = K_{34}$
- Minimize $K_h = K_{13} = K_{24}$
- Co-planar ground shield to improve the quality factor

On-chip Transformer Design

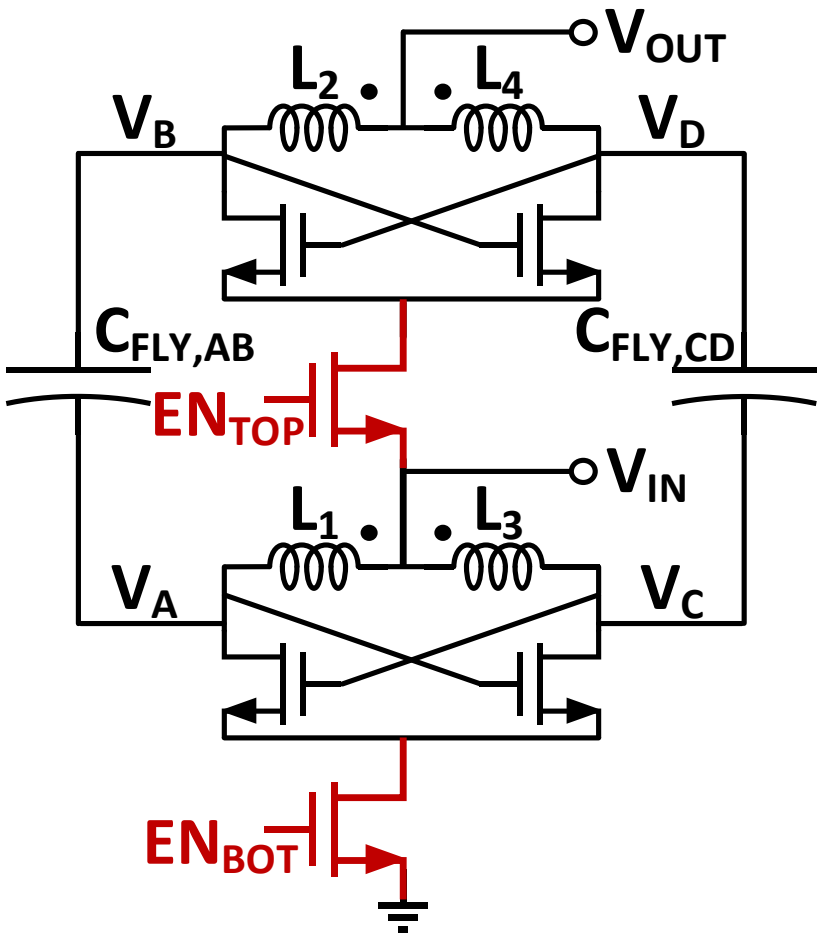






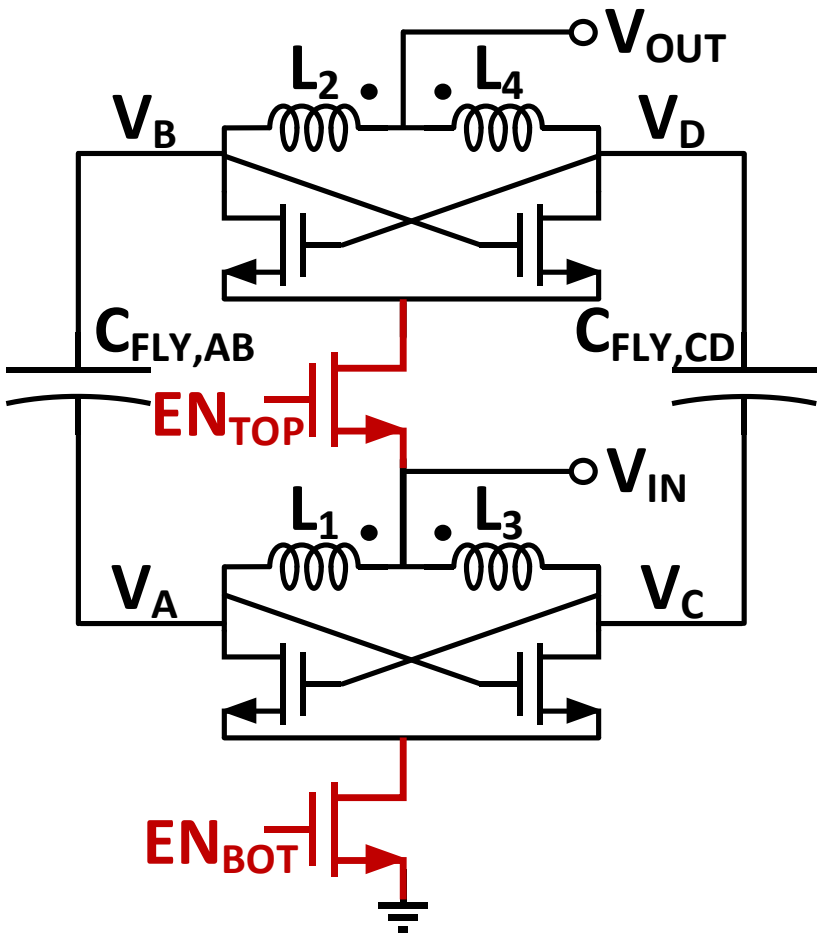


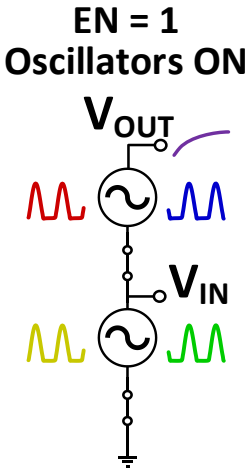
Duty cycling scheme for light load

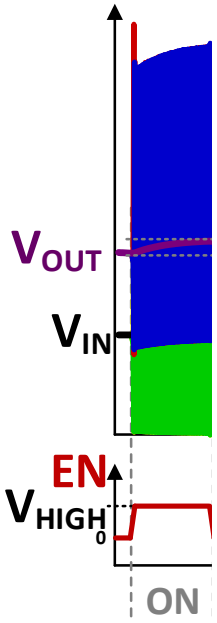


- Footer NMOS placed to switch ON and OFF the oscillators

Duty cycling scheme for light load

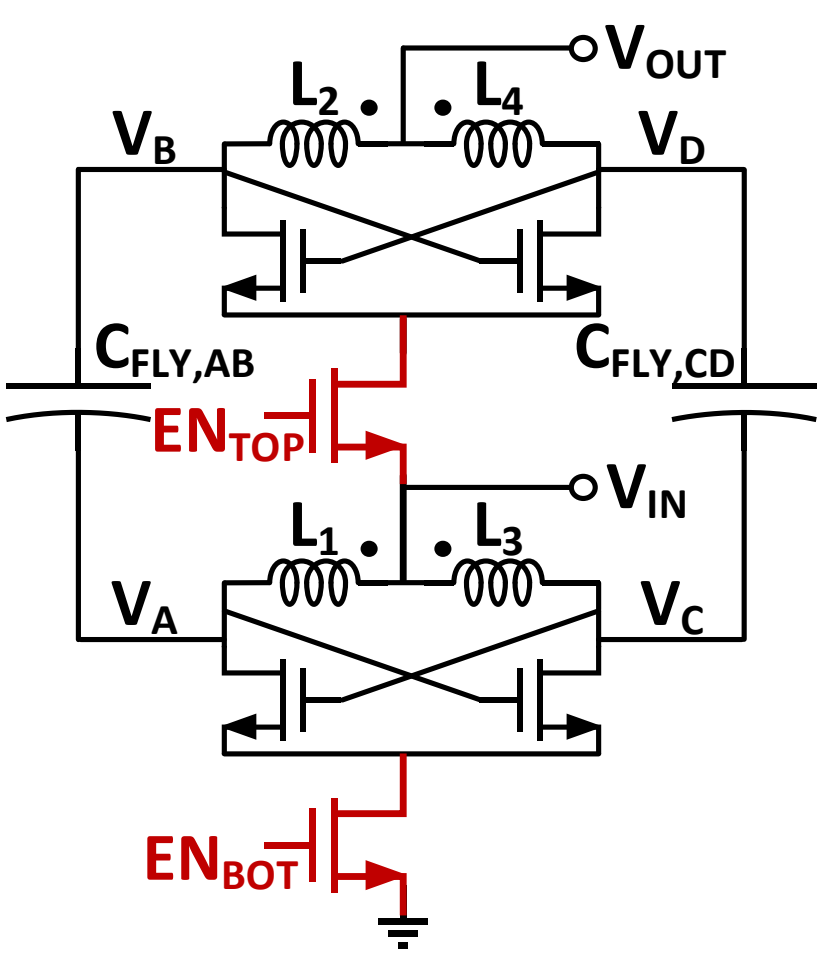


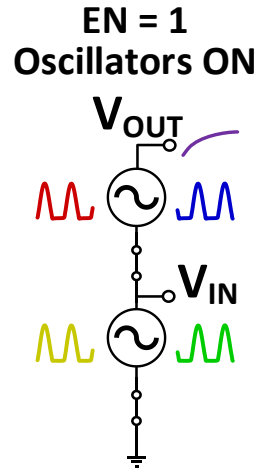


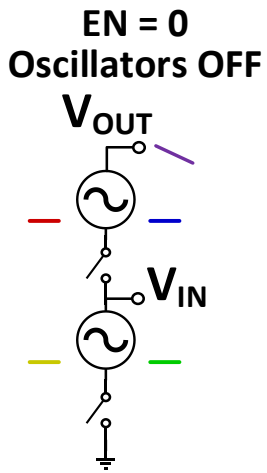


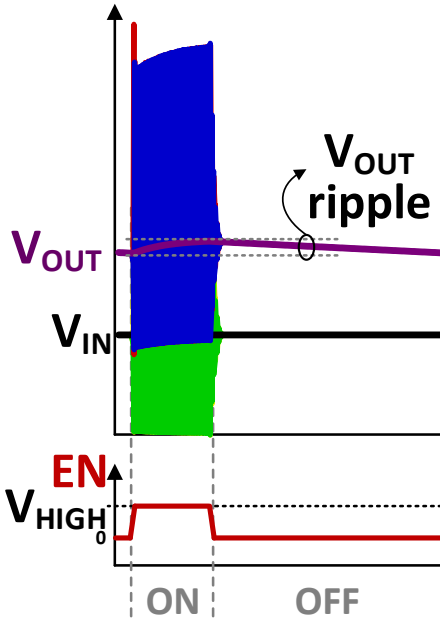
- During the ON state power is delivered to VOUT

Duty cycling scheme for light load



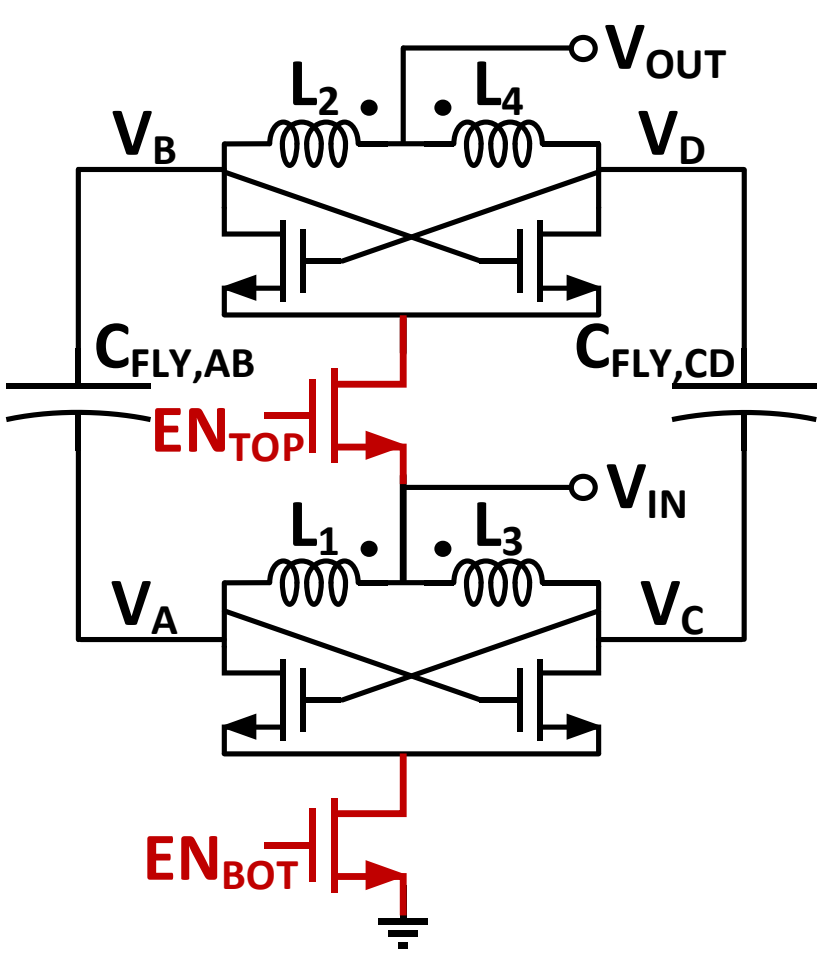


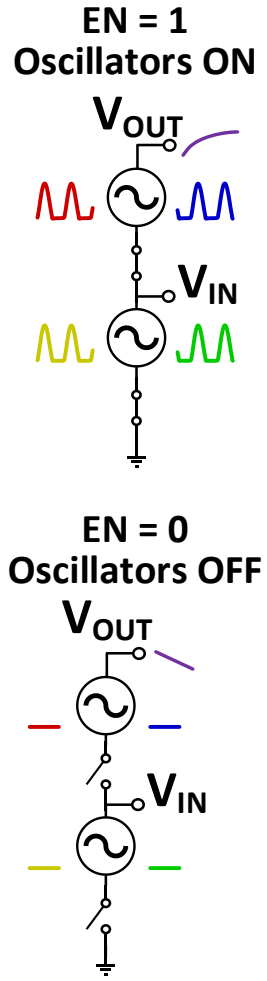


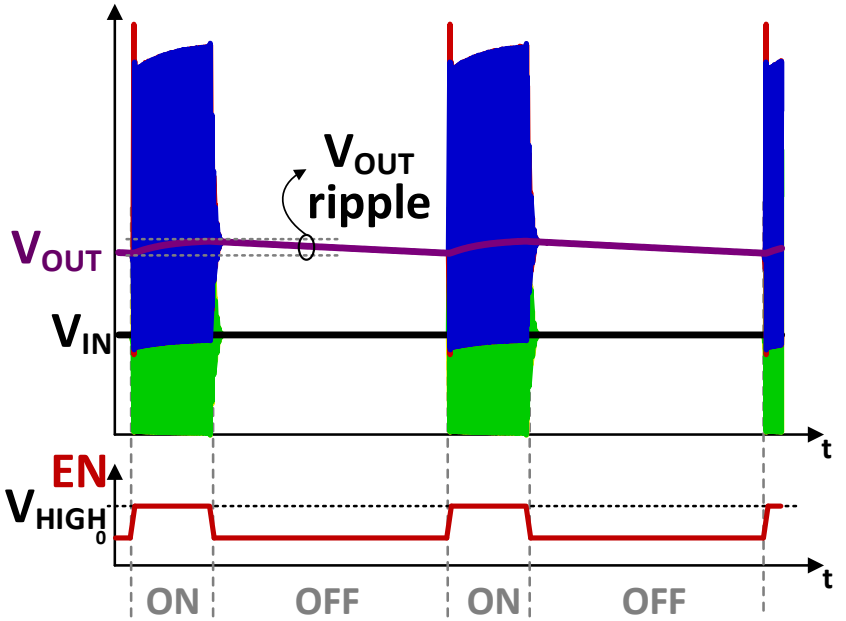


- During the OFF state no power is delivered to the output

Duty cycling scheme for light load

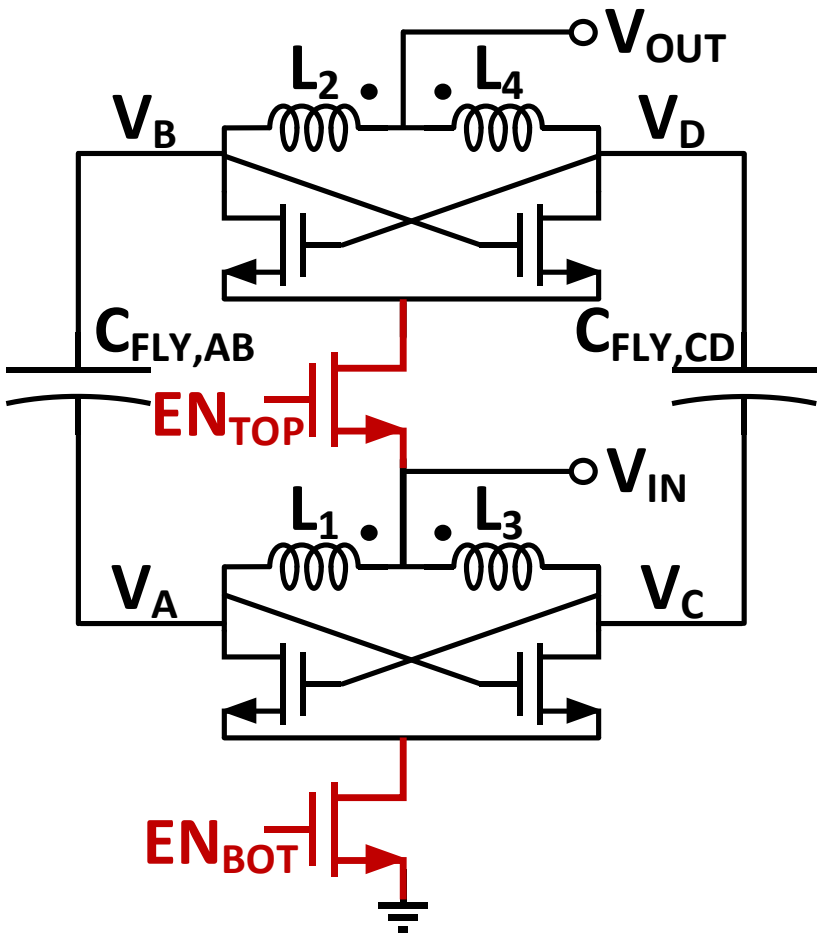


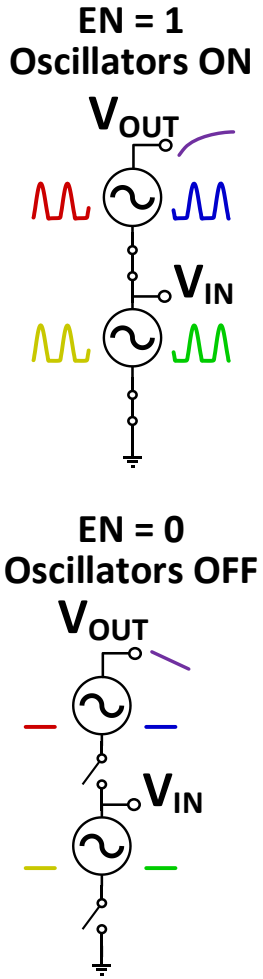


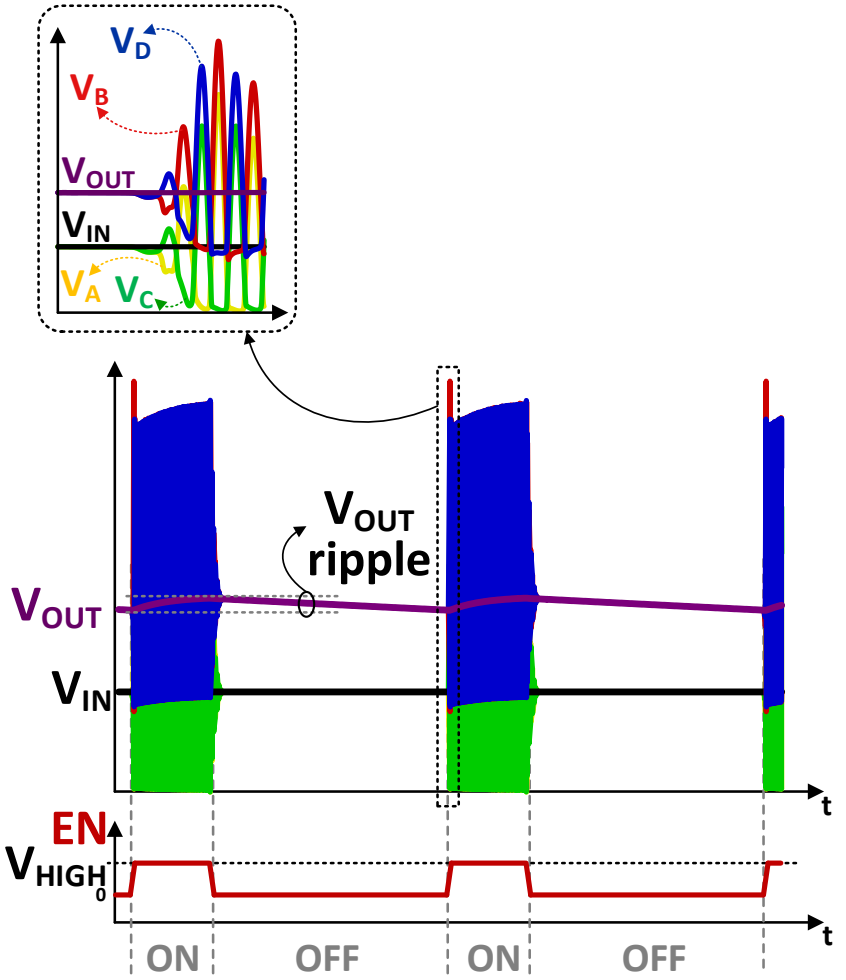


- The duty cycling reduces power losses in light load conditions

Duty cycling scheme for light load

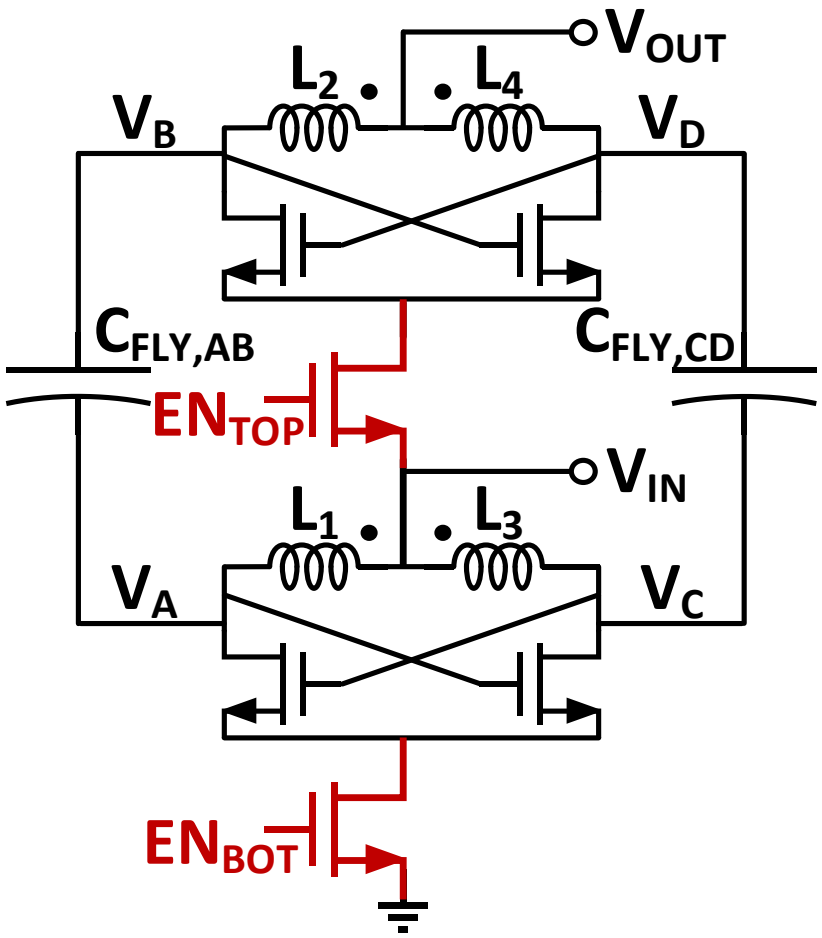




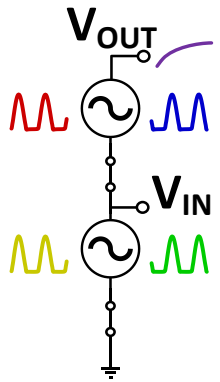


- Oscillators are switched ON and they start to resonate

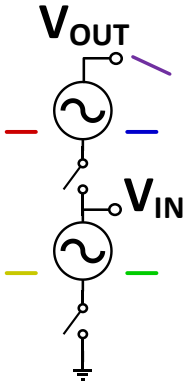
Duty cycling scheme for light load

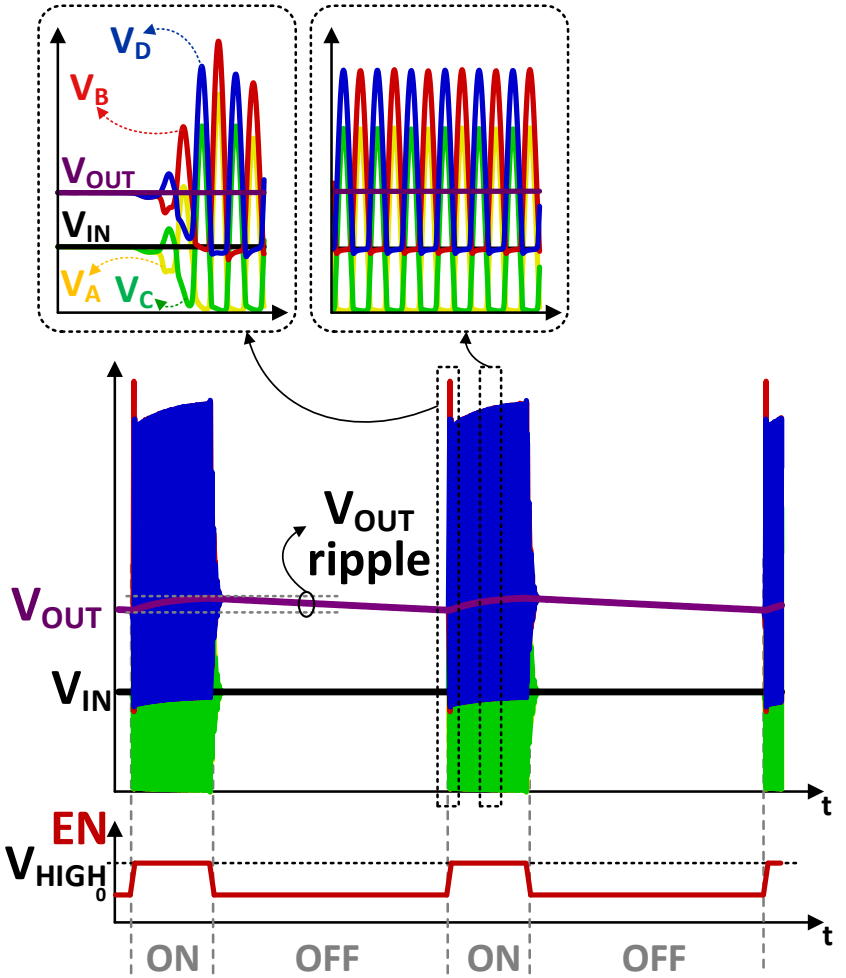


EN = 1
Oscillators ON



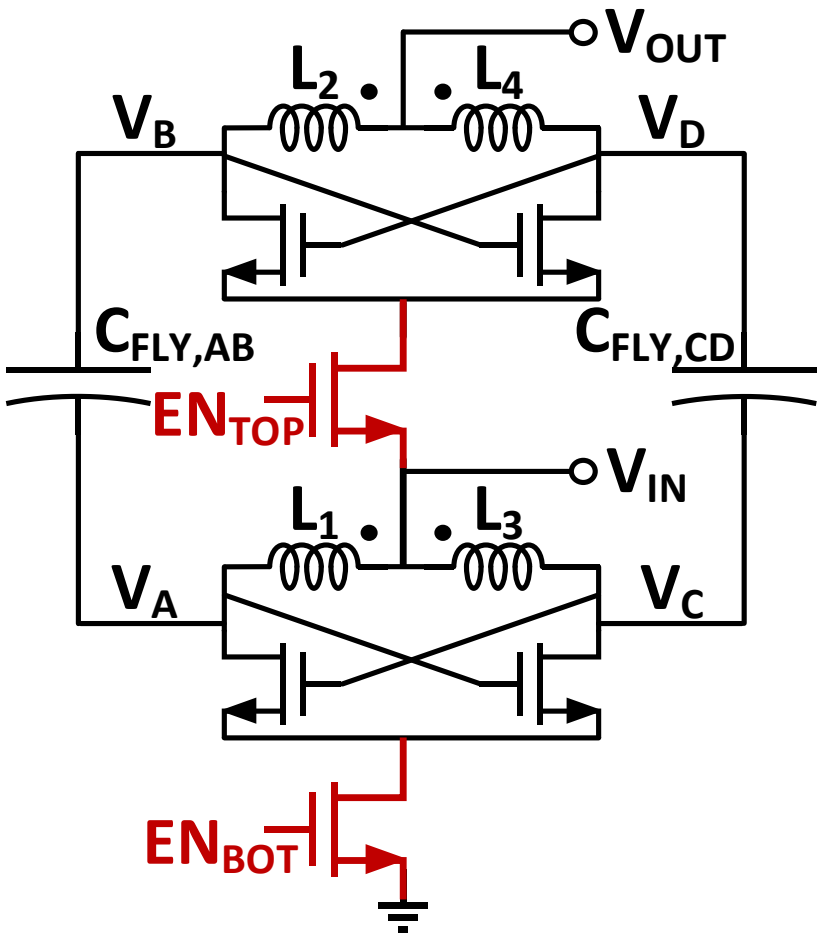
EN = 0
Oscillators OFF



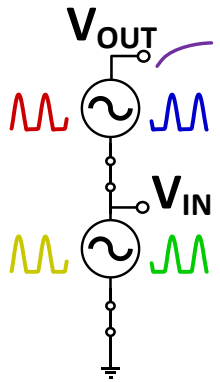


- Oscillators fully ON

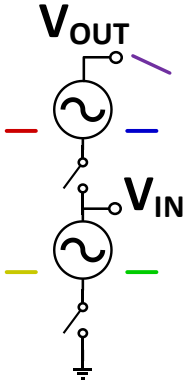
Duty cycling scheme for light load

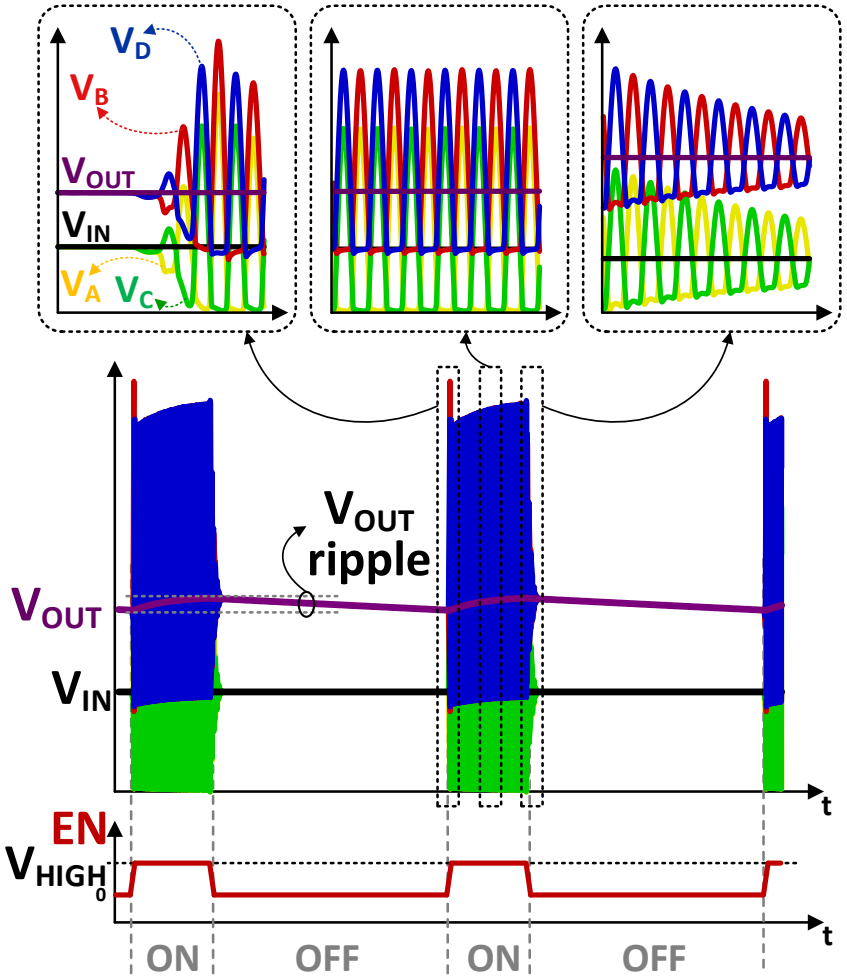


EN = 1
Oscillators ON



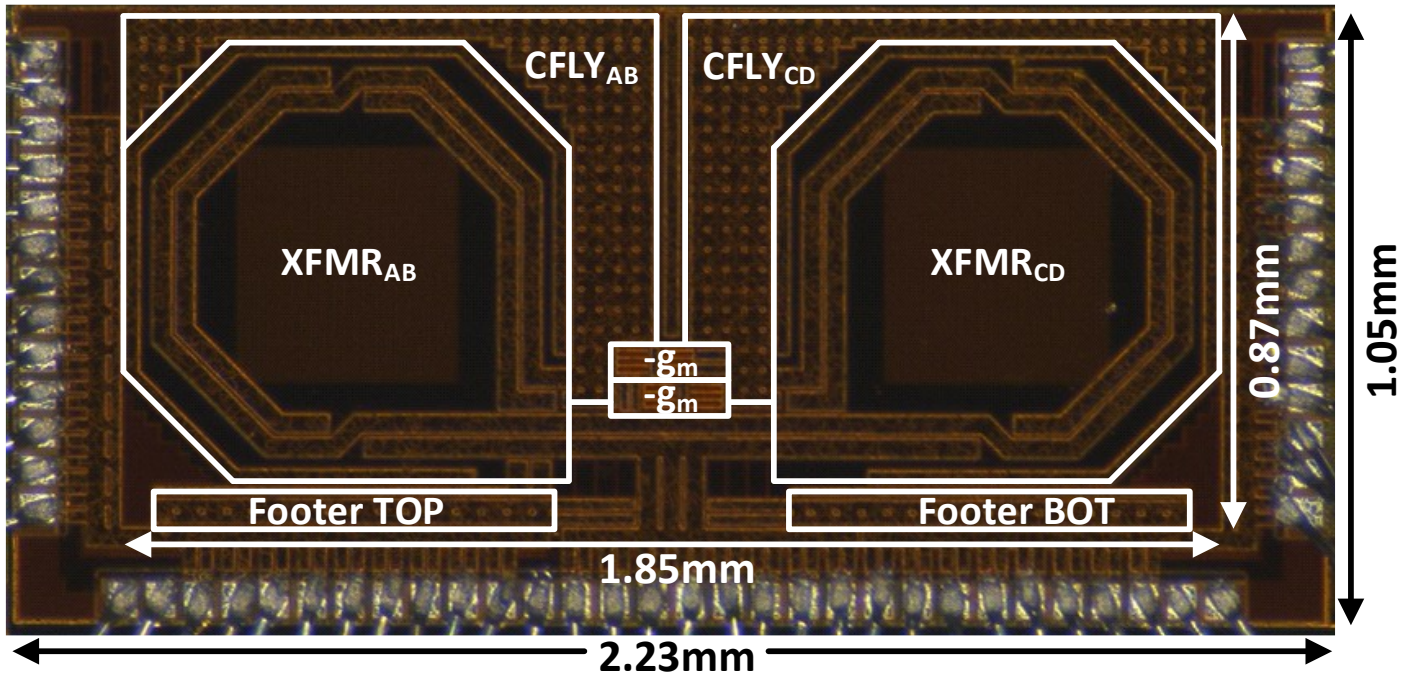
EN = 0
Oscillators OFF

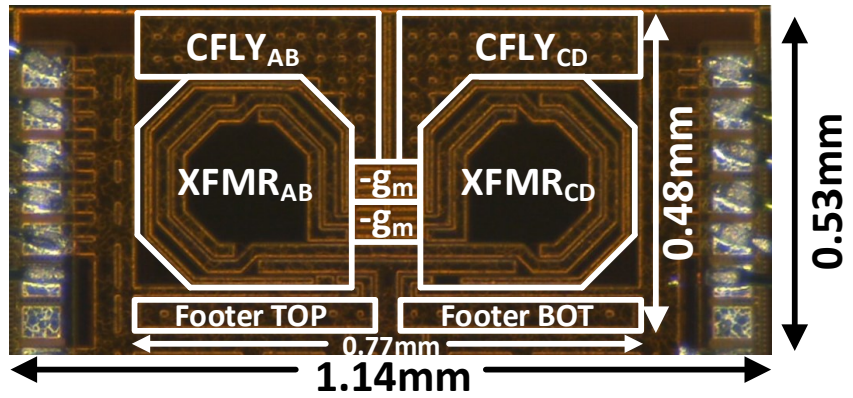




- Oscillation dying out

Chip Micrograph



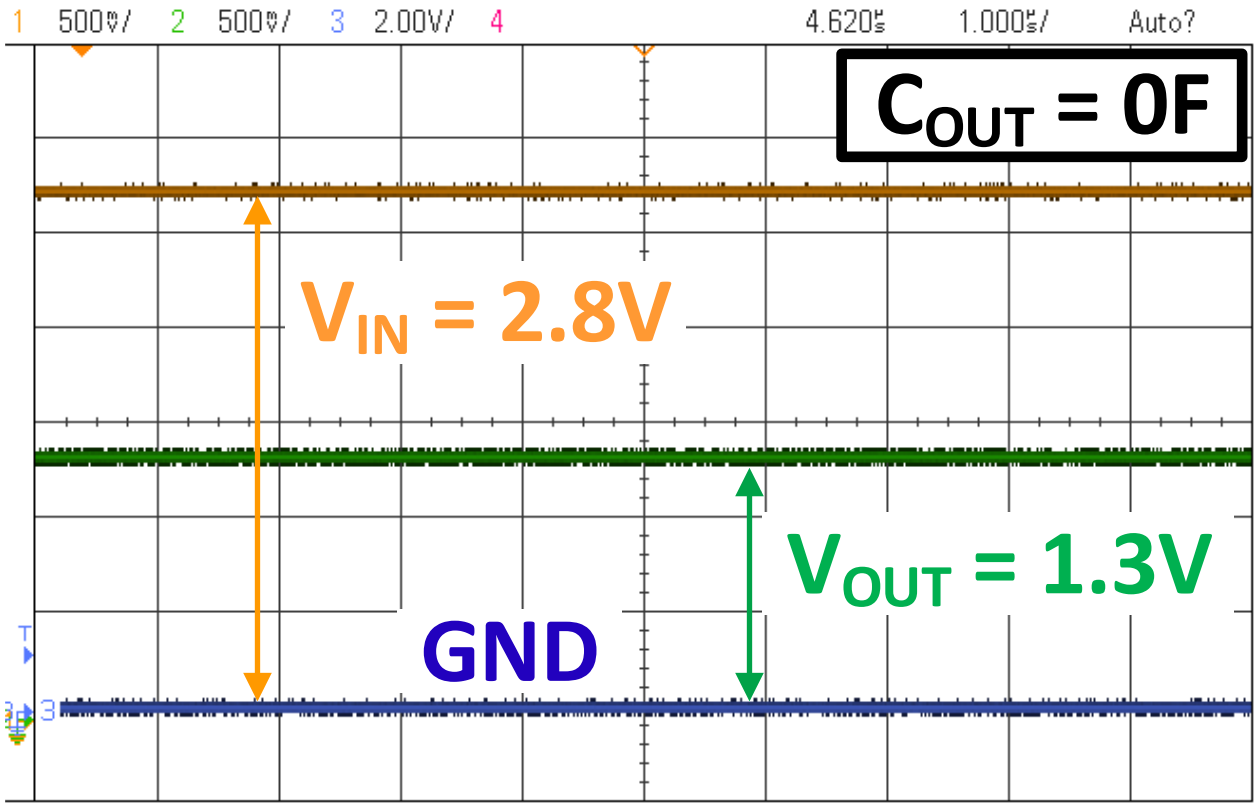


- **High Efficiency**
  - L_{TOT} = 7.8nH coupled
  - $C_{FLY,TOT}$ = 458pF
- **High Power Density**
  - L_{TOT} = 3.1nH coupled
  - $C_{FLY,TOT}$ = 152pF

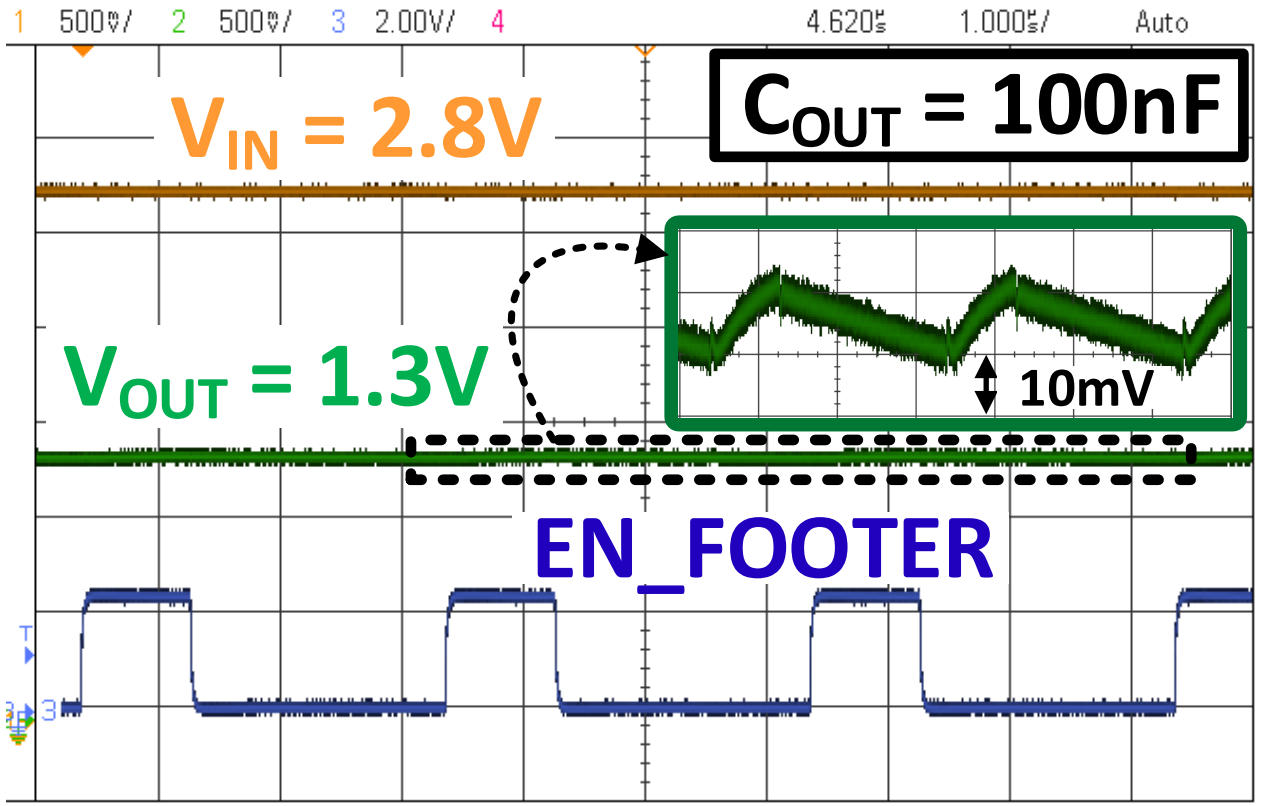
180nm bulk CMOS process

Measurement Result

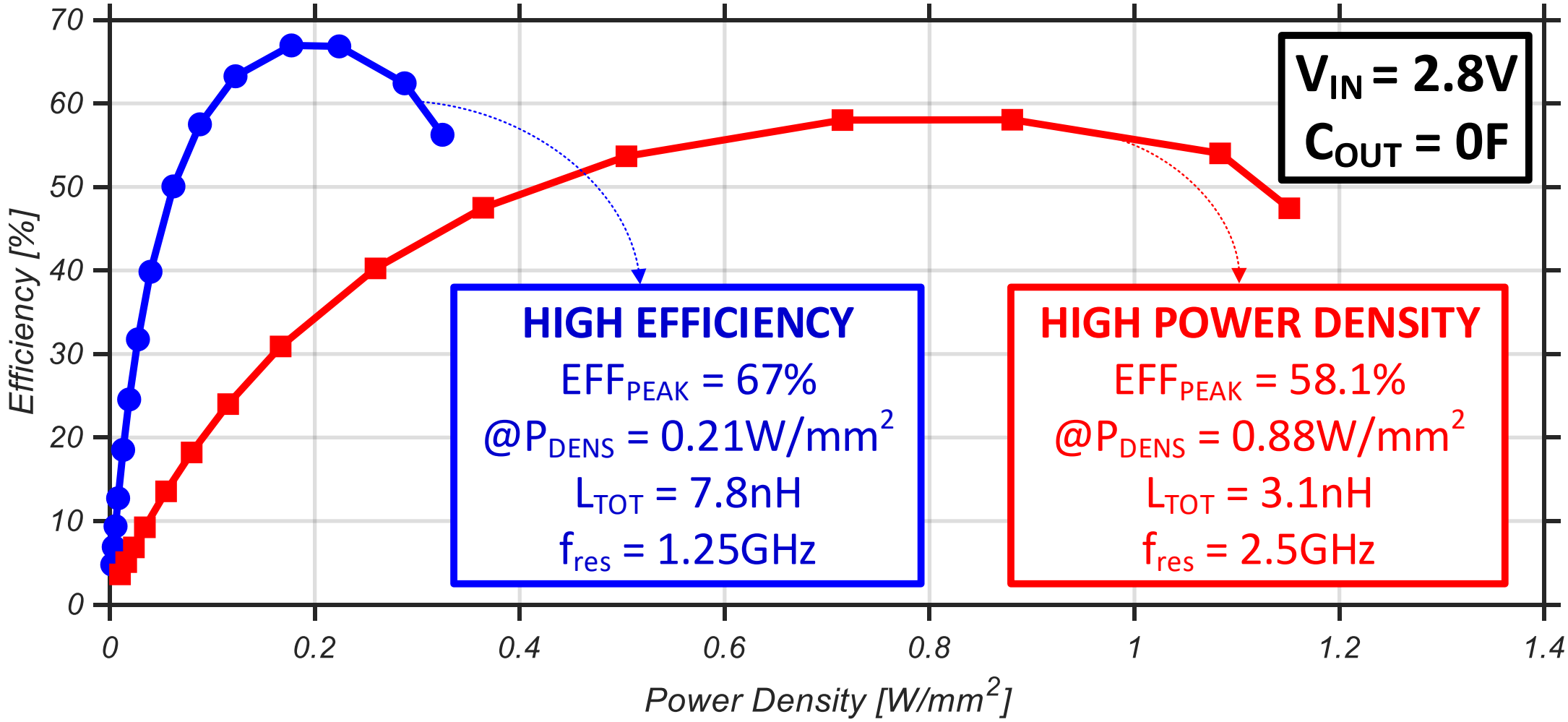
Full Load



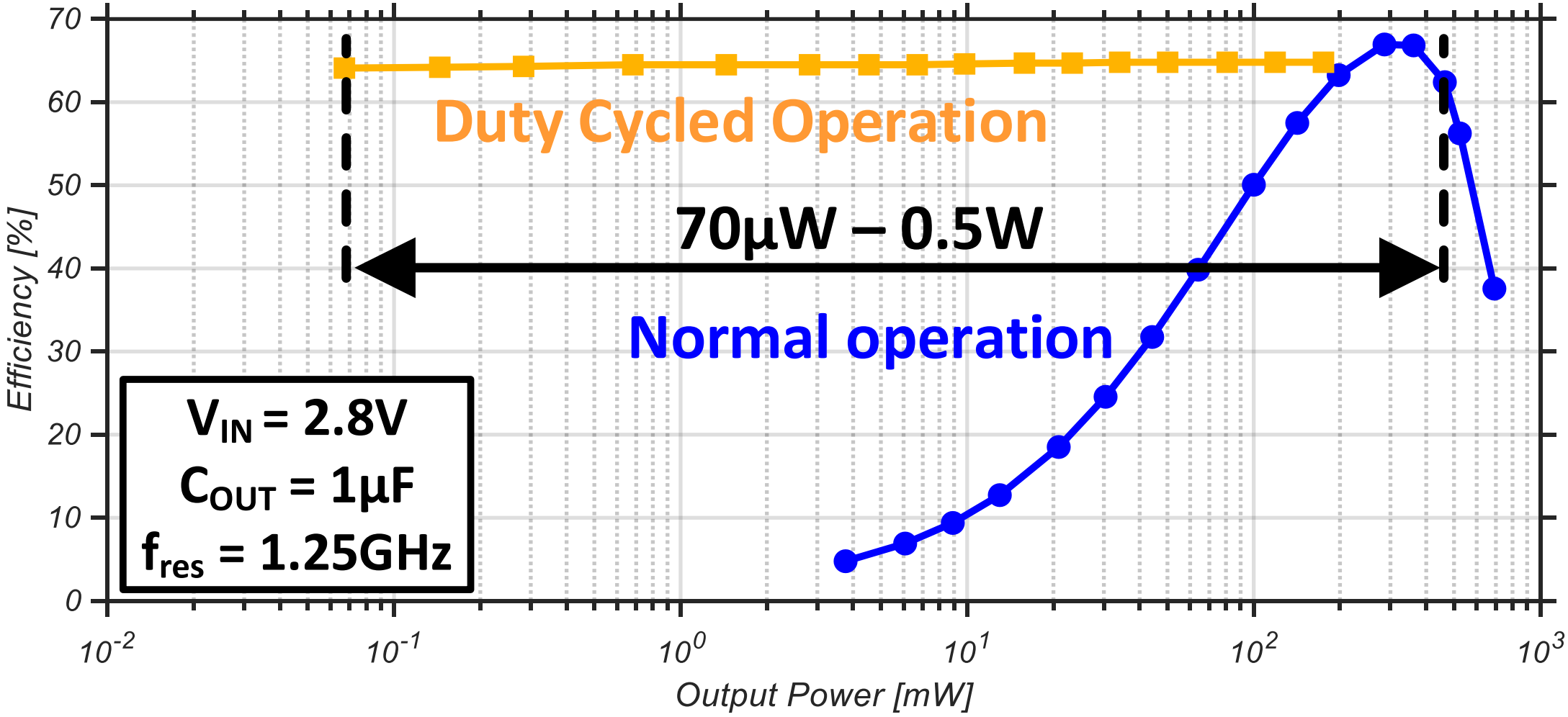
Duty Cycled



Measurement Results - Full Load



Measurement Results - Duty Cycled



Comparison Table

	Godycki ESSCIRC '14	Tang ISSCC '19	Schaef ISSCC '19	Renz ISSCC '19	McLaughlin ISSCC '20	**This Work HIGH EFF**	**This Work HIGH PD**
Topology	3-level Buck	SIC	Buck	ReSC	ReSC	**EM-coupled class-D LC**	**EM-coupled class-D LC**
Technology	65nm	65nm	14nm	130nm	180nm	**180nm**	**180nm**
f_{SW} (GHz)	not reported	0.45	0.07	0.0355	0.0475	**1.25**	**2.5**
V_{IN} (V)	1.8	1.2	1.6	3.0 - 4.5	2.4 - 4.4	**1.0 – 3.6**	**1.0 – 3.0**
V_{OUT} (V)	0.7	0.6 - 0.9	1.2	1.5 - 1.8	1.0-2.2	**0.4 – 1.6**	**0.4 – 1.3**
L_{TOT} (nH)	2 x 1.5	0.85	2.5 package	9	7.7 coupled	**7.8 coupled**	**3.1 coupled**
$C_{FLY,TOT}$ (nF)	2 x 1.5	1.72	-	2x1.0	2x 1.7	**2x 0.229**	**2x 0.076**
C_{IN} (nF)	not reported	not reported	not reported	0.18+off-chip	7	**0**	**0**
C_{OUT} (nF)	1.9	3.1	10 + off-chip	10	7	**0**	**0**
Area (mm^2)	2.09	0.65	2.16	7.83	8.93	**1.61**	**0.37**
Peak Eff (%) @P_{DENS} (W/mm^2)	64 0.067	78 0.55	88 0.28	85.5 0.033	85.5 0.053	**67** **0.21**	**58.1** **0.88**
Peak P_{DENS} (W/mm^2) @Eff (%)	0.067 64	0.73 74.6	0.28 88	0.033 85	0.097 74.5	**0.30** **65.2**	**1** **57.5**

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Conclusion

- **Proposed converter architecture**
  - Fully Integrated DC-DC converter
  - Adiabatic switching of C_{BOT} & C_G enabling GHz-range f_{SW}
  - No timing, shifters and bootstrap circuitry needed
  - No load capacitor needed in full load operation
- **Performance**
  - 1 W/mm^2 peak power density
  - Wide 70µW – 0.5W load range with duty-cycled operation

Key References

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