IC Chip and Packaging Interactions in Design for SI, PI, EMC and ESD

Makoto Nagata

Kobe University
Graduate School of Science, Technology and Innovation

April 22nd, 2021
in Switzerland Chapter

About Prof. Dr. Makoto Nagata

Hardware Security and Safety
Secafy

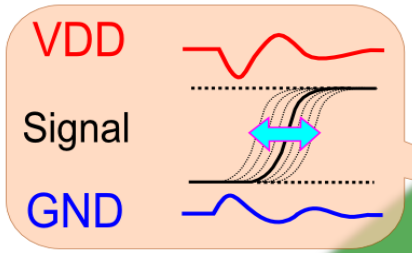
1. 1991, 1993, B.S., and M.S. degrees in physics from the Gakushuin University, Tokyo.
2. 2001 Ph.D. in electronics engineering from Hiroshima University, Hiroshima.
3. 2002-2009, Associate professor at Kobe University
4. 2009, Full professor at Kobe University
5. 2020 - SSCS AdCom member
6. Distinguished contribution to SSCs

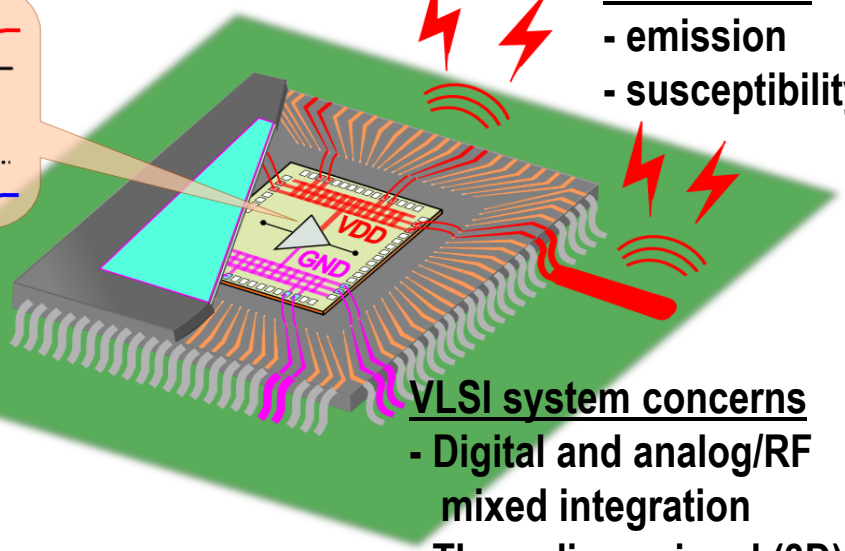
http://www.edu.kobe-u.ac.jp/stin-secafy/

Outline

1. Introduction
2. Power noise simulation and diagnosis techniques
3. Power noise problems and solutions in advanced packaging
4. Summary

Power noise problems



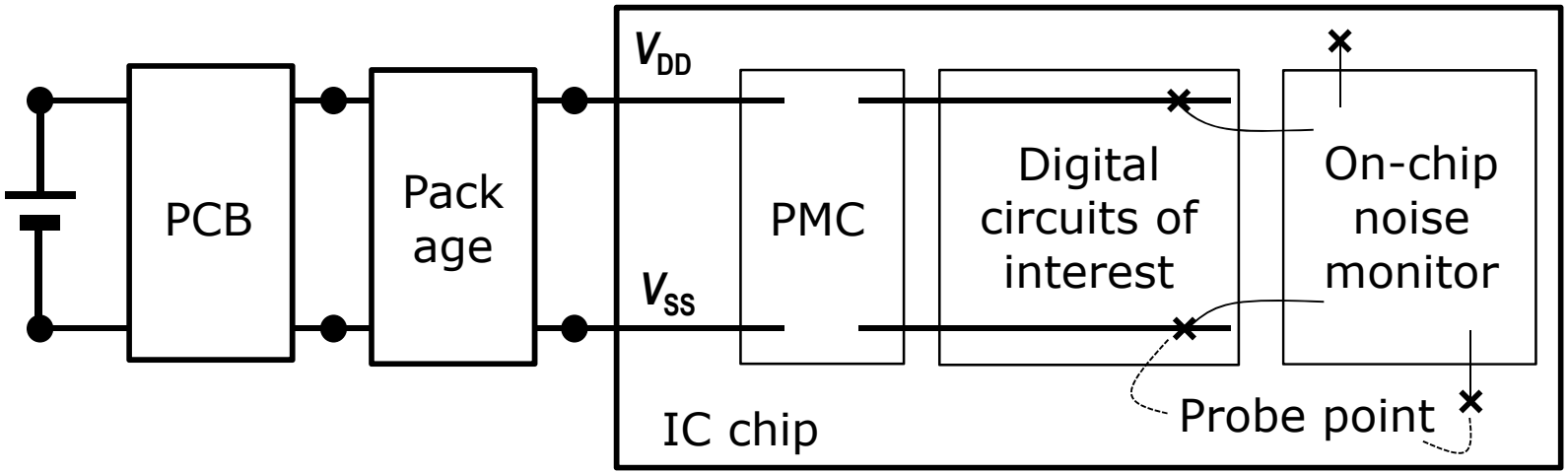


EMC issues
- emission
- susceptibility

Chip issues
- Power integrity (PI)
- Signal integrity (SI)
- Substrate noise (SN)
- Timing variation
- Performance degradation
- Operation failures

VLSI system concerns
- Digital and analog/RF mixed integration
- Three dimensional (3D) heterogeneous integration

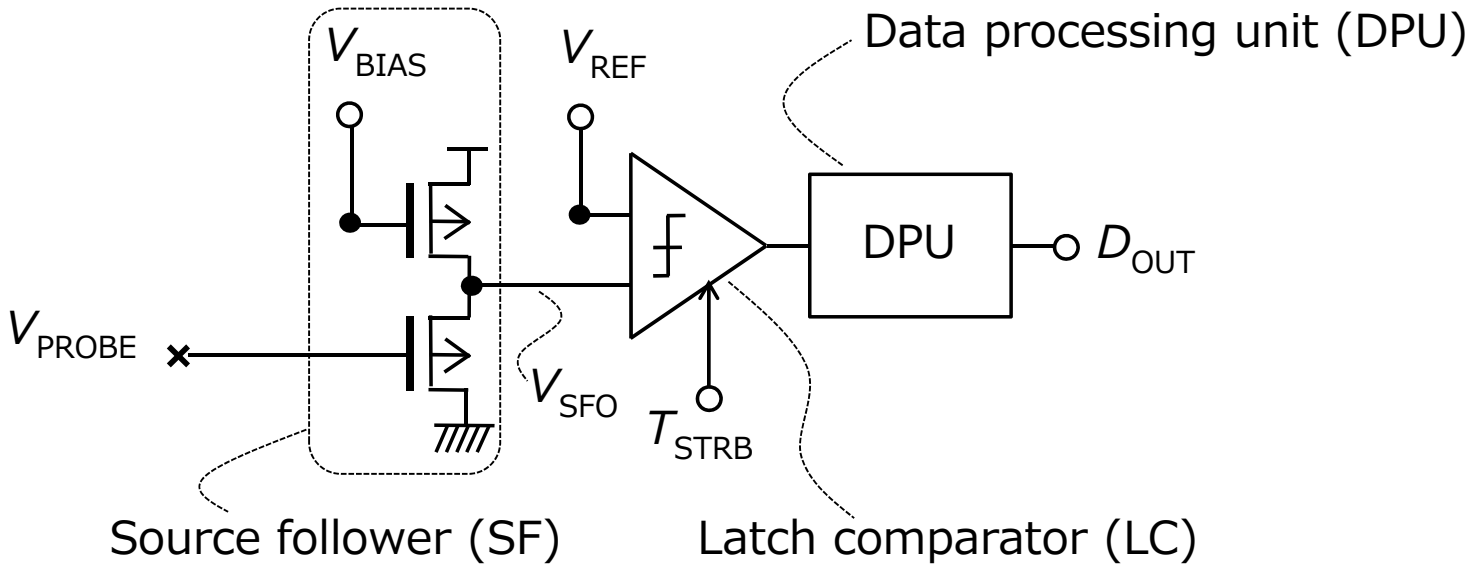
Power noise analysis and diagnosis



- Analysis: full-system level power noise simulation using C-P-S*1 models
- Diagnosis: on-chip power noise measurements using OCM*2

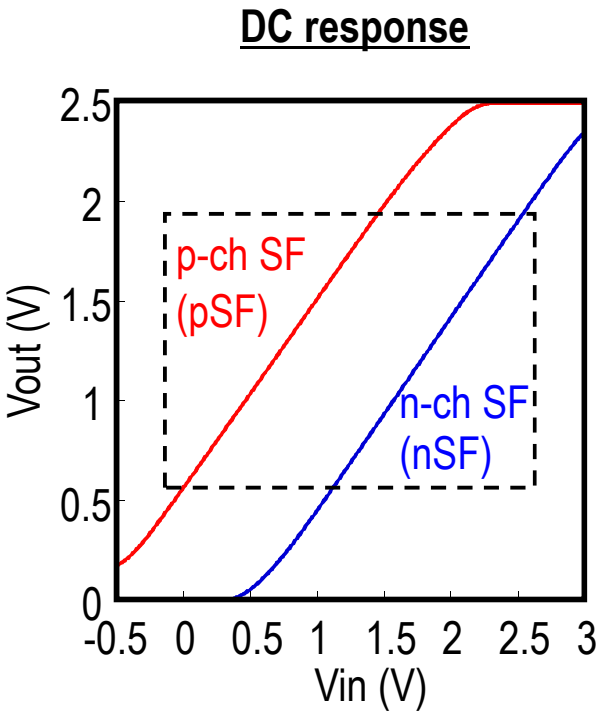
*1Chip-package-system board *2On-chip noise monitor

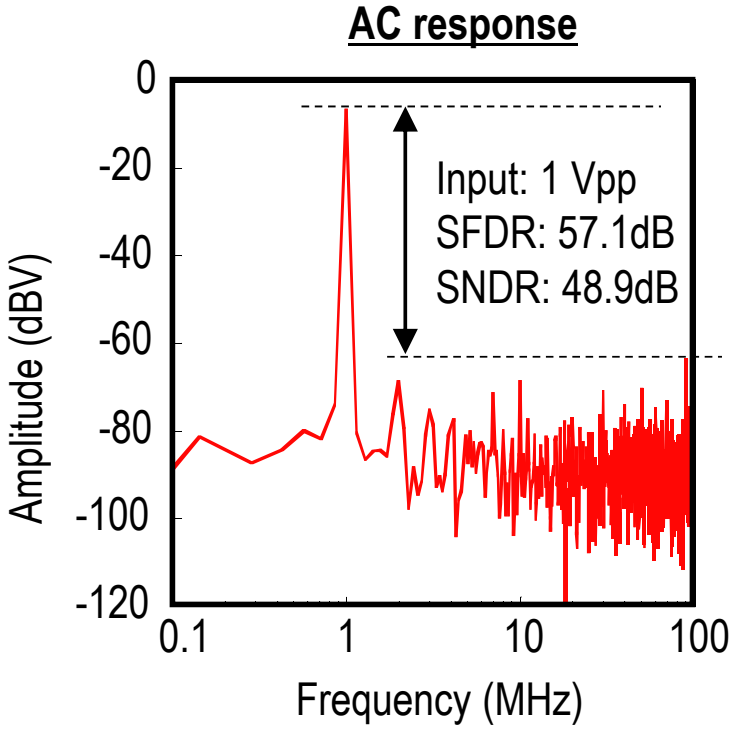
On-chip power noise monitoring



M. Nagata *et al.*, "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment," CICC 1999.

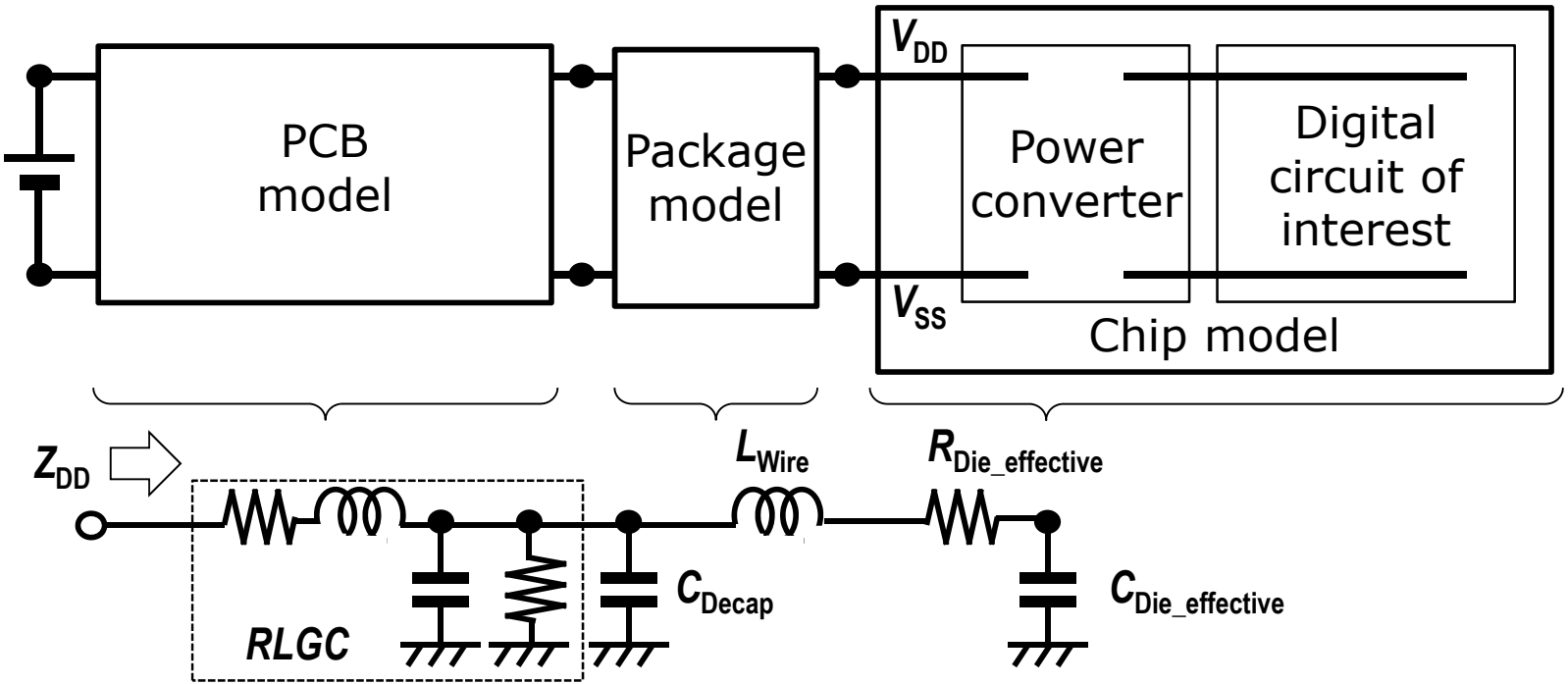
OCM typical example





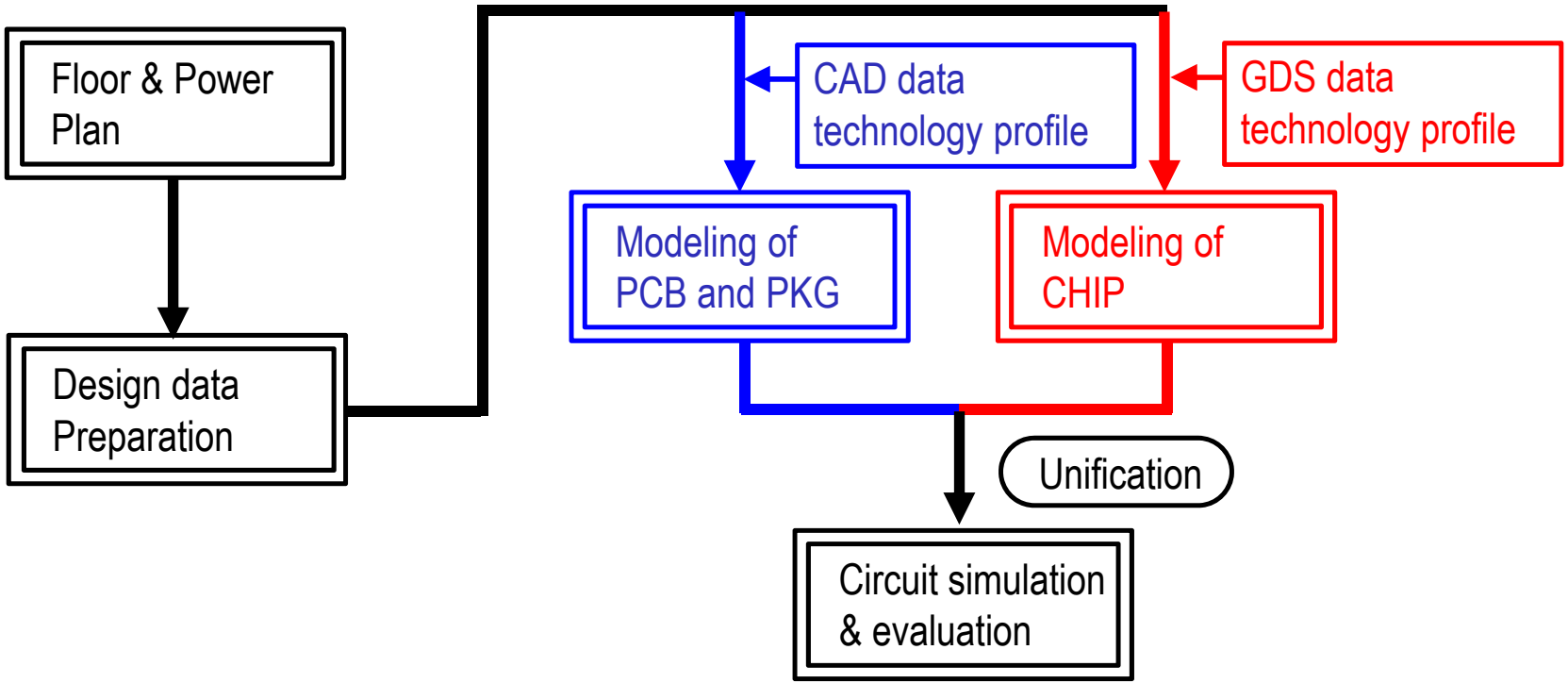
C-P-S* model for power noise analysis

*Chip-Package-System board

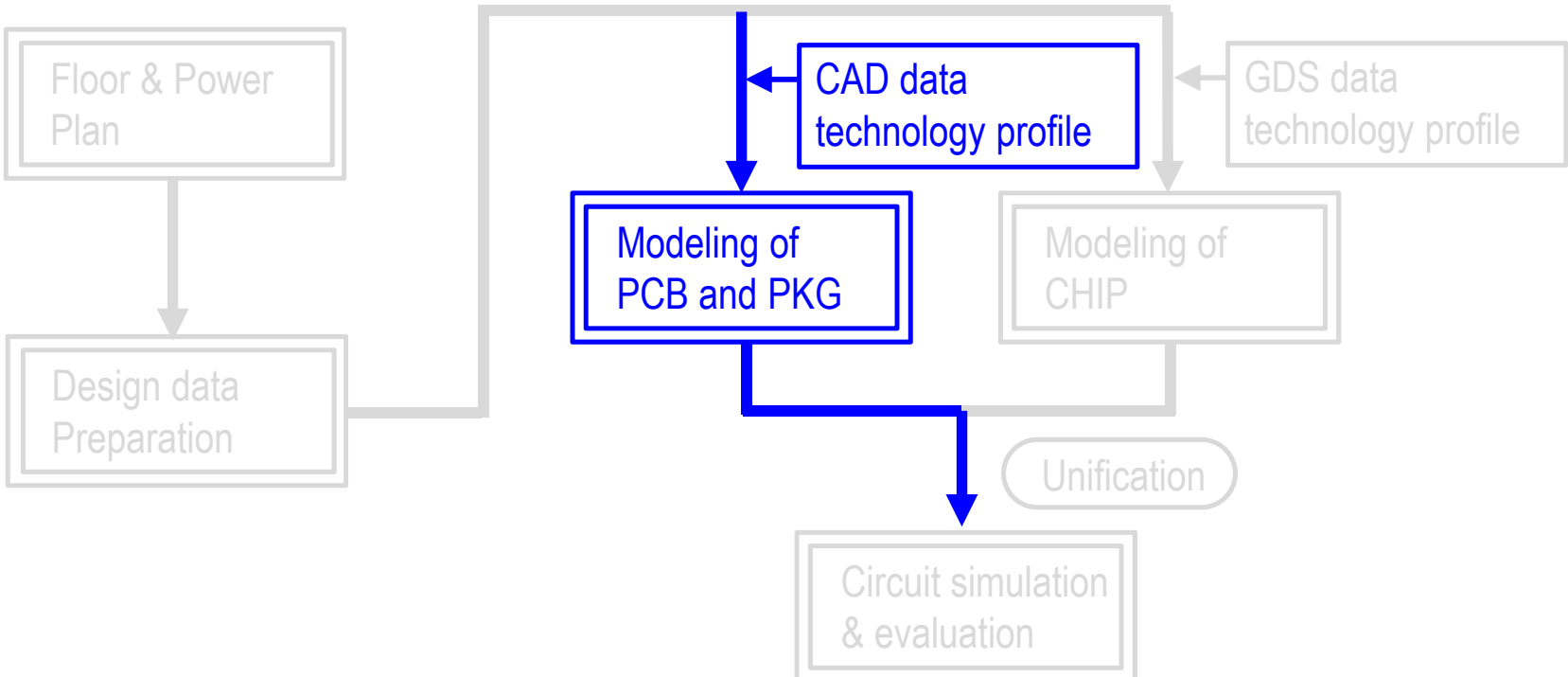


- Full-system level simulation of power-noise generation and interference

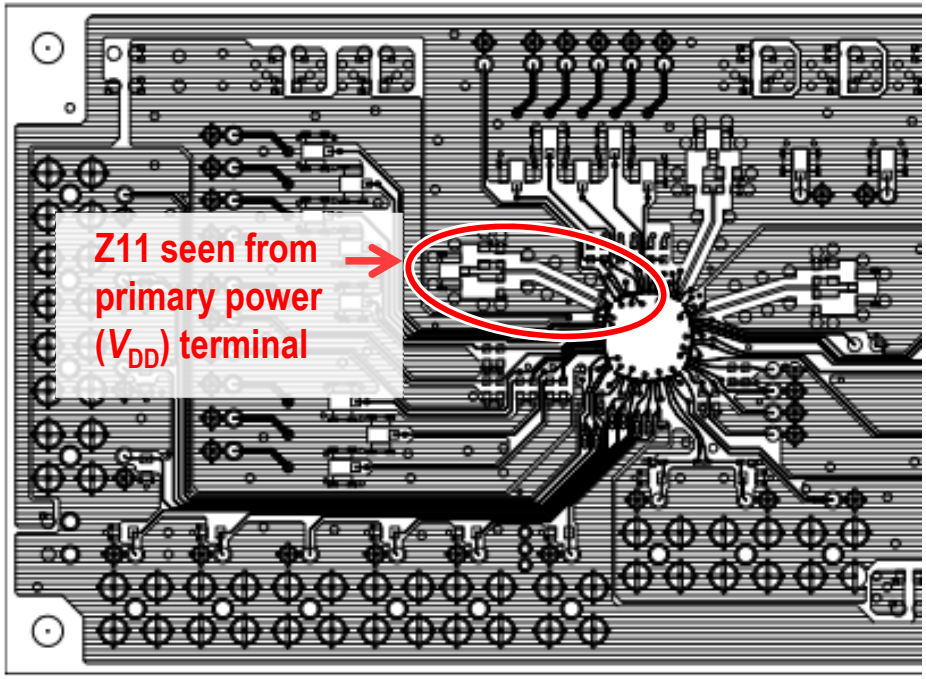
General flow of C-P-S modeling

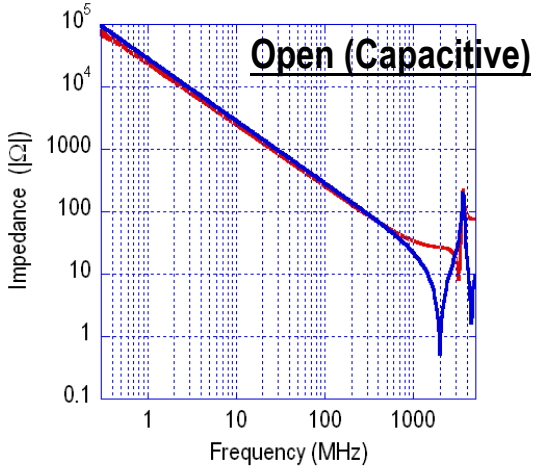


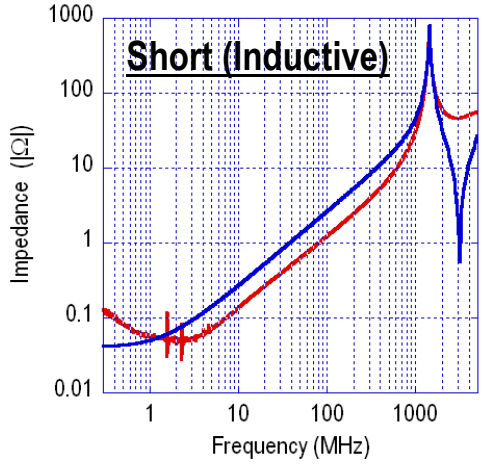
General flow of C-P-S modeling



PCB impedance

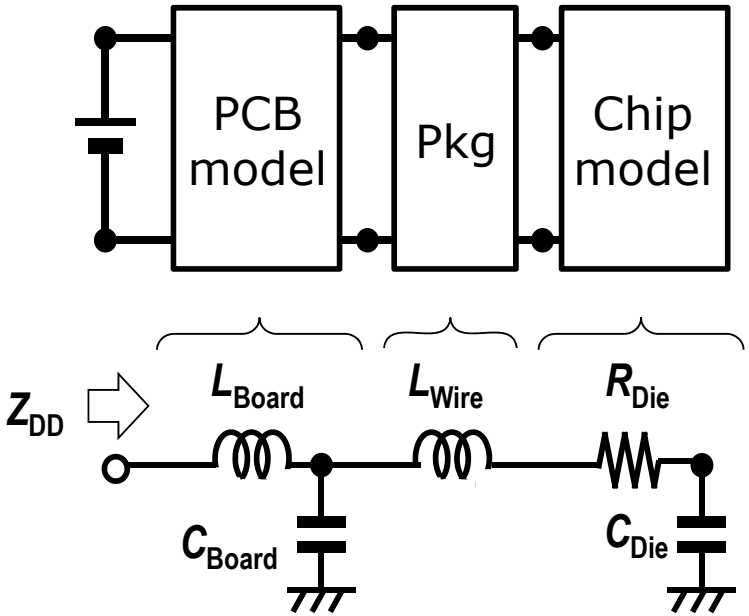


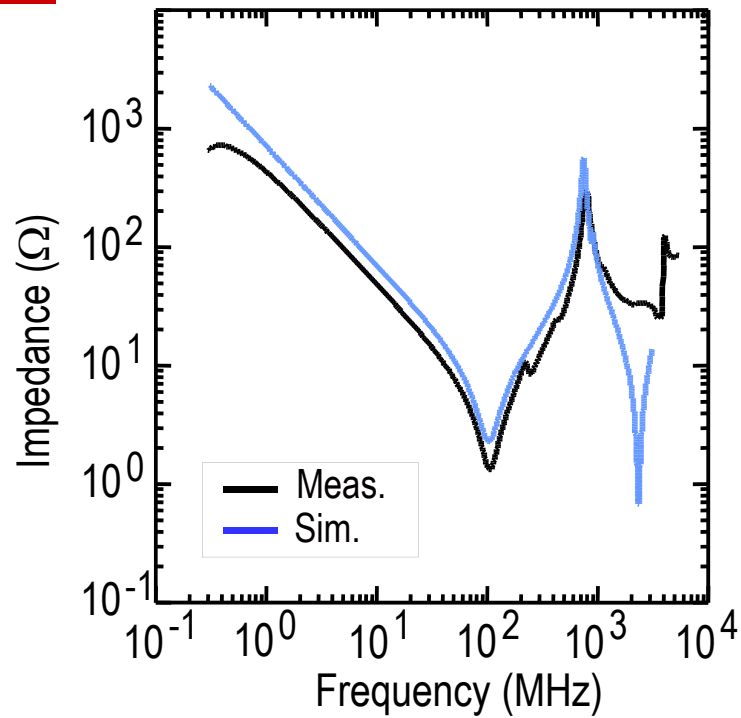




- Full-wave EM simulator solves PCB with FR-4 multiple layers.

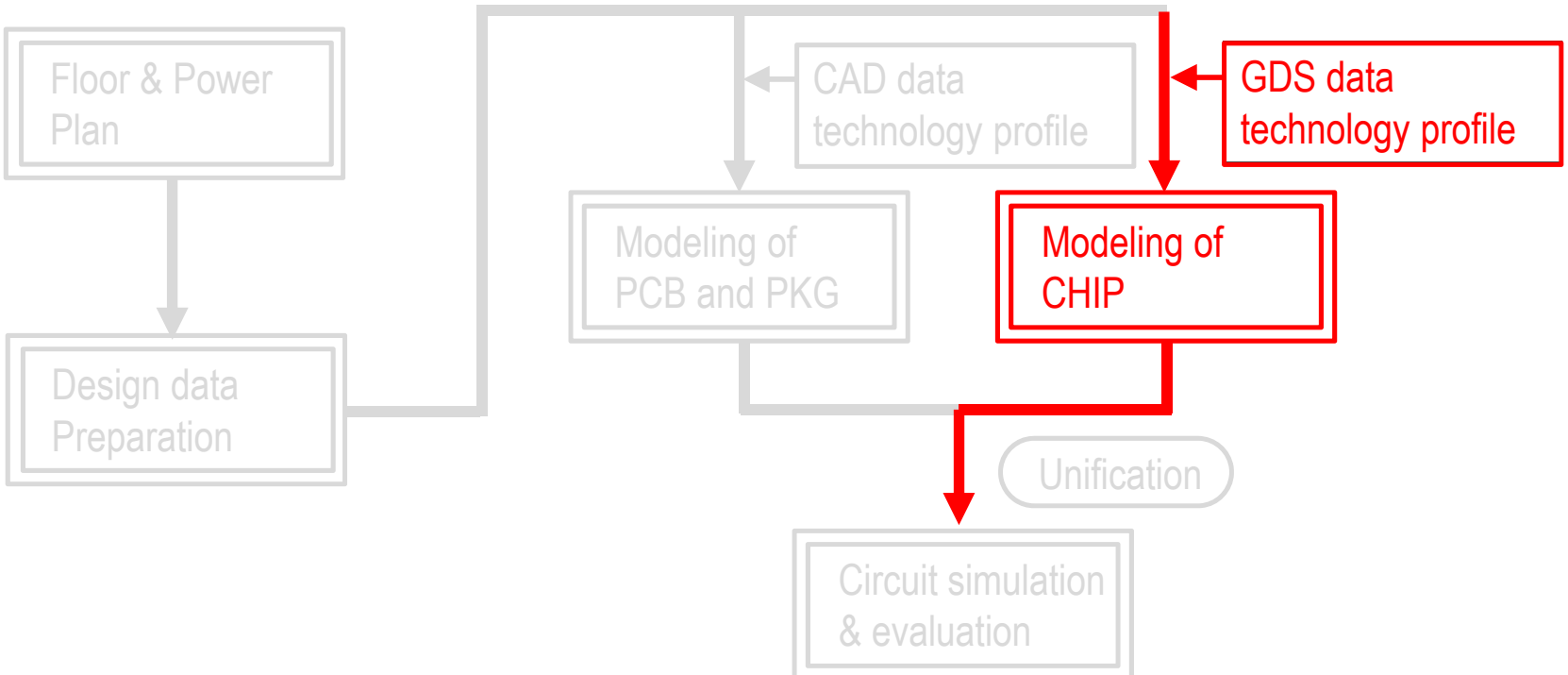
PDN impedance model



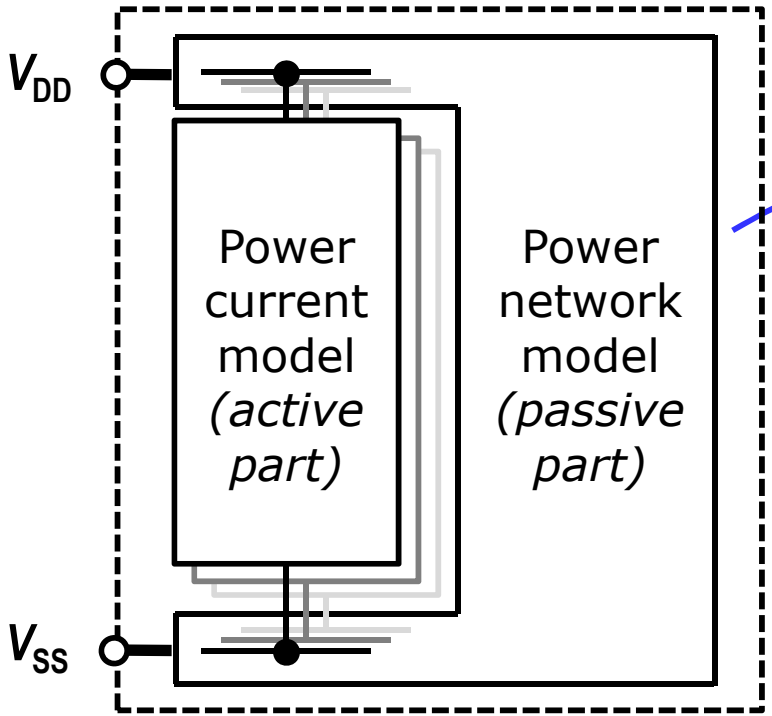


- C-P-B integrated passive model, capturing AC impedance seen from power source side (VDD)

General flow of C-P-S modeling



Chip power model

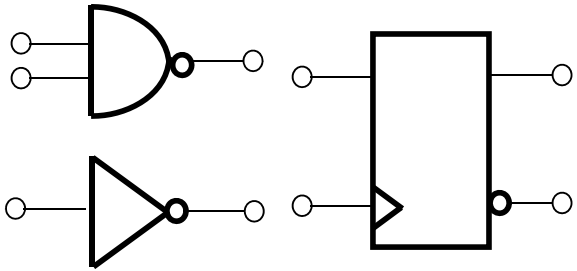


Chip power model (CPM) of either "digital circuit block" or "whole chip"

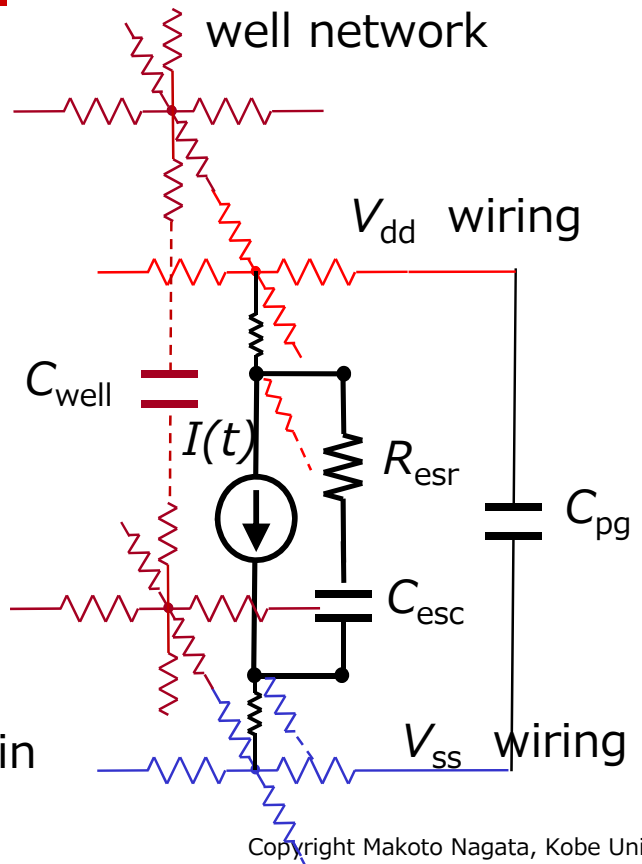
- CPM -- power delivery network involving multiple power current models

Power current model (active part)

Standard cell library (LEF/DEF)

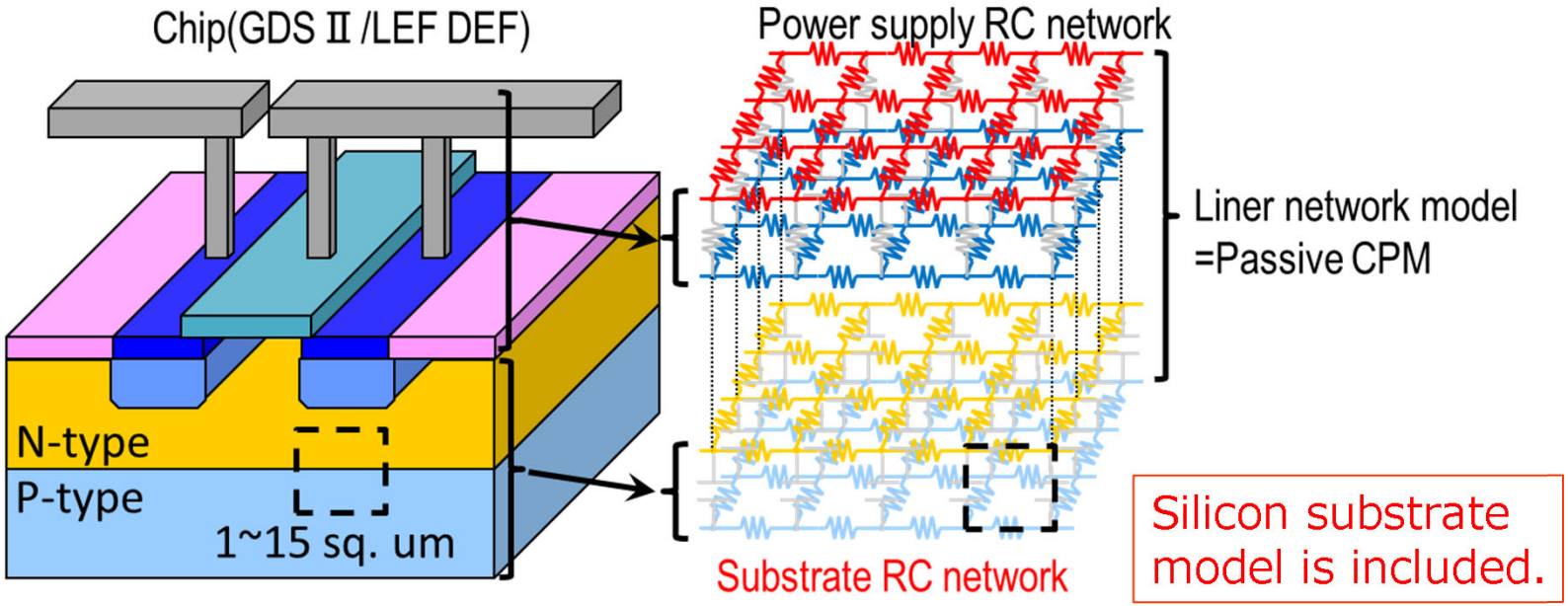


- SPICE simulation: *I(t)*
  LUT for in/out condition, load caps
- Post-layout extraction
  logic cell level: C_{esc}, R_{esr}



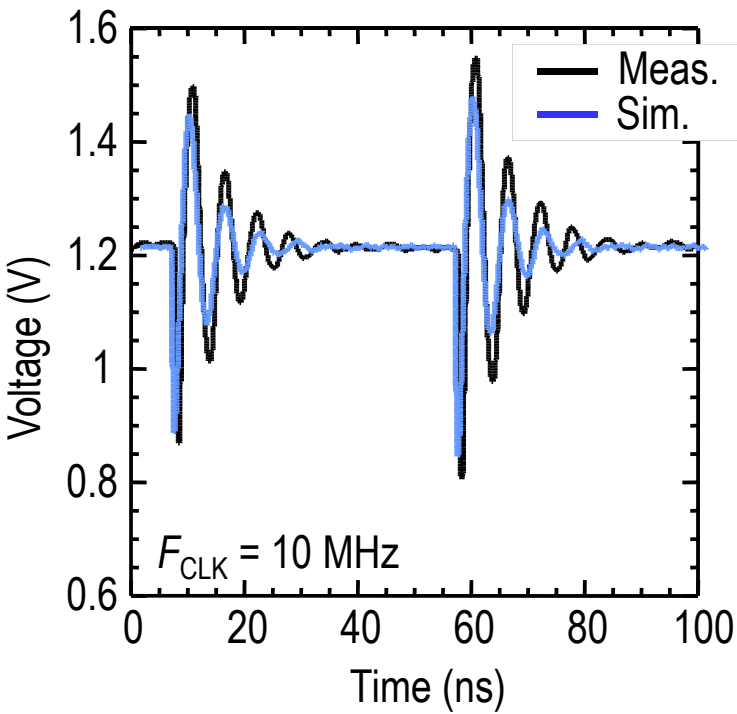
- Cell based -- Logic cells are characterized in power current model.

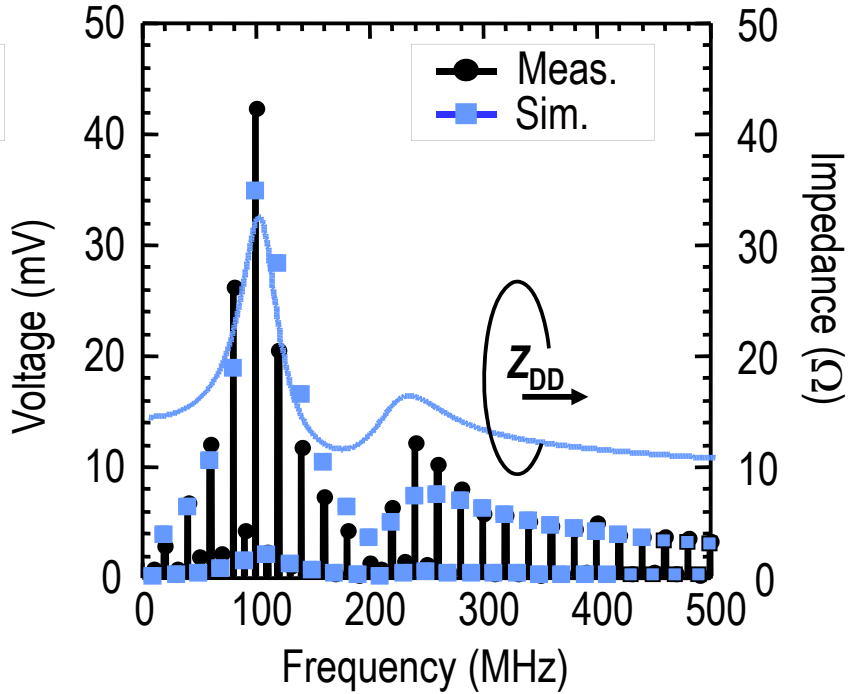
Liner network model (passive part)



- Liner network model (passive CPM) -- reduced and distributed RC network among explicit ports

Power noise: C-P-S active interaction





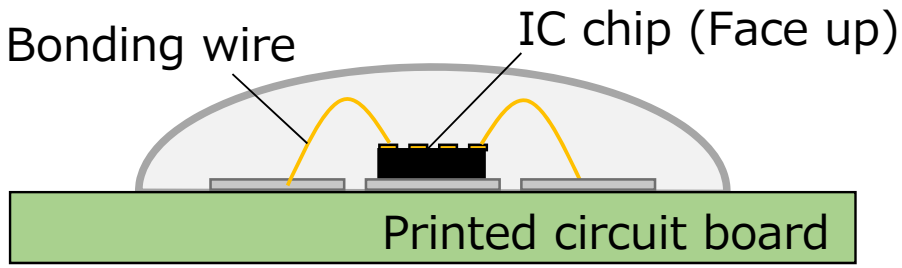
- Power current (I_{DD}, active part of IC) interacts with PDN AC impedance.
- C-P-S integrated models for power noise in IC chips and PCB

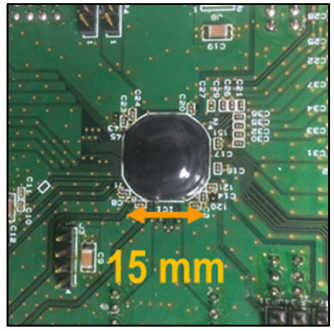
Outline

1. Introduction
2. Power noise simulation and diagnosis techniques
3. Power noise problems and solutions in advanced packaging
4. Summary

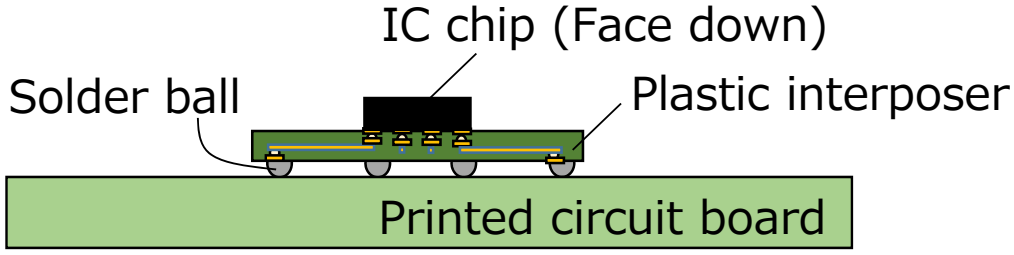
IC chip packaging (2D)

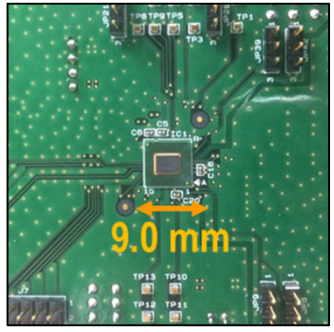
Chip on board (CoB)





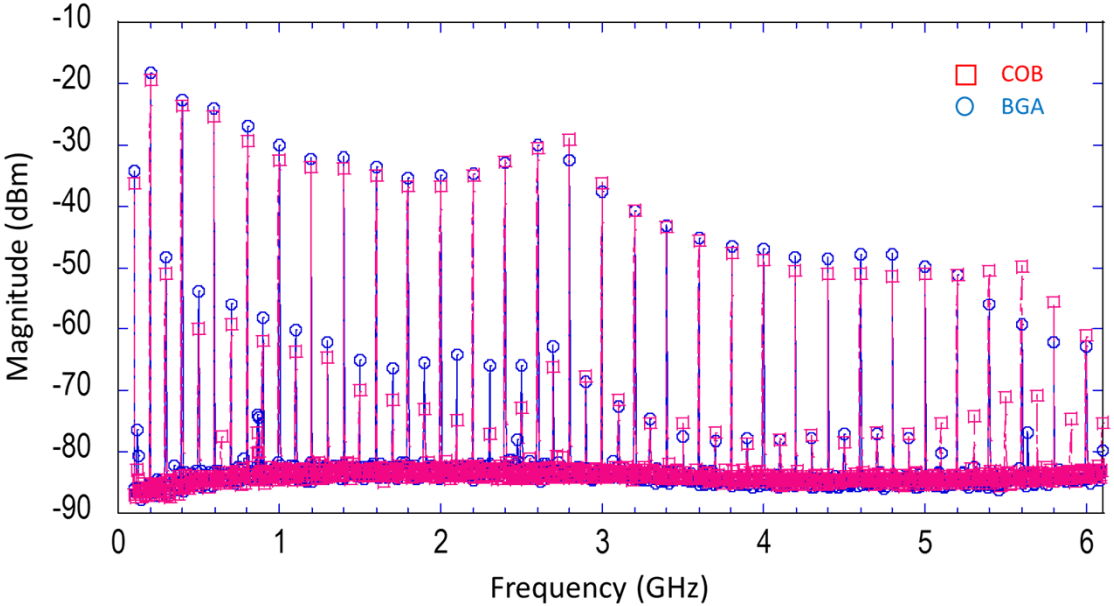
Ball grid array (BGA)

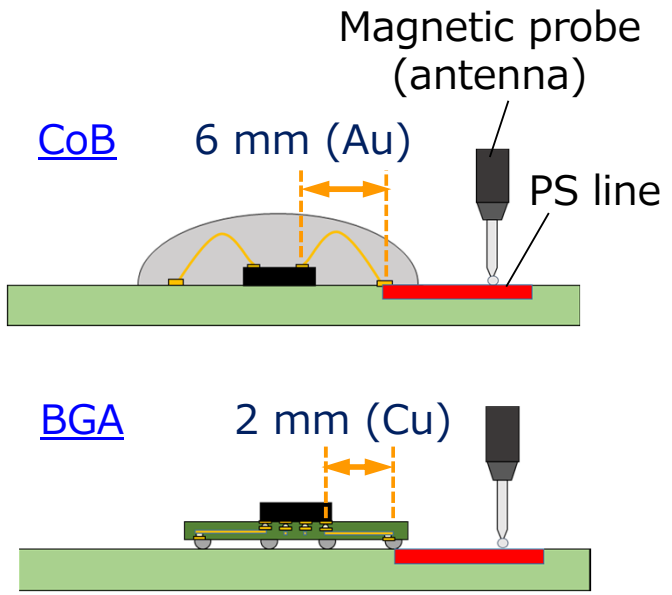




- Most popularly used IC chip packaging structures

EM noise emission (measured)

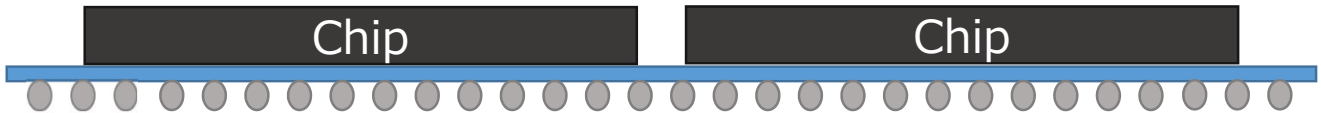




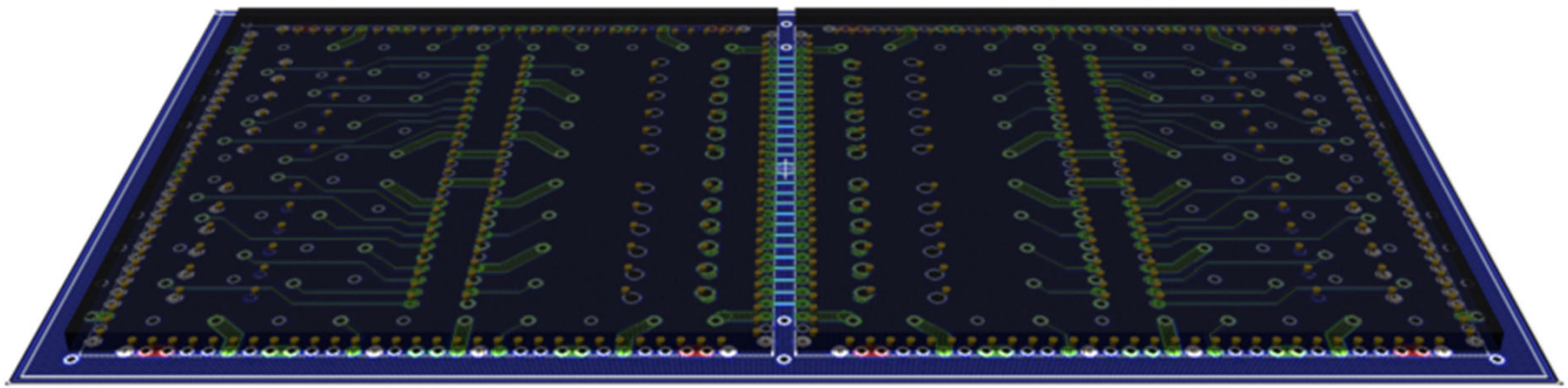
- CMOS gates switching at 100 MHz (clock signal) produce high order harmonics in electromagnetic (EM) radiation over 6 GHz.
- Insignificant difference in EM radiation among CoB and BGA packaging structures.

Fan-out packaging (2.5D)

Cross-section view

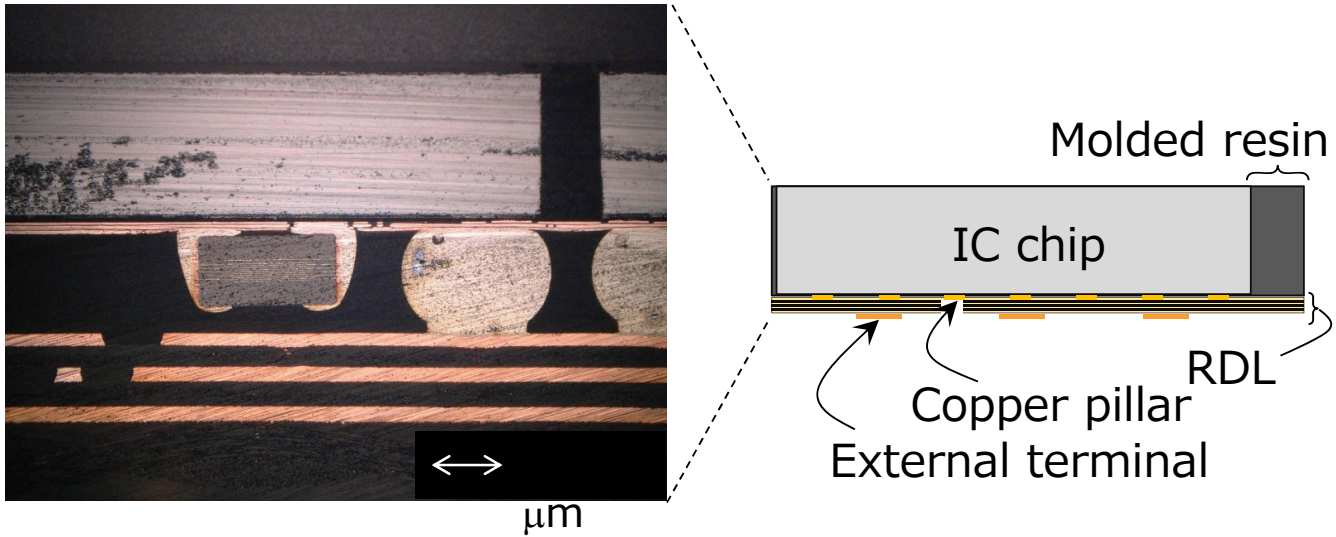


Birds view



- A thin-film, multiple layer interconnect interposer for accommodation of multiple chips in a package

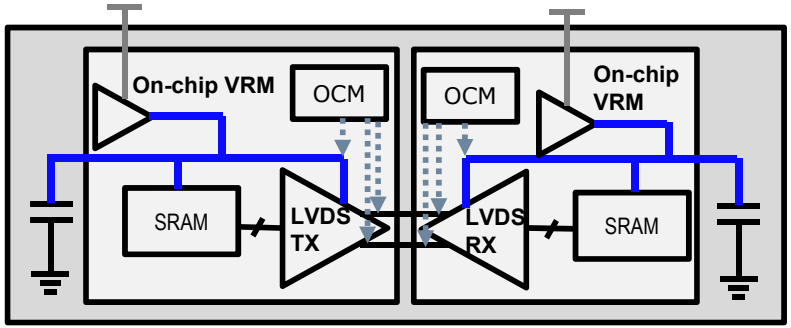
PDN with land-side capacitors



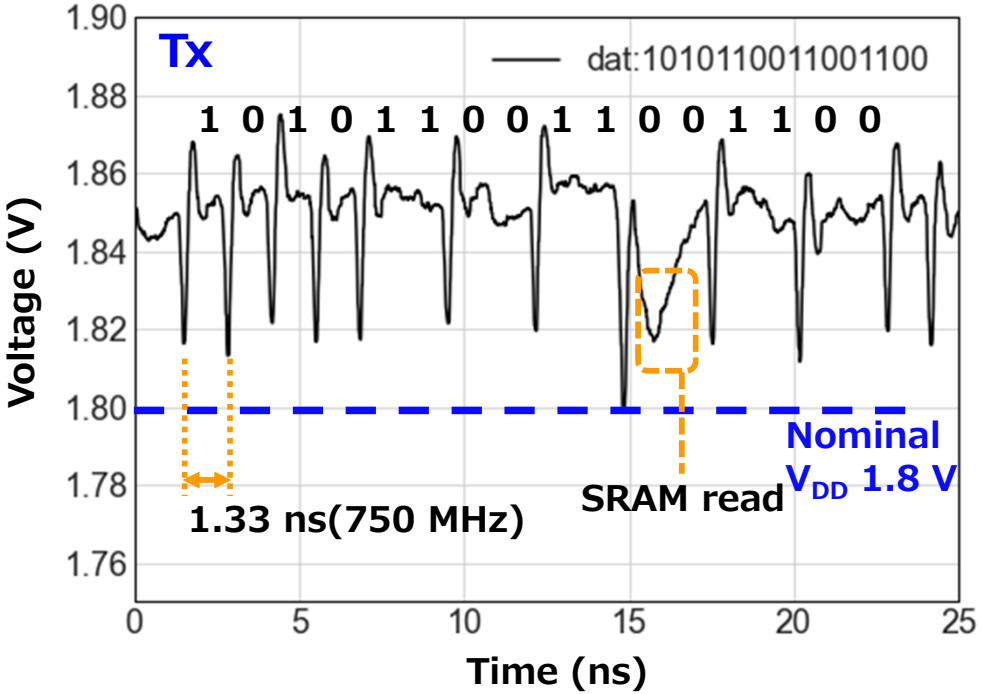
- Very proximate placements of capacitors (land-side caps) to chip pads, potentially suppressing PS noise.

H. Sonoda *et al*., "In-Place Power Noise and Signal Waveform Measurements on LVDS Channels in Fan-Out Multiple IC Chip Packaging," EMC Compo 2019.

On-chip waveforms in FO package

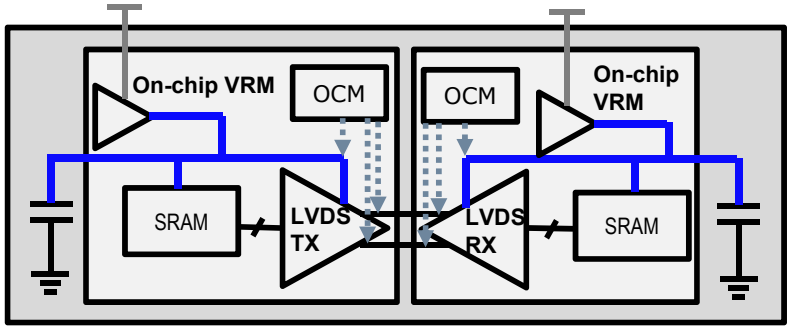


Data pattern : 1010110011001100
Clock frequency : 750 MHz
Voltage resolution : 100 μV
Time resolution : 10 ps

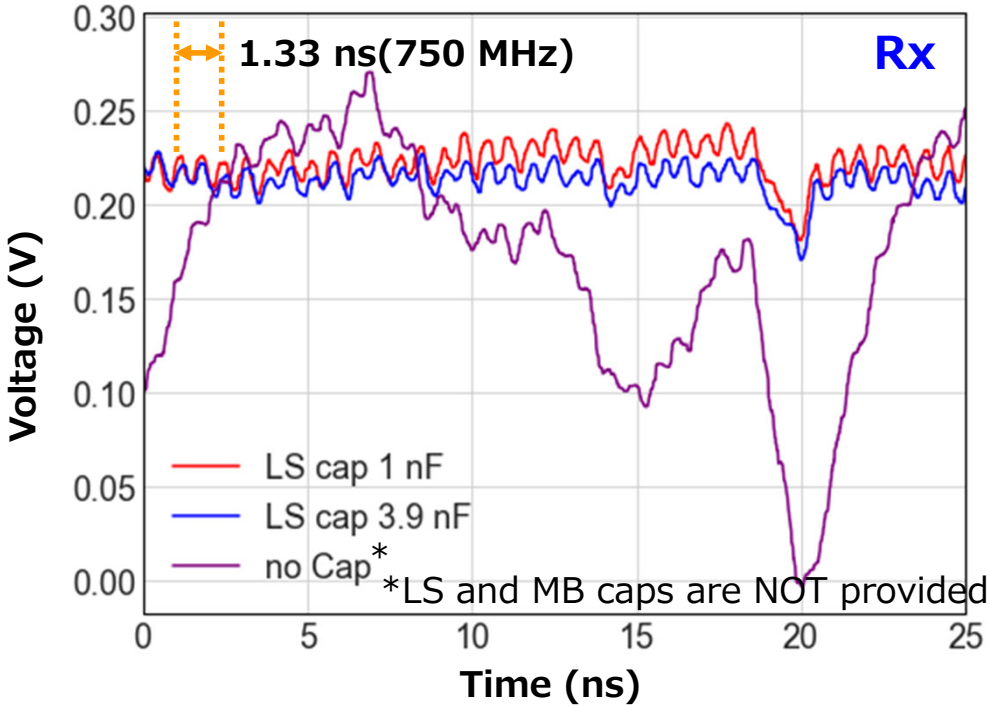


- In-place waveforms over V_{DD} of LVDS channels (Tx) within fan-out packaging

Power noise suppression by LS caps

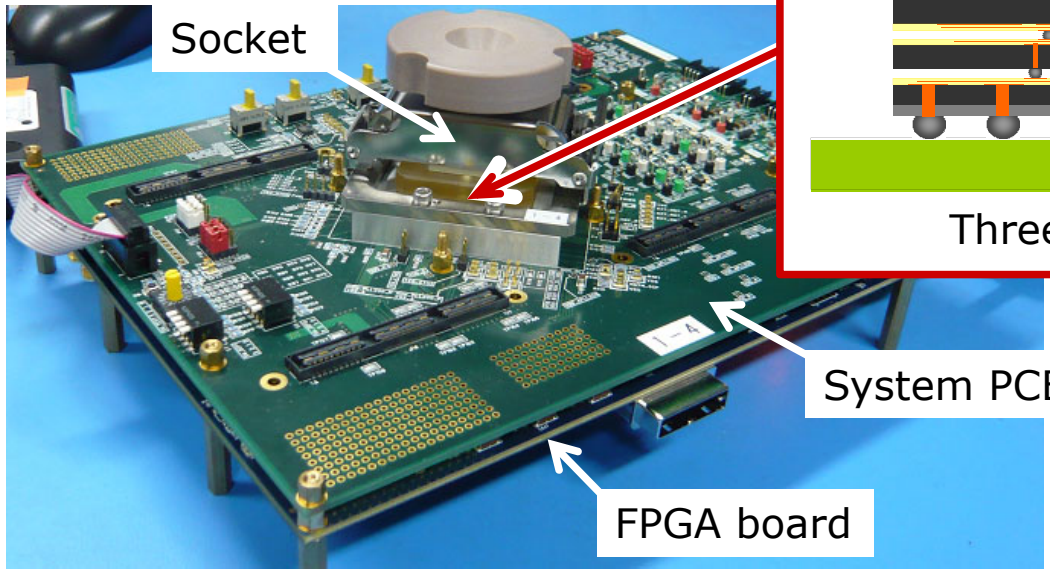


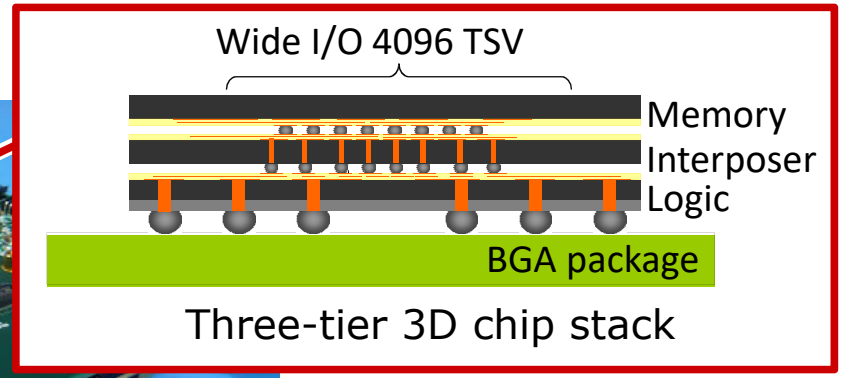
Data pattern : 1010110011001100
Clock frequency : 750 MHz
Voltage resolution : 100 μV
Time resolution : 10 ps



- Fan-out landside (LS) caps attenuate dynamic power noise within IC chips.

Wide I/O test vehicle (3D)



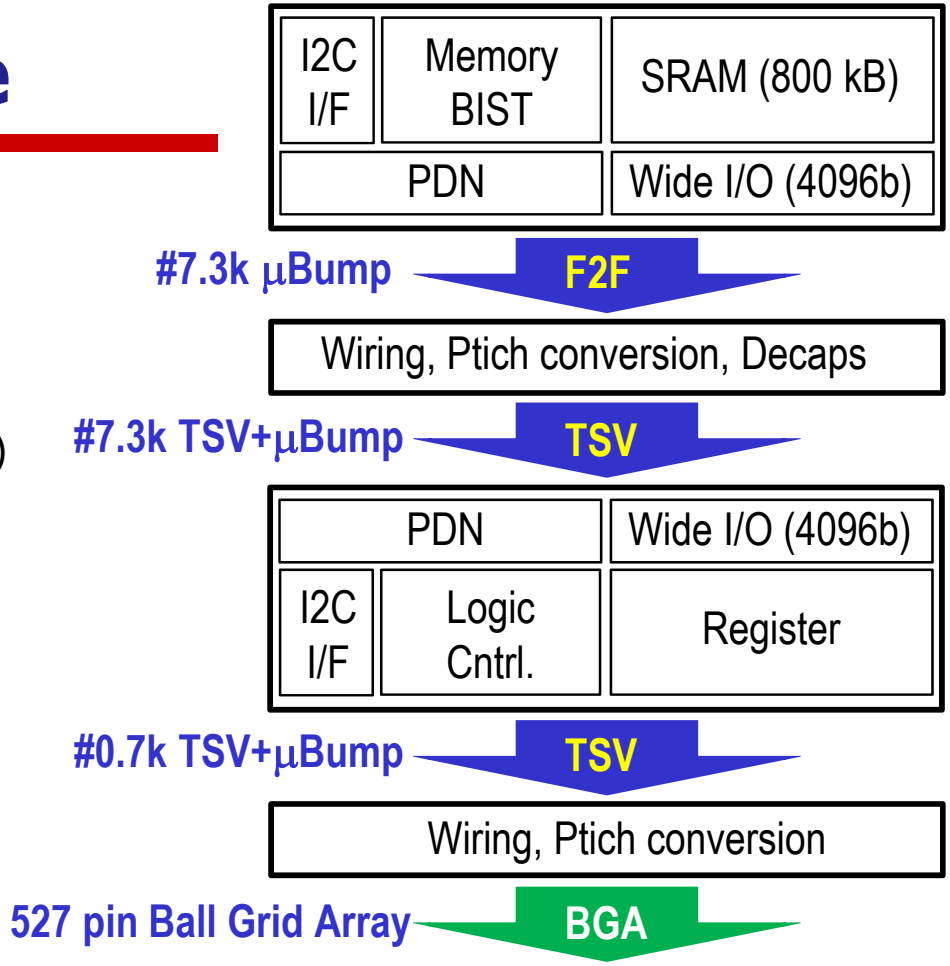


- 3D TSV chip stack demonstrator featuring 4096b Wide I/O at 100 GB/s

S. Takaya *et al.*, "A 100GB/s Wide I/O with 4096b TSVs Through an Active Silicon Interposer with In-Place Waveform Capturing," ISSCC 2013.

Stack structure

- Silicon technology
  - 90 nm CMOS, 8LM, 1.2 V
  - 9.9 mm x 9.9 mm
  - Mem. chip (1.8 Mgate, 800 kB)
  - Interposer
  - Logic chip (1.8 Mgate)
- Organic substrate
  - FR4, 8 layer
  - 26 mm x 26 mm



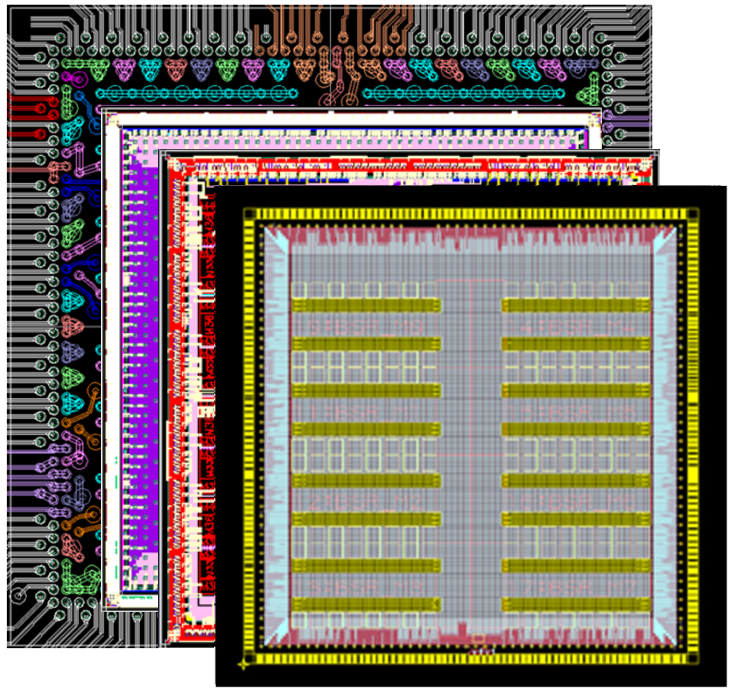
Stack operation and performance

- Operation modes:
  - Memory write (Logic → Mem)
  - Memory read (Mem → Logic)
  - BIST (Fail bit capture)
  - PLL clocking/external clocking
  - Setting up from I2C

  *All signaling through TSVs
- Maximum operation frequency:

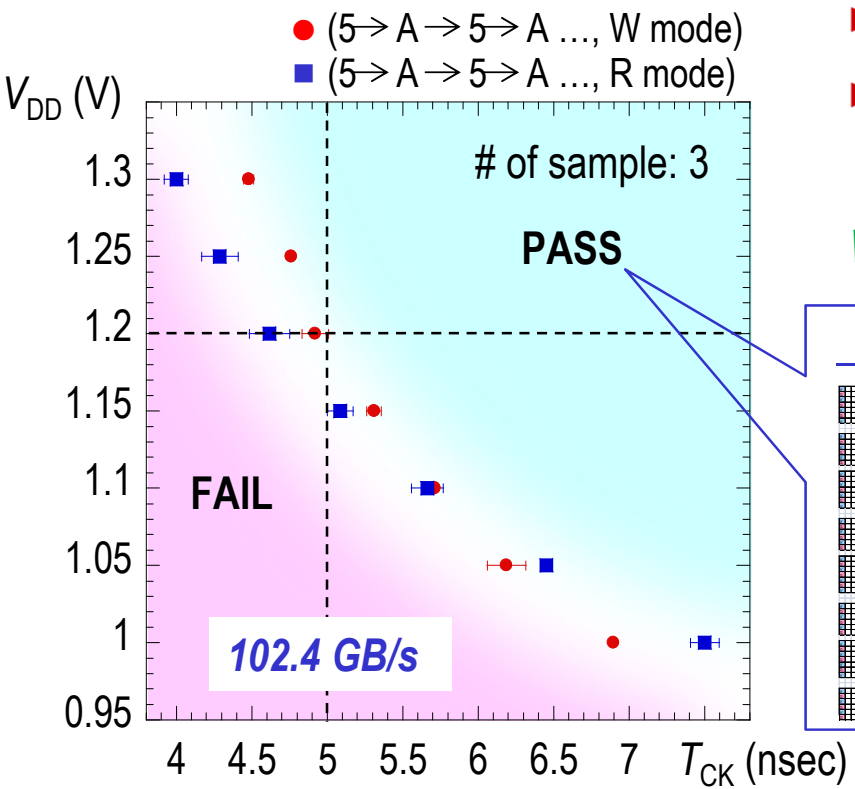
  200 MHz (typical), 100 Gbyte/sec
- Power consumption (wide I/O bus) :

  0.56 mW/Gbps at 1.2 V



Layout view of 3D chip stacks after physical synthesis.

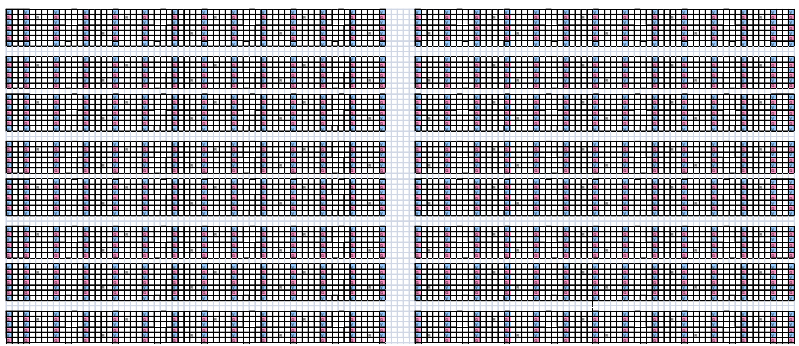
Demonstrated performance



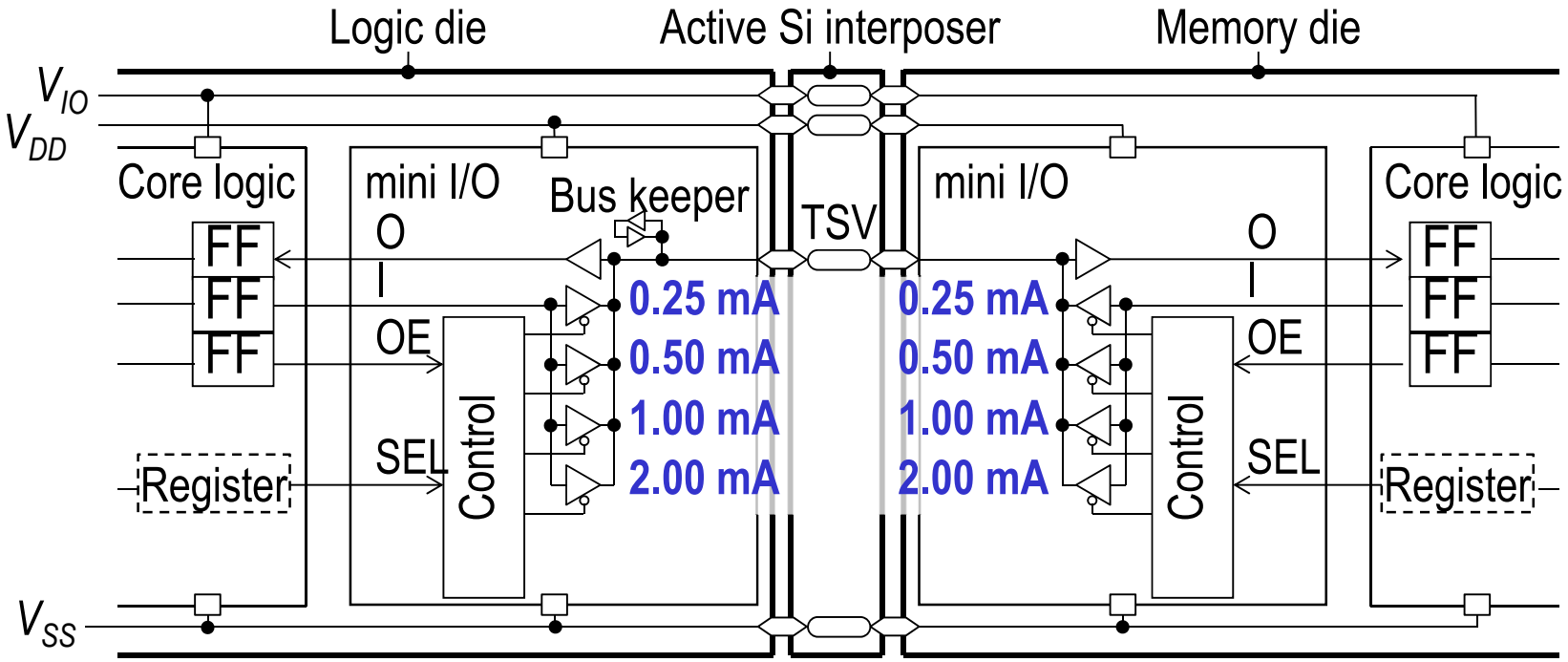
- 102.4 GB/s at 1.2 V
- 0.56 mW/Gbps, 0.56 pJ/bit (0.5 mA driving strength)

World-top energy efficiency (2013)

BIST fail map: no errors exist

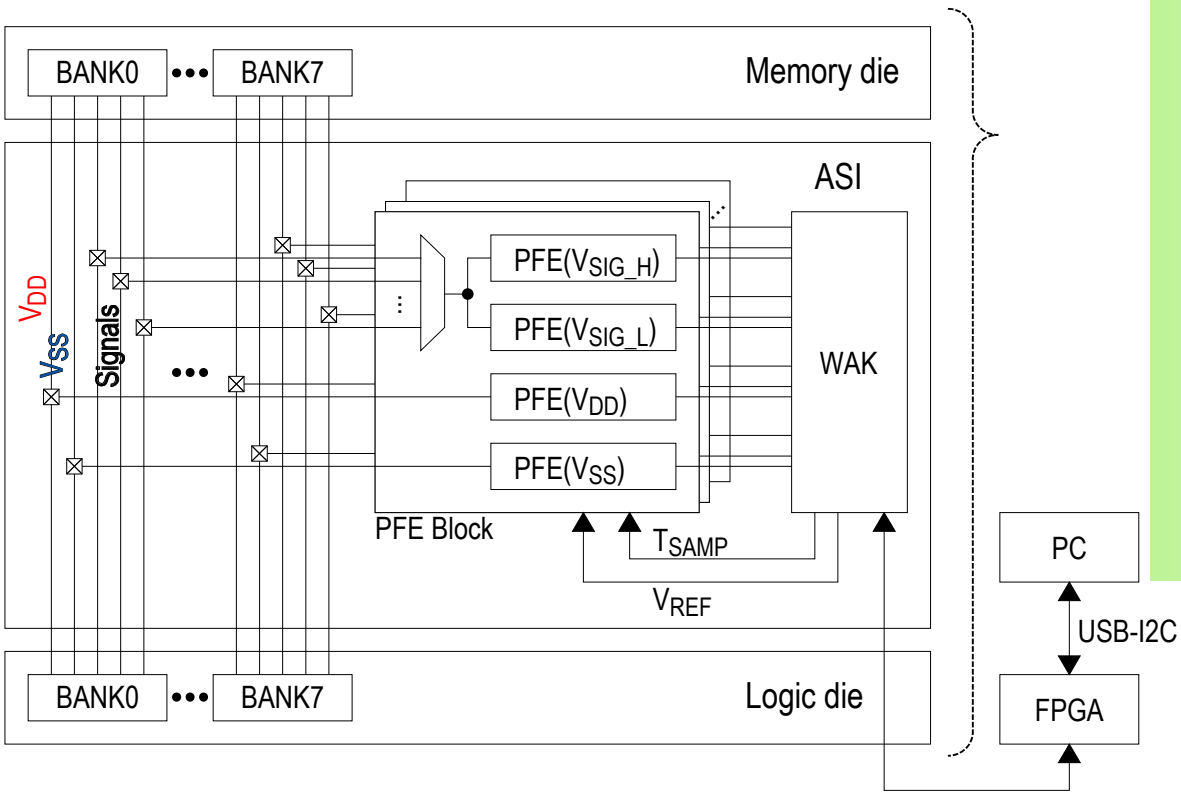


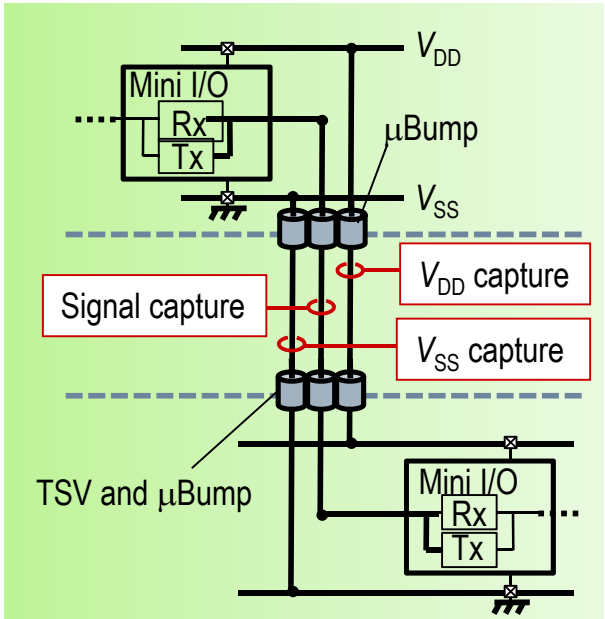
Mini I/O circuit schematic



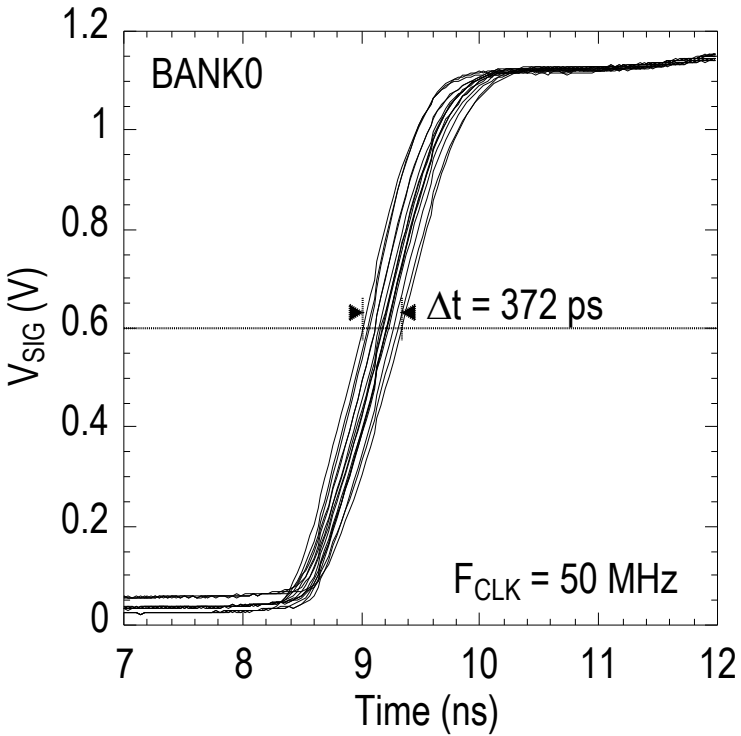
- Mini I/O circuit consists of a pair of driver & receiver buffers.
- The driver has 4 levels of drive strengths for adaptability to TSV properties.

In-place monitoring in 3D chip stack

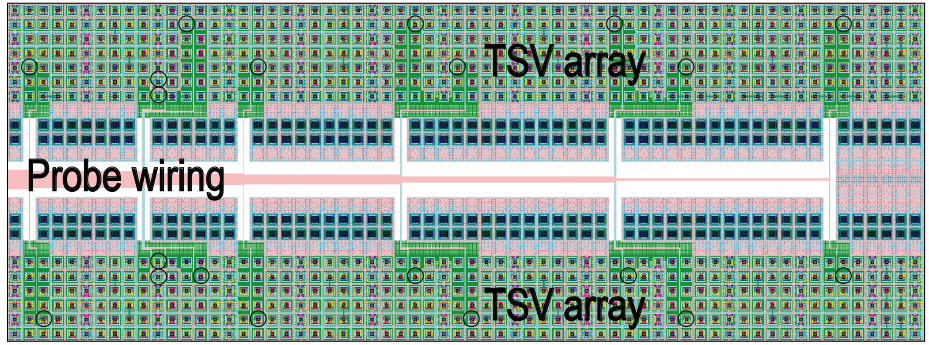




Signal skew in 3D stack



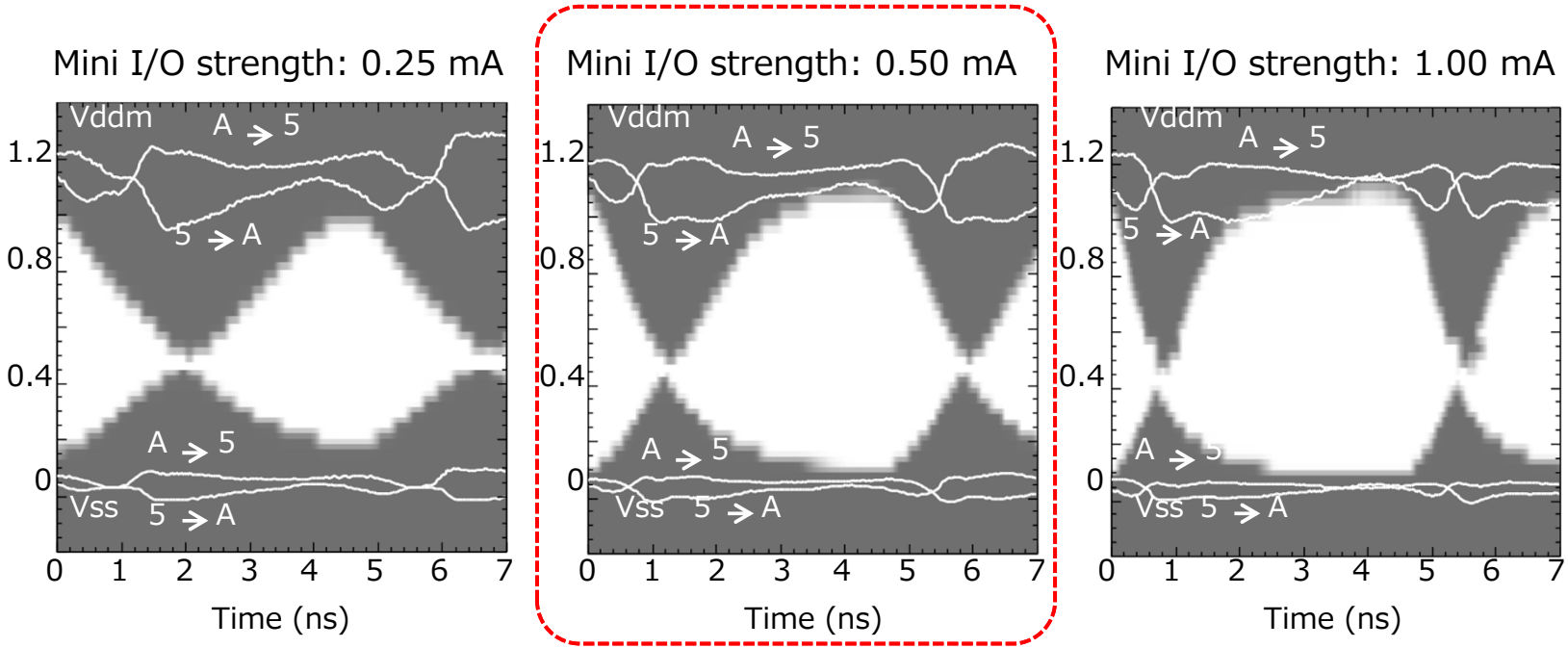
16 vertical channels in 512-bit BANK



○: Redundancy channel TSVs
○: Monitored power supply TSVs

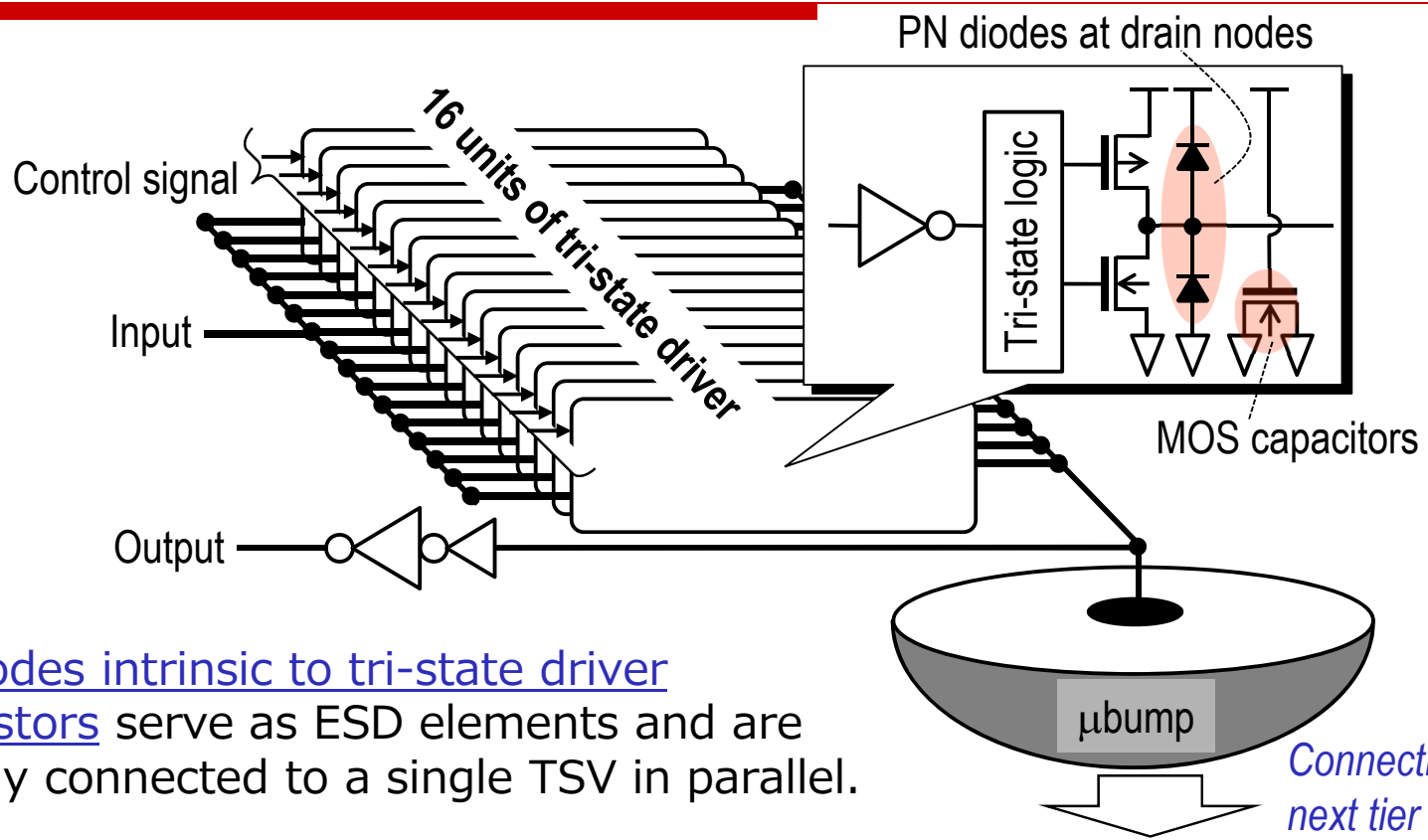
- Redundant channel (32:1) is tapped by on-chip monitor channel
- No degradation found in data rate

In-place captured eye diagrams



- Wider eye-opening for higher driving strength
- The dynamic power noise remains less than 20% of signal swing

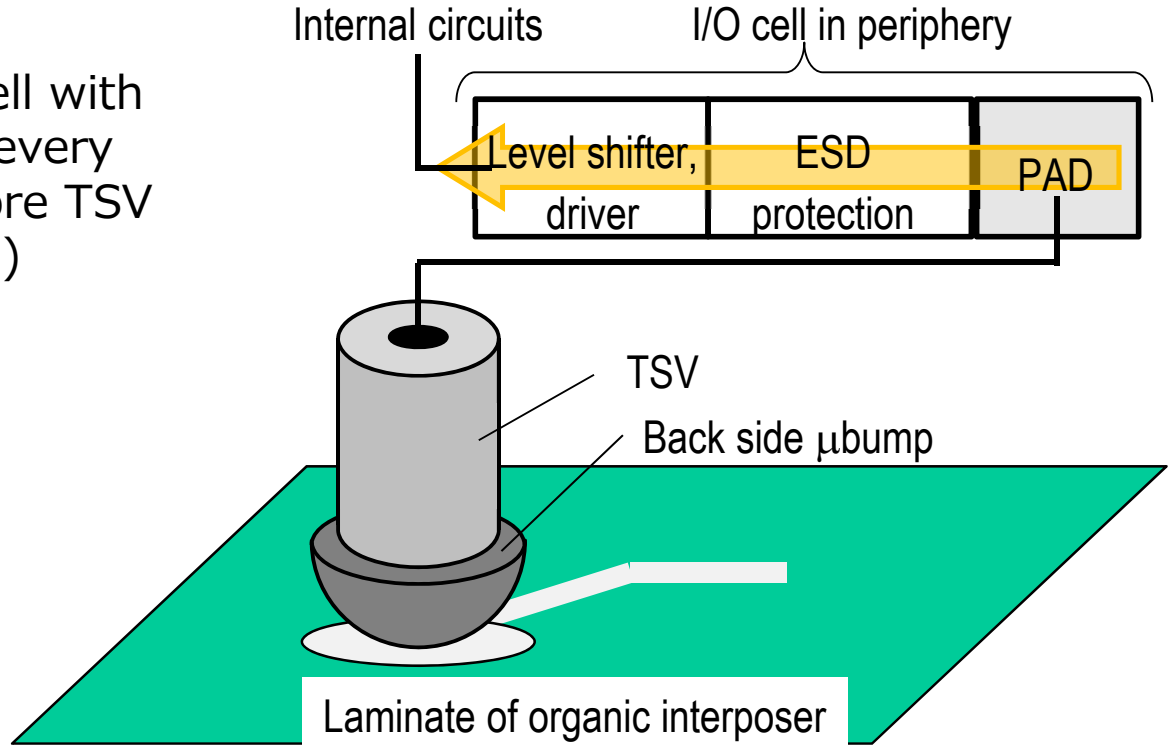
Hierarchical ESD protection (1/2)



- PN diodes intrinsic to tri-state driver transistors serve as ESD elements and are directly connected to a single TSV in parallel.

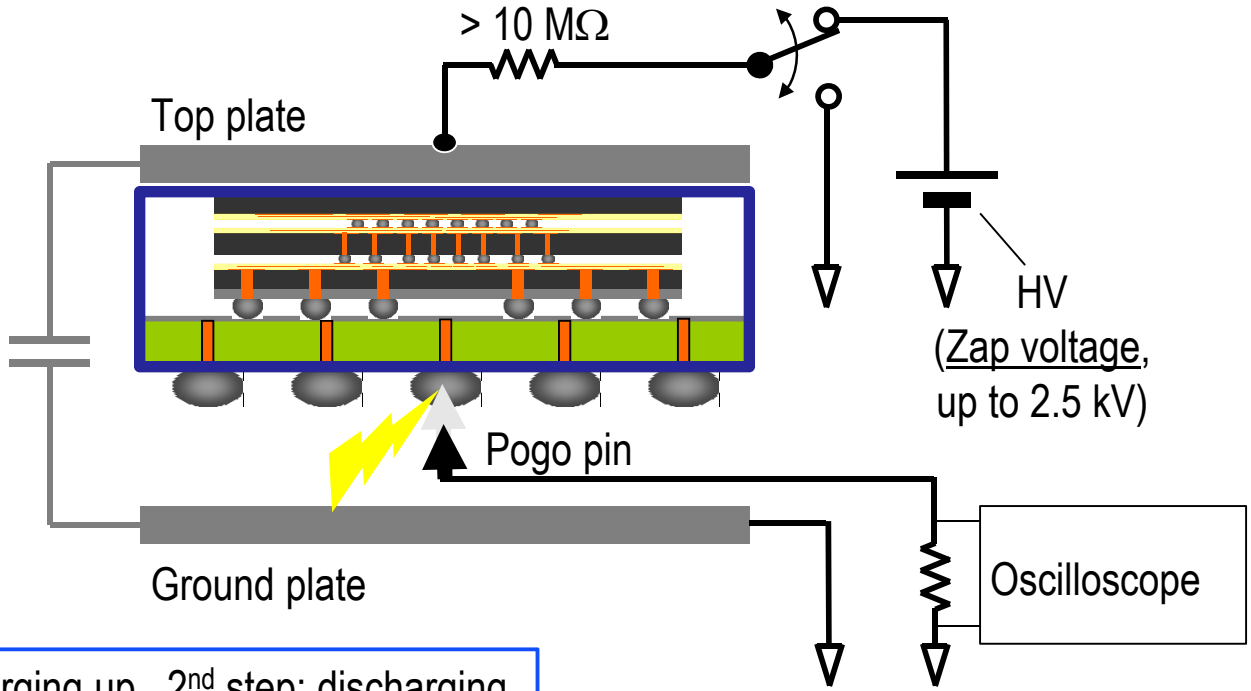
Hierarchical ESD protection (2/2)

- Conventional I/O cell with ESD protection for every external signal before TSV (in bottom logic die)



M. Nagata *et al*., "CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus," EOS/ESD Symposium, pp. 1-7, Sep. 2014.

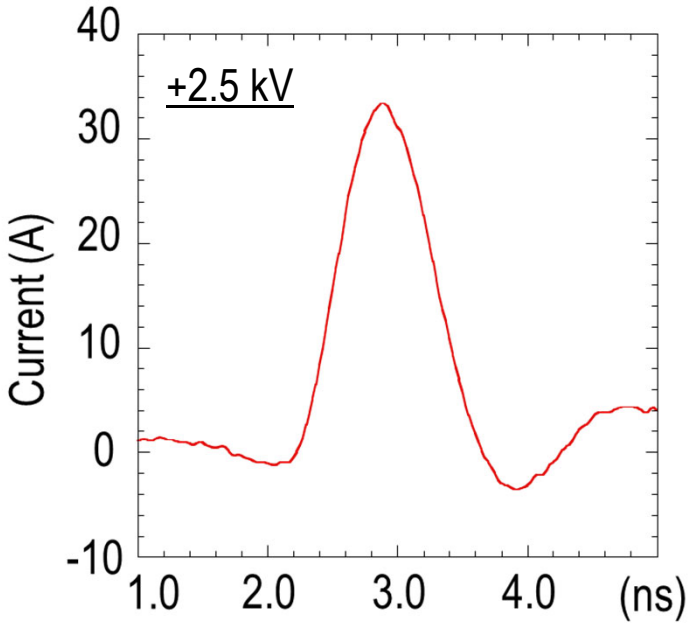
CDM ESD stress test

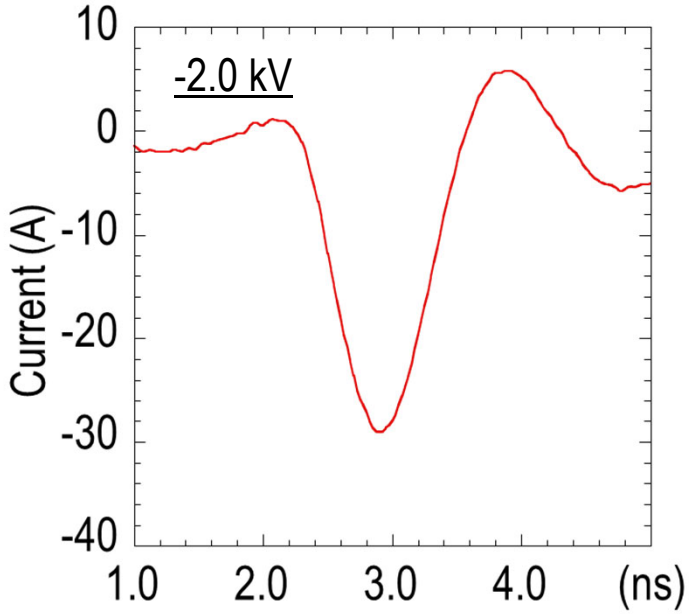


1st step: charging up, 2nd step: discharging

Ref. HANWA HED-C5000R

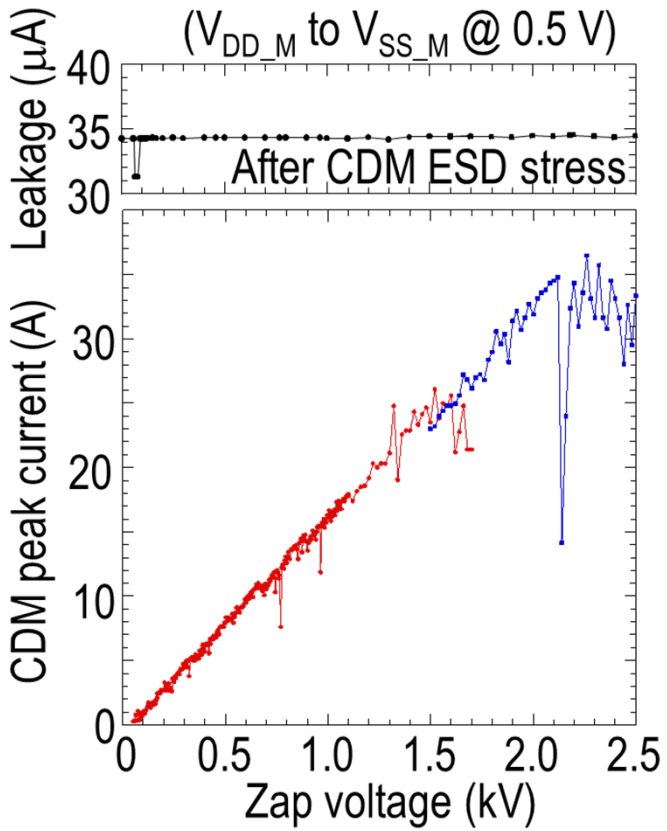
CDM stress at pin VDD_M





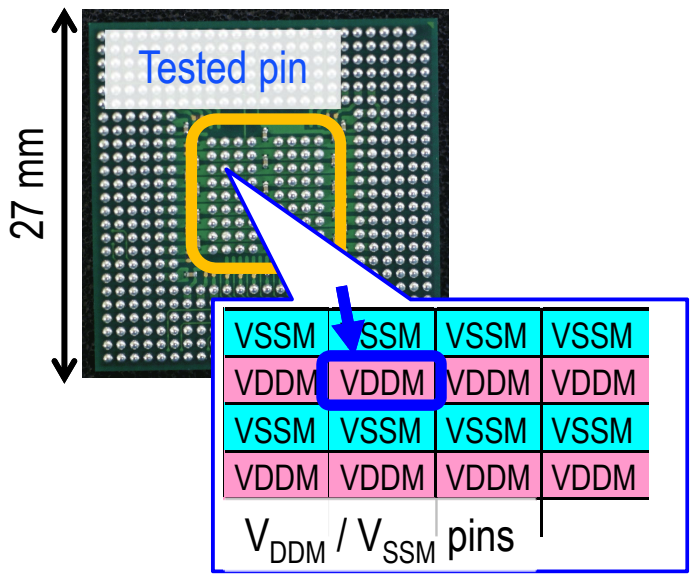
- No damage after positive (+) and negative (-) CDM ESD stress on V_{DD_M}

CDM peak current / leakage current

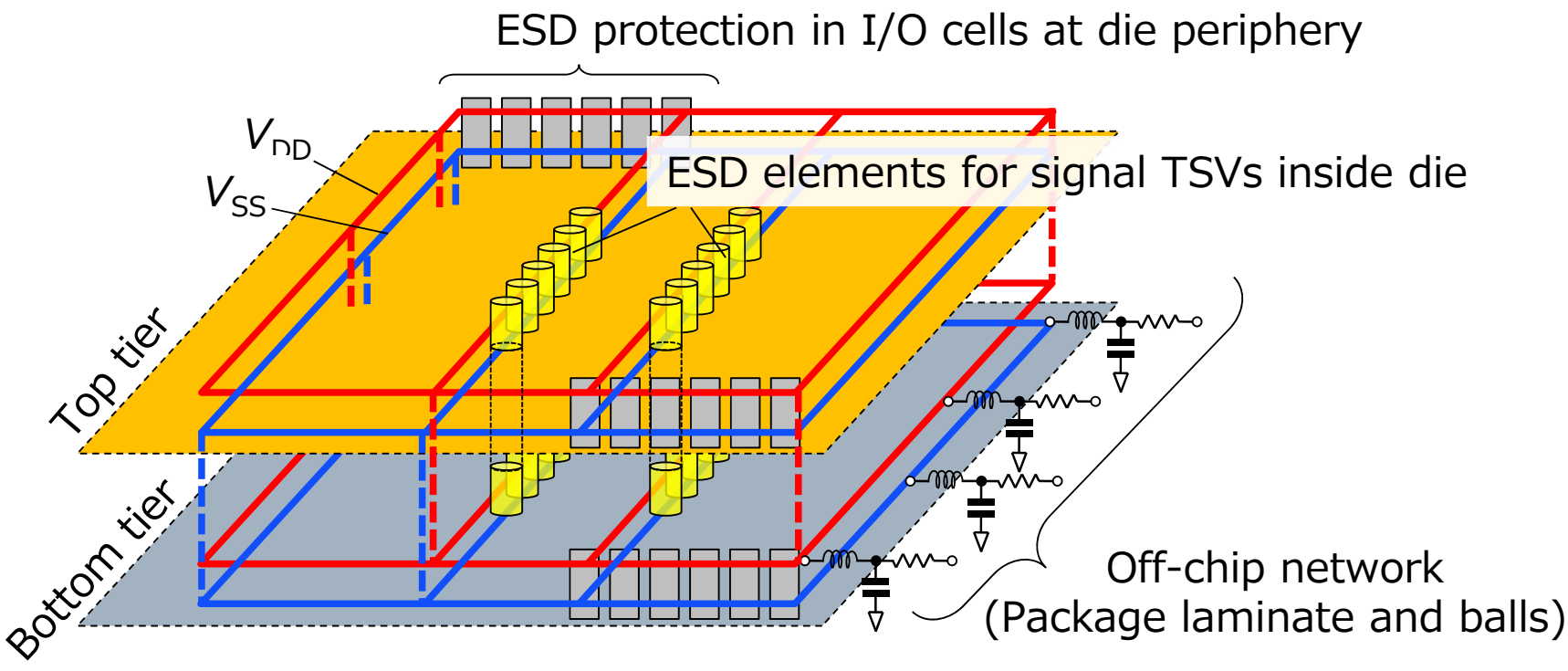


No increase of leakage up to 2.5 kV CDM stress

527 pin BGA package

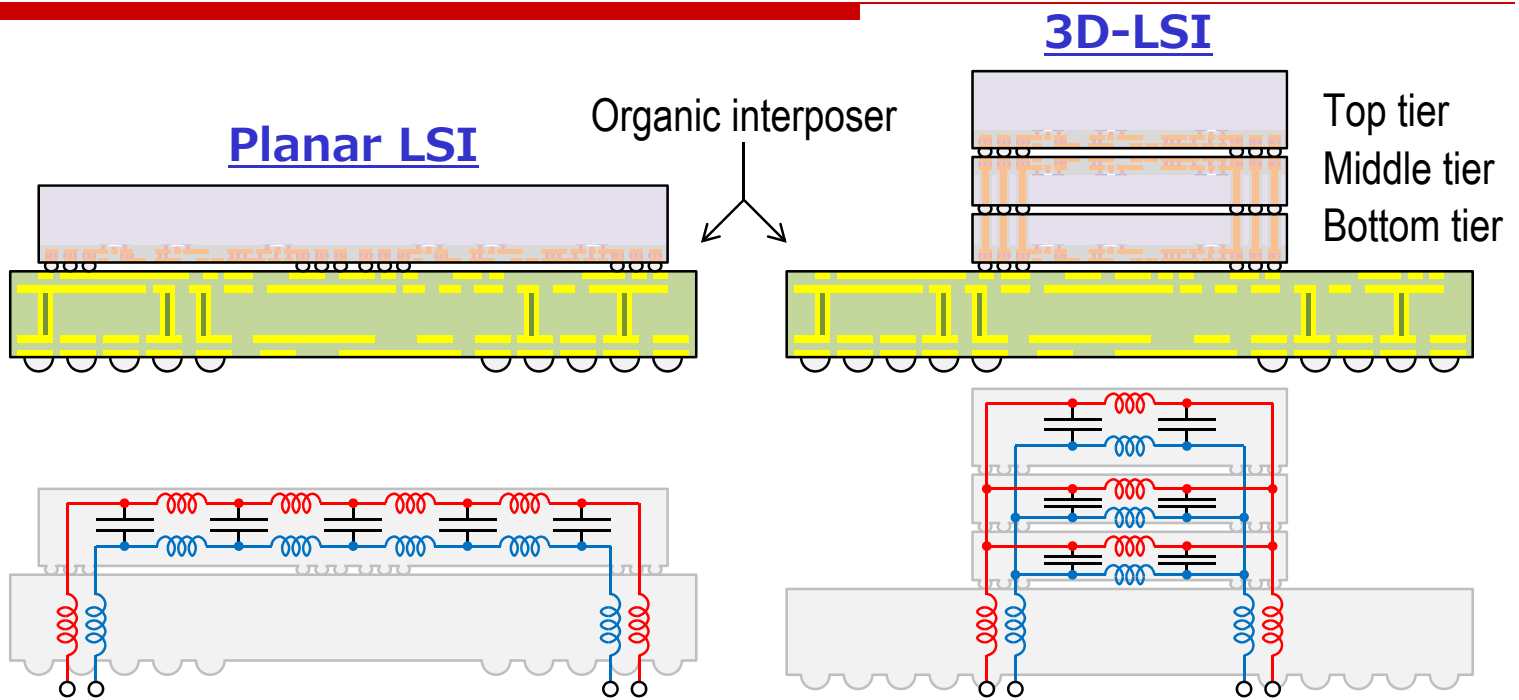


Global PDN in 3D stacked IC chip



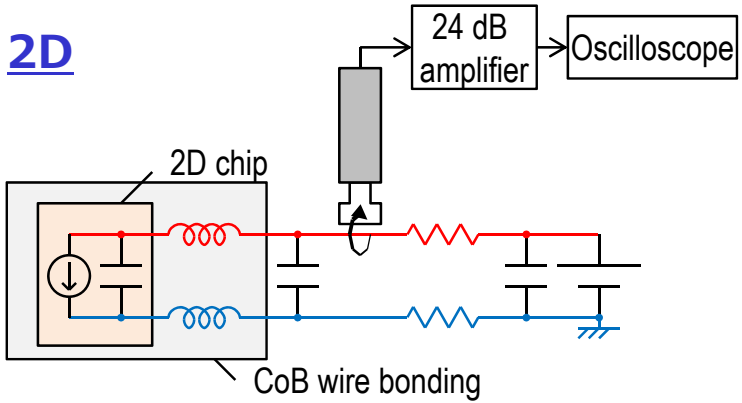
- Combination of ESD structures sharing PDNs

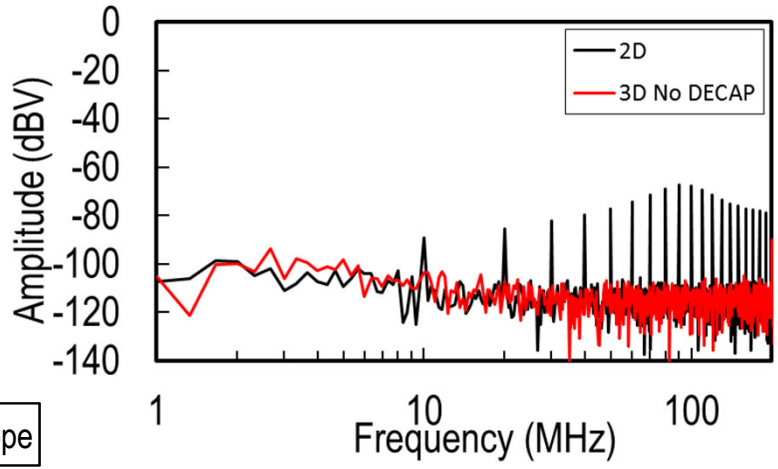
Global PDN from PI/EMC standpoints

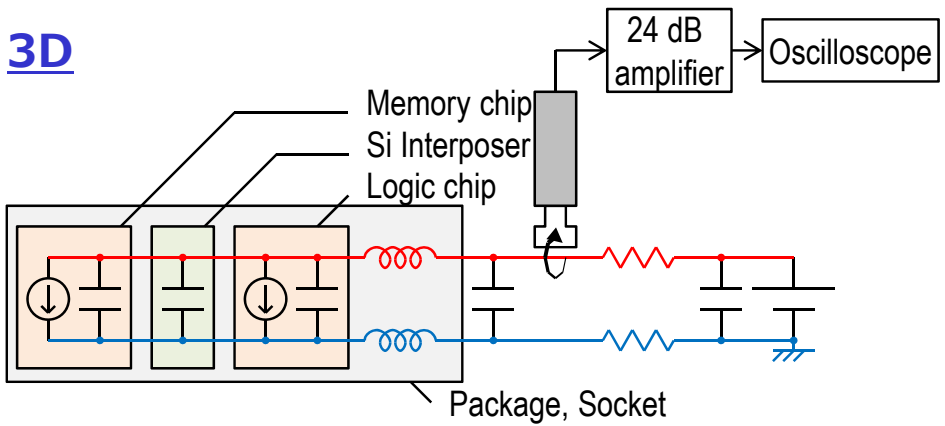


- Vertical integration of distributed parasitic capacitances
- Mitigation of power supply noise and electromagnetic interference

Electromagnetic interference (EMI)







Y. Araga *et al.*, "EMI Performance of Power Delivery Networks in 3D TSV Integration," IEEE EMC Europe 2016.

Summary

- **C-P-S power noise simulation includes packaging-circuits interaction for SI, PI, EMC and ESD characteristics**
  Importance of multi-level noise analyses increases from viewpoints of highly heterogeneous integration.
- **In-place diagnosis uses OCM and sheds lights on in-package problems.**
  Exploration of on-chip SI/PI diagnostic features within advanced packaging structure – 2D (face down), 2.5D (fan out), and even 3D (stacked).
- **3D IC packaging provides potential advantage.**
  The densely integrated 3D P/G grids with distributed TSVs – advantageous for EMC and ESD standpoints.

Key references (by lecturer)

1. M. Nagata *et al*., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment," IEEE Trans. CAD, Vol. 19, No. 6, pp. 671-678, June 2000.
2. A. Afzali-Kusha *et al*., "Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation (Invited)," Proceedings of the IEEE, Vol. 94, No. 12, pp. 2109-2138, Dec. 2006.
3. M. Nagata, "On-Chip Measurements Complementary to Design Flow for Integrity in SoCs," DAC 2007, pp. 400-403, June 2007.
4. T. Hashida, M. Nagata, "An On-Chip Waveform Capturer and Application to Diagnosis of Power Delivery in SoC Integration," IEEE Journal of Solid-State Circuits, Vol. 46, No. 4, pp. 789-796, Apr. 2011.
5. K. Yoshikawa *et al*., "Measurements and Co-Simulation of On-Chip and On-Board AC Power Noise in Digital Integrated Circuits," EMC Compo 2011, pp. 76-81, Nov. 2011.
6. S. Takaya, *et al*., "A 100GB/s Wide I/O with 4096b TSVs Through an Active Silicon Interposer with In-Place Waveform Capturing," ISSCC 2013, pp. 434-435, Feb. 2013.
7. M. Nagata *et al*., "CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus," EOS/ESD Symposium, pp. 1-7, Sep. 2014.
8. M. Nagata, "Noise Simulation in Mixed-Signal SoCs (Invited Tutorial)," ISSCC 2016, Tutorial, T8, Feb. 2016.
9. Y. Araga *et al*., "EMI Performance of Power Delivery Networks in 3D TSV Integration," EMC Europe 2016, pp 428-433, Sep. 2016.
10. A. Tsukioka *et al*., " Simulation Techniques for EMC Compliant Design of Automotive IC Chips and Modules," EMC Europe 2017, pp. 1-5, Sep. 2017.
11. Y. Araga *et al*., "Measurement and Analysis of Power Noise Characteristics for EMI Awareness of Power Delivery Networks in 3-D Through-Silicon Via Integration," IEEE Trans. Components, Packaging and Manufacturing Technology, Vol. 8, No. 2, pp. 277-285, Feb. 2018.
12. A. Tsukioka *et al*., "Interaction of RF DPI with ESD protection Devices in EMS Testing of IC Chips," EMC Europe 2018, pp. 445-450, Aug. 2018.
13. H. Sonoda *et al*., "In-Place Power Noise and Signal Waveform Measurements on LVDS Channels in Fan-Out Multiple IC Chip Packaging," EMC Compo 2019, pp. 1-3, Oct. 2019.
14. K. Monta *et al*., "3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance," IEEE Trans. Electron Devices, vol. 68, no. 4, pp. 2077-2082, Apr. 2021.