Prof. Armin Tajalli visit at SSCS Switzerland Chapter Lecture on Circuits and Signalling Co-Design for Ultra-Wideband Communications at ETH Zurich

The IEEE Solid-State Circuits Society (SSCS) Switzerland Chapter Organized a Lecture on Circuits and Signalling Co-Design for Ultra-Wideband Communications at ETH Zurich on 18st June 2019 from 5:30pm to 6:30 pm.

Prof. Tajalli of the University of Utah offered the chapter with a high standard tutorial from the signalling and circuit design perspective fulfilling some industrial problems in the wireline communication.

Figure 1 Prof. Taekwang Jang Introducing Prof. Tajalli

The meeting started by Prof. Taekwang Jang, the chair of Switzerland Solid-State Circuits Chapter, introducing the lecturer to the audience. The audience included students and engineers from the hosting university, local companies and research centers forming a friendly group of 15 attendees.

Figure 2 : Audience attended the lecture on high-speed data communication

The lecture began with an introduction on the requirements of high-bandwidth links. Modern computing systems rely on high-bandwidth data communication between different units. From a computing perspective, the CMOS technology scaling has been successful, until 2005 [Horowitz et al], when the heat dissipation started to limit the single-core frequency provoking the development of multicore processors.

More recently, around 2015 a study based on the cost and fabrication yield, reached the conclusion that the optimal number of cores in a multicore processor is 8 and further integration should be performed by including multiple chips in a computing platform. In such a distributed system, chip-to-chip communication over a very short distances is a highly demanding topic of research.

According to Prof. Tajalli, many companies are moving toward multi-chip-module (MCM) SoCs due to heat, yield, and performance concerns. Where the data rate as well as energy consumption are extremely crucial. Due to a stringent power budget, industry is seeking out for new design methodologies to implement very dense and energy-efficient links.

Most critical limitation of high speed is the inter-symbol interference and equalization. The main focus of this talk was on architectural design and circuit techniques to overcome the challenge using data encoding on a many-wire parallel bus and optimal binary decoders.

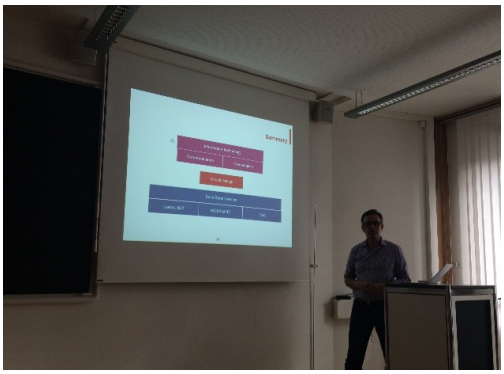

Figure 3 : Prof. Tajalli Concluding his lecture

The meeting was closed after fruitful and intutive questions by the audiences on channel cross talk, linearity, speed limit and circuit toplogies.

REFERENCES

[1] M. Horowitz, E. Alon, D. Patil, S. Naffziger, Rajesh Kumar and K. Bernstein, "Scaling, power, and the future of CMOS," IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, 2005.

[2] N. Beck, S. White, M. Paraschou and S. Naffziger, "'Zeppelin': An SoC for multichip architectures," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018

Taekwang Jang, Michel Bron, and Mathieu Coustans, For IEEE SSCS Switzerland Chapter.