High Efficiency Reconfigurable Monolithic Switched-Capacitor DC-DC Converter

Man-Kay Law (羅文基)

Institute of Microelectronics
State Key Laboratory of
Analog and Mixed-Signal VLSI
(University of Macau)
微電子研究院
漠擬與混合信號超大規模集成電路
國家重點實驗室（澳門大學）

澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

Outline

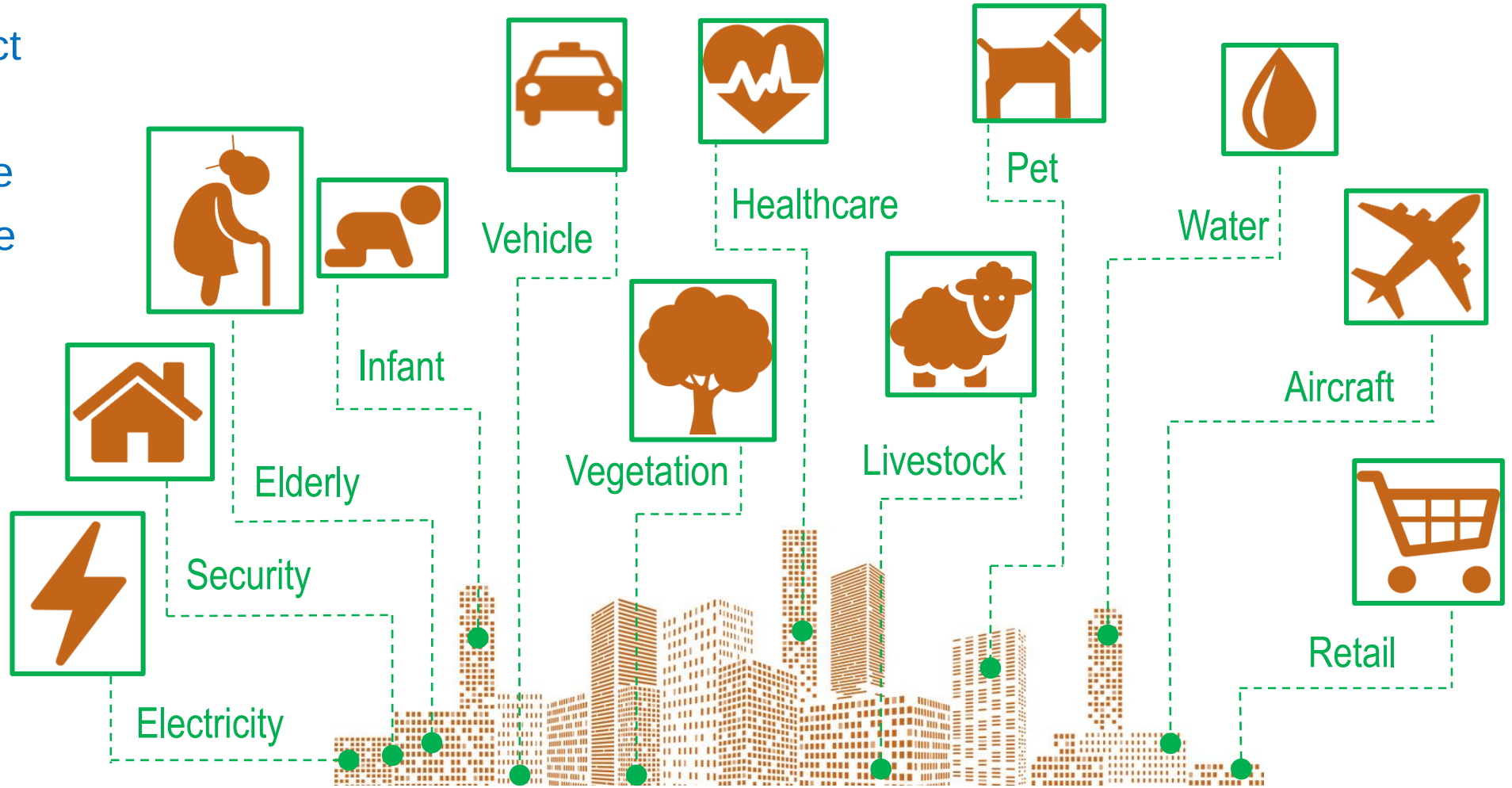
- Background and Motivation
- Algebraic Series-Parallel (ASP)-based Boost Topology
- Algorithmic Voltage-Feed-In (AVFI) Buck/Boost Topology
- Summary

Powering the IoE Devices

■ Plentiful Devices Required for IoE Applications

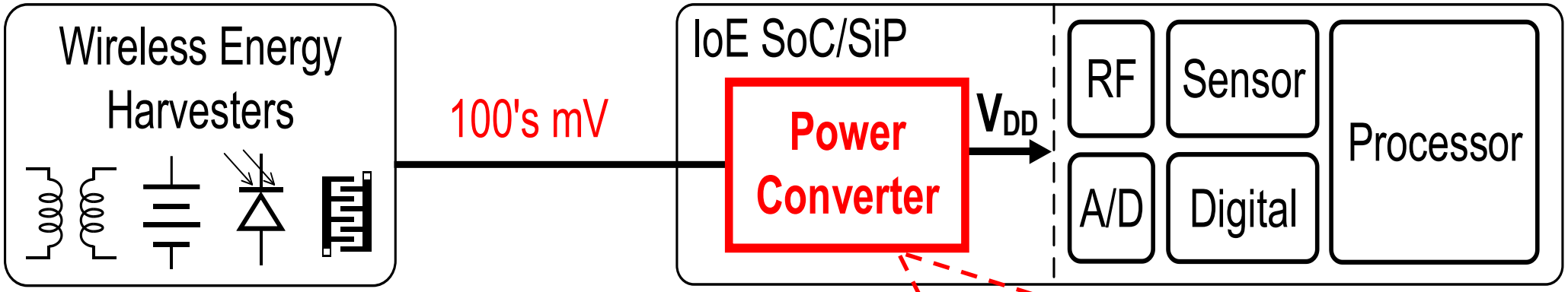
- ➢ Sense
- ➢ Measure
- ➢ Identify
- ➢ Monitor
- ➢ Connect
- ➢ Control
- ➢ Analyze
- ➢ Execute

B A S E

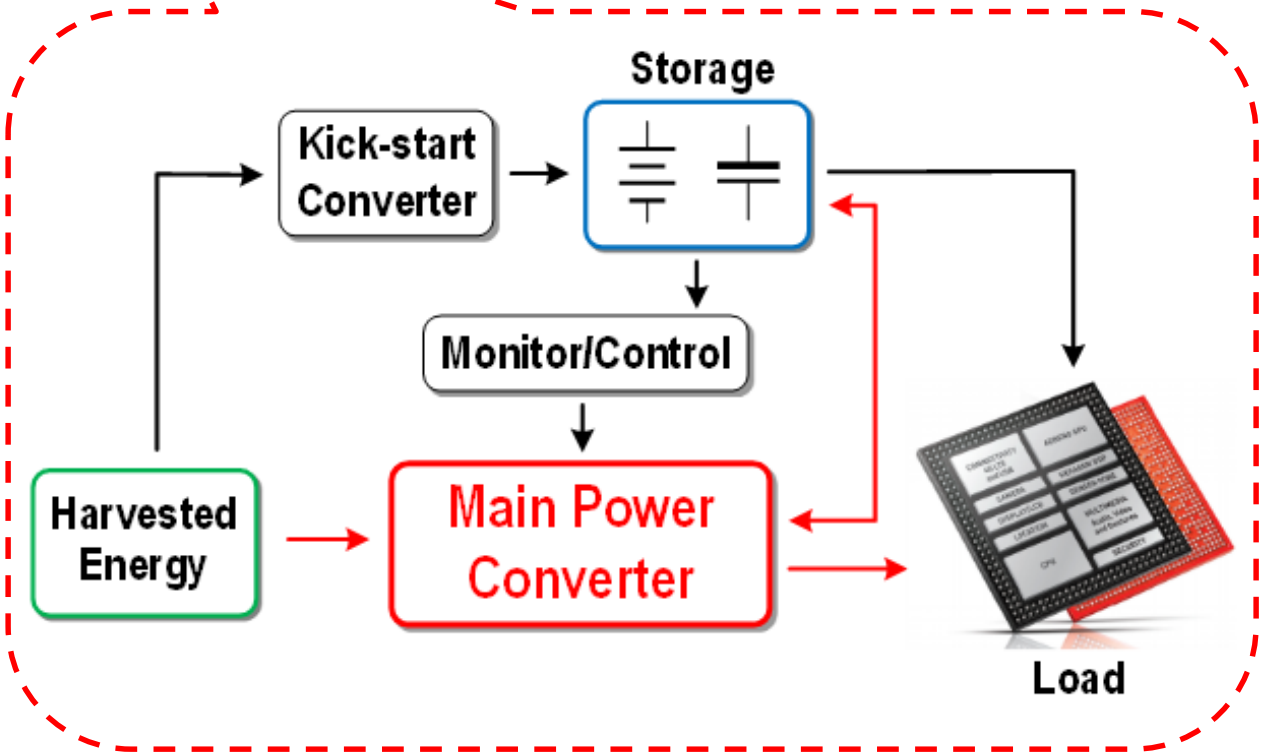


Billions of "things" connected together

Power Management with Energy Harvesting Sources



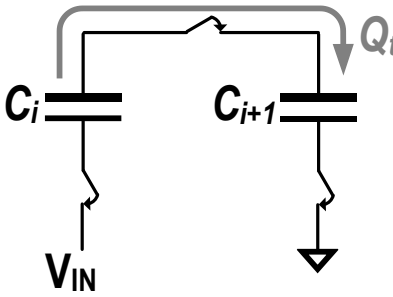
- **Wide Input Range**
- **Switched-Capacitor (SC) for Power Conversion**
  - ✓ **Full integration**
  - ✓ **Fine-grained VCR (FVCR)**
  - ✓ **High efficiency**
  - ✓ **High power density**



Conduction/Parasitic Loss in SC Power Stage

- **Conduction loss:** Slow switching (R_{SSL})

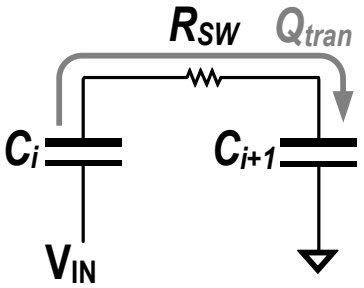
  Charge sharing loss: Energy loss occurs when there is charge transferred between two capacitors.



$$E_{ls,qs} = \frac{Q_{tran}^2}{2(C_i \,||\, C_{i+1})}$$

- **Conduction loss**: Fast switching (R_{FSL})

  Switch on-impedance loss: Finite settling effect during Q_{tran} sharing.

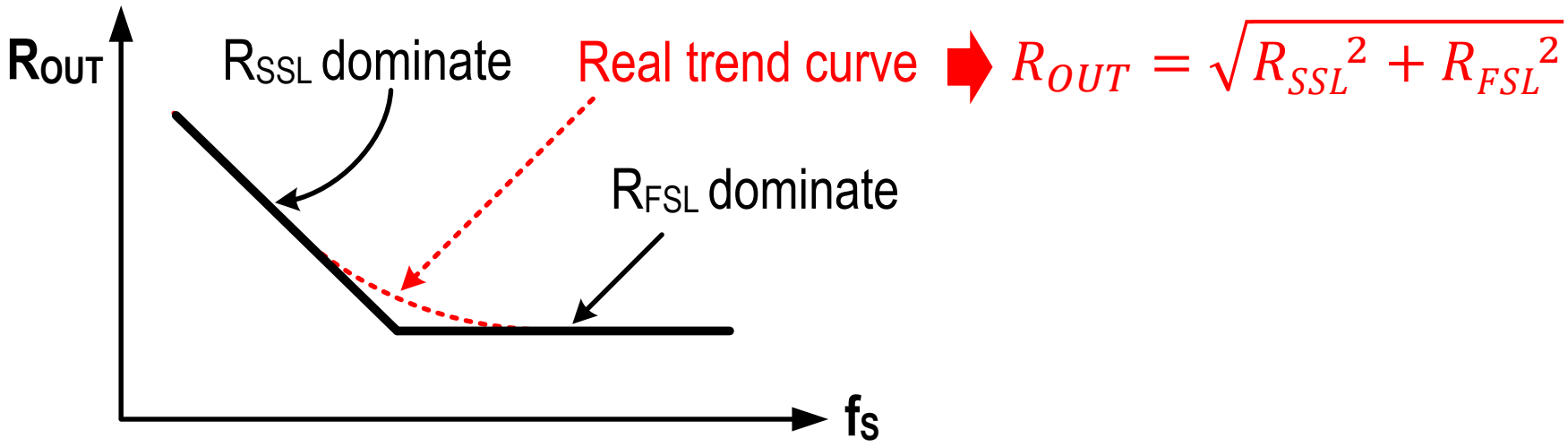


$$E_{ls,qs} = \frac{Q_{tran}^2}{2C_{||}} \coth\left(\frac{T}{2R_{SW}C_{||}}\right)$$

$$C_{||} = C_i \,||\, C_{i+1}$$

Conduction/Parasitic Loss in SC Power Stage

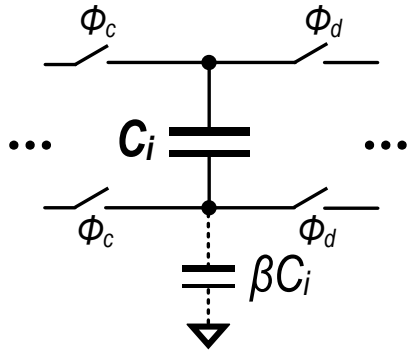
- **Total conduction loss**



$$R_{OUT} = \sqrt{{R_{SSL}}^2 + {R_{FSL}}^2}$$

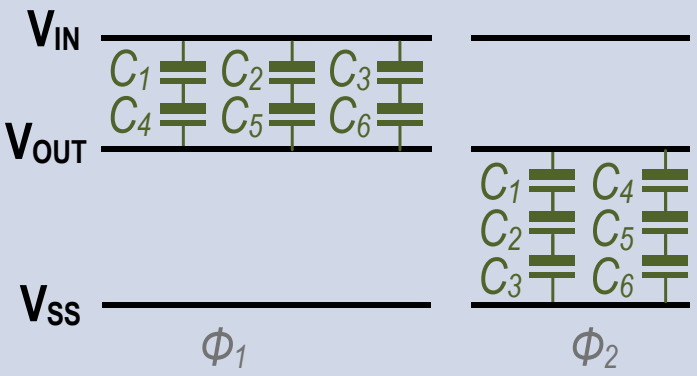
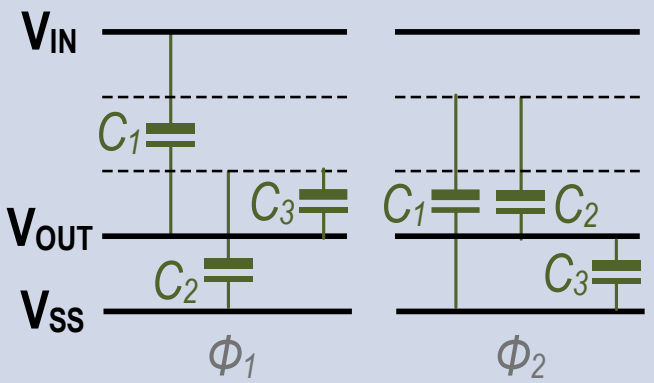
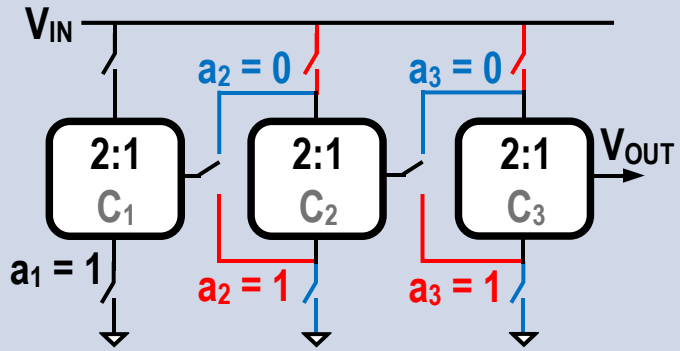
- **Parasitic loss**

Due to charging and discharging the bottom-plate parasitic capacitance βC_i, where β depends on the choice of capacitor.

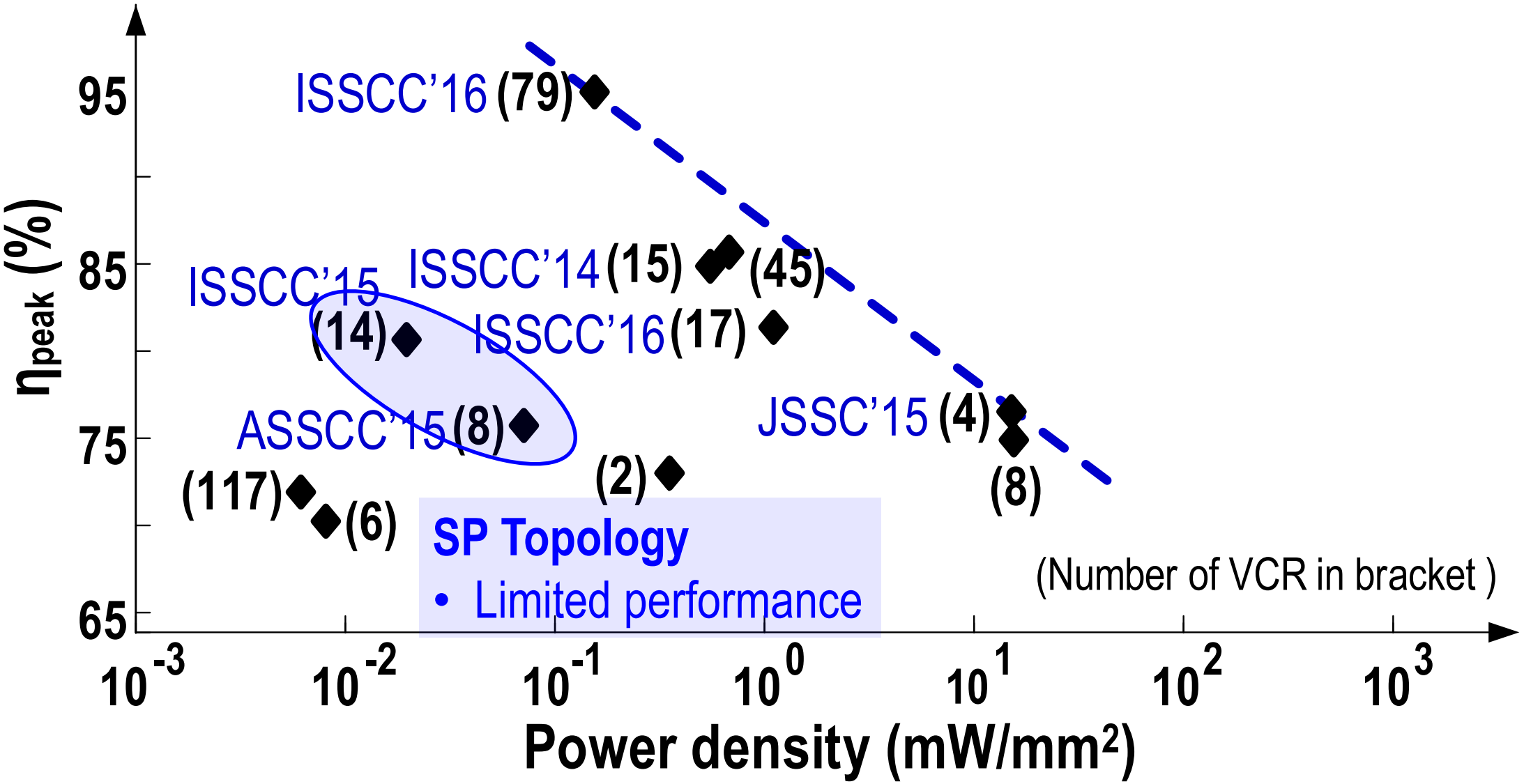


$$E_{ls,par} = \beta C_i \cdot \Delta V_{CB}^2$$

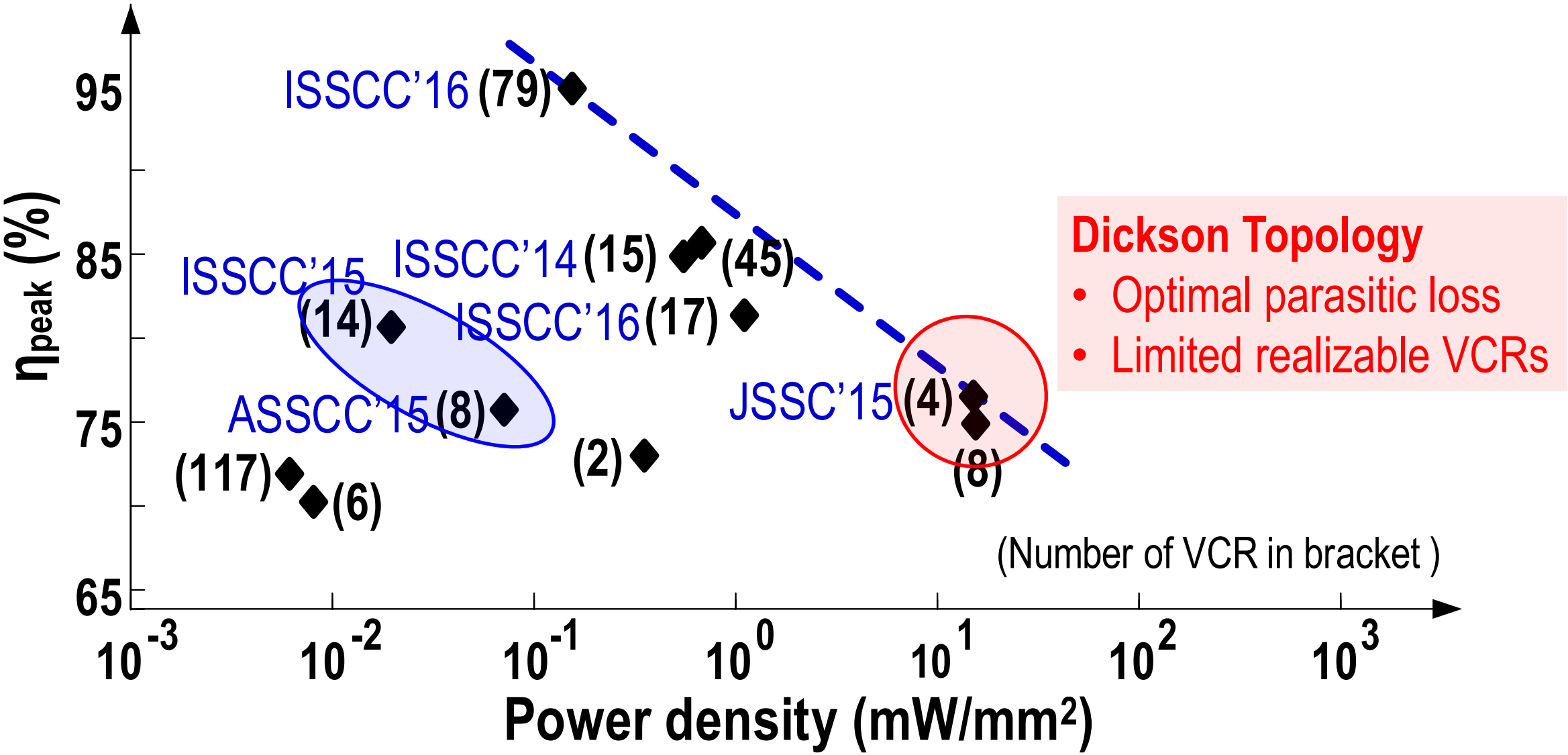
Fully Integrated FVCR SC Converter Comparison

Topology	Series-Parallel	Dickson	Binary
	 $VCR = \frac{m}{m+n}, \{m, n \in \mathbb{Z}^+\}$	 $VCR = \left\{\frac{1}{2}, \frac{1}{3}, \ldots, \frac{1}{n+1}\right\}$	 $VCR = \frac{X}{2^n}, \{X = 1, 3, \ldots, 2^n - 1\}$
VCR Flexibility	High	Low	Medium
Conduction Loss	VCR dependent	Optimal	Optimal
Parasitic Loss	Large	Optimal	Large

Fully Integrated FVCR SC Converter in bulk CMOS



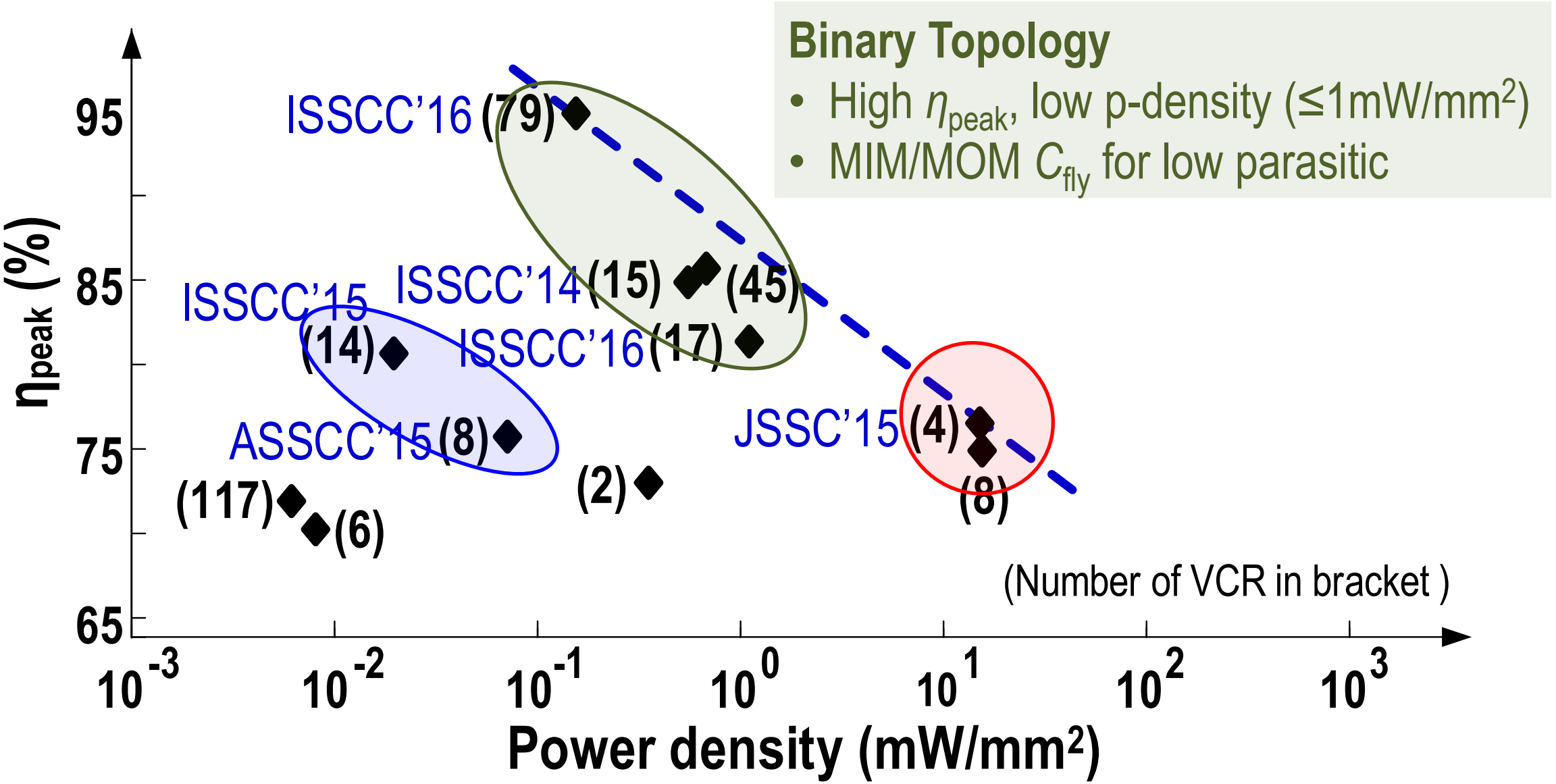
Fully Integrated FVCR SC Converter in bulk CMOS



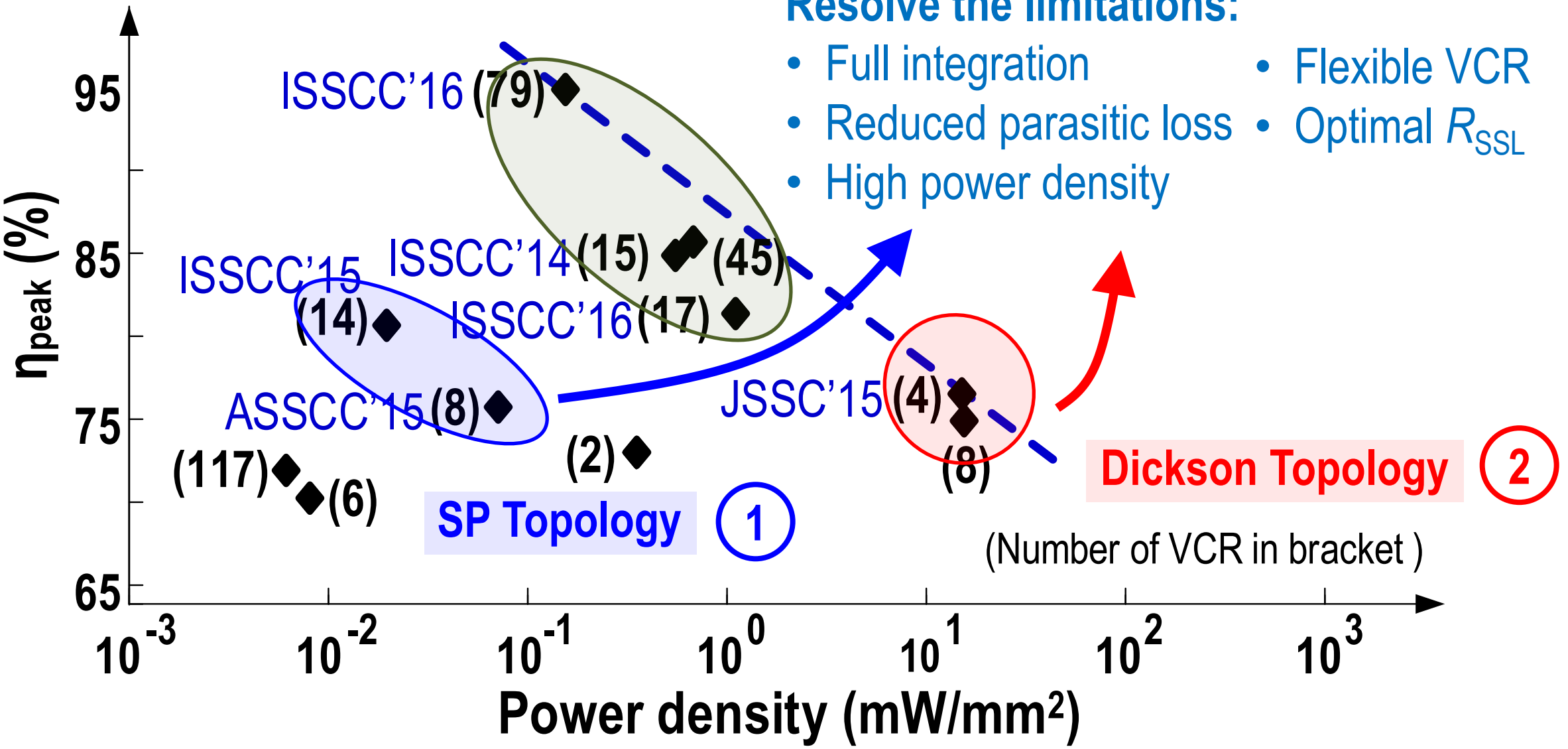
Dickson Topology

- Optimal parasitic loss
- Limited realizable VCRs

Fully Integrated FVCR SC Converter in bulk CMOS



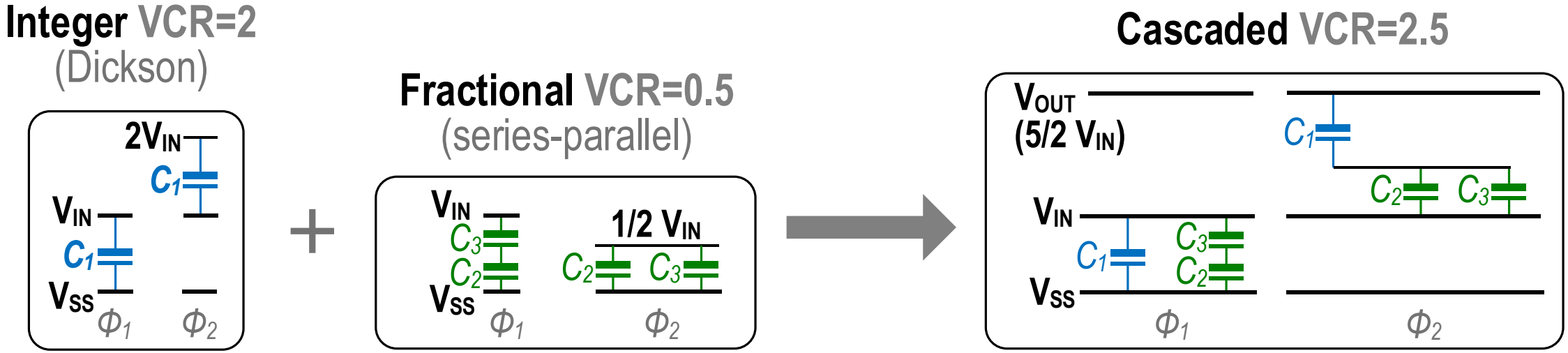
Fully Integrated FVCR SC Converter in bulk CMOS



Outline

- Background and Motivation
- Algebraic Series-Parallel (ASP)-based Boost Topology
- Algorithmic Voltage-Feed-In (AVFI) Buck/Boost Topology
- Summary

Conventional FVCR SC SP Boost Converter

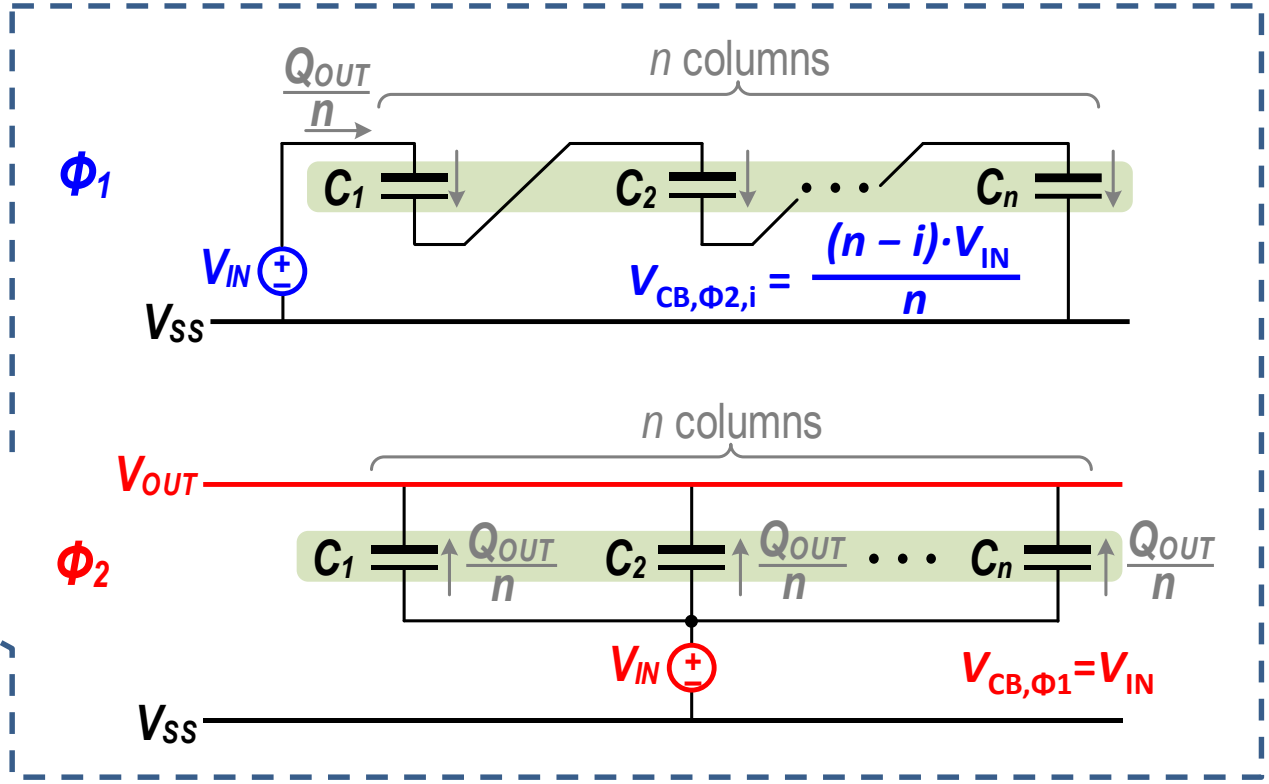


- Cascaded Integer + Fractional Topology
  - ✓ Intuitive implementation
  - ✓ High flexibility with separate SC stages (e.g. Dickson + Series Parallel)
  - ✓ Wide VCR generation for V_{IN} adaptation
  - × VCR Flexibility vs. conduction loss (R_{SSL})
  - × High parasitic loss

Conventional SP Topology

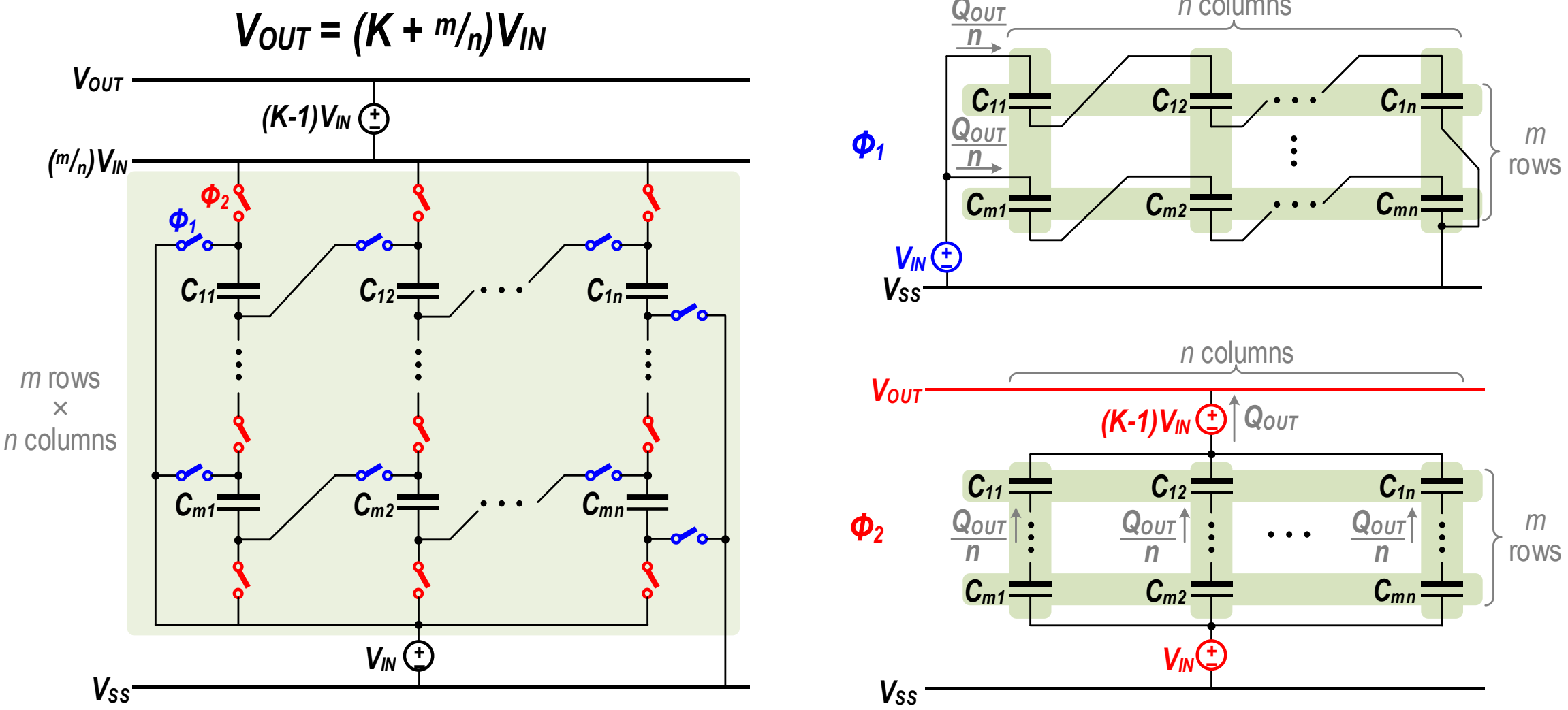
$$VCR = \frac{V_{OUT}}{V_{IN}} = K + \frac{m}{n}$$

K = 1, *m* = 1



- Parallel discharge (*n* branches) + Series charge (1 branch) with *n* capacitors
- Limited VCR generation: $VCR = \{\frac{1}{2}, \frac{1}{3}, \frac{1}{4}, \ldots\}$
- High bottom-plate parasitic loss: $E_{par} \propto \sum(\Delta V_{CB,i})^2 = \sum\left(\frac{i \cdot V_{IN}}{n}\right)^2$

Conventional 2DSP Topology



- Fine-grained VCR using an *m*×*n* capacitor matrix
- High VCR flexibility as the capacitor matrix increases

Limitations of 2DSP

- Under the area-constrained condition:

Optimal R_{SSL} Expression

$$VCR = \frac{V_{OUT}}{V_{IN}} = K + \frac{m}{n}$$

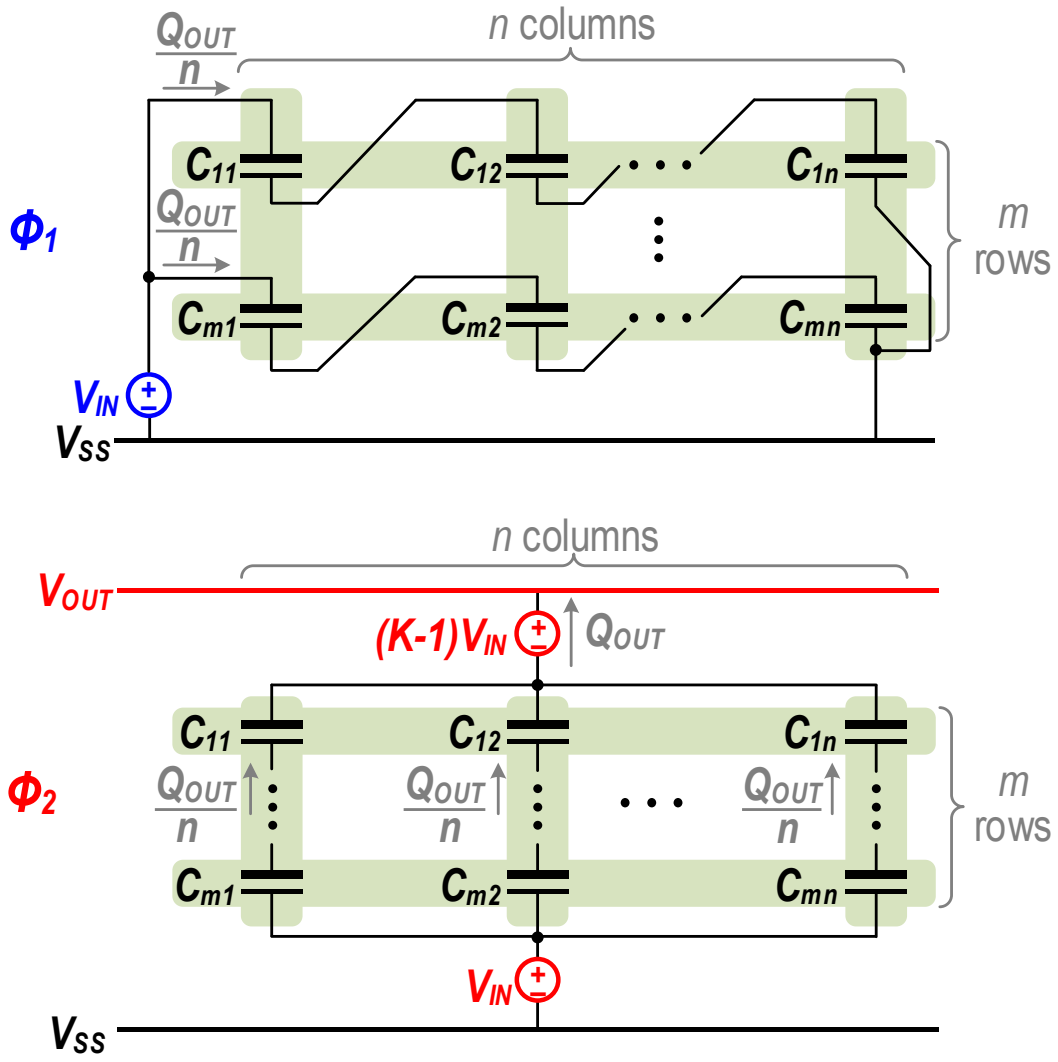
$$a_{c,i} = \frac{Q_{c,i}}{Q_{out}}$$

$$*R_{SSL,opt} = \frac{\left(\sum |a_{c,i}|\right)^2}{C_{TOT} f_S} = \frac{1}{C_{TOT} f_S}\left(\frac{Kn + m - 1}{n}\right)^2$$

2DSP R_{SSL} Expression

$$R_{SSL,2DSP} = \frac{1}{C_{TOT} f_S}(m + K - 1)^2$$

→ $R_{SSL,2DSP} > R_{SSL,opt}$ except for m=1



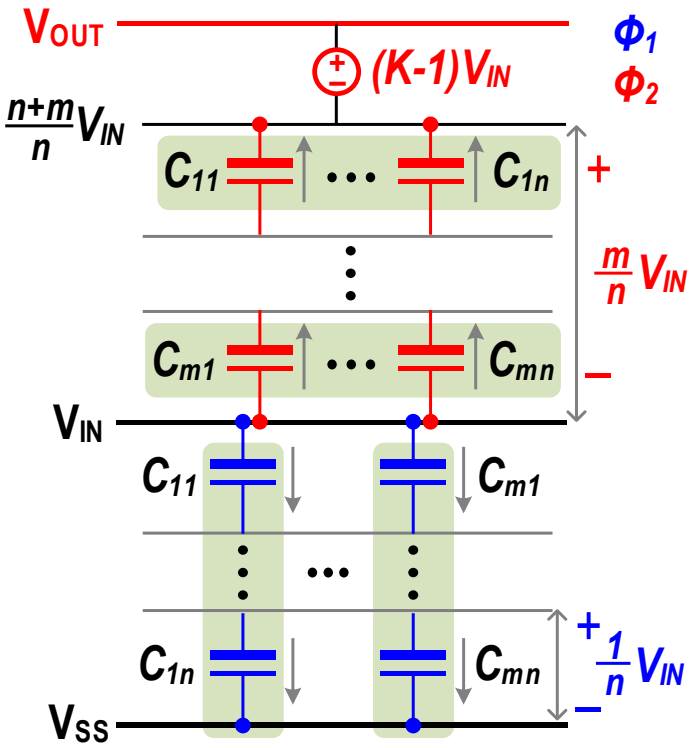
- Also, large parasitic loss still unresolved

[M. D. Seeman, TPEL'08]

ASP VCR Elaboration

■ 2DSP-Based Topology ($m \times n$)

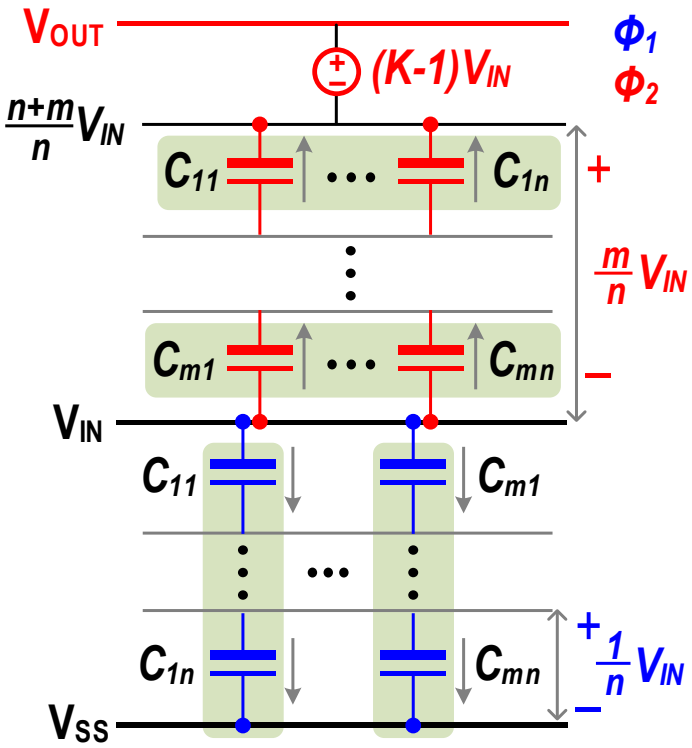
$$V_{OUT} = V_{IN} + \underbrace{\left(m \times \frac{V_{IN}}{n} \right)}_{\text{Fractional}} + \underbrace{(K-1)V_{IN}}_{\text{Integer}}$$



ASP VCR Elaboration

■ 2DSP-Based Topology ($m \times n$)

$$V_{OUT} = V_{IN} + \underbrace{\left(m \times \frac{V_{IN}}{n}\right)}_{\text{Fractional}} + \underbrace{(K-1)V_{IN}}_{\text{Integer}}$$



■ Proposed ASP VCR Elaboration ($2n-2$)

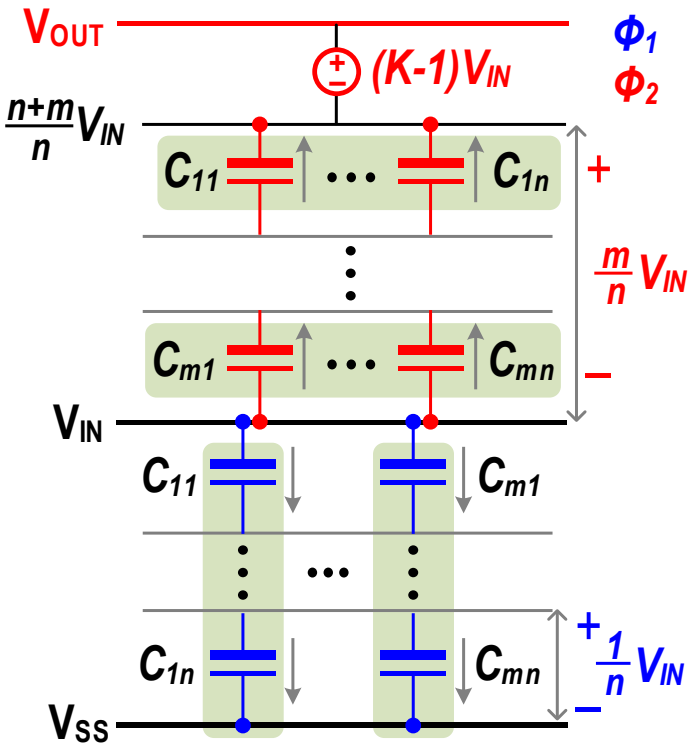
$$VCR = \frac{V_{OUT}}{V_{IN}} = K + \frac{m}{n}$$

$$nV_{OUT} = (Kn + m)V_{IN}$$

ASP VCR Elaboration

■ 2DSP-Based Topology ($m \times n$)

$$V_{OUT} = V_{IN} + \underbrace{\left(m \times \frac{V_{IN}}{n}\right)}_{\text{Fractional}} + \underbrace{(K-1)V_{IN}}_{\text{Integer}}$$



■ Proposed ASP VCR Elaboration ($2n-2$)

$$VCR = \frac{V_{OUT}}{V_{IN}} = K + \frac{m}{n}$$

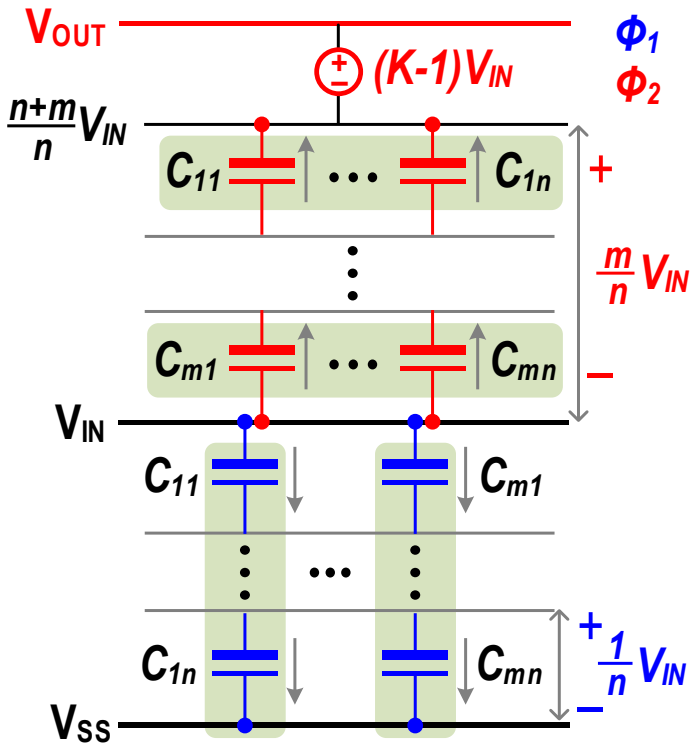
$$nV_{OUT} = (Kn + m)V_{IN}$$

$$V_{OUT} = (Kn + m)V_{IN} - (n-1)V_{OUT}$$

ASP VCR Elaboration

■ 2DSP-Based Topology ($m \times n$)

$$V_{OUT} = V_{IN} + \underbrace{\left(m \times \frac{V_{IN}}{n}\right)}_{\text{Fractional}} + \underbrace{(K-1)V_{IN}}_{\text{Integer}}$$



■ Proposed ASP VCR Elaboration ($2n-2$)

$$VCR = \frac{V_{OUT}}{V_{IN}} = K + \frac{m}{n}$$

$$nV_{OUT} = (Kn + m)V_{IN}$$

$$V_{OUT} = (Kn + m)V_{IN} - (n-1)V_{OUT}$$

$$V_{OUT} = KV_{IN} + (n-m-1)(K-1)V_{IN} + mKV_{IN} + (n-1)(V_{IN} - V_{OUT})$$

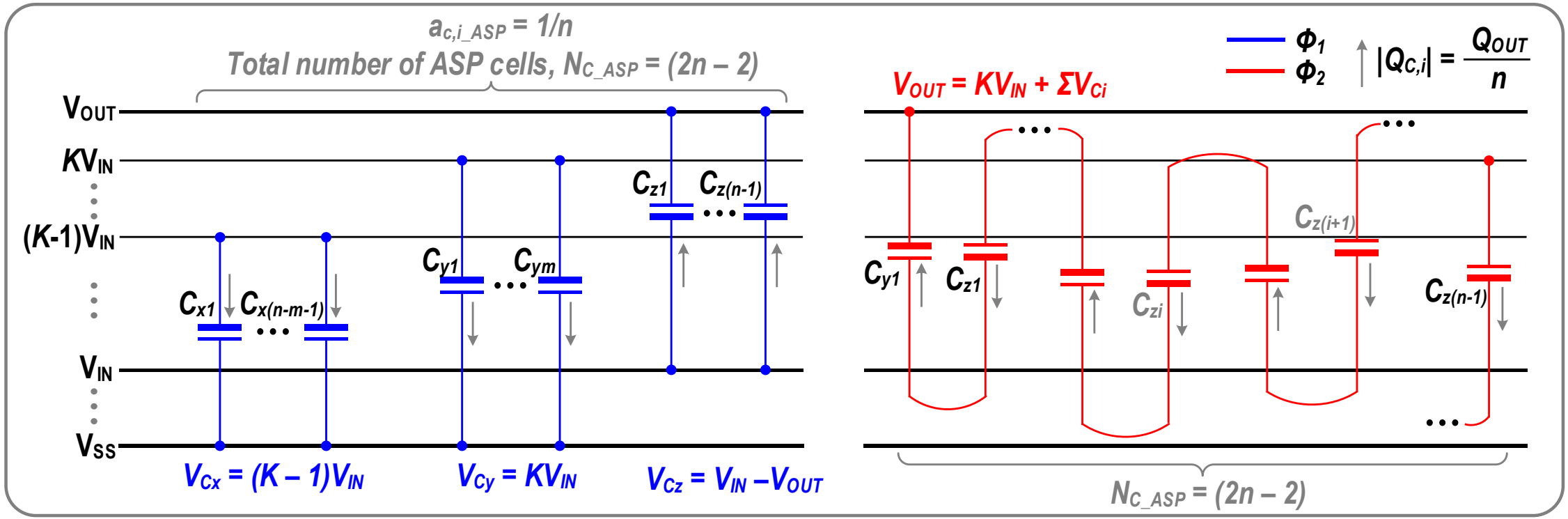
Number of unit capacitors · Sustained voltage

ASP Operation

■ Proposed Implementation for the VCR Expression

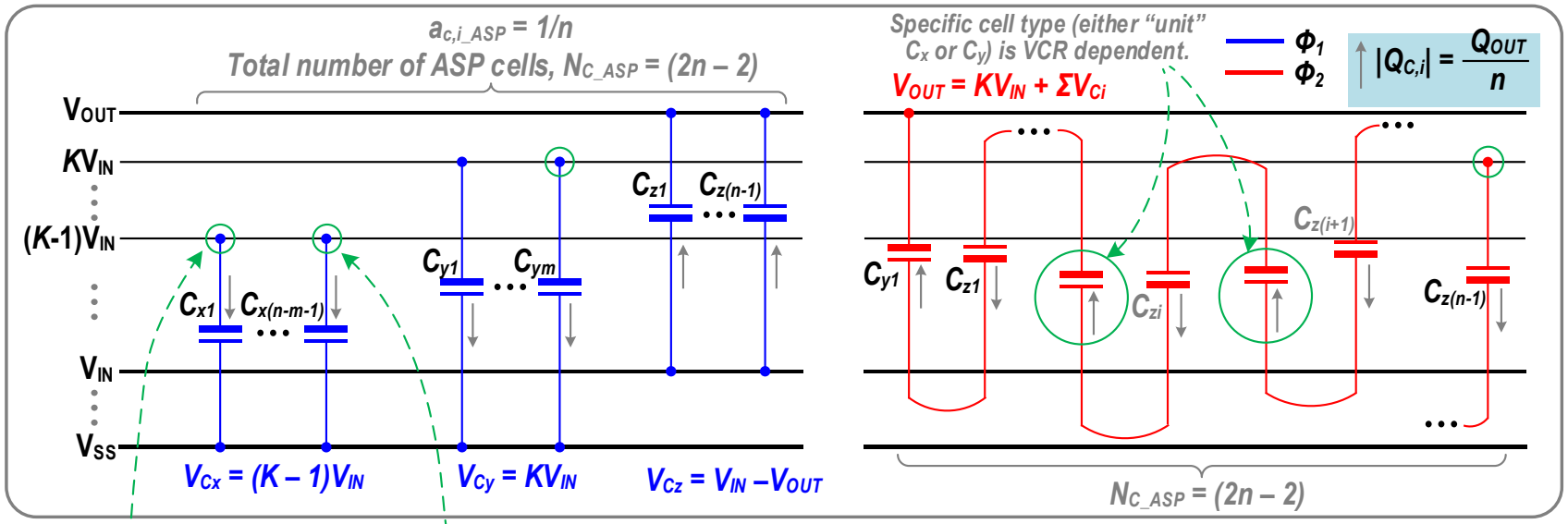
$$V_{OUT} = \underbrace{KV_{IN}}_{\text{Phase 2}} + \underbrace{(n-m-1)(K-1)V_{IN}}_{\text{Phase 1}} + \underbrace{mKV_{IN}}_{\text{Phase 1}} + \underbrace{(n-1)(V_{IN}-V_{OUT})}_{\text{Phase 1}}$$

Algebraic series-parallel stage

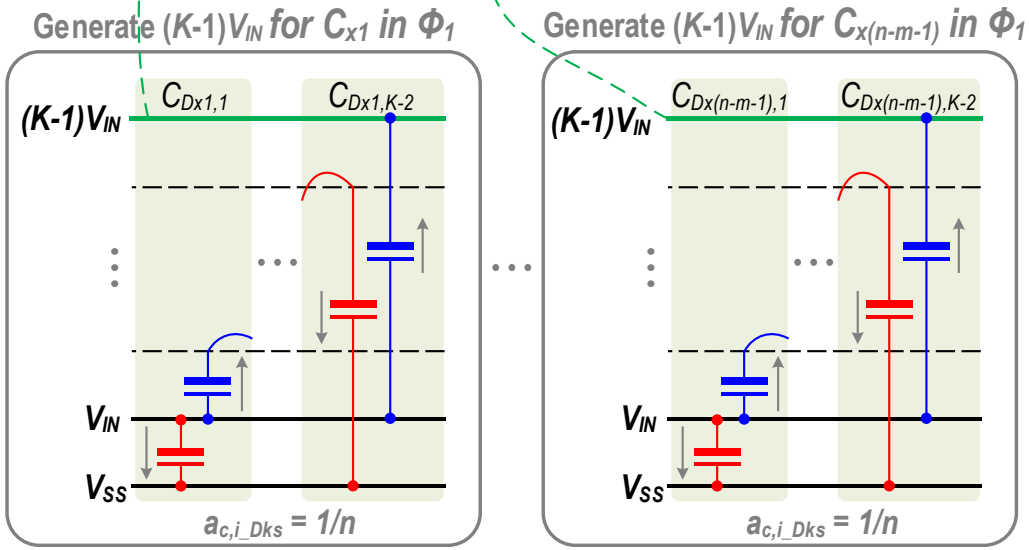


Integer Level Generation in ASP

Algebraic series-parallel stage



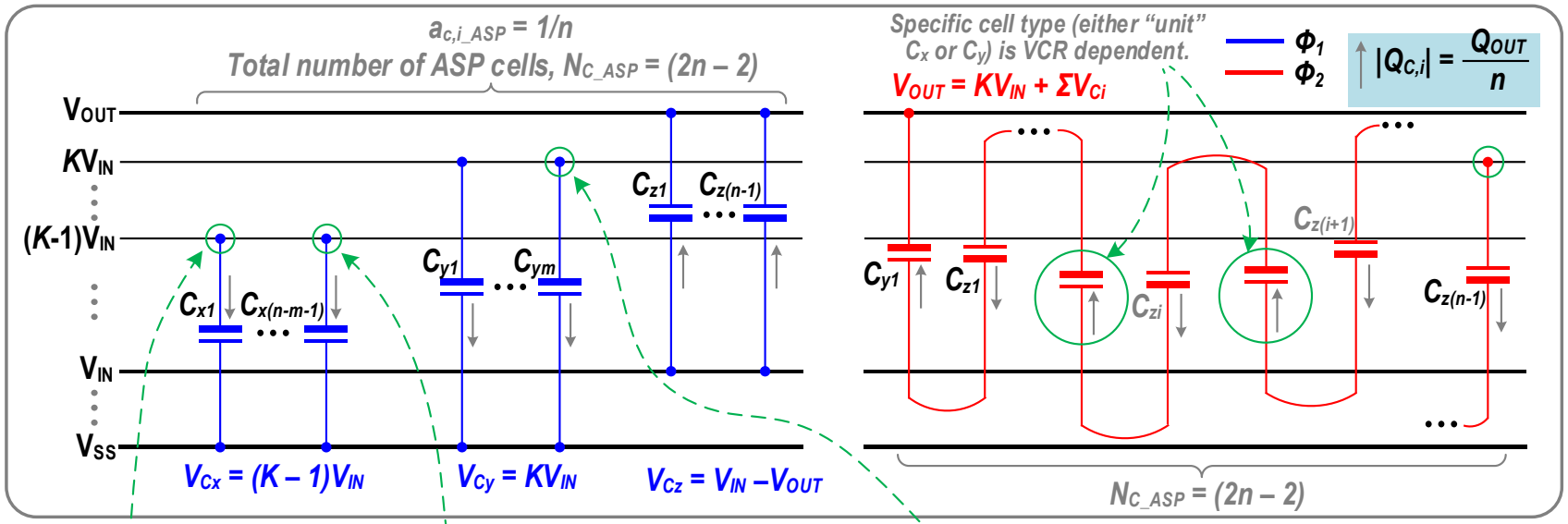
Dickson stage examples:



For all C_x: total number of C_{Dx}, $N_{C\_Dks,x} = (n - m - 1)(K - 2)$

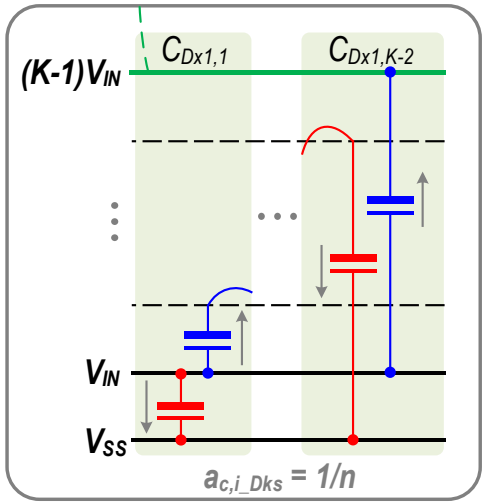
Integer Level Generation in ASP

Algebraic series-parallel stage

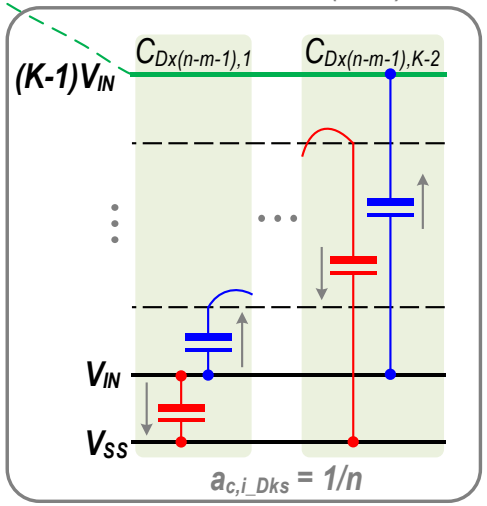


Dickson stage examples:

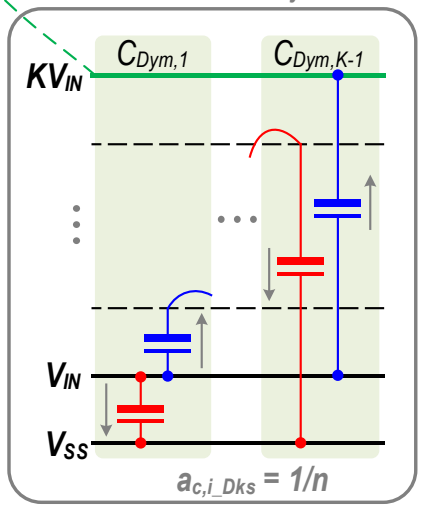
Generate $(K\text{-}1)V_{IN}$ for C_{x1} in Φ_1



Generate $(K\text{-}1)V_{IN}$ for $C_{x(n-m-1)}$ in Φ_1



Generate KV_{IN} for C_{ym} in Φ_1

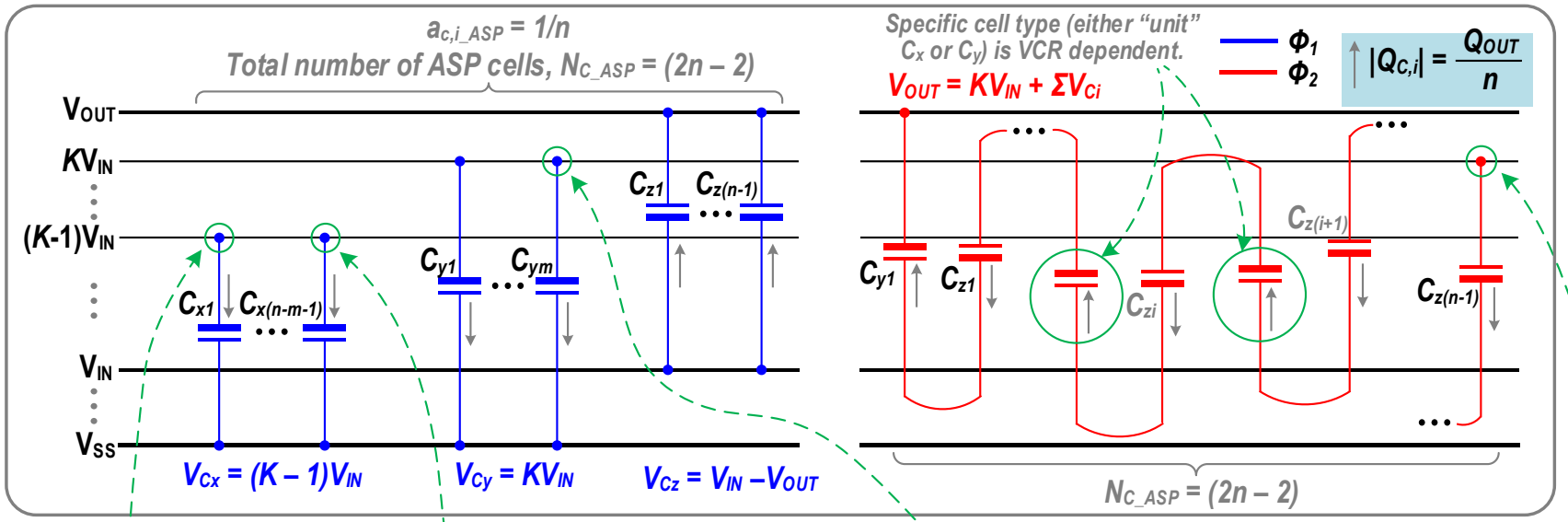


For all C_x: total number of C_{Dx}, $N_{C\_Dks,x} = (n - m - 1)(K - 2)$

For all C_y: $N_{C\_Dks,y} = m(K - 1)$

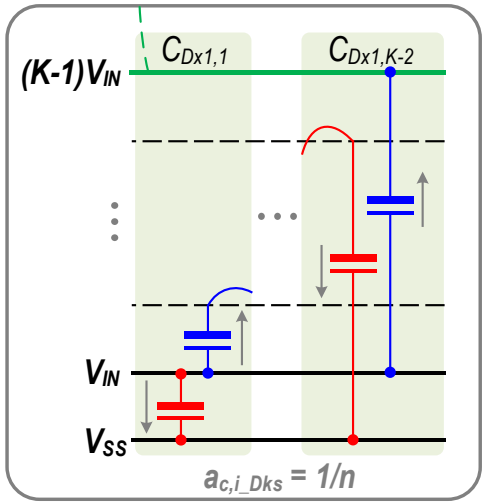
Integer Level Generation in ASP

Algebraic series-parallel stage

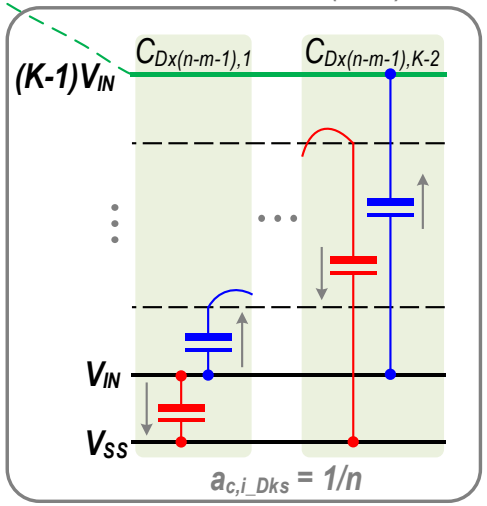


Dickson stage examples:

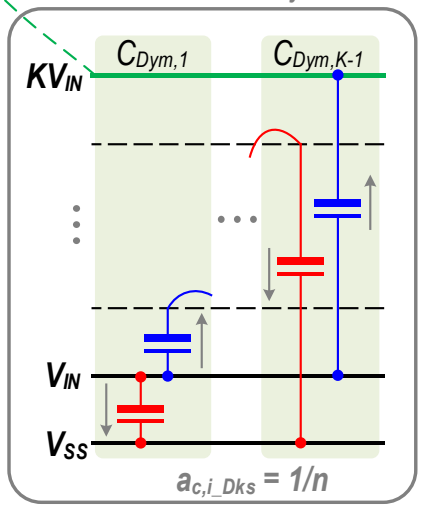
Generate $(K\text{-}1)V_{IN}$ for C_{x1} in Φ_1



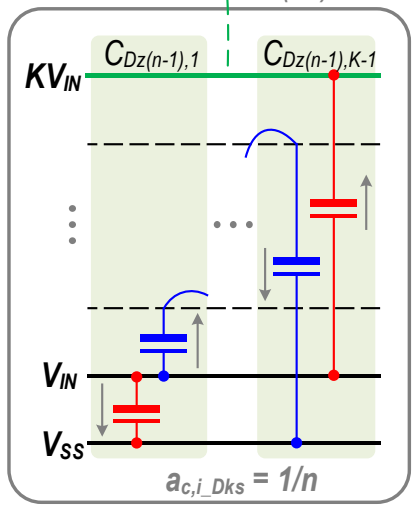
Generate $(K\text{-}1)V_{IN}$ for $C_{x(n-m-1)}$ in Φ_1



Generate KV_{IN} for C_{ym} in Φ_1



Generate KV_{IN} for $C_{z(n-1)}$ in Φ_2



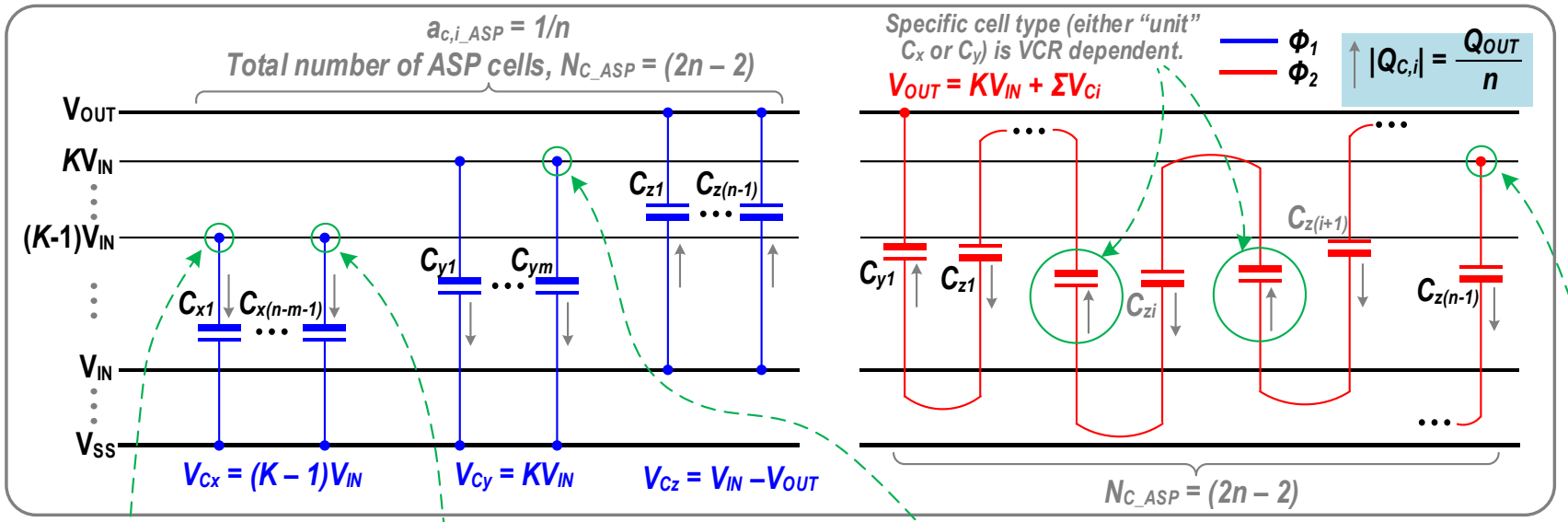
For all C_x: total number of C_{Dx}, $N_{C\_Dks,x} = (n - m - 1)(K - 2)$

For all C_y: $N_{C\_Dks,y} = m(K - 1)$

For $C_{z(n-1)}$: $N_{C\_Dks,z} = (K - 1)$

Complete ASP Topology Implementation

Algebraic series-parallel stage



No. of ***ASP*** cells:

$$N_{C-ASP} = 2n - 2$$

No. of ***integer*** cells:

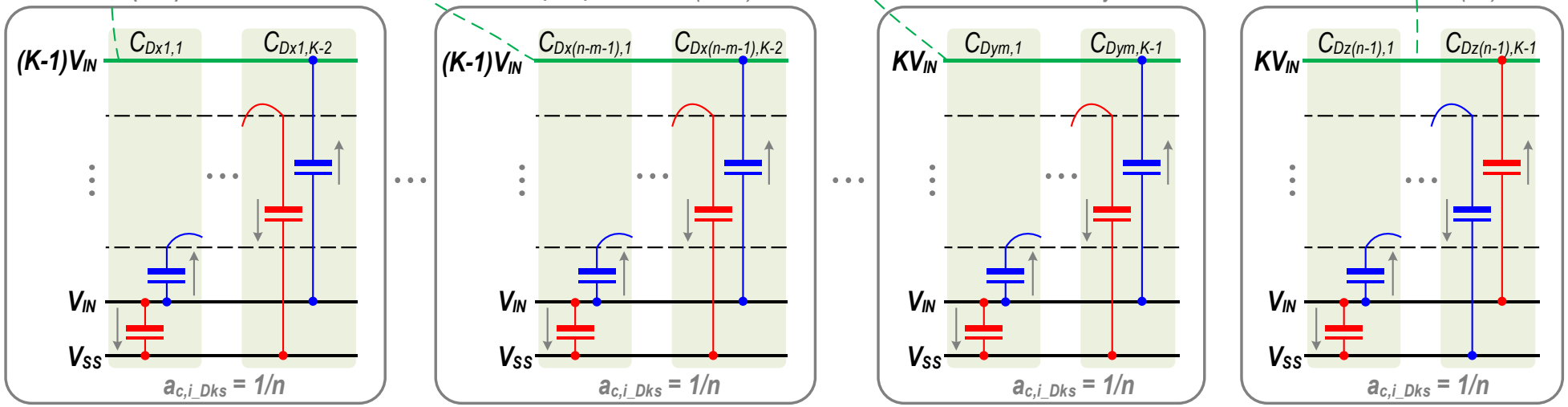
$$N_{C-int} = Kn - 2n + m + 1$$

Total no. of cells:

$$N_{C-total} = Kn + m - 1$$

Dickson stage examples:

Generate $(K\text{-}1)V_{IN}$ for C_{x1} in Φ_1 | Generate $(K\text{-}1)V_{IN}$ for $C_{x(n-m-1)}$ in Φ_1 | Generate KV_{IN} for C_{ym} in Φ_1 | Generate KV_{IN} for $C_{z(n-1)}$ in Φ_2



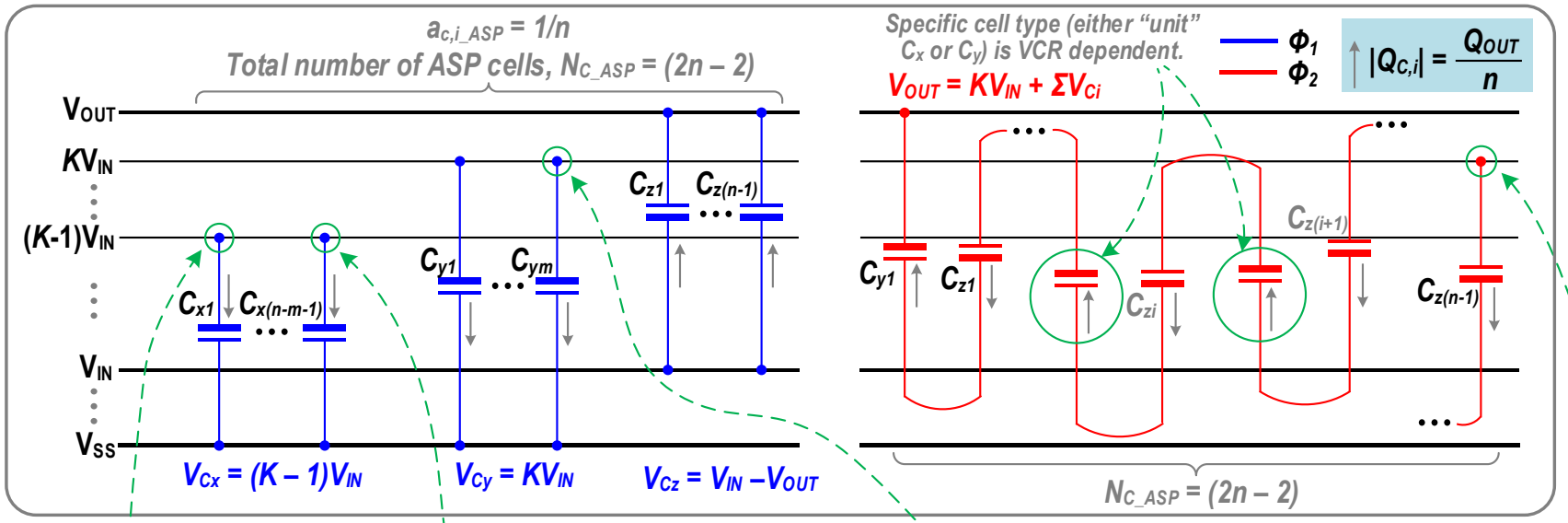
For all C_x: total number of C_{Dx}, $N_{C\_Dks,x} = (n - m - 1)(K - 2)$

For all C_y: $N_{C\_Dks,y} = m(K - 1)$

For $C_{z(n-1)}$: $N_{C\_Dks,z} = (K - 1)$

Complete ASP Topology Implementation

Algebraic series-parallel stage



No. of **ASP** cells:

$$N_{C-ASP} = 2n - 2$$

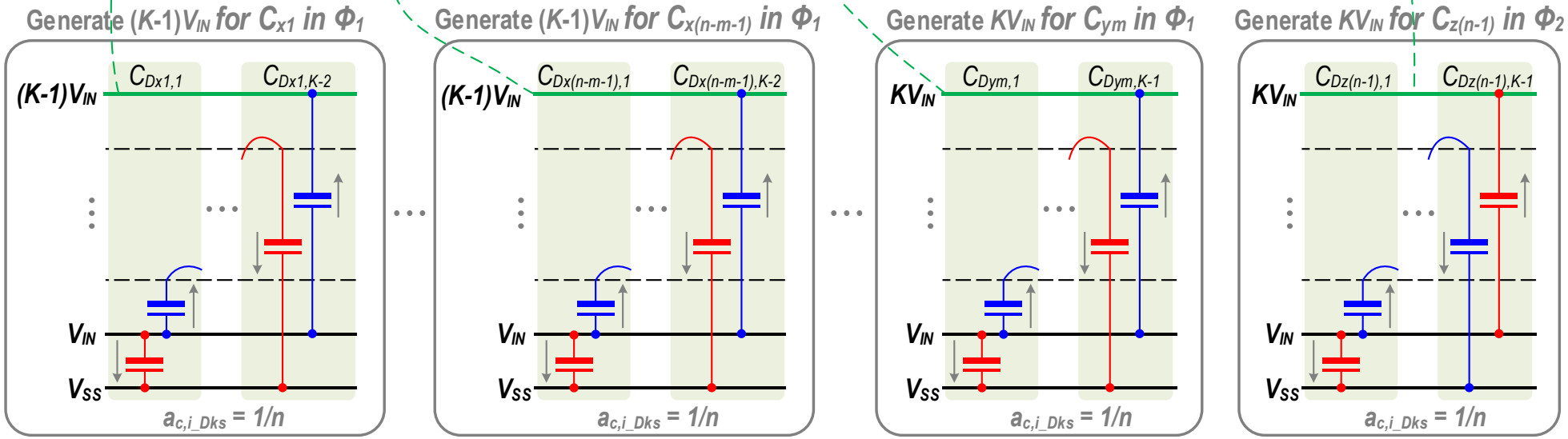
No. of **integer** cells:

$$N_{C-int} = Kn - 2n + m + 1$$

Total no. of cells:

$$N_{C-total} = Kn + m - 1$$

Dickson stage examples:



For all C_x: total number of C_{Dx}, $N_{C\_Dks,x} = (n - m - 1)(K - 2)$

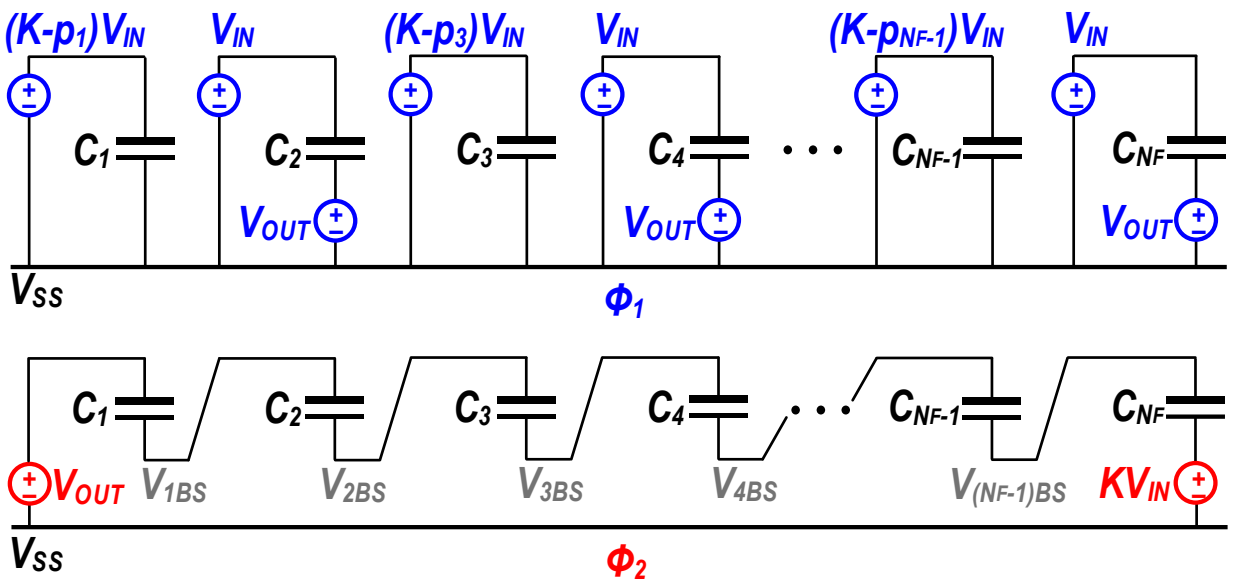
For all C_y: $N_{C\_Dks,y} = m(K - 1)$

For $C_{z(n-1)}$: $N_{C\_Dks,z} = (K - 1)$

$$R_{SSL,ASP} = R_{SSL,opt} = \frac{1}{C_{TOT} f_S} \left(\frac{Kn + m - 1}{n} \right)^2$$

ASP topology attains optimal R_{SSL}

ASP Topology Design Framework

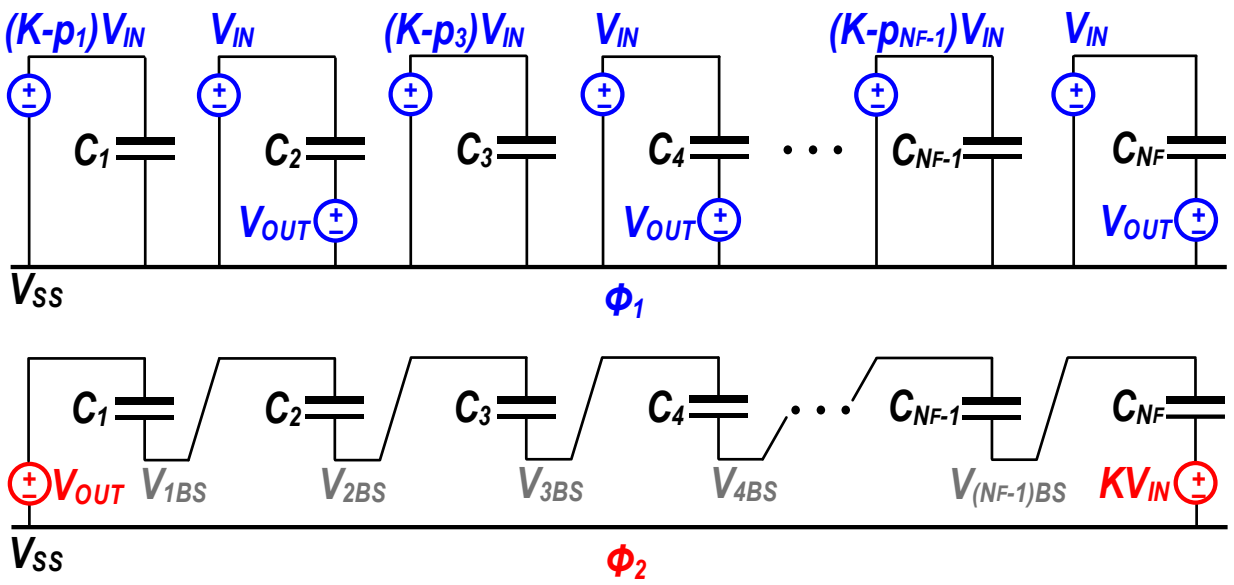


p_i = {0,1} is a design parameter $N_F = 2n - 2$

Capacitor voltage balance:

$$\underbrace{(K-p_1)V_{IN} + (V_{IN} - V_{OUT}) + (K-p_3)V_{IN} + (V_{IN} - V_{OUT})}_{\Phi_1}$$
$$\underbrace{+ \cdots + \left(K - p_{N_F-1}\right)V_{IN} + (V_{IN} - V_{OUT})}_{\Phi_1} = \underbrace{V_{OUT} - KV_{IN}}_{\Phi_2}$$

ASP Topology Design Framework



p_i = {0,1} is a design parameter $N_F = 2n - 2$

Capacitor voltage balance:

$$(K-p_1)V_{IN} + (V_{IN} - V_{OUT}) + (K-p_3)V_{IN} + (V_{IN} - V_{OUT}) + \cdots + \left(K - p_{N_F-1}\right)V_{IN} + (V_{IN} - V_{OUT}) = V_{OUT} - KV_{IN}.$$

Φ_1 Φ_2

$$VCR_{ASP} = \frac{V_{OUT}}{V_{IN}} = K + \frac{N_F - 2\sum_{k=1}^{N_F/2} p_{2k-1}}{N_F + 2}$$

m/n

$\because N_F = 2n - 2$

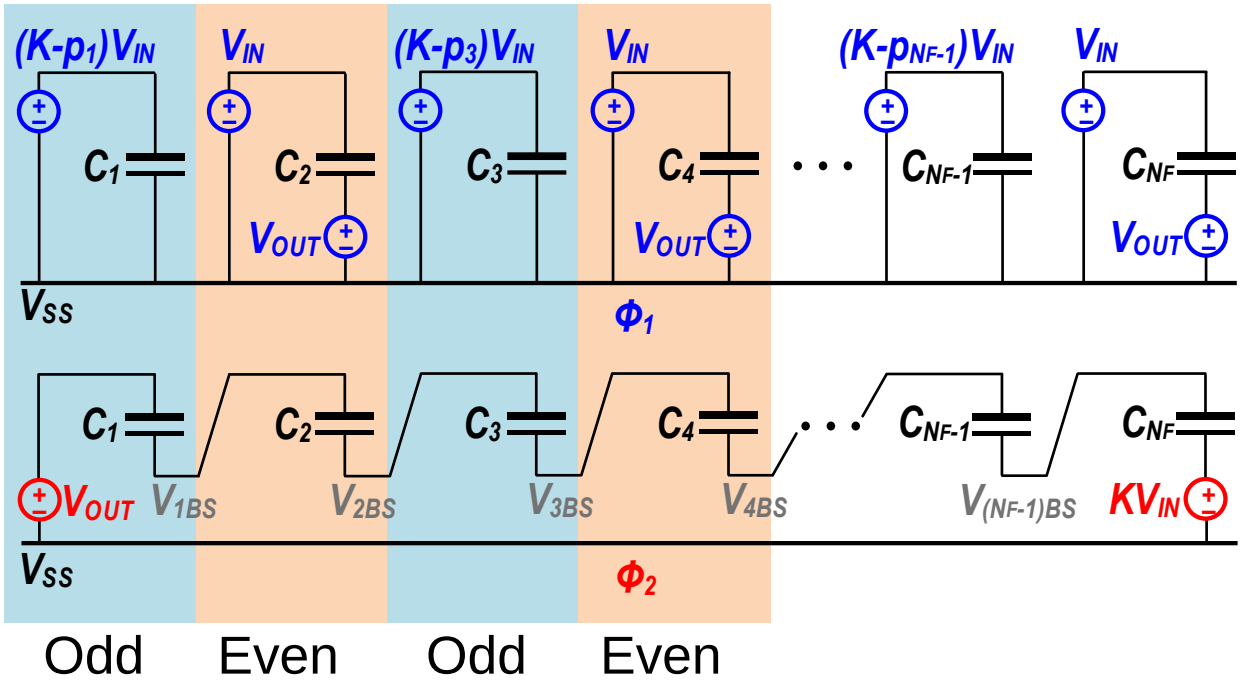
$\therefore \Sigma p_i = n - m - 1$ with optimal R_{SSL}

However, there can be different options for the result of p_1, p_3, p_5 ...

- p_i selection for parasitic loss reduction

Determination of Parameter p_i

- **Strategy: Limit Bottom-plate Switching Voltage $|\Delta V_{CB}|$**



$$(K-1)V_{IN} < V_{OUT} - V_{IN} < KV_{IN}$$

Constraint condition: $|\Delta V_{CBi}| < V_{IN}$

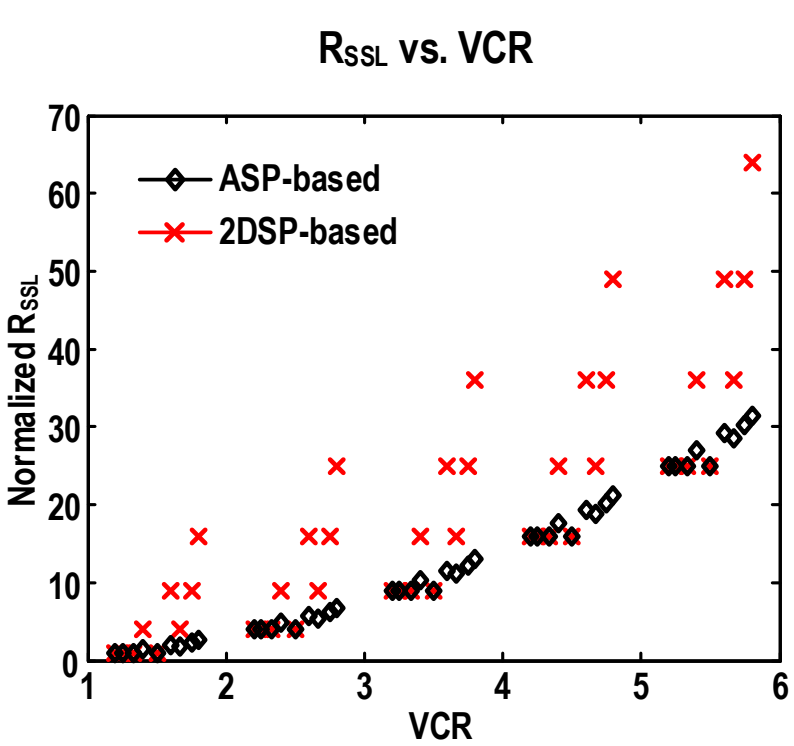
$$p_i(i\ is\ odd) = \begin{cases} 1, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) > 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \\ 0, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) < 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \end{cases}$$

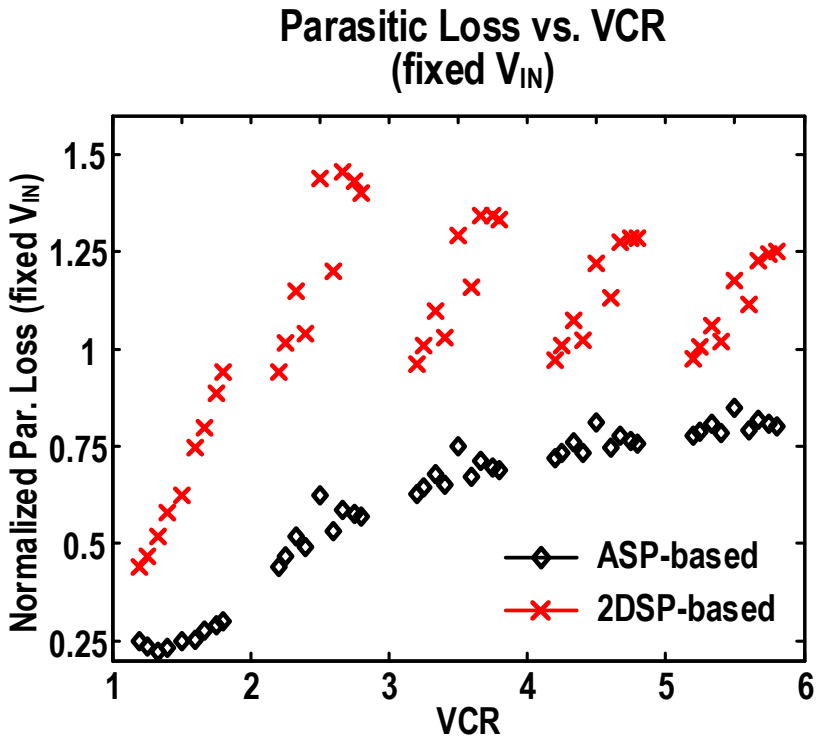
[Y. Jiang, JSSC'19]

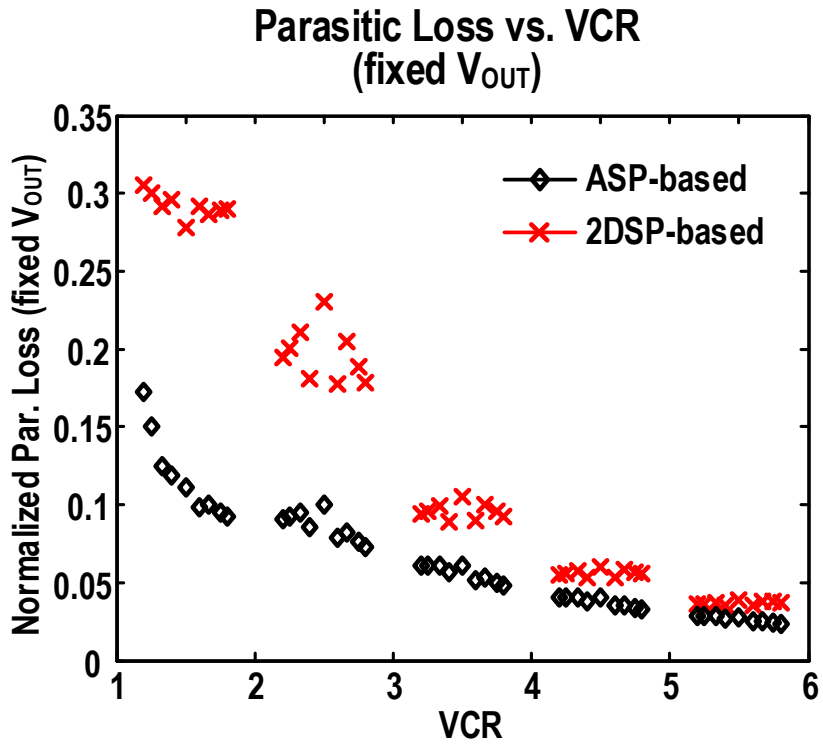
$$|\Delta V_{CBi}| = \begin{cases} \left|\Delta V_{CB(i-1)} + \left(\frac{m}{n} + p_i\right) V_{IN}\right|, & (i\ is\ odd) \\ \left|\Delta V_{CB(i-1)} - V_{IN}\right|, & (i\ is\ even) \end{cases}$$

Loss Comparison

- **ASP-based vs. 2DSP-based Topology (on conduction and parasitic Losses)**

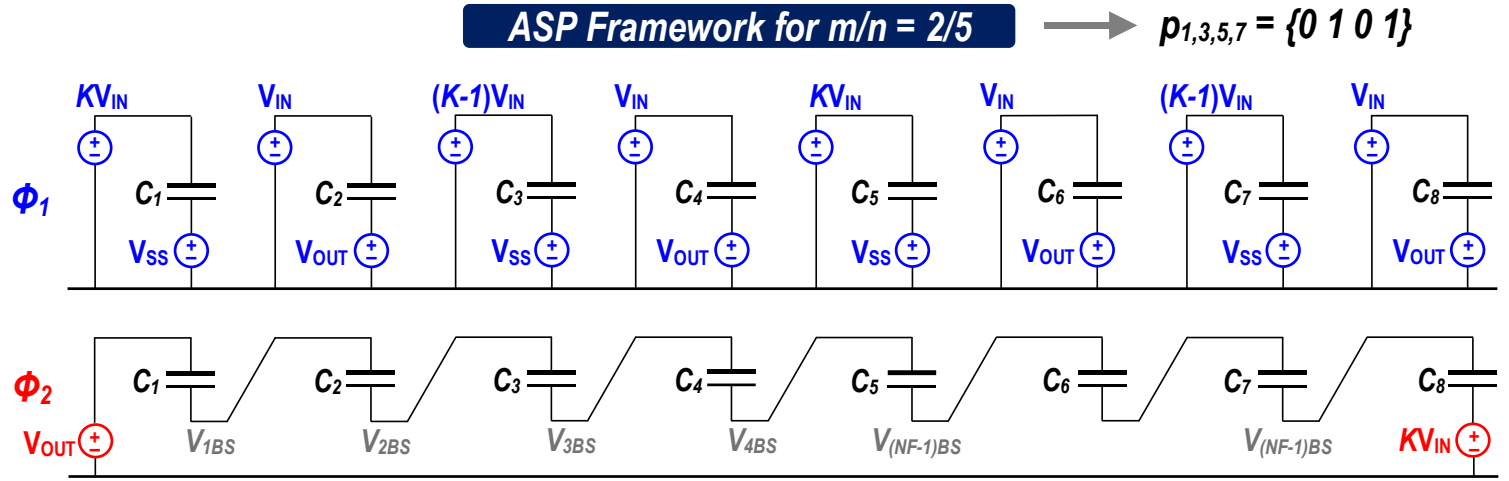






- ✓ $R_{SSL,ASP} < R_{SSL,2DSP}$ *(except for m = 1)*
- ✓ **ASP-based ones achieve lower parasitic loss in both fixed V_{IN} and V_{OUT} cases.**

ASP-based Topology Example



Step 1

Targeted VCR:

5:7 → *K = 1, m = 2, n = 5*

5:12 → *K = 2, m = 2, n = 5*

Step 2

No. of ASP cells:

$N_F = 2n - 2$

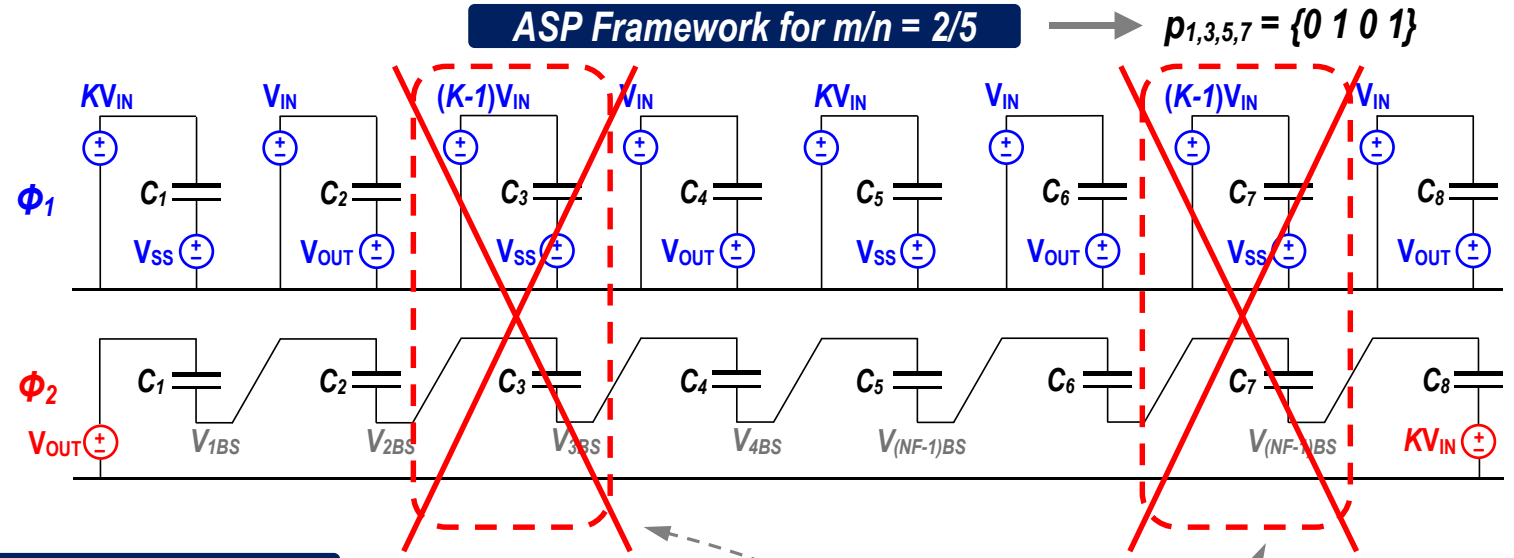
→ 8 cells for ASP

Step 3

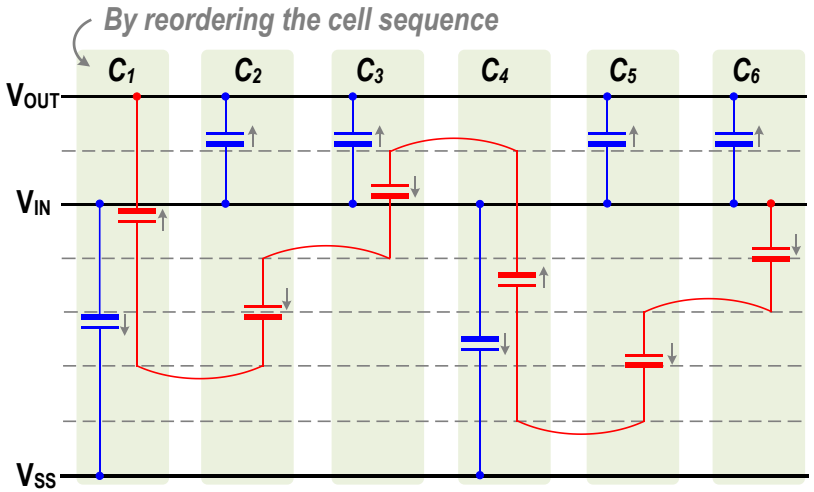
Determine p_i

$$p_i(i\ is\ odd) = \begin{cases} 1, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) > 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \\ 0, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) < 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \end{cases}$$

ASP-based Topology Example



ASP-Based 5:7 (K = 1)



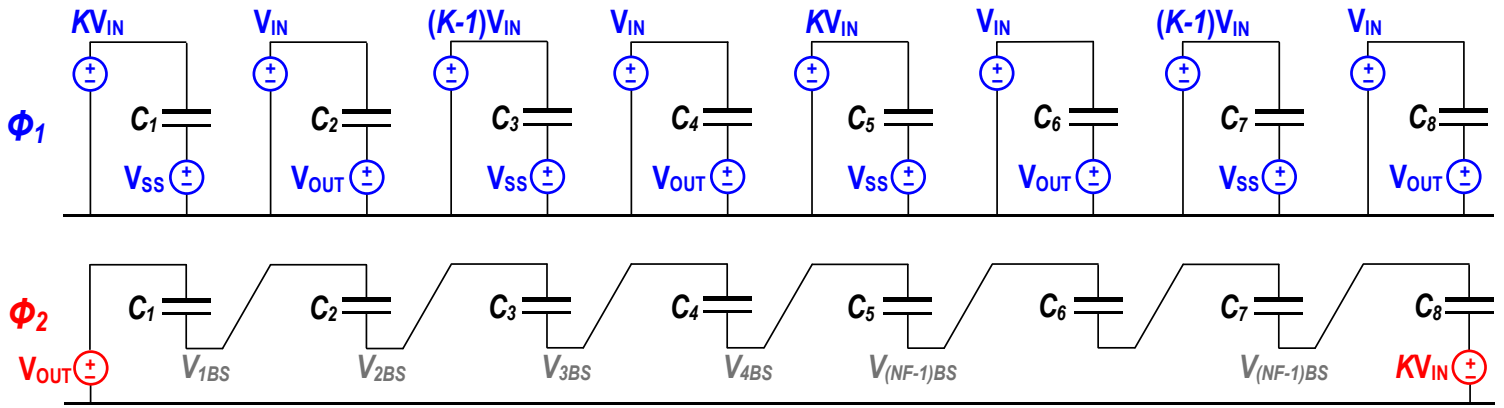
$$\frac{\Delta V_{CB}}{V_{IN}} = \{\frac{2}{5} \quad -\frac{3}{5} \quad -\frac{1}{5} \quad \frac{1}{5} \quad -\frac{4}{5} \quad -\frac{2}{5}\}$$

Notice:

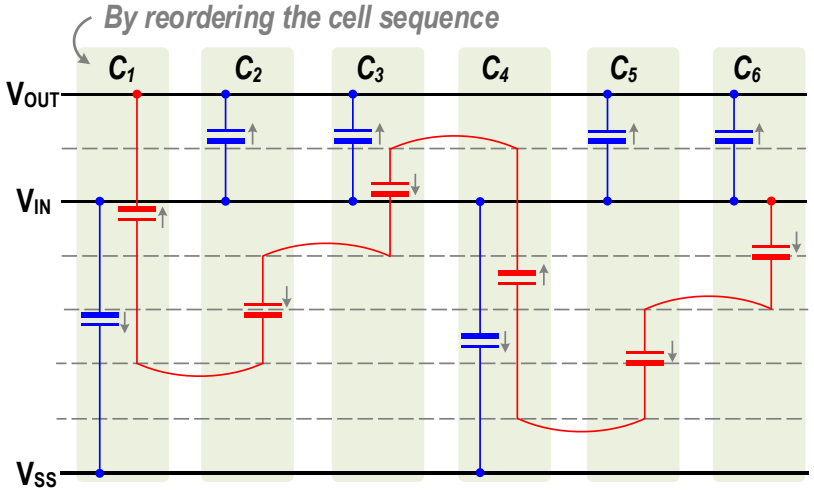
With K = 1, C_3 and C_7 in the framework are simply eliminated.

ASP-based Topology Example

ASP Framework for m/n = 2/5 → $p_{1,3,5,7} = \{0\ 1\ 0\ 1\}$



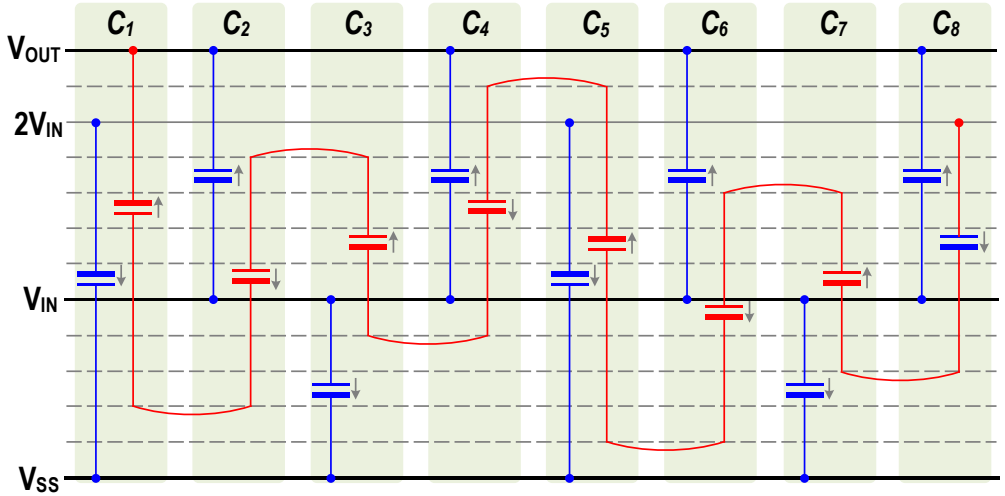
ASP-Based 5:7 (K = 1)



$$\frac{\Delta V_{CB}}{V_{IN}} = \{\frac{2}{5} \quad -\frac{3}{5} \quad -\frac{1}{5} \quad \frac{1}{5} \quad -\frac{4}{5} \quad -\frac{2}{5}\}$$

ASP-Based 5:12 (K = 2)

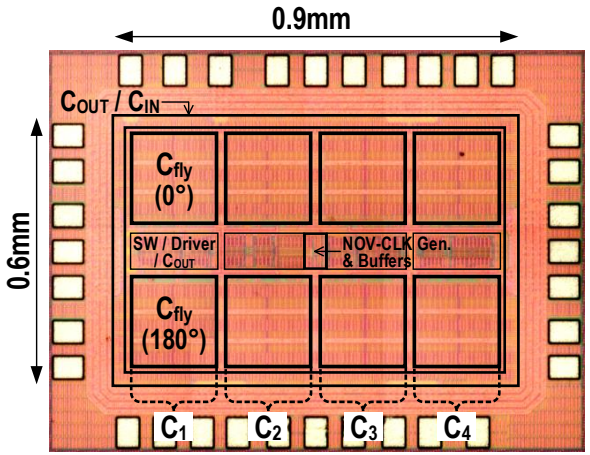
With K > 1, no cell should be eliminated.



$$\frac{\Delta V_{CB}}{V_{IN}} = \{\frac{2}{5} \quad -\frac{3}{5} \quad \frac{4}{5} \quad -\frac{1}{5} \quad \frac{1}{5} \quad -\frac{4}{5} \quad \frac{3}{5} \quad -\frac{2}{5}\}$$

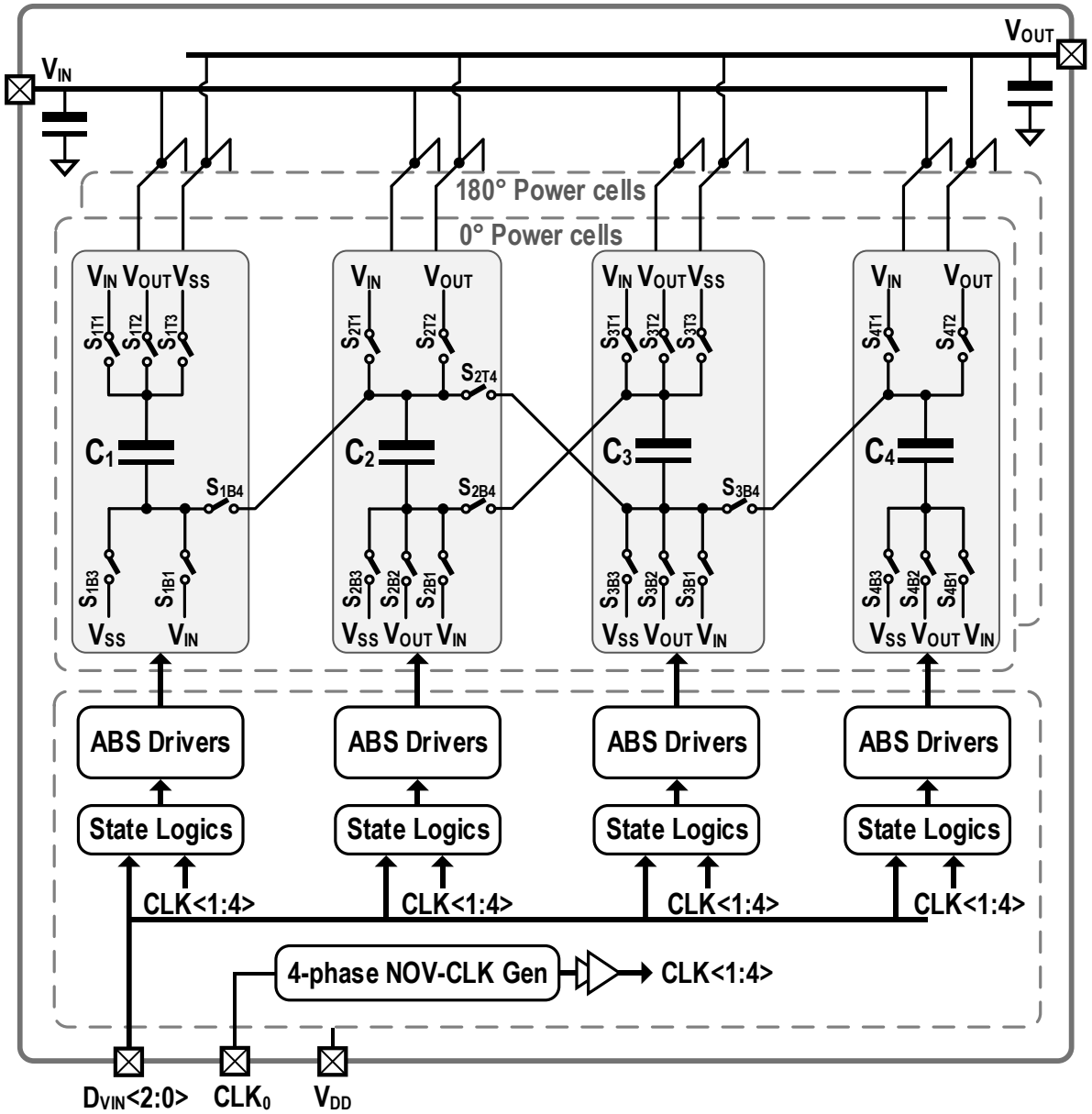
ASP-based Boost Converter Design Overview

- Fully integrated in 65-nm bulk CMOS using 1-V core devices
- 7 reconfigurable rational boost VCRs (from 1:1.25 to 1:5)
- V_{IN}: 0.25~1V, V_{OUT} = 1V
- Dual-branch interleaving architecture
- Adaptive bootstrapping (ABS) switch driving circuits



Active area: 0.54mm^2

Total C_{fly} ~3nF using MIM+MOS capacitors

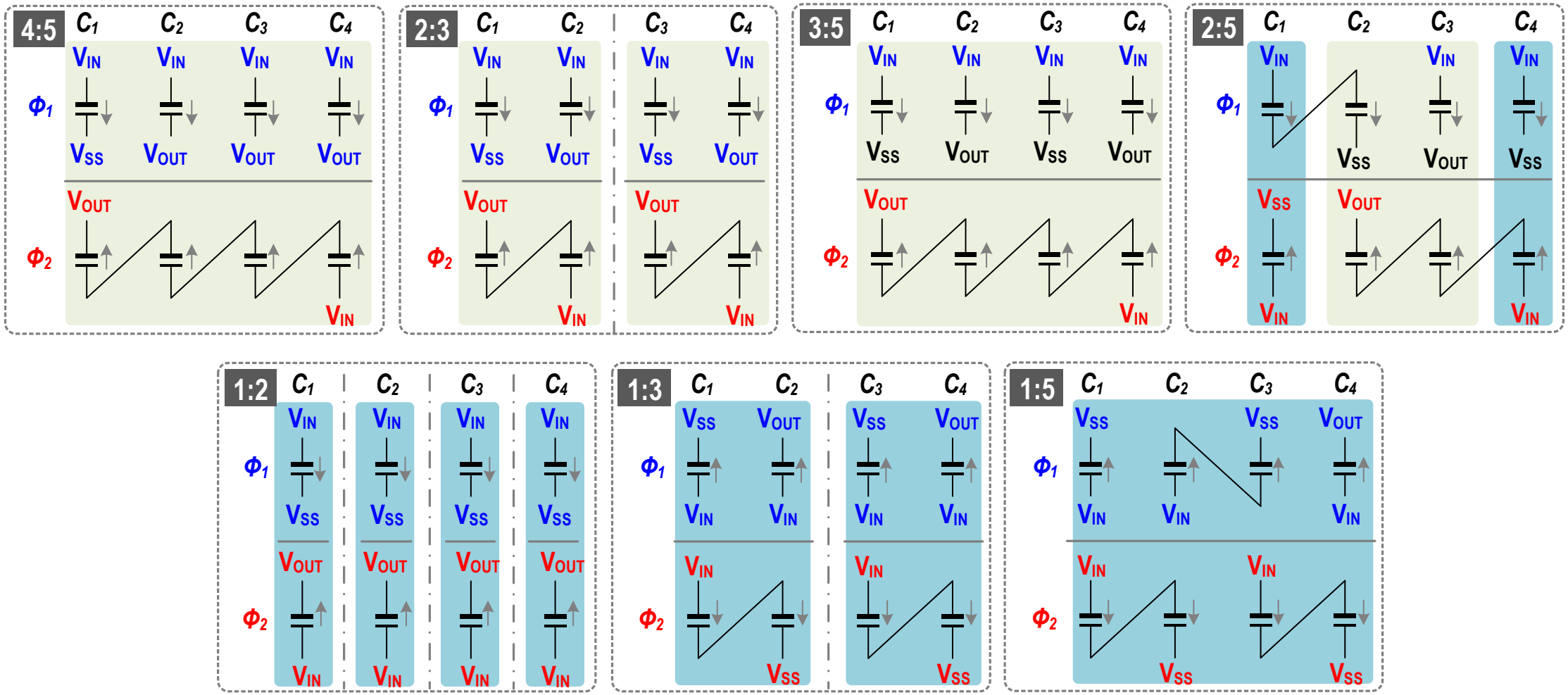


Power Stage Reconfiguration Modes Summary

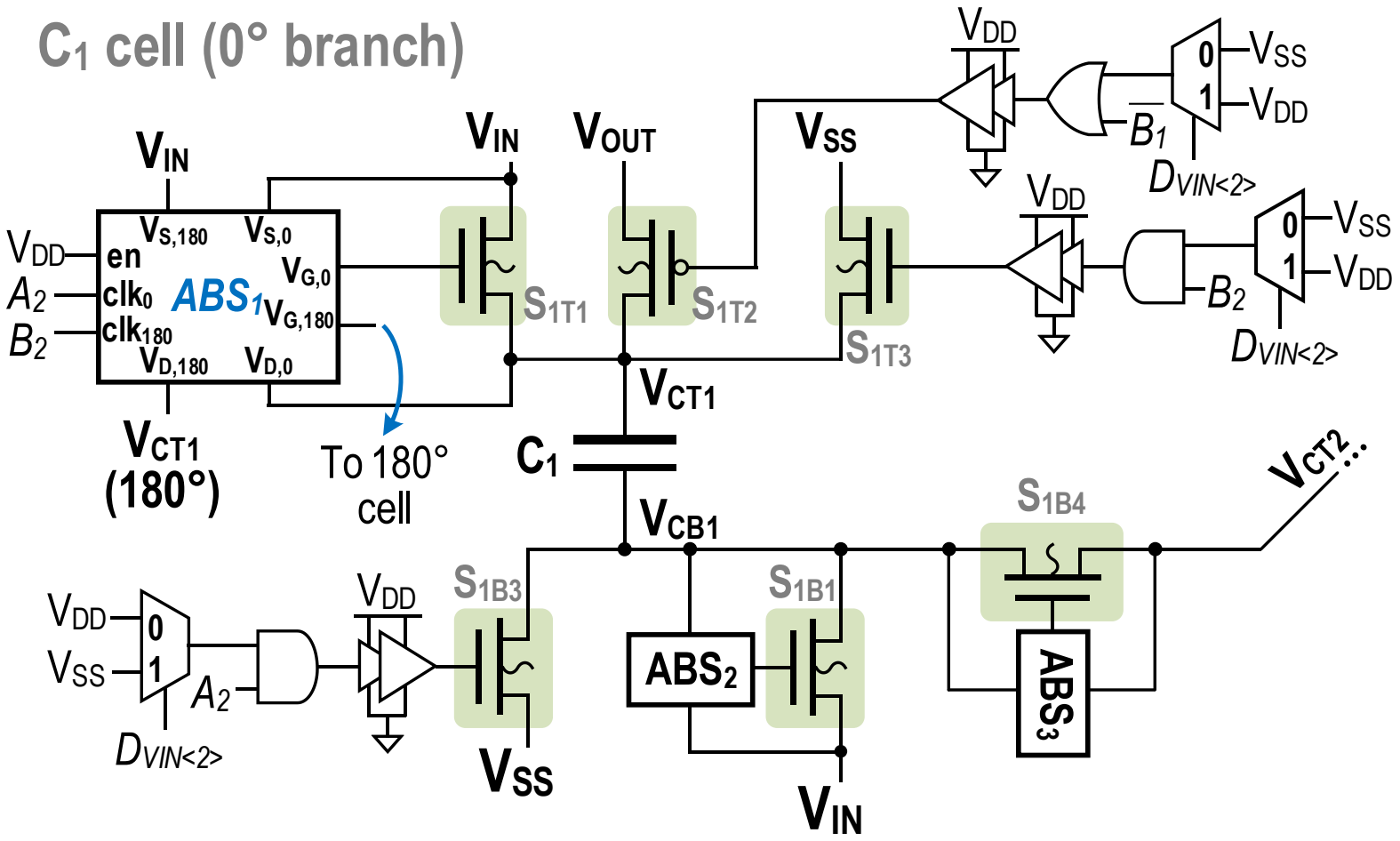
■ 7 Boost Topologies

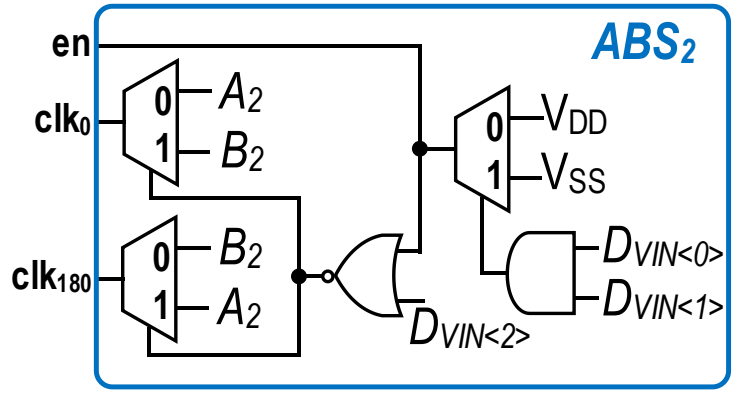
Fractional Part (ASP)

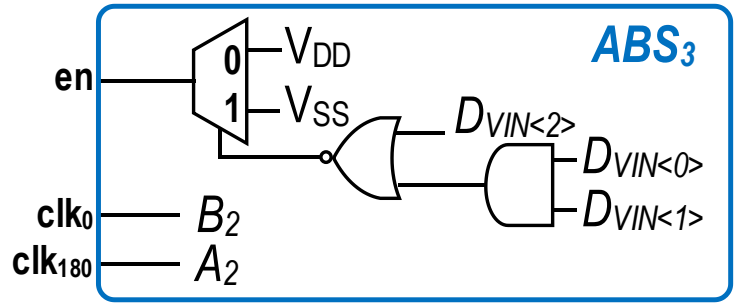
Integer Part (Dickson)



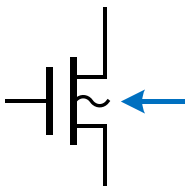
Power Cell Implementation (C_1)



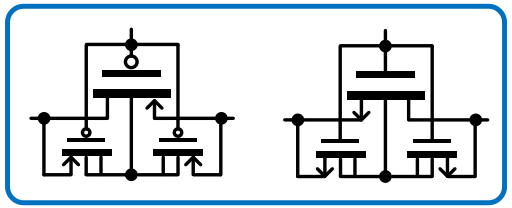




$D_{VIN<2:0>}$ = 000 ~ 110 → VCR = 4:5 ~ 1:5



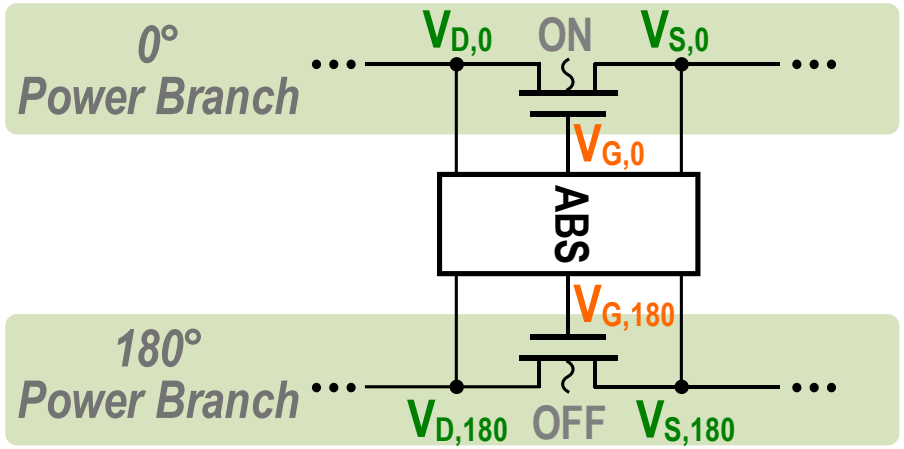
Dynamic body biasing
for P-/N-switch



- ***Signals from state logics and D_{VIN}***
- ***LV power switches***
- ***Supports dual-branch operations***

Working Principle of Adaptive Bootstrapping Driver

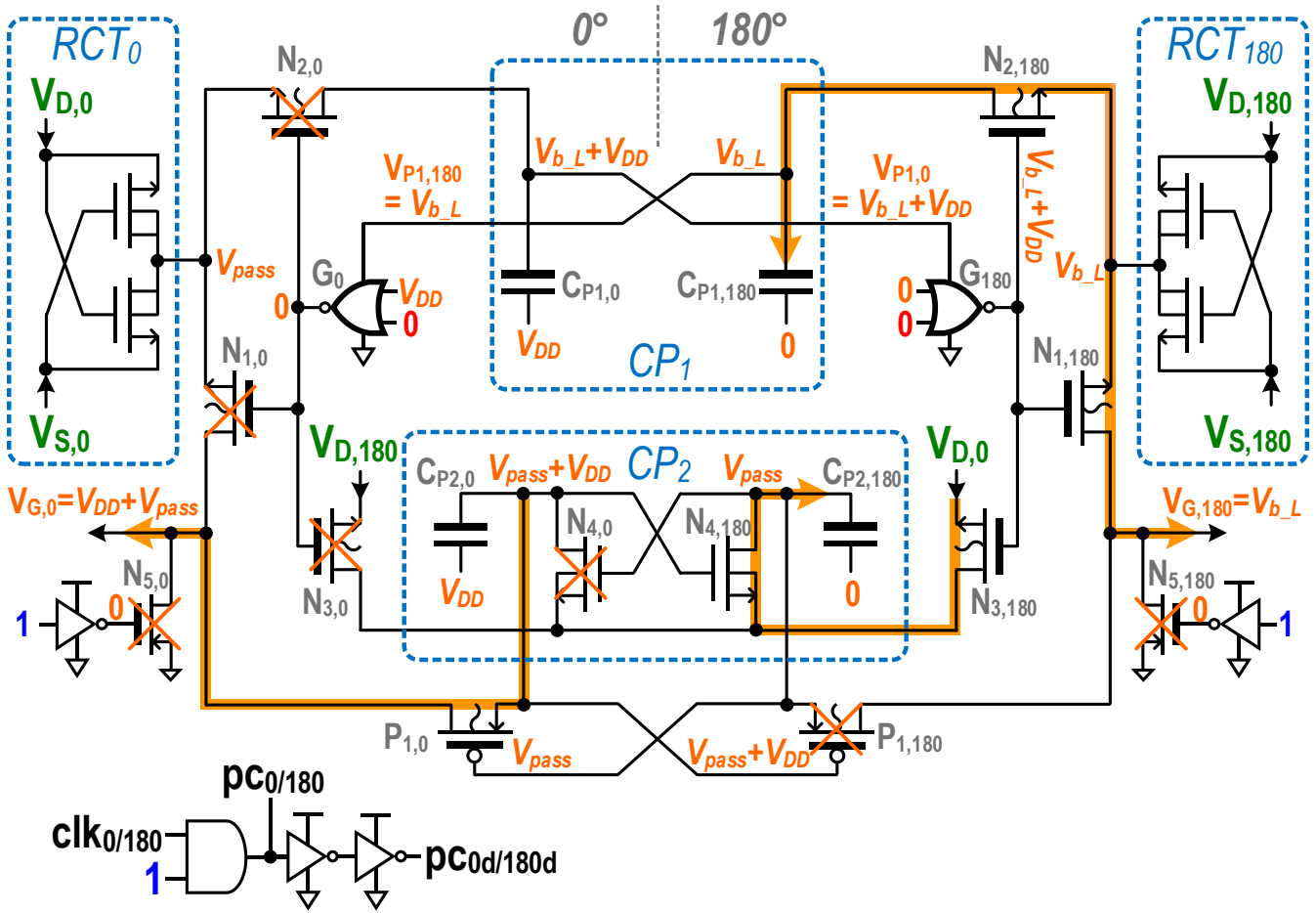
Active State (en=1, $\overline{en}$=0)



$V_{D,0} = V_{S,0} = V_{pass}$

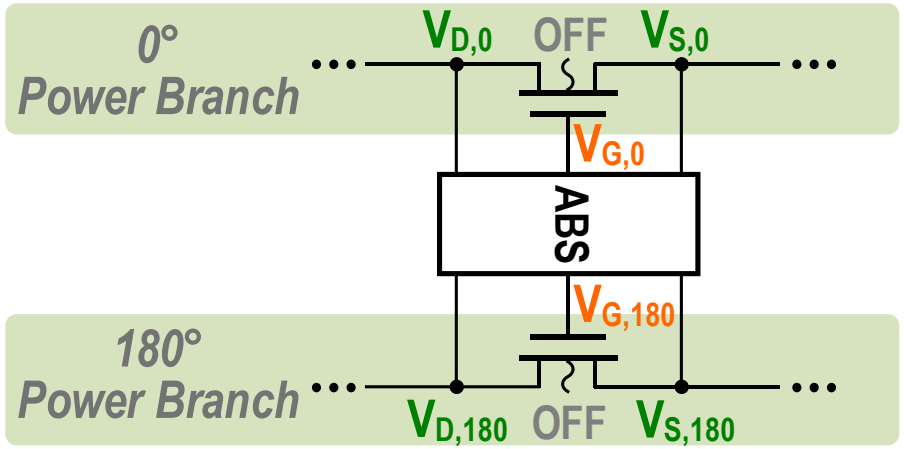
$V_{D,180} \neq V_{S,180}$

$Min(V_{D,180}, V_{S,180}) = V_{b\_L}$



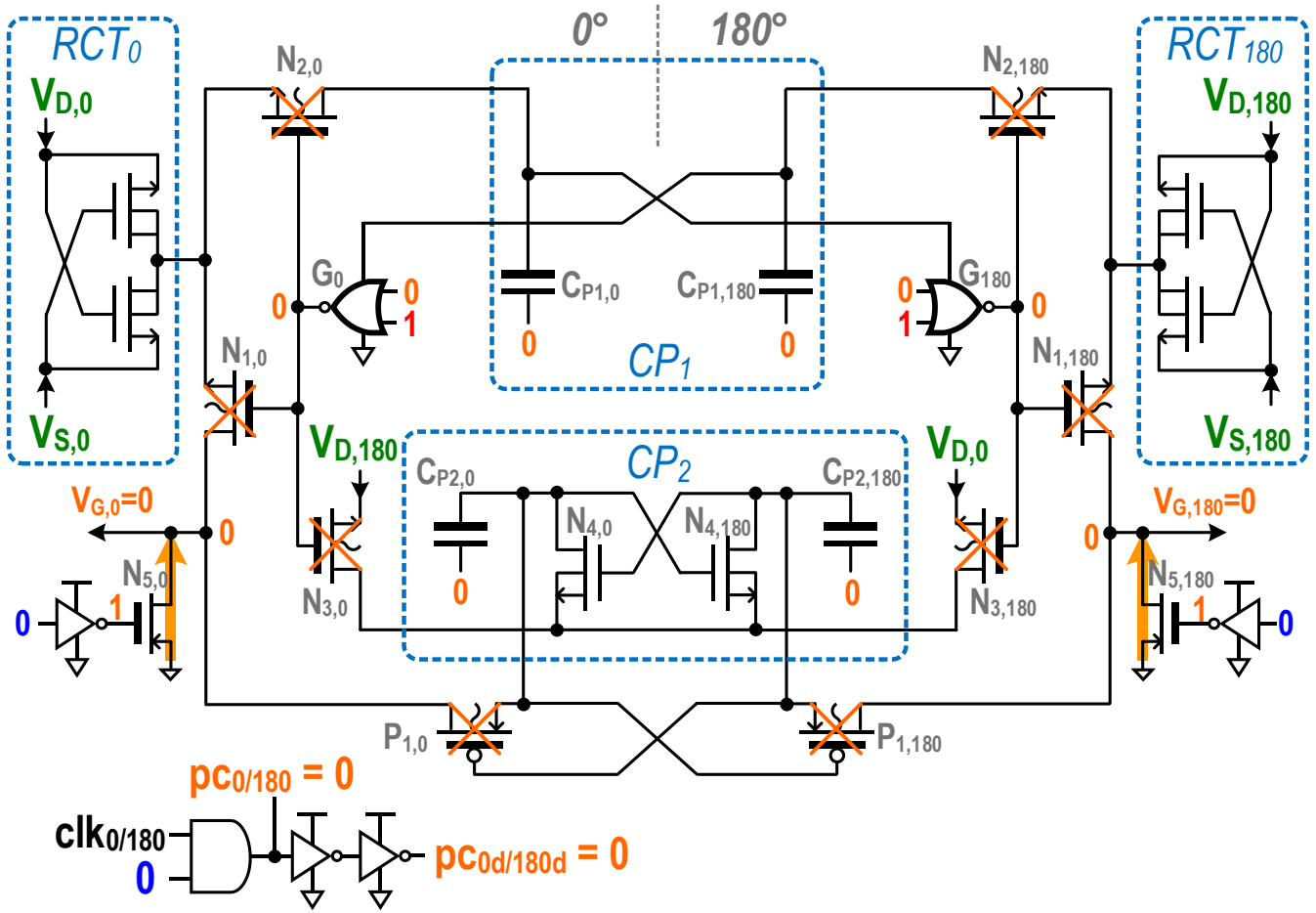
Working Principle of Adaptive Bootstrapping Driver

Disable State (en=0, $\overline{en}$=1)

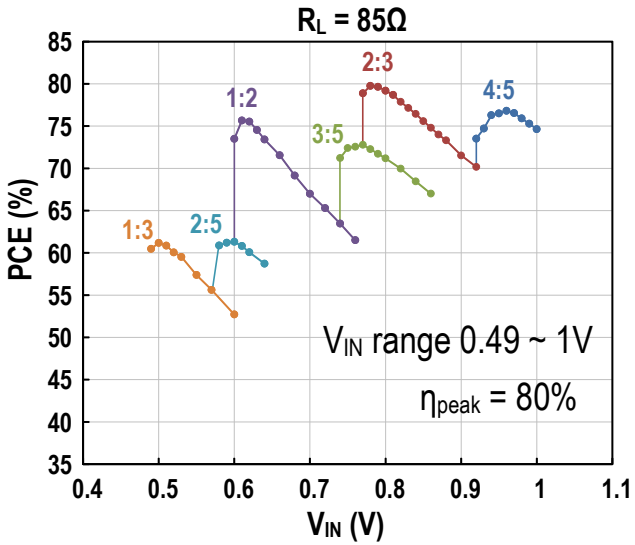


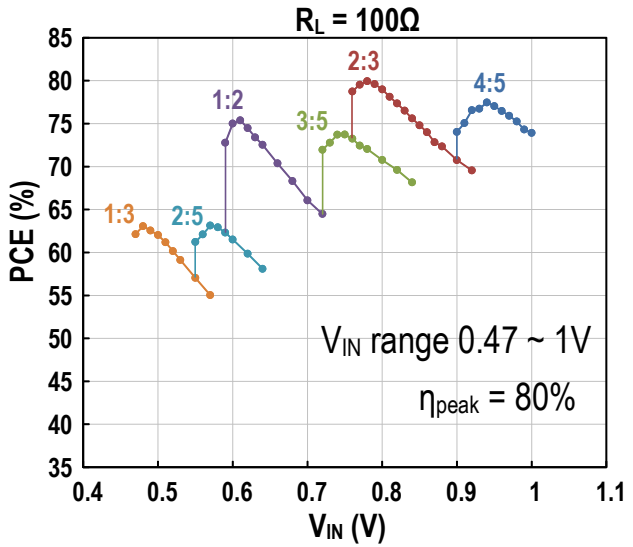
$V_{D,0} \neq V_{S,0}$

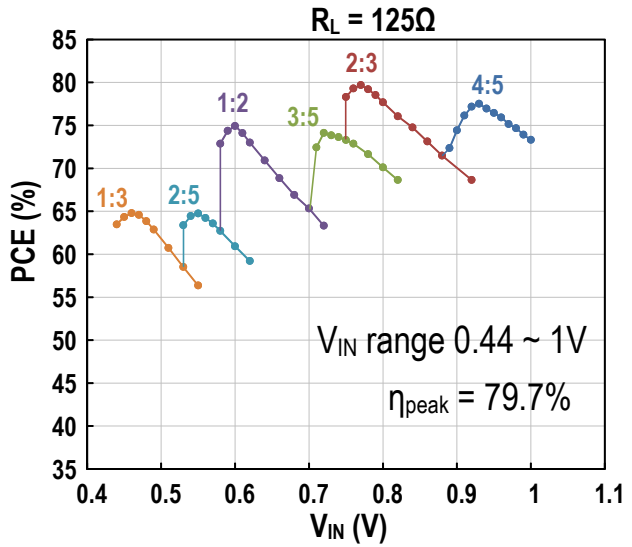
$V_{D,180} \neq V_{S,180}$

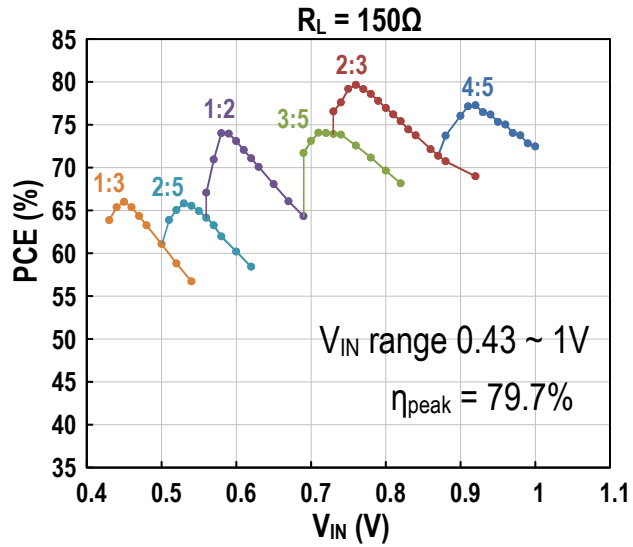


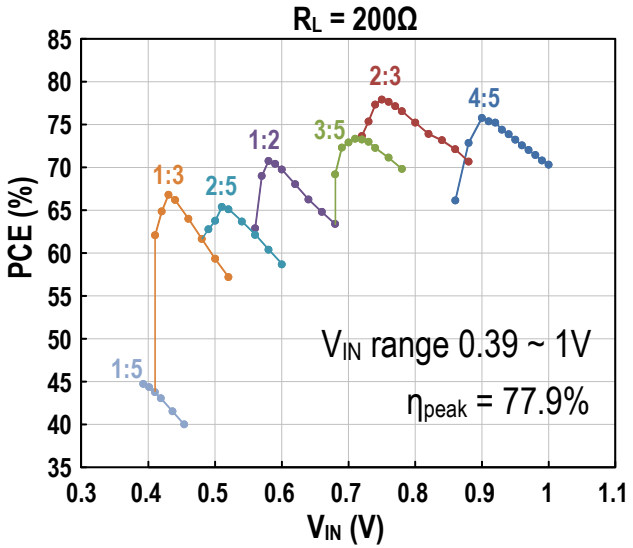
Measured Conversion Efficiency over V_{IN}

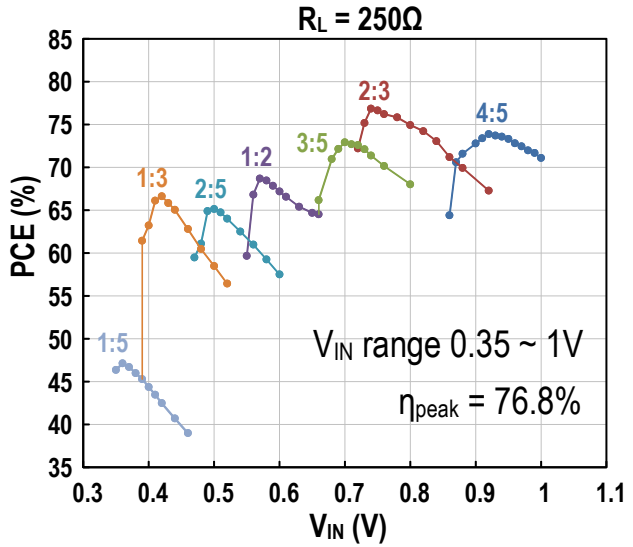


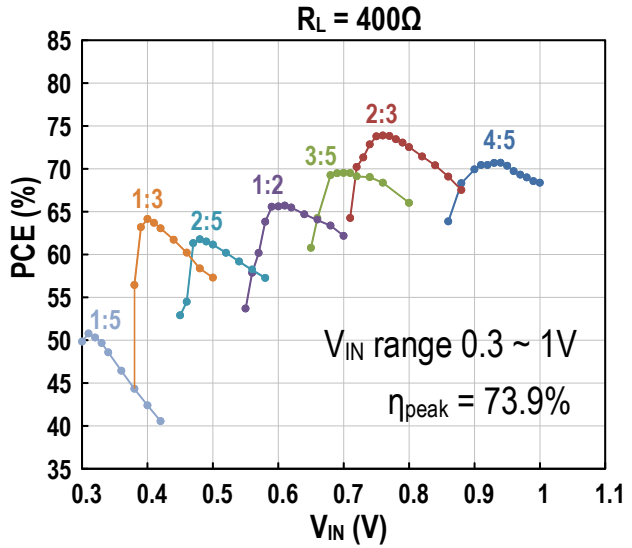


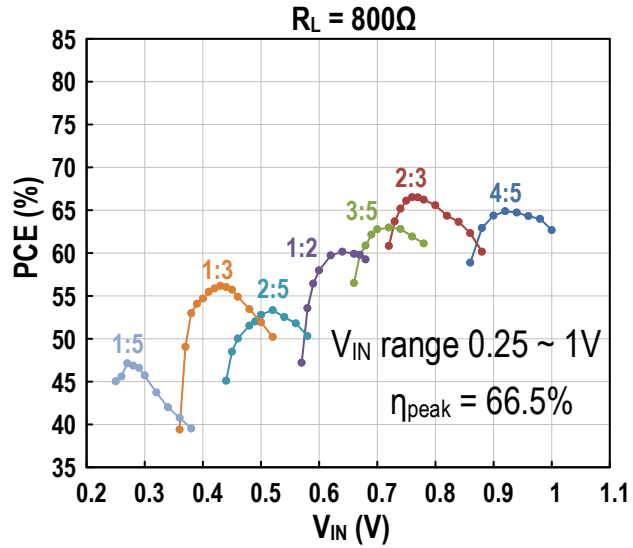






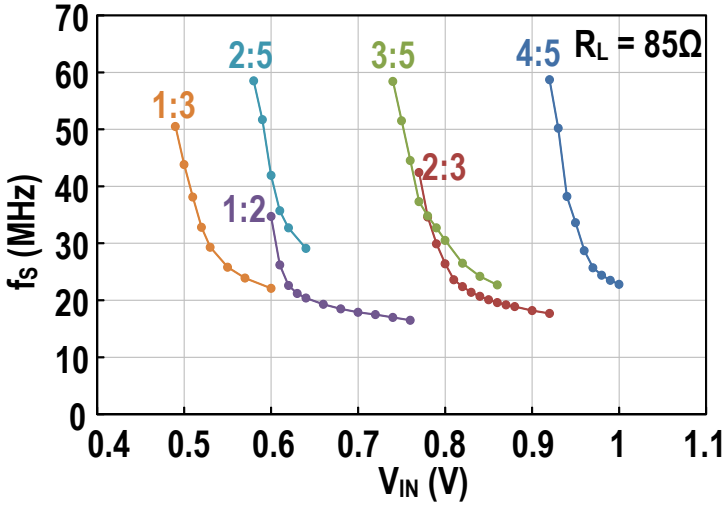


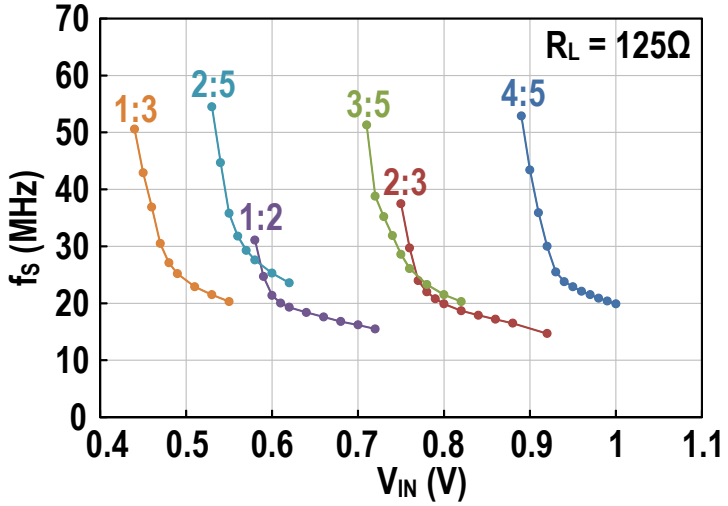


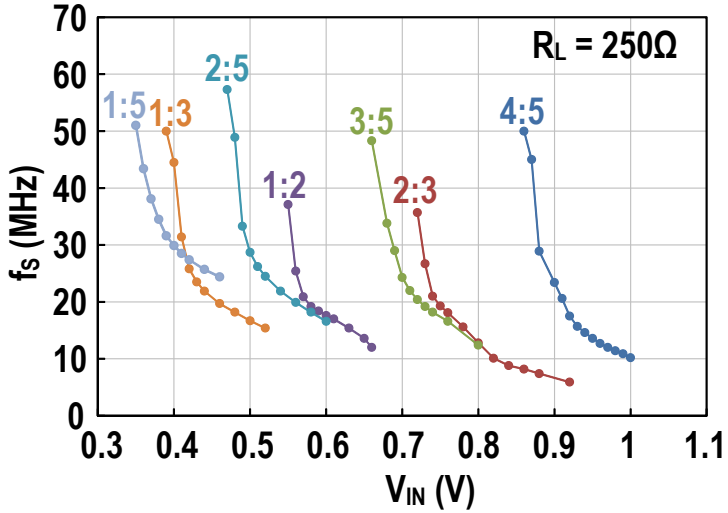


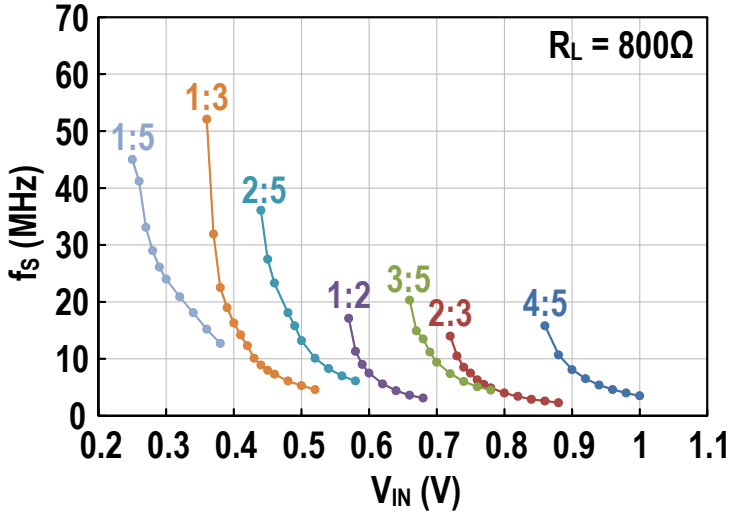
- **Peak efficiency of 80%** at 2:3 is attained in heavy load cases with V_{OUT} = 1V

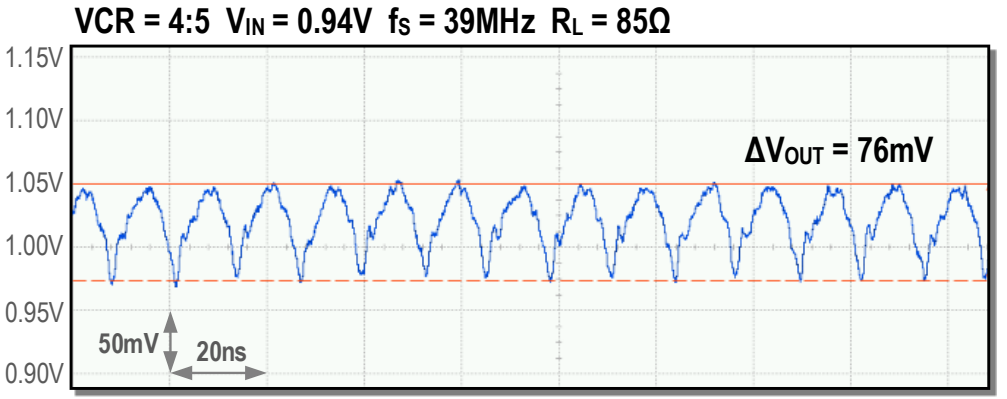
Converter Operating Frequency and Output Waveform

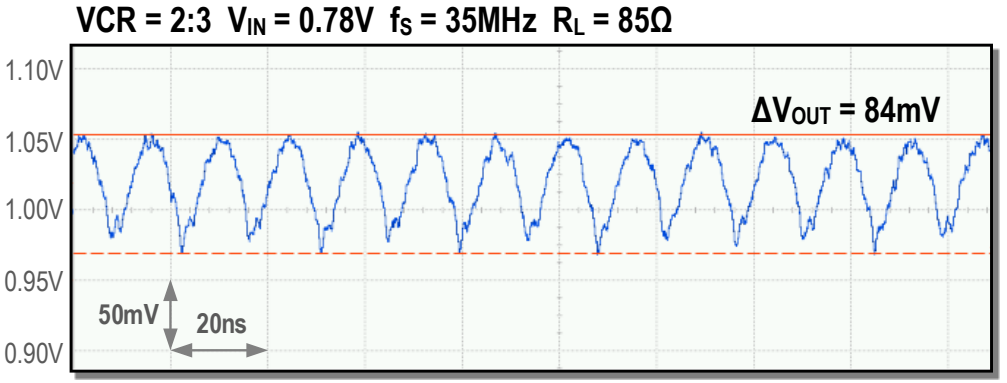












- V_{IN} vs. f_s at different R_L and VCR with V_{OUT} = 1V
- Measured V_{OUT} for 4:5 and 2:3 without using off-chip filtering capacitors.

Performance Summary and Comparison

	This work	JSSC'16 [15]	JSSC'15 [24]	JSSC'15 [30]	TVLSI'15 [13]	JSSC'17 [16]	JSSC'18 [34]	ISSCC'16 [35]
Technology	**65nm CMOS**	180nm CMOS	28nm FD-SOI	180nm CMOS	0.35µm CMOS	180nm CMOS	65nm CMOS	0.35µm HVCMOS
Conversion type	**Boost**	Boost	Boost	Boost	Boost	Boost	Buck-Boost	Buck-Boost
Topology type	**ASP-based (ASP+Dickson)**	SP-based (transposed SP)	Customized	Customized	SP-based (transposed SP)	Moving-sum (Dickson+SP)	AVFI	Binary Recursive
VCR type	**Rational**	Rational	Rational	Integer	Rational	Integer	Rational	Rational
Number of VCR	**7**	14	3	2	4	*22	13 (boost)	9 (boost)
VCR range	**1.25 ~ 5**	1.33 ~ 8	1.5 ~ 2.5	4 ~ 6	2 ~ 4 (boost)	10 ~ 31	1.1 ~ 7 (boost)	1.14 ~ 4 (boost)
Integrated C_{fly}	**MOS + MIM**	HD-MIM	MOS + MOM	MOS + MIM	Off-chip	N/R	MOS + MIM	MIM
V_{IN} Range [V]	**0.25 ~ 1**	0.45 ~ 3	1	1	1.4 ~ 3	0.25 ~ 0.65	0.26 ~ 1.3 (boost)	2 ~ 6 (boost)
V_{OUT} [V]	**1**	3.3	1.2 ~ 2.4	3 ~ 6	4.8	4	1.2	5
I_{OUT_MAX} [mA]	**20.1**	0.015	1	0.24	10	*0.001	21.7 (boost)	1.4 (boost)
η_{peak} [%]	**#80**	81	#88	58	82	60	83.2 (boost)	70.9 (boost)
P-density @η_{peak} [mW/mm^2]	**#22.7**	*0.0174	#4.9	*2.4	N/A	*~0.0001	10.8 (boost)	*0.15 (boost)
Fully integrated	**Yes**	Yes	Yes	Yes	No	Yes	Yes	Yes

*Estimated from the corresponding literature

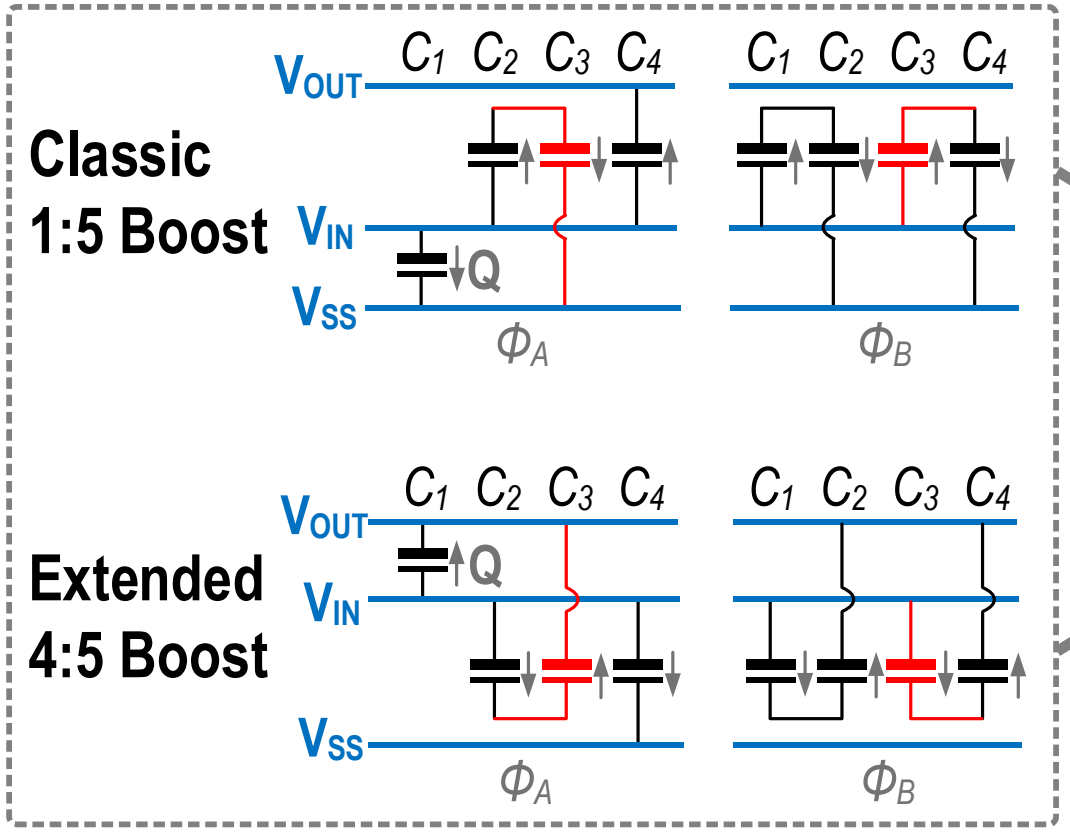
#Regulation control executed externally

Outline

- Background and Motivation
- Algebraic Series-Parallel (ASP)-based Boost Topology
- Algorithmic Voltage-Feed-In (AVFI) Buck/Boost Topology
- Summary

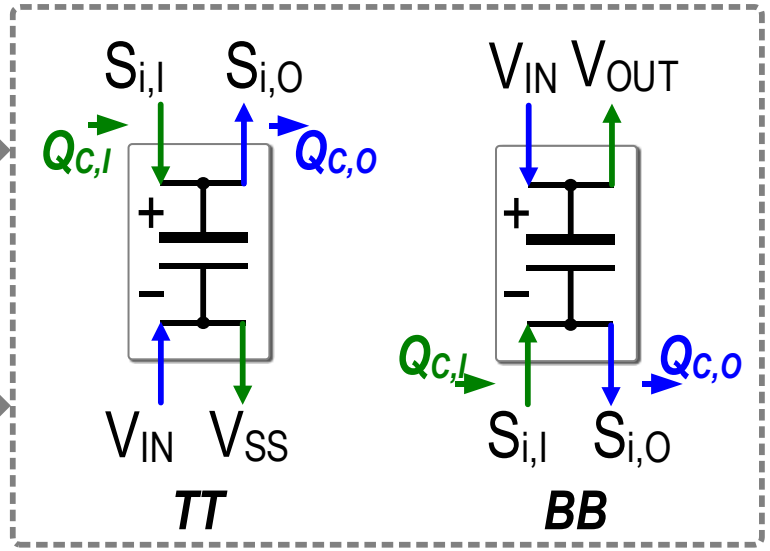
Cell Extraction from Existing Dickson Topologies

Existing Dickson Topologies *(Boost)*



Basic Cell Extraction

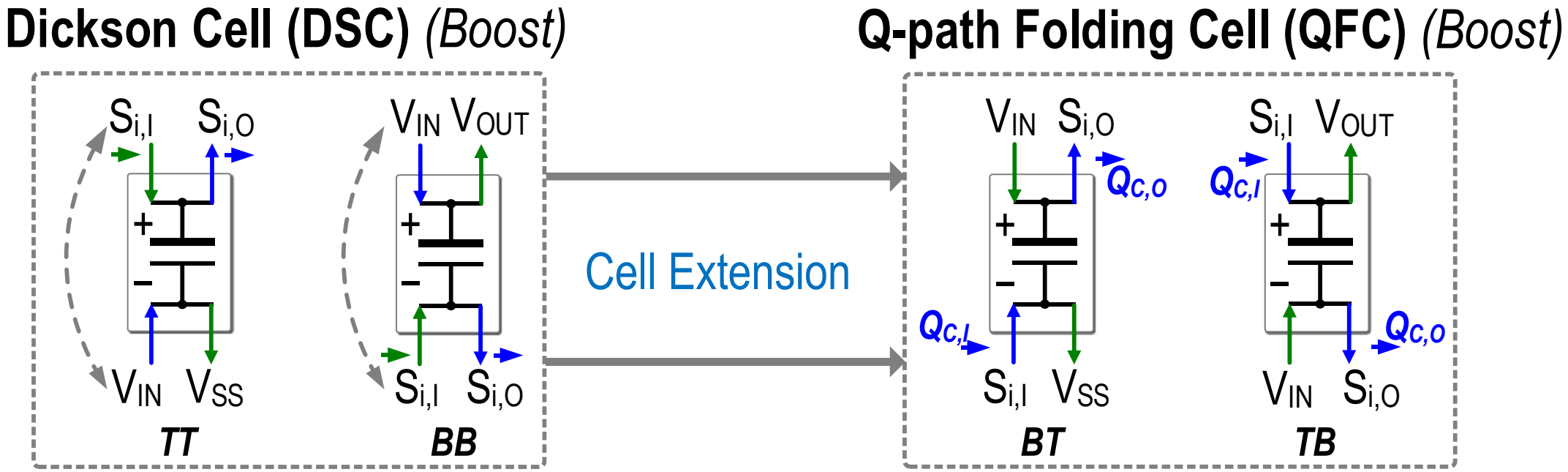
Dickson Cell (DSC) *(Boost)*



- **Optimal** bottom plate switching (ΔV_{CB})
- **Limited** VCR of 1:N, (N-1):N

- **ΔV_{CB}:** V_{IN} or $V_{OUT} - V_{IN}$
- **Inter-Cell Q-Transfer Path:**
  Top Plate in **T**op Plate out (**TT**)
  Bott. Plate in **B**ott. Plate out (**BB**)

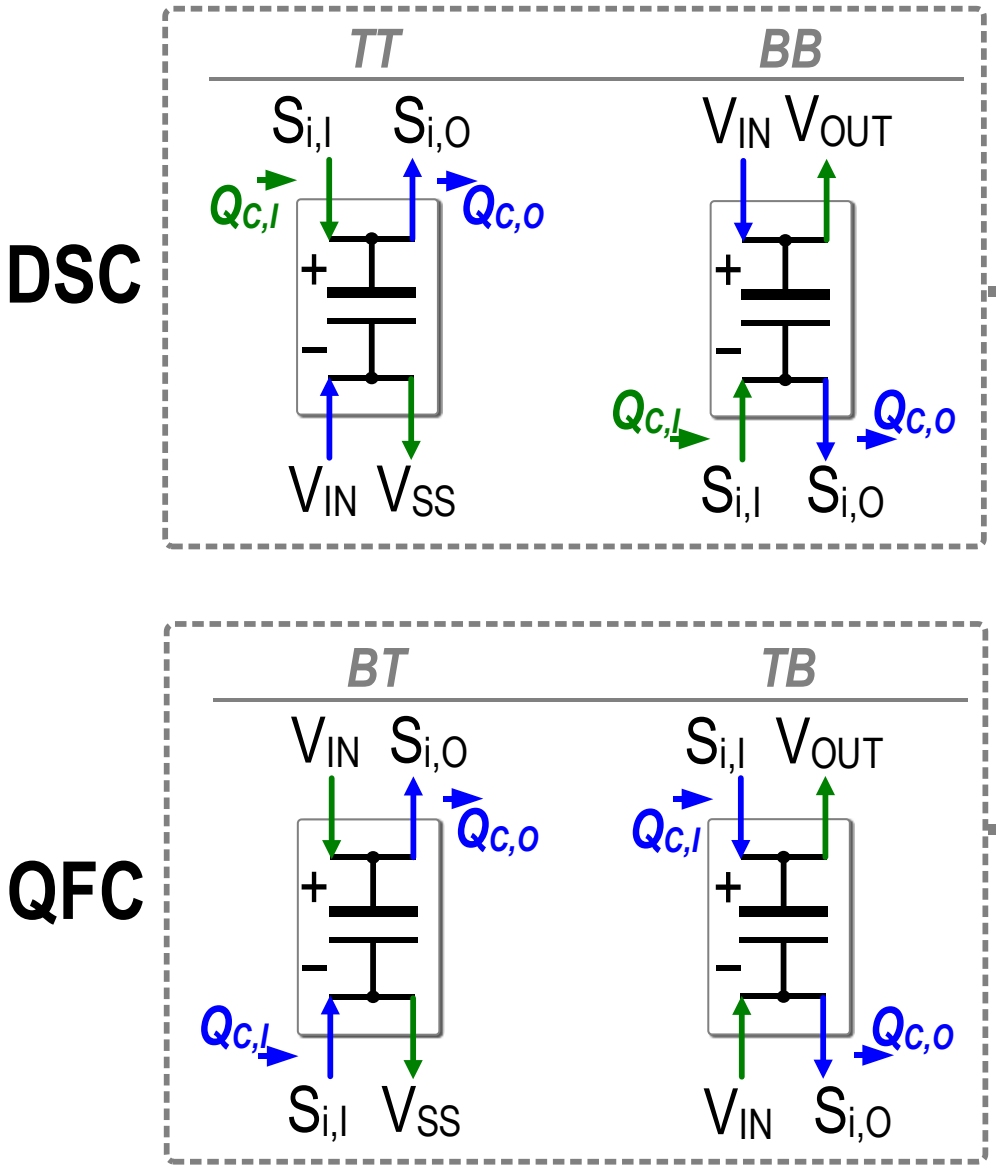
Generating of Charge-path Folding Cell (QFC)



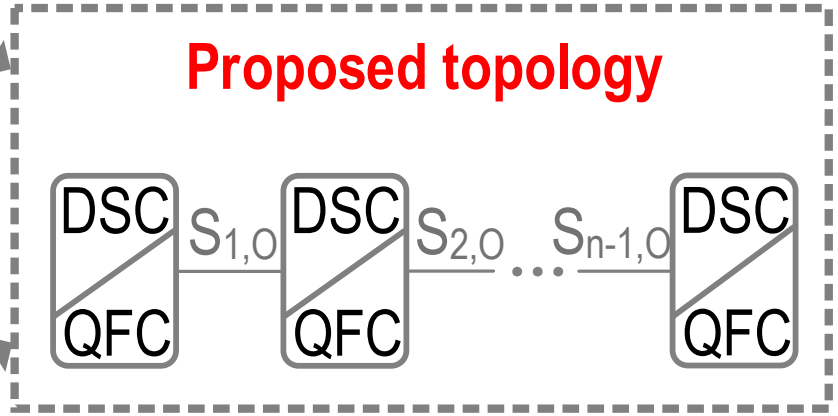
- **Lacks VCR flexibility**

- **ΔV_{CB}:** Internal-node dependent
- **Inter-Cell Q-Transfer Path: "***Folded***"**
  Bottom Plate in **T**op Plate out (**BT**)
  Top Plate in **B**ottom Plate out (**TB**)

Cell-Based Topology Design Concept *(Boost)*



Algorithmic Topology Generation



- Rational FVCR implementation
- Optimal R_{SSL}
- Cell by cell ΔV_{CB} optimization

Cell Parameterization (*Boost*): b_i & m_i

V_{OUT} feed-in coefficient: b_i

$$S_{i,O} = S_{i,I} + V_{IN} - b_i V_{OUT}$$

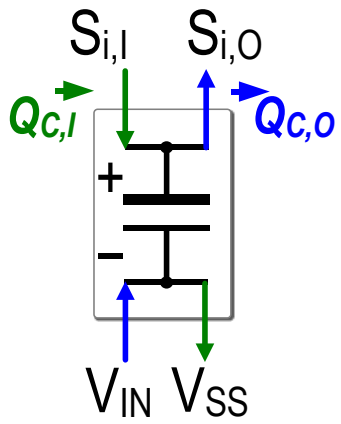
$b_i = 0$: $S_{i,O} = S_{i,I} + V_{IN}$

$b_i = 1$: $S_{i,O} = S_{i,I} + V_{IN} - V_{OUT}$

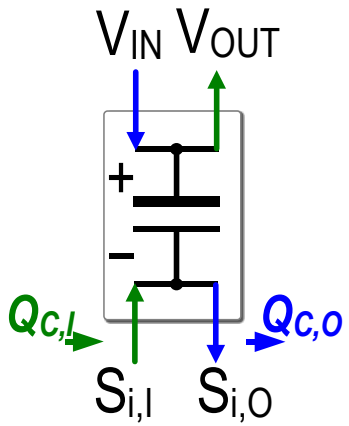
Unique cell configuration by **b_i** & **m_i**

$b_i = 0$ | **$b_i = 1$**

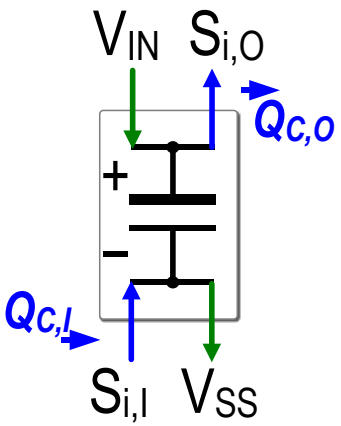
TT



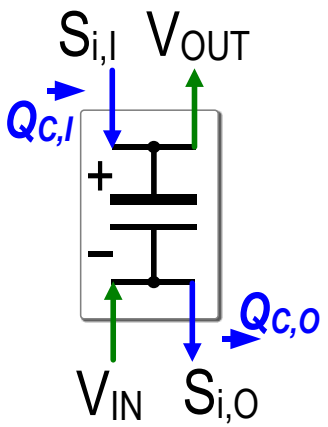
BB



BT



TB



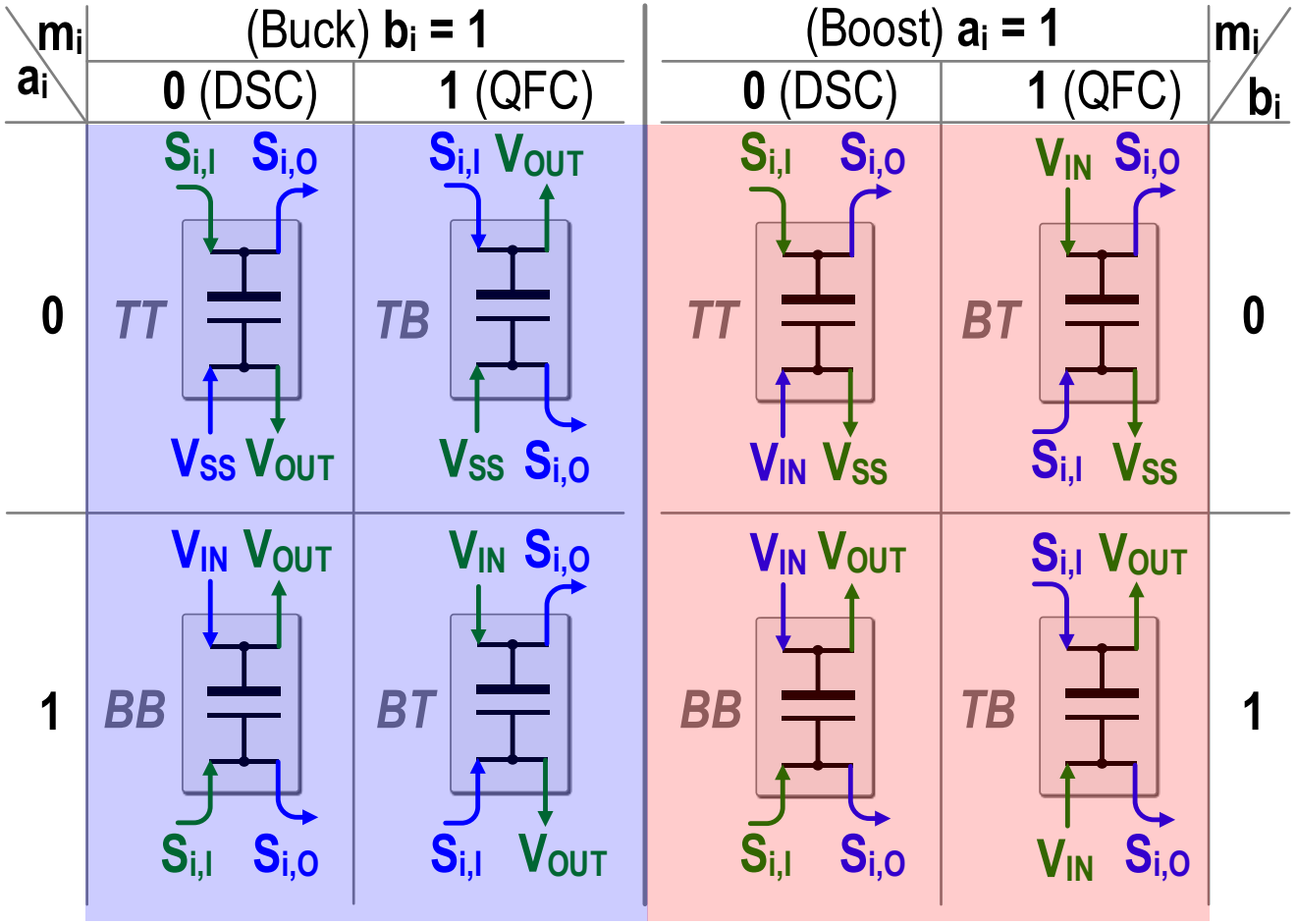
Q-folding (QF) coefficient: m_i

DSC: $m_i = 0$

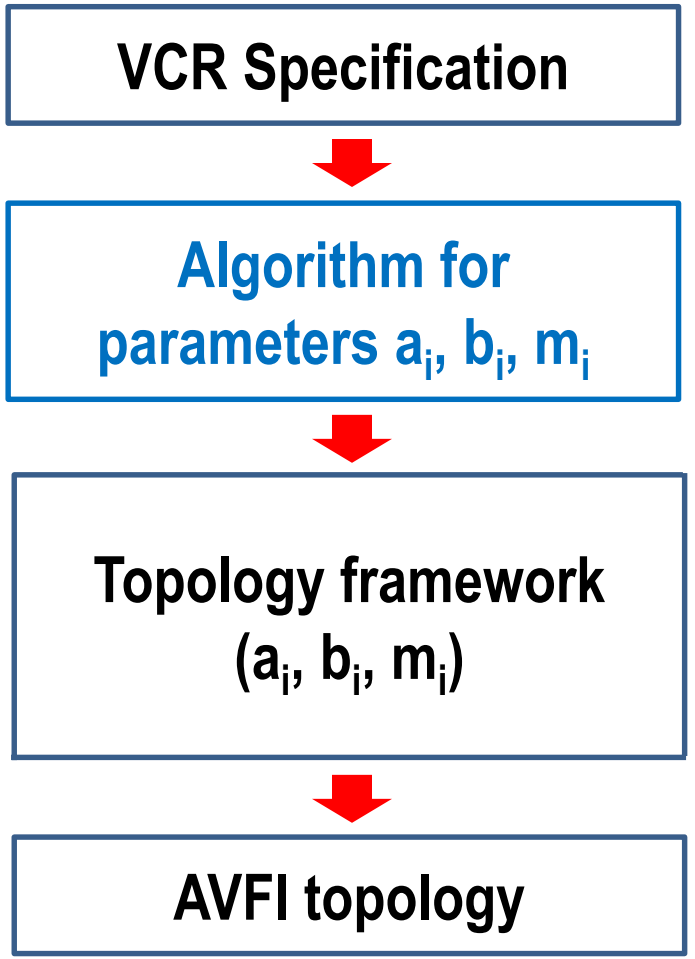
QFC: $m_i = 1$

Cell Parameter Summary (*Buck*/*Boost*): a_i, b_i, m_i

Basic Power Cells:

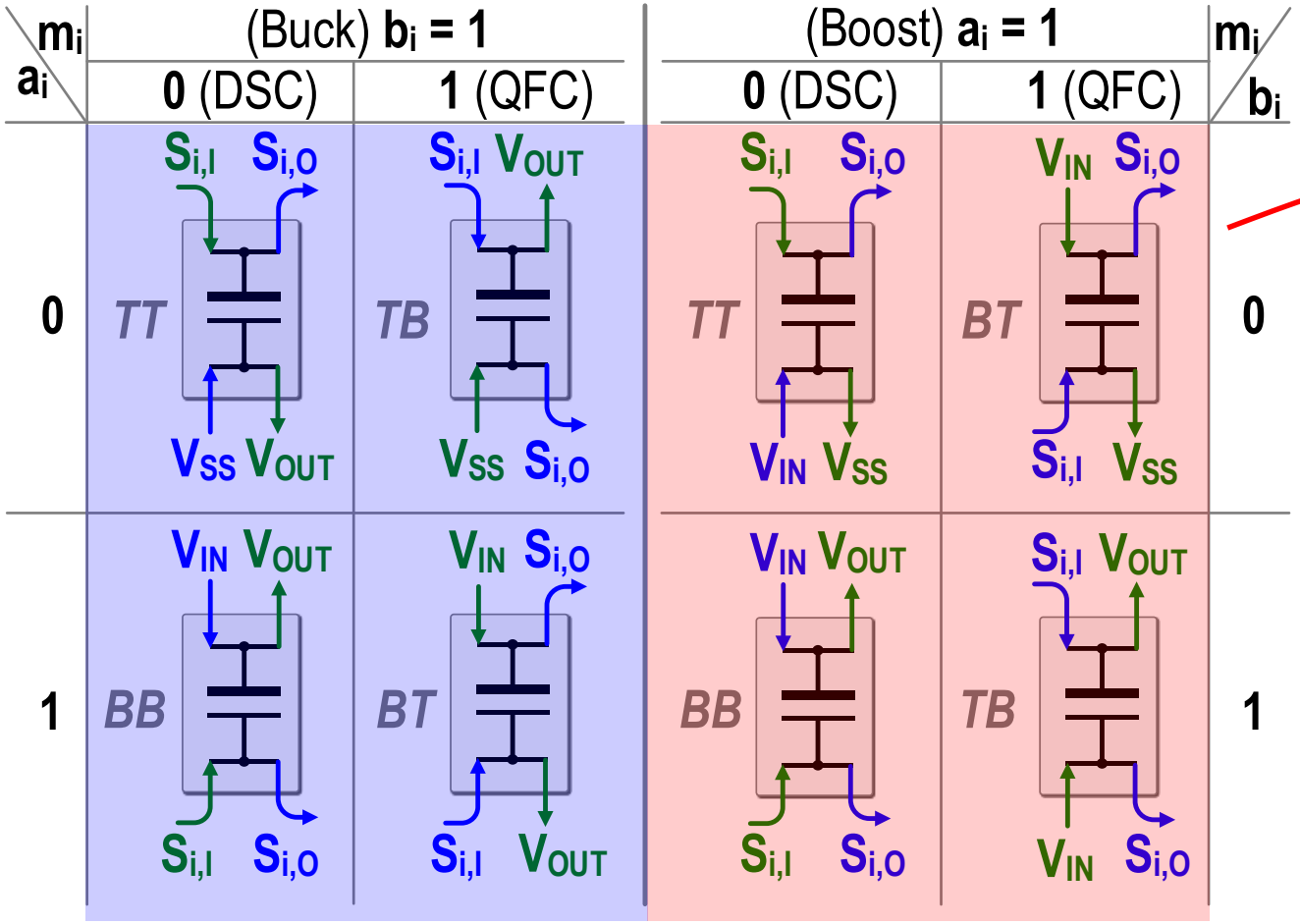


Topology generation steps:

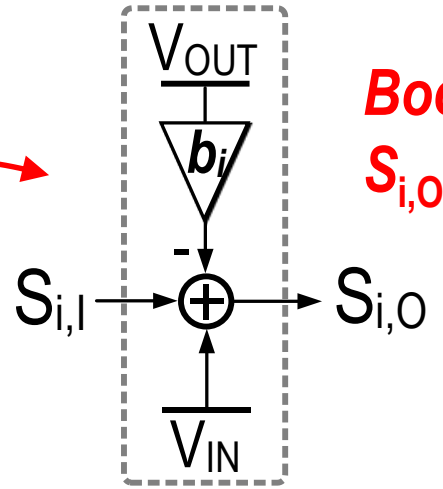


Cell Parameter Summary (Buck/Boost): a_i, b_i, m_i

Basic Power Cells:

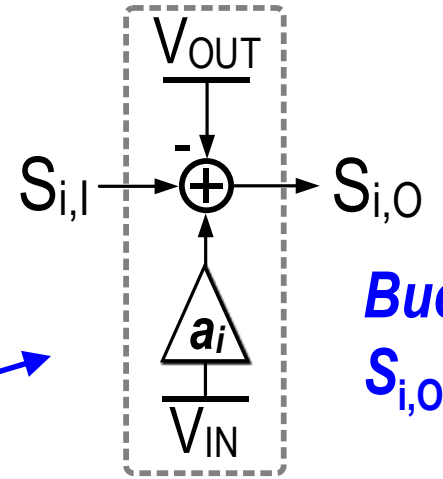


Algorithmic Power Cell Model:



Boost (V_{OUT} Feed-In):

$$S_{i,O} = S_{i,I} + V_{IN} - b_i V_{OUT}$$

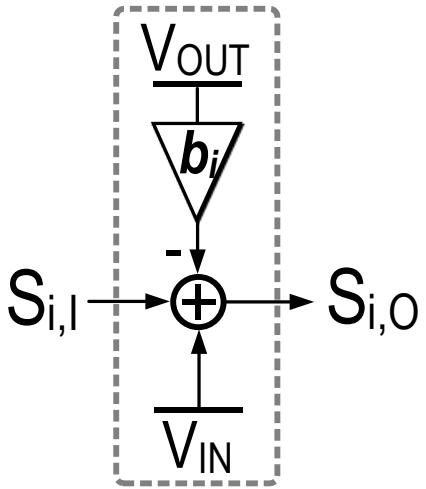


Buck (V_{IN} Feed-In):

$$S_{i,O} = S_{i,I} + a_i V_{IN} - V_{OUT}$$

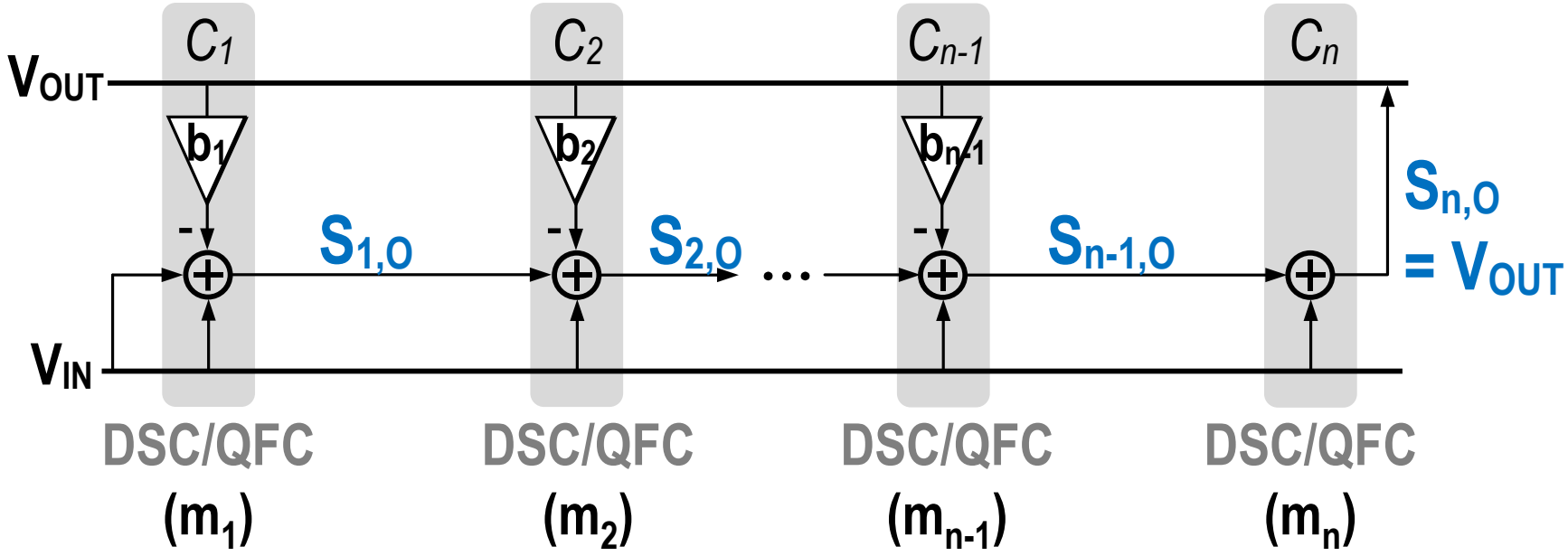
$AV_{OUT}FI$ Topology Framework *(Boost)*

$S_{i,O} = S_{i,I} + V_{IN} - b_i V_{OUT}$



Algorithmic Power Cell Model

Algorithmic V_{OUT} feed-in ($AV_{OUT}FI$) Topology Framework



$$S_{i,O} = (1+i)V_{IN} - (\sum_{j=1}^{i} b_j)V_{OUT}$$

$$VCR = \frac{Y}{X} = \frac{V_{OUT}}{V_{IN}} = \frac{1+n}{1+\sum_{i=1}^{n-1} b_i}$$

$AV_{OUT}FI$ Topology Framework *(Boost)*

Boost X : Y

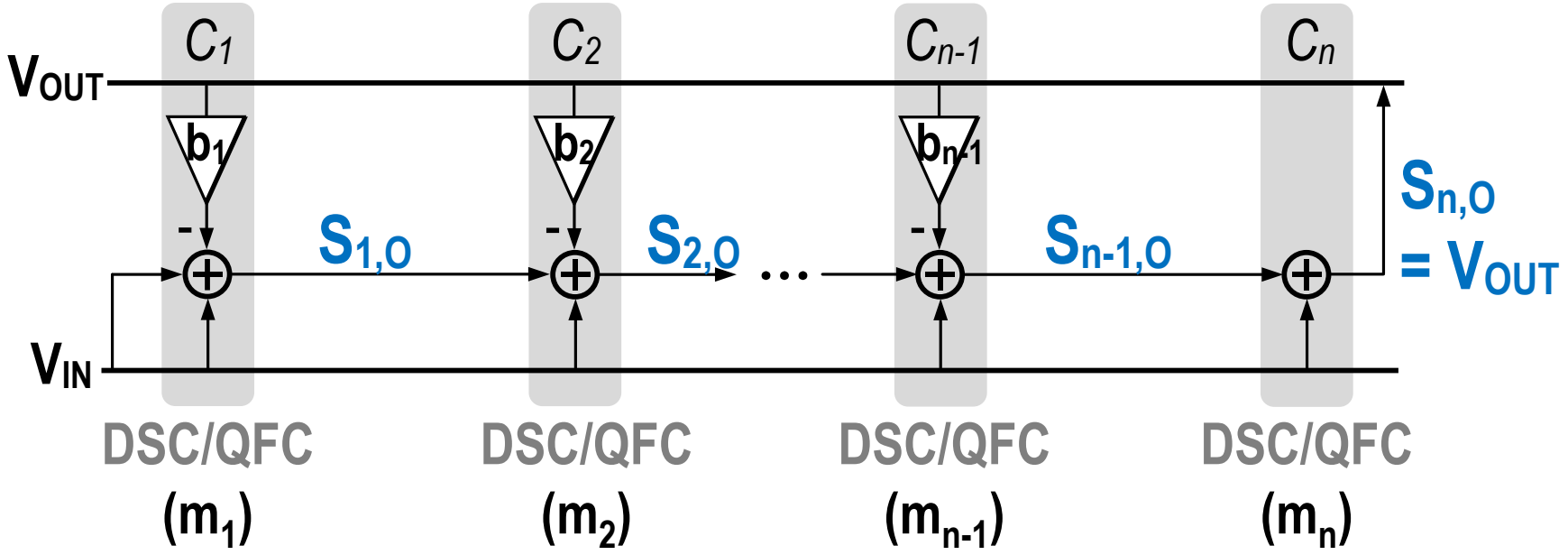
$$*R_{SSL,min} = \frac{Y-1}{X}$$

$$R_{SSL,AVFI} = \sum\left(\frac{Q_{Ci}}{Q_{OUT}}\right) = \frac{n}{1+\sum_{i=1}^{n-1} b_i} = \frac{Y-1}{X} = R_{SSL,min}$$

** Area-Constrained*

[M. D. Seeman, TPEL'08]

Algorithmic V_{OUT} feed-in ($AV_{OUT}FI$) Topology Framework



$$S_{i,O} = (1+i)V_{IN} - \left(\sum_{j=1}^{i} b_j\right)V_{OUT}$$

$$VCR = \frac{Y}{X} = \frac{V_{OUT}}{V_{IN}} = \frac{1+n}{1+\sum_{i=1}^{n-1} b_i}$$

$AV_{OUT}FI$ Topology Framework *(Boost)*

Design Concept

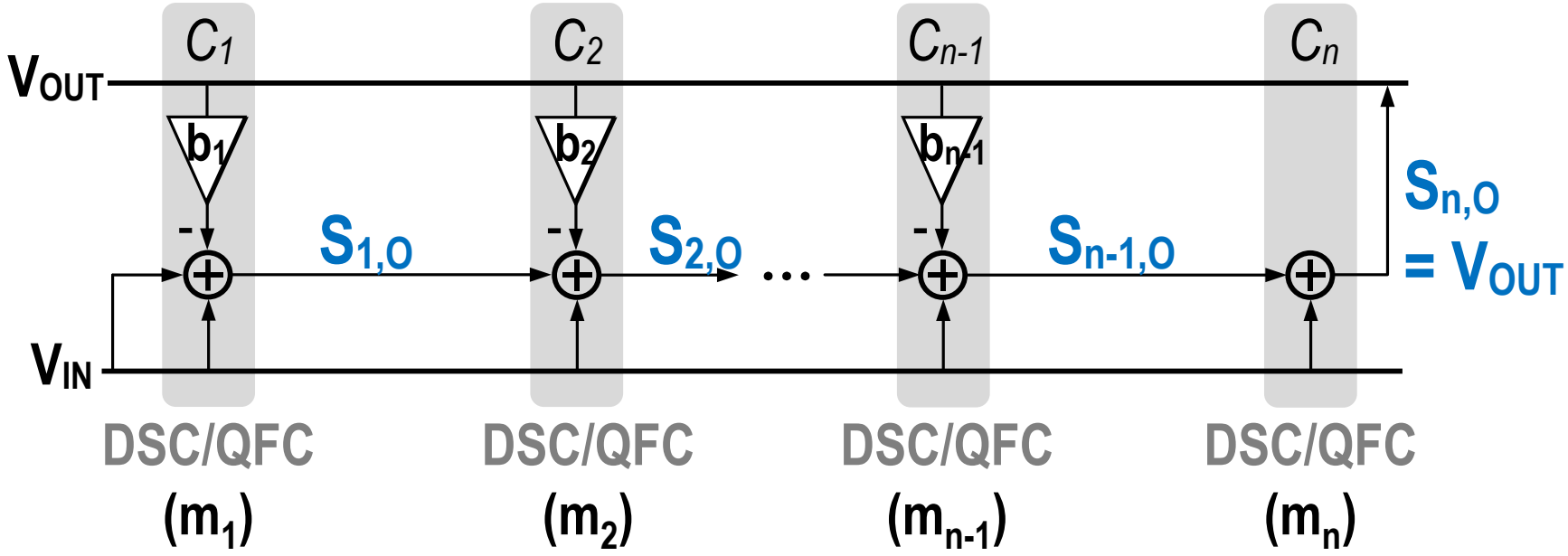
With a VCR Target

DSC: TT, BB

QFC: BT, TB

Algorithm to determine b_i & m_i

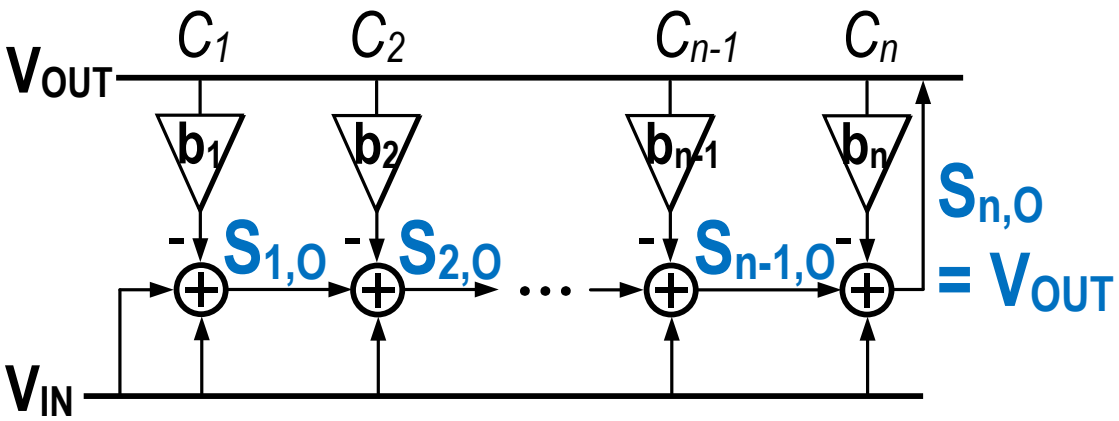
Algorithmic V_{OUT} feed-in ($AV_{OUT}FI$) Topology Framework



Generating a topology with reduced parasitic loss.

Algorithm for b_i Determination *(Boost)*

Level Bounded Rule (LBR) *(boost)*: $S_{1\sim(n-1),O} \in (V_{SS}, V_{OUT})$.



$$S_{i,O} = (1+i)V_{IN} - (\Sigma b_{1\sim i})V_{OUT}$$

Applying the ***LBR****:*

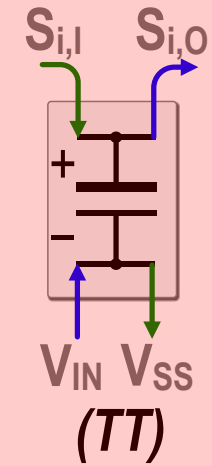
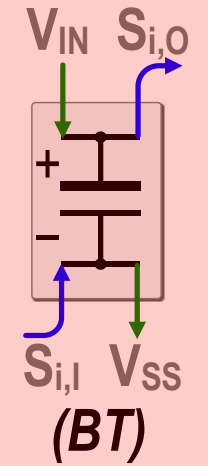
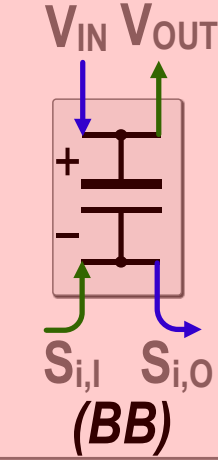
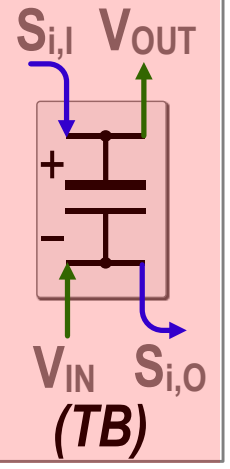
$$0 < S_{i,O} < V_{OUT}$$

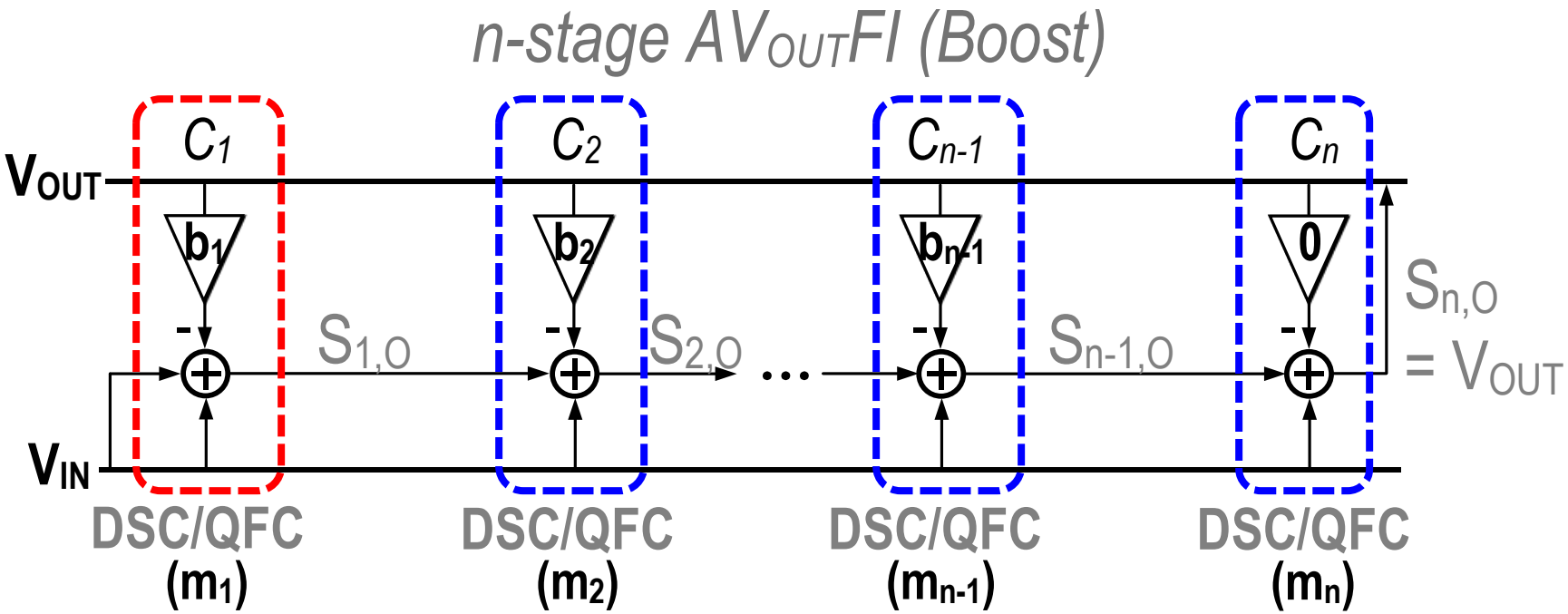
b_i algorithm

$$b_i = \begin{cases} 1, & (1+b_1+\ldots+b_{i-1})VCR < i+1 \\ 0, & (1+b_1+\ldots+b_{i-1})VCR > i+1 \end{cases}$$

$$b_n = 0$$

Determination of m_i (Boost)

m_i / b_i	0 (DSC)	1 (QFC)
0	 (TT)	 (BT)
1	 (BB)	 (TB)



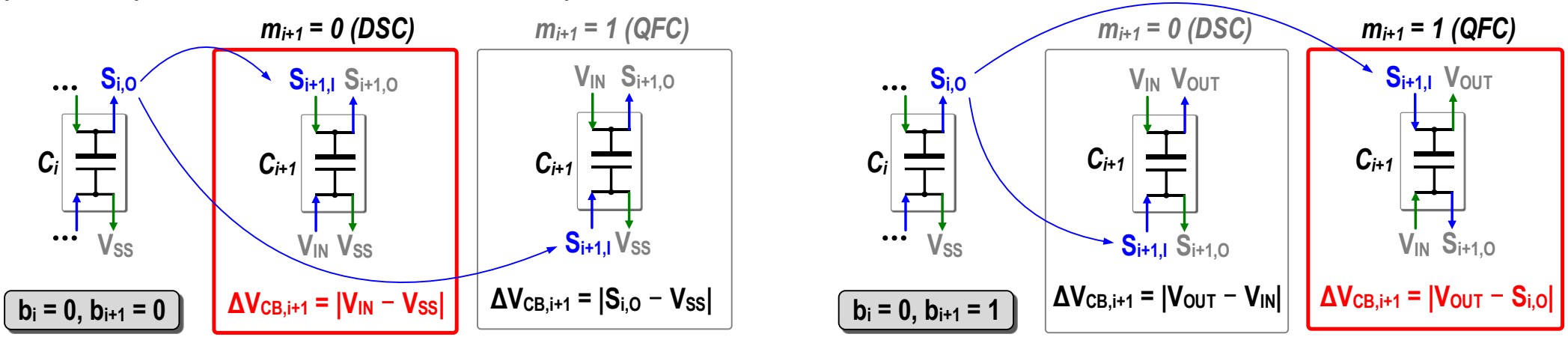
C_1 implementation solely depends on b_1.
(identical for m_1 = 0 or 1)

$C_{2\sim n}$ implementation depends on both $b_{2\sim n-1}$ & $m_{2\sim n}$.

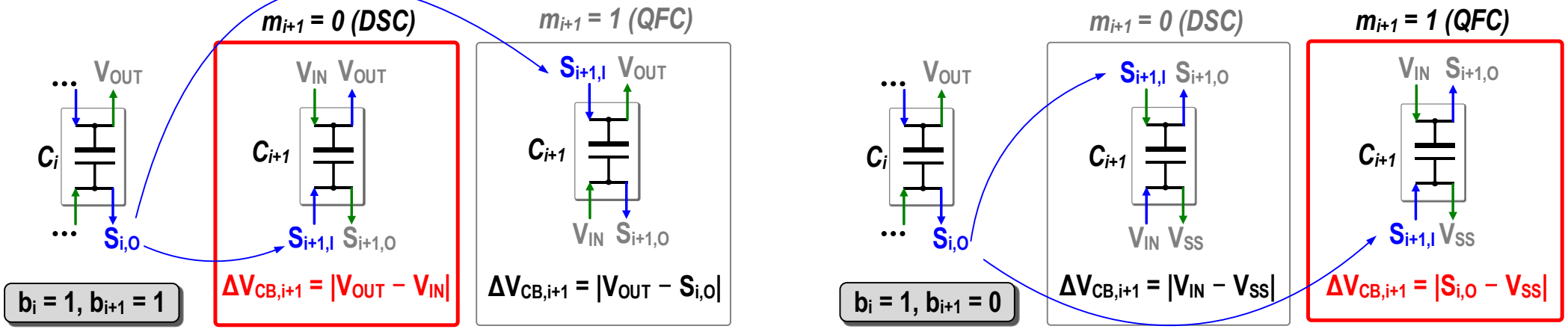
→ Explore m_i algorithm with stage-by-stage ΔV_{CB} optimization.

Determination of m_i (Boost)

- $S_{i,O} = S_{i,I} + V_{IN} - b_i V_{OUT} \rightarrow S_{i,O} > V_{IN}$ when $b_i = 0$



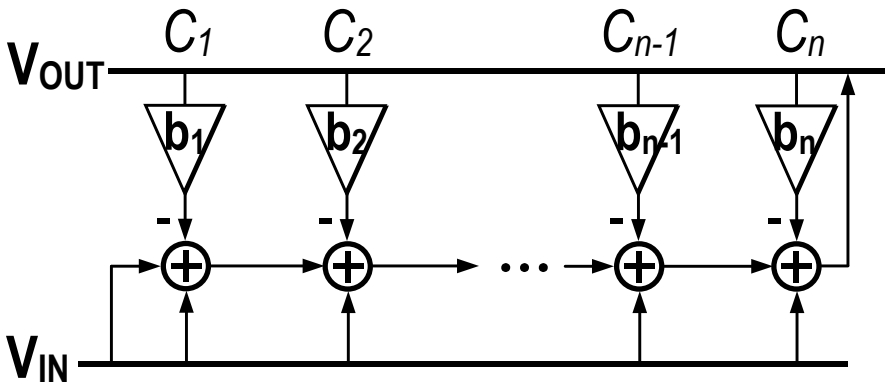
- $S_{i,O} = S_{i,I} + V_{IN} - b_i V_{OUT} \rightarrow S_{i,O} < V_{IN}$ when $b_i = 1$



Lower $\Delta V_{CB} \rightarrow m_i = b_{i-1} \oplus b_i \rightarrow C_{TOP} - C_{TOP}$ or $C_{BOT} - C_{BOT}$ Inter-cell Q-Transfer

Proposed $AV_{OUT}FI$ Topology Summary (Boost)

Topology Model



$$\frac{V_{OUT}}{V_{IN}} = \frac{1+n}{1+\Sigma b_{1\sim(n-1)}}$$

Coefficients Algorithm

$V_{OUT}FI$ Coefficient

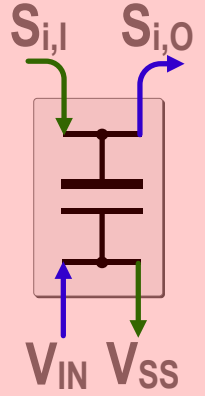
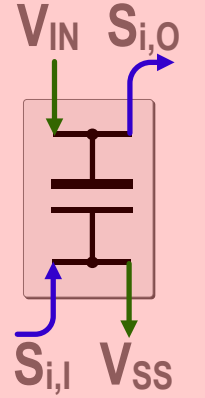
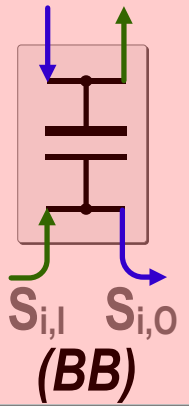
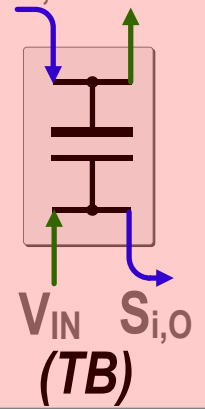
$$b_i = \begin{cases} 1, & (1+b_1+\ldots+b_{i-1})VCR < i+1 \\ 0, & (1+b_1+\ldots+b_{i-1})VCR > i+1 \end{cases}$$

$$b_n = 0$$

QF Coefficient

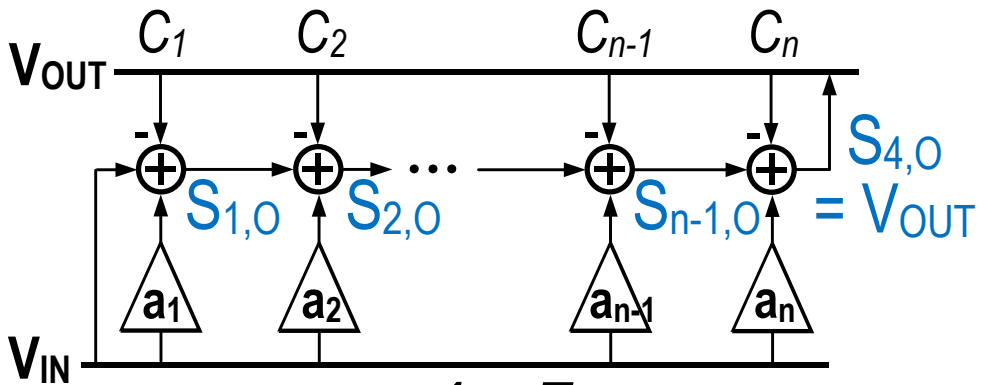
$$m_i = b_{i-1} \oplus b_i, \quad m_1 = \textit{either 1 or 0}$$

Power Cell Table

m_i / b_i	0 (DC)	1 (QFC)
0	 (TT)	 (BT)
1	 (BB)	 (TB)

Proposed $AV_{IN}FI$ Topology Summary *(buck)*

Topology Model



$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + \Sigma a_{1\sim n}}{1 + n}$$

Coefficients Algorithm

LBR (buck):

$S_{1\sim(n-1),O} \in (V_{SS}, V_{IN})$

$$S_{i,O} = (1+\Sigma a_{1\sim i})V_{IN} - iV_{OUT}$$

$$0 < S_{i,O} < V_{IN}$$

$V_{IN}FI$ Coefficient

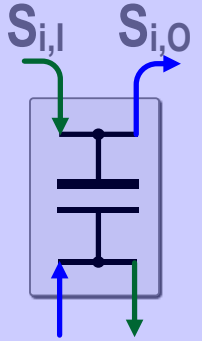
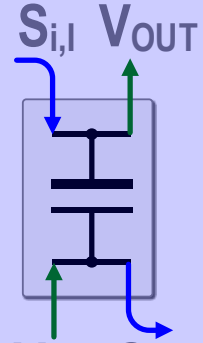
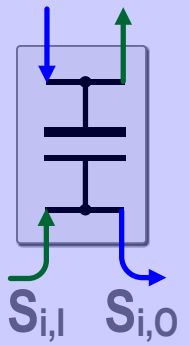
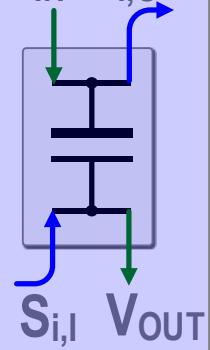
$$a_i = \begin{cases} 1, & iVCR > 1+a_1+a_2+\ldots a_{i-1} \\ 0, & iVCR < 1+a_1+a_2+\ldots a_{i-1} \end{cases}$$

$$a_1 = 0$$

QF Coefficient

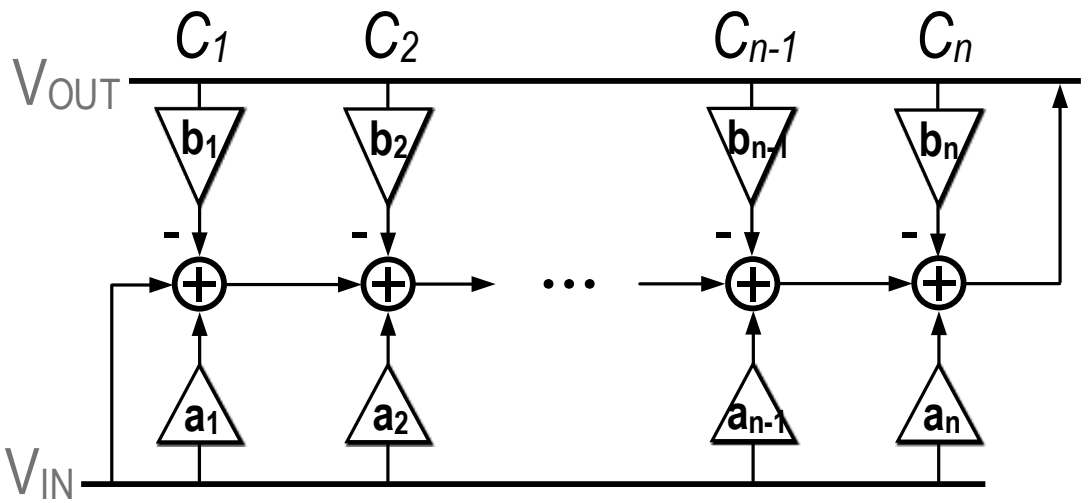
$$m_i = a_i \oplus a_{i+1}, \quad m_n = \textit{either 1 or 0}$$

Power Cell Table

m_i / a_i	0 *(DSC)*	1 *(QFC)*
0	 *(TT)*	 *(TB)*
1	 *(BB)*	 *(BT)*

Proposed AVFI Topology Summary (*Buck*/*Boost*)

n-stage AVFI buck-boost topology



$$VCR = \frac{1 + \Sigma a_{1\sim n}}{1 + \Sigma b_{1\sim n}}$$

a_i, b_i, m_i for arbitrary VCR can be algorithmically determined

Buck:

$a_1 = 0$, $b_{1\sim n} = 1$

$$a_i = \begin{cases} 1, & iVCR > 1+a_1+a_2+\ldots a_{i-1} \\ 0, & iVCR < 1+a_1+a_2+\ldots a_{i-1} \end{cases}$$

$m_i = a_i \oplus a_{i+1}$, $m_n = X$ (1 or 0)

Boost:

$a_{1\sim n} = 1$, $b_n = 0$

$$b_i = \begin{cases} 1, & (1+b_1+\ldots +b_{i-1})VCR < i+1 \\ 0, & (1+b_1+\ldots +b_{i-1})VCR > i+1 \end{cases}$$

$m_i = b_{i-1} \oplus b_i$, $m_1 = X$ (1 or 0)

Proposed AVFI Example 7:4 *(Buck)*

1. Aribtrary **VCR** = 7:4

2. Number of cell $\mathbf{N_C}$:

Buck: $N_C = p - 1$

Boost: $N_C = q - 1$

3. Calculate VFI coefficients $\boldsymbol{a_i}$ / $\boldsymbol{b_i}$.

4. Calculate QF coefficient $\boldsymbol{m_i}$.

5. Apply corresponding **power cell configurations** from the table with the calculated a_i / b_i / m_i.

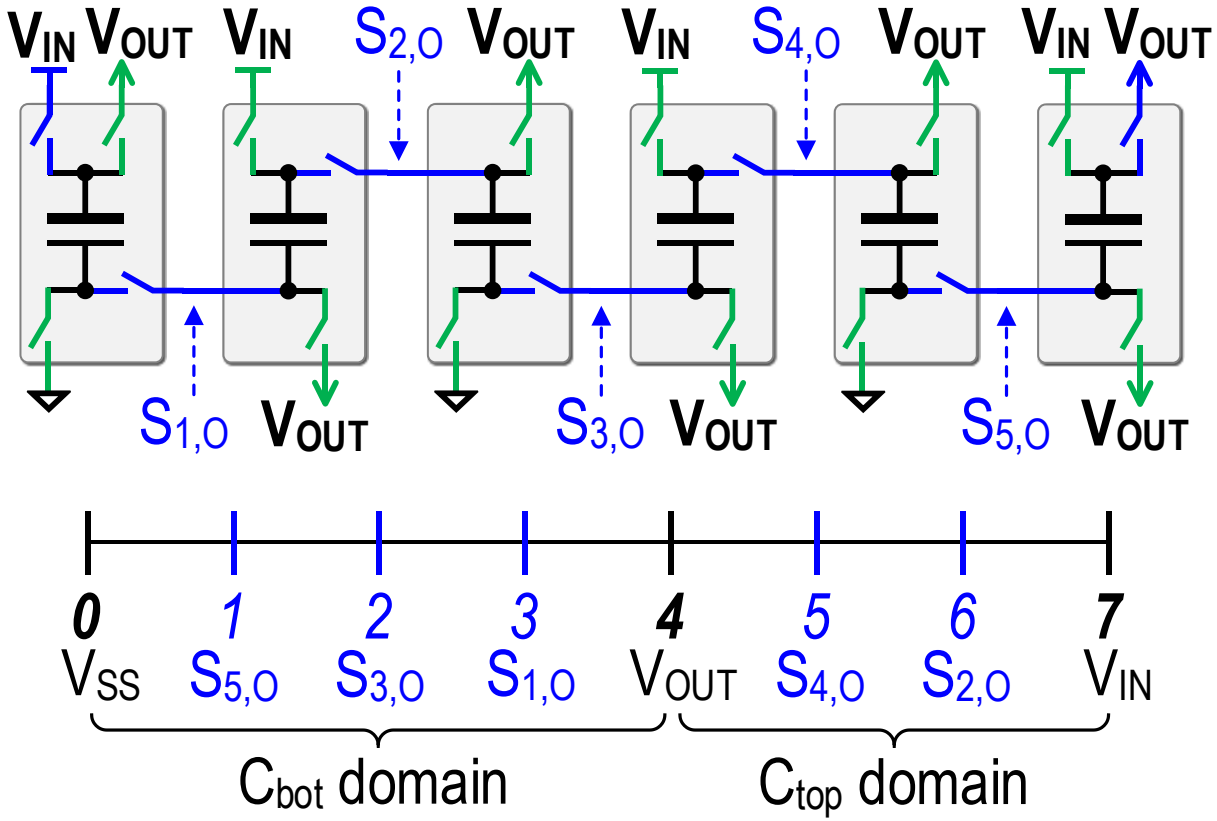
6. Assign proper **switching phase** for all power stages.

1~2). VCR = 7:4 ⟶ number of cell $\mathbf{N_C = 6}$.

3~4). Coefficients: buck ⟶ $\mathbf{b_{1\sim6} = 1}$,

$\mathbf{a_{1\sim6} = \{0\ 1\ 0\ 1\ 0\ 1\} \longrightarrow m_{1\sim6} = \{1\ 1\ 1\ 1\ 1\ X\}}$

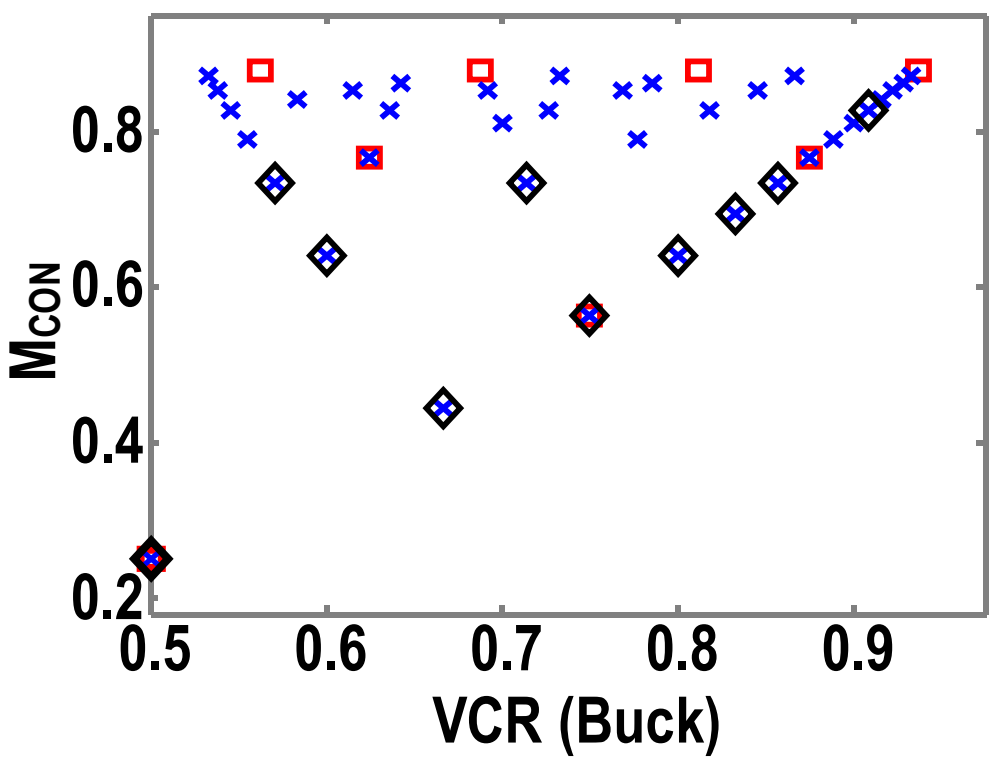
5~6). Topology implementation:

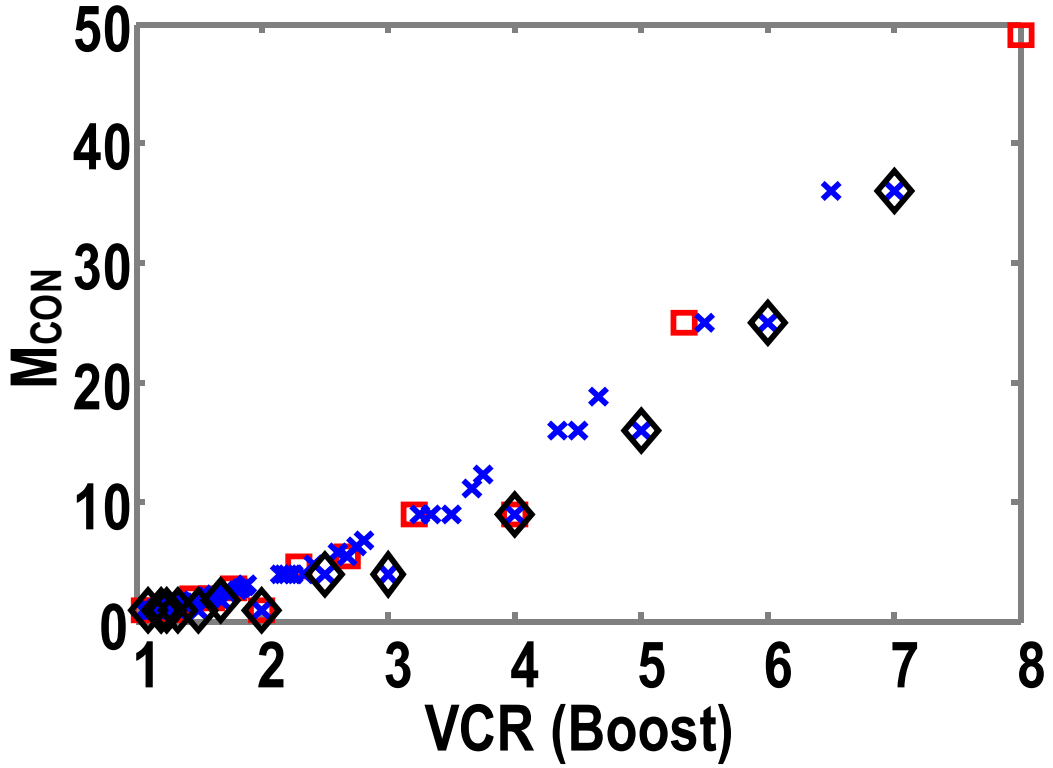


Q-Conduction Loss Comparison

$$M_{CON} = \left(\Sigma \frac{Q_{C,i}}{Q_{OUT}}\right)^2$$

◇ AVFI (24 VCRs) [Jung ISSCC'16] × NSC (3-stage) [Salem ISSCC'14] [Lutz ISSCC'16] □ RSC (4-stage)





Optimal conduction loss factor as in existing topologies.

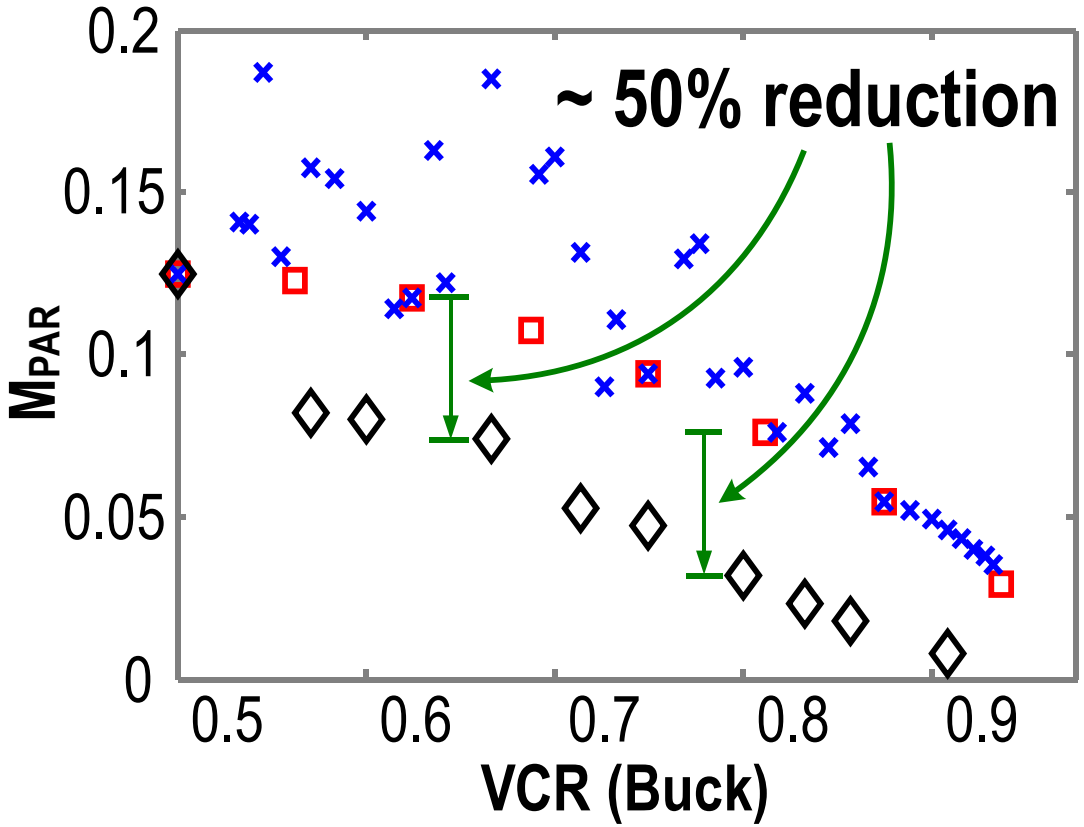
Parasitic Loss Comparison

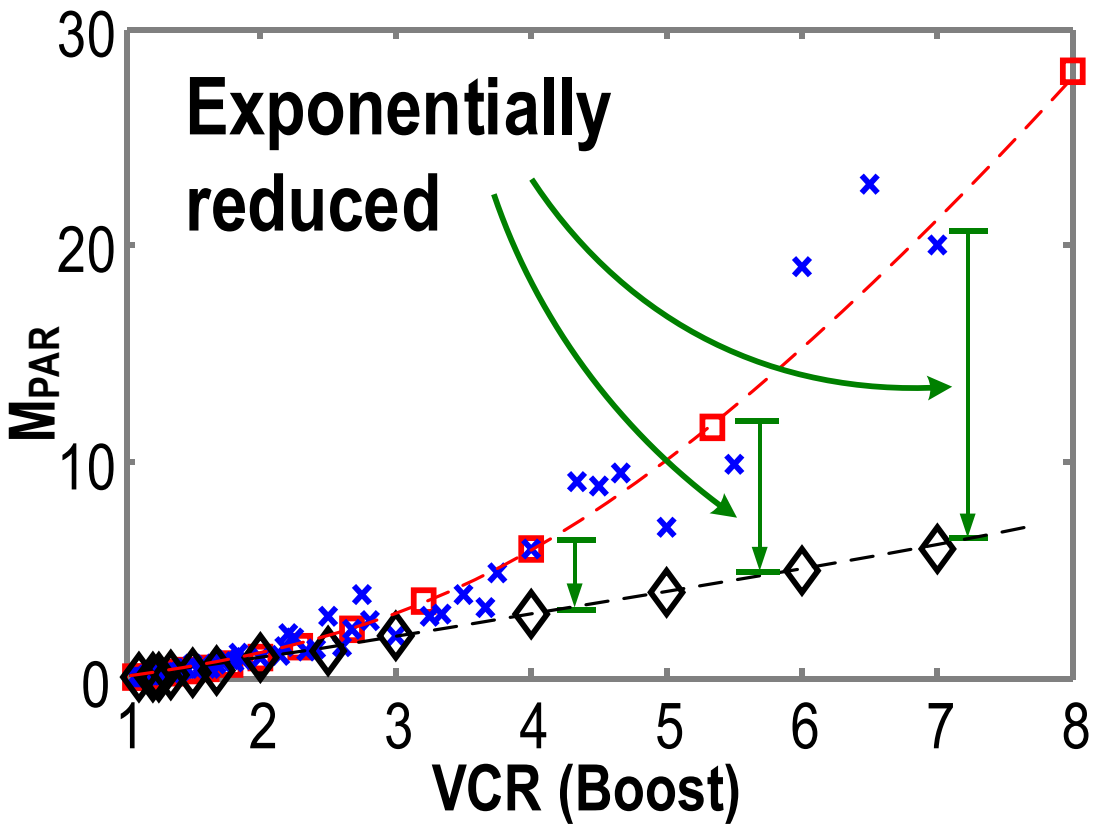
$$M_{PAR} = \frac{1}{M_{CON}} \Sigma\left[\left(\frac{Q_{C,i}}{Q_{OUT}}\right)\left|\frac{\Delta V_{CB}}{V_{IN}}\right|^2\right]$$

◇ AVFI (24 VCRs)

[Jung ISSCC'16] × NSC (3-stage)

[Salem ISSCC'14] [Lutz ISSCC'16] □ RSC (4-stage)

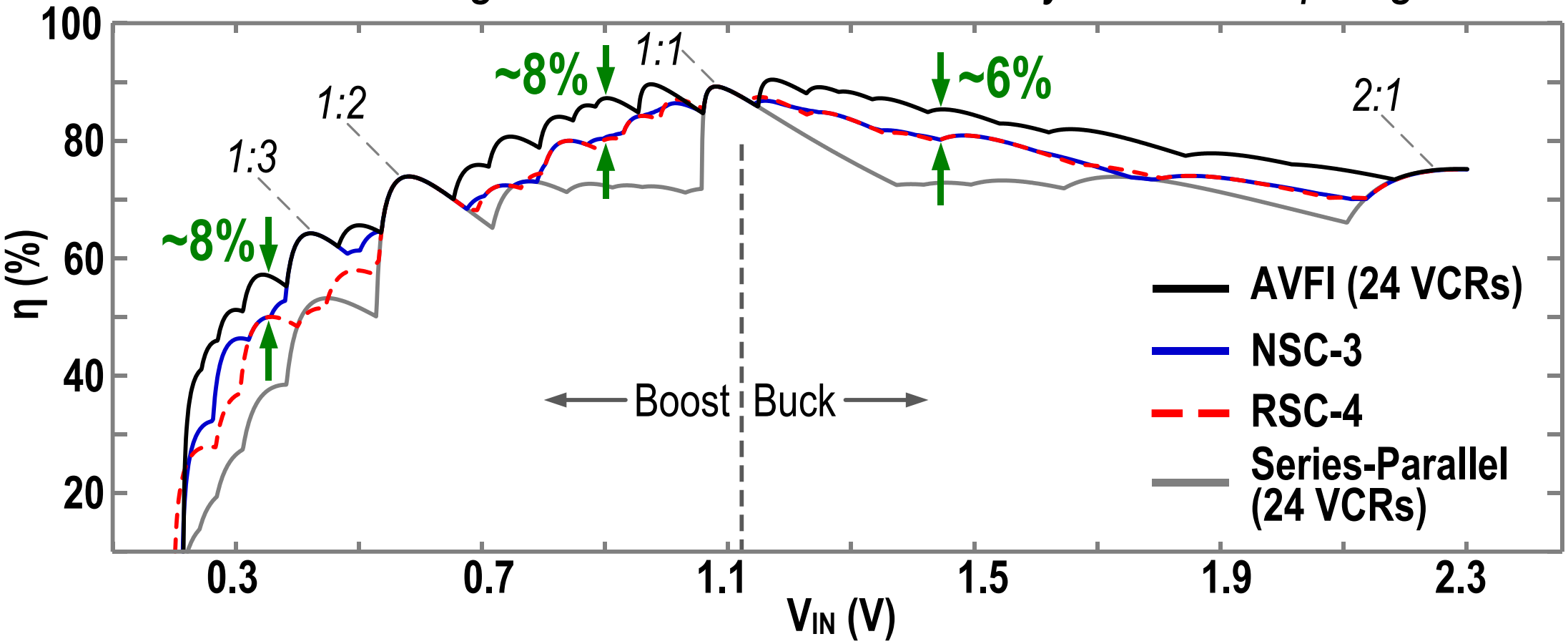




Improved parasitic loss factor than existing topologies.

Simulation Results & Comparison

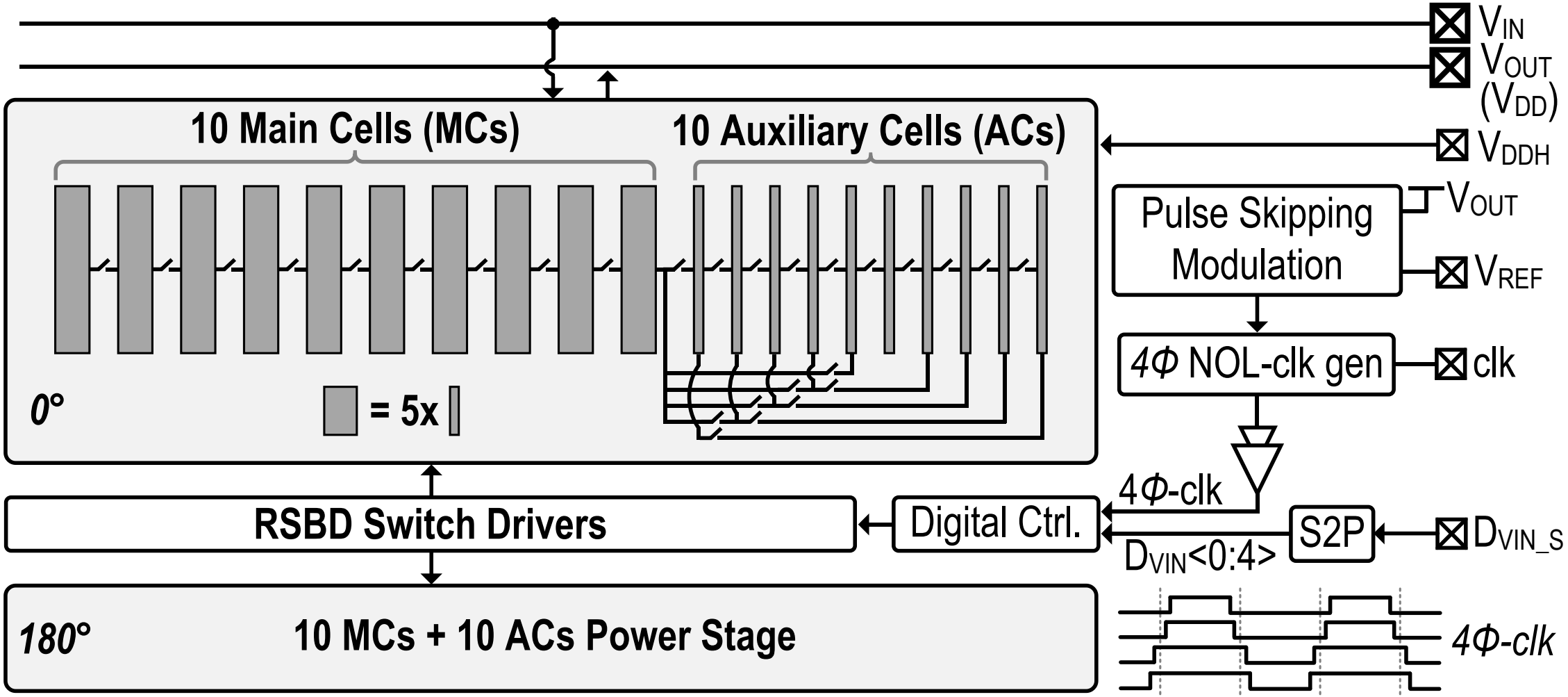
Wide V_{IN} range buck-boost conversion by different topologies



$0.2V < V_{IN} < 2.3V$, $V_{OUT} = 1V$, $I_{load} = 20mA$
$C_{Bot\text{-}par} = 8\%$, $A_{cap} = 1mm^2$

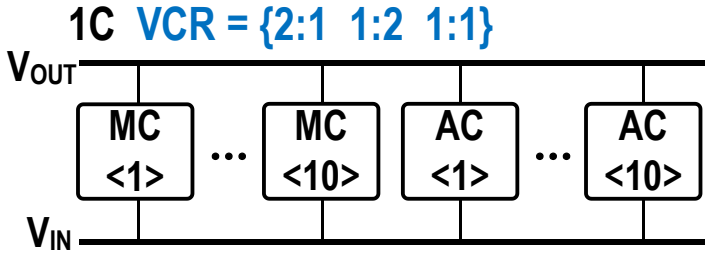
R_{SSL}: AVFI = NSC = RSC < S-P
R_{PAR}: AVFI < NSC ≤ RSC < S-P

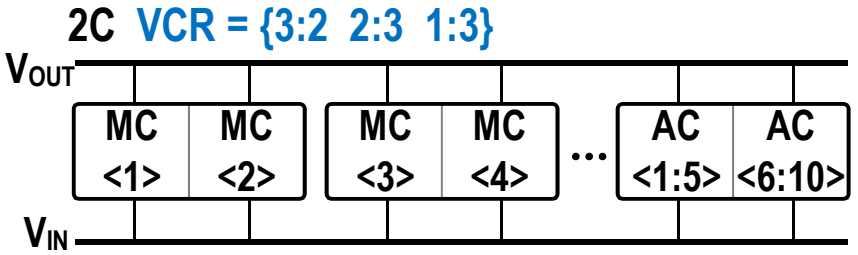
Converter Overview

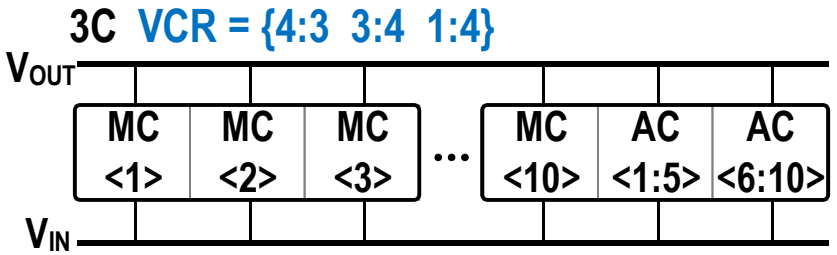


- 10 main + 10 auxiliary cells
- VCRs: 11 buck + 13 boost
- Dual-branch interleaved
- 25MHz clock pulse-skipping modulation

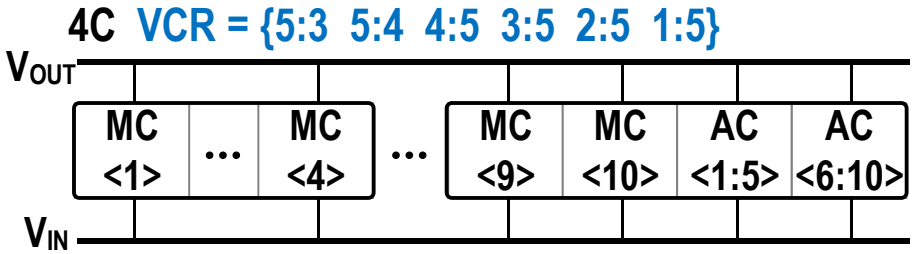
Cells Partitioning Mode Summary

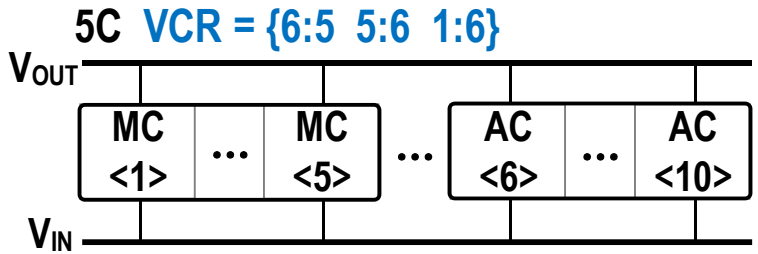


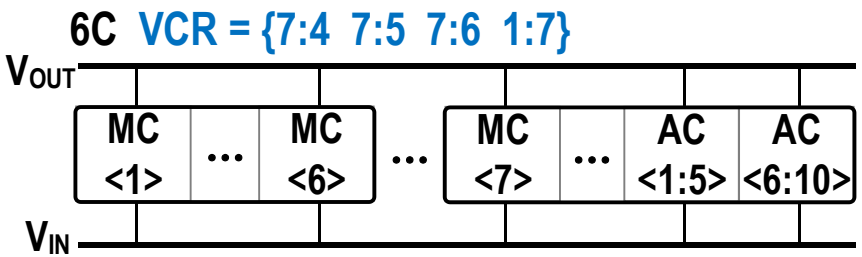


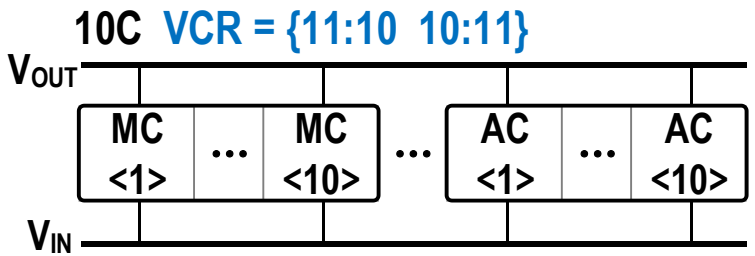


- C_{MC}:C_{AC} = 5:1
- 7 partition modes with cascaded or parallel cells
- Support 24 VCRs
- Full cap. utilization
- # of cell reduction: 60 → 20



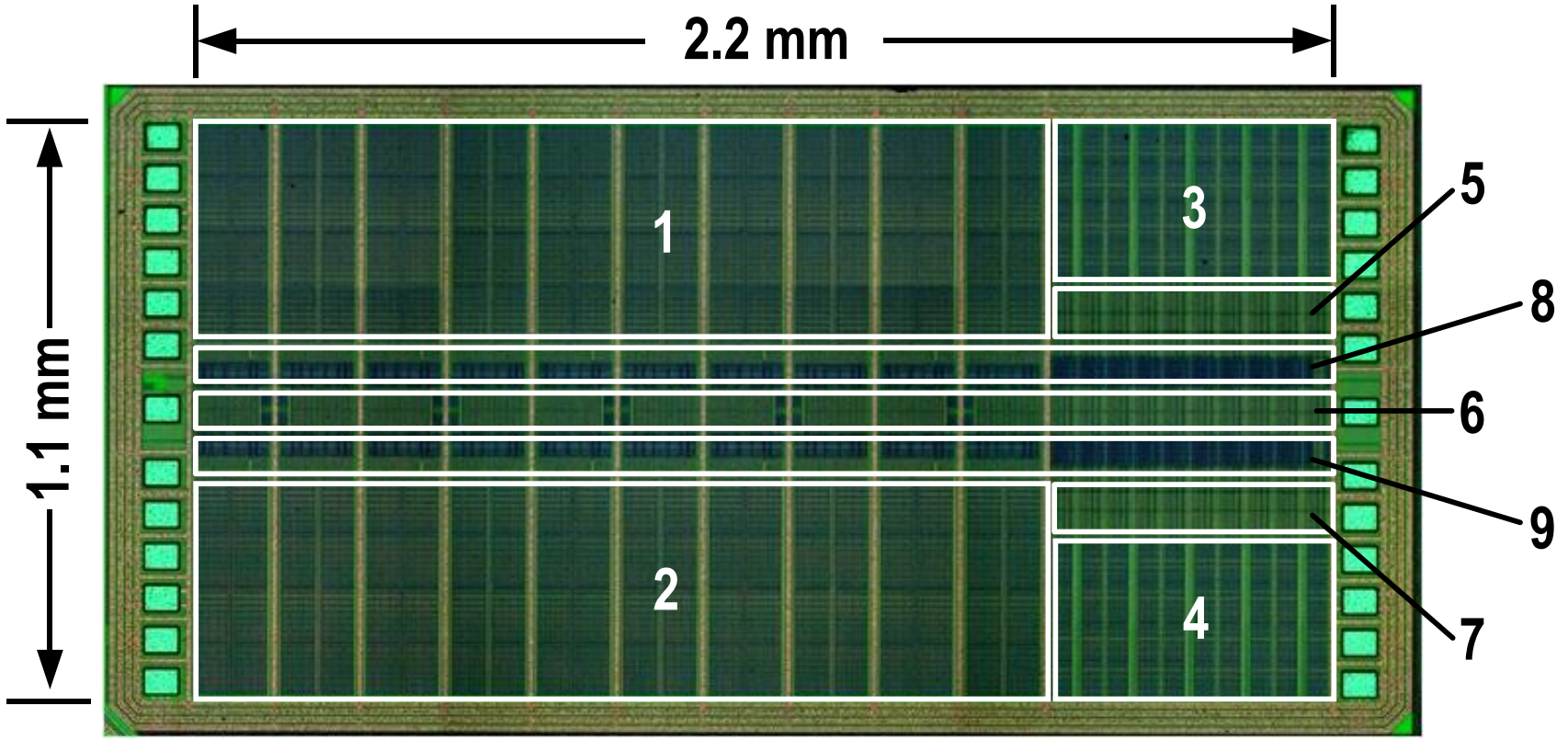






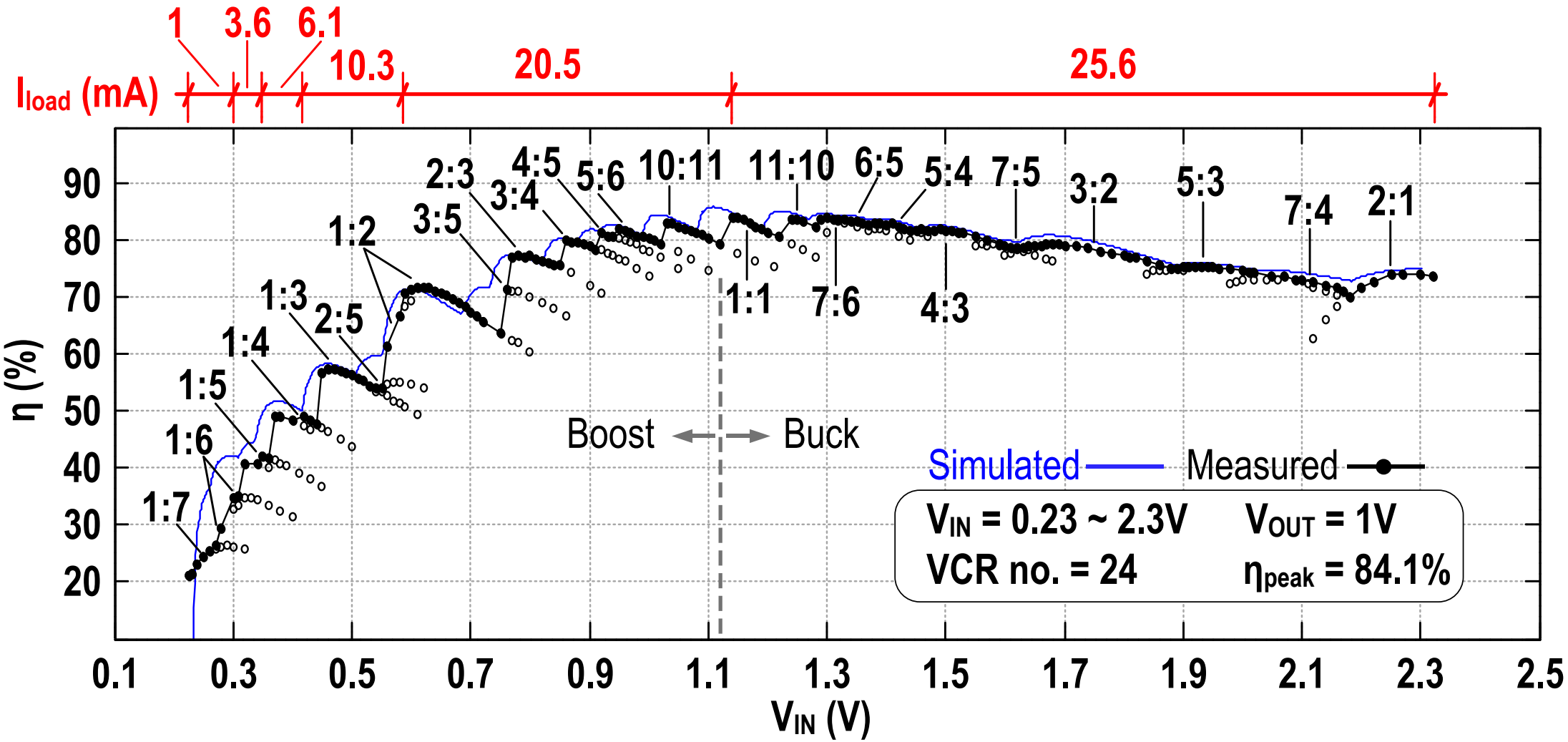
Chip Implementation

65nm bulk CMOS
C_{fly} = 8 nF
C_{OUT} = 6 nF
Area = 2.42mm²

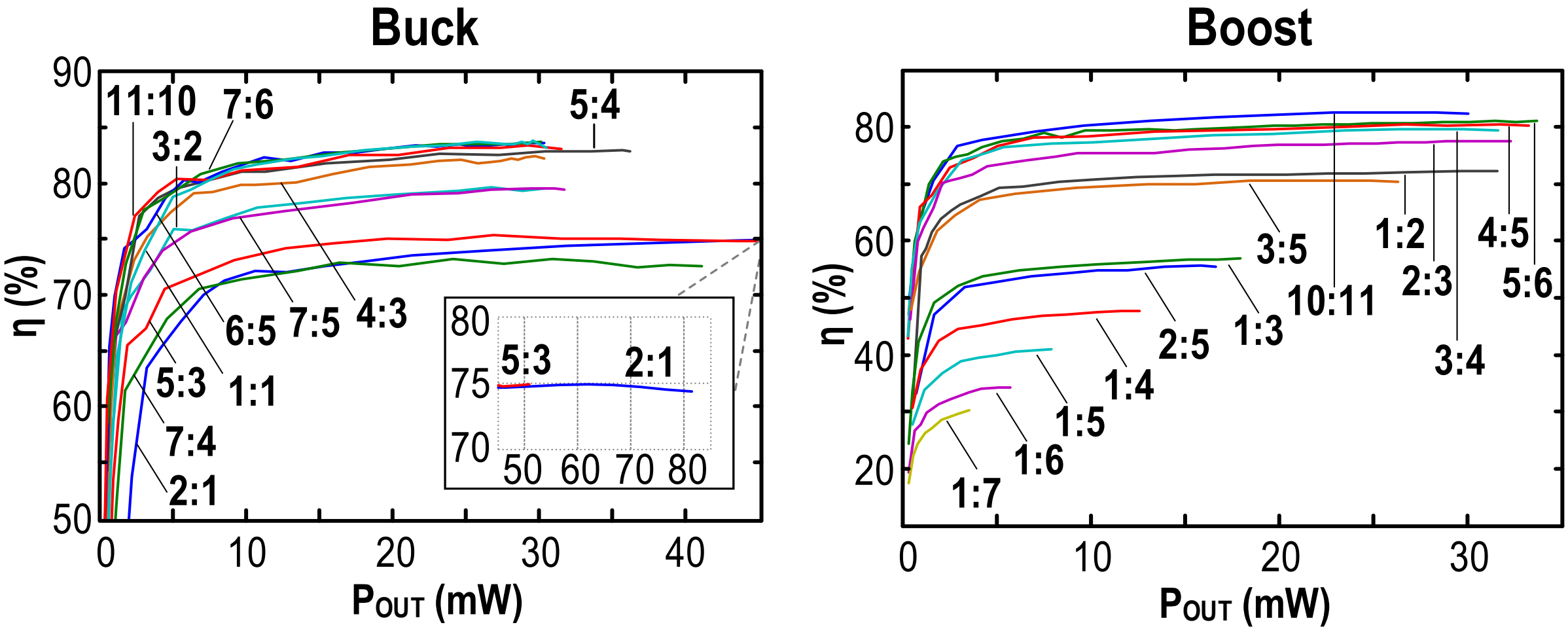


1~2) 10 MC C_{fly} (MIM + MOS) and C_{OUT} (MOS) for 0° and 180° branches
3~4) 10 AC C_{fly} (MIM + MOS) and C_{OUT} (MOS) for 0° and 180° branches
5~7) RSBDs + digital control
8~9) Power switches

Measured Conversion Efficiency over V_{IN} (V_{OUT} = 1V)



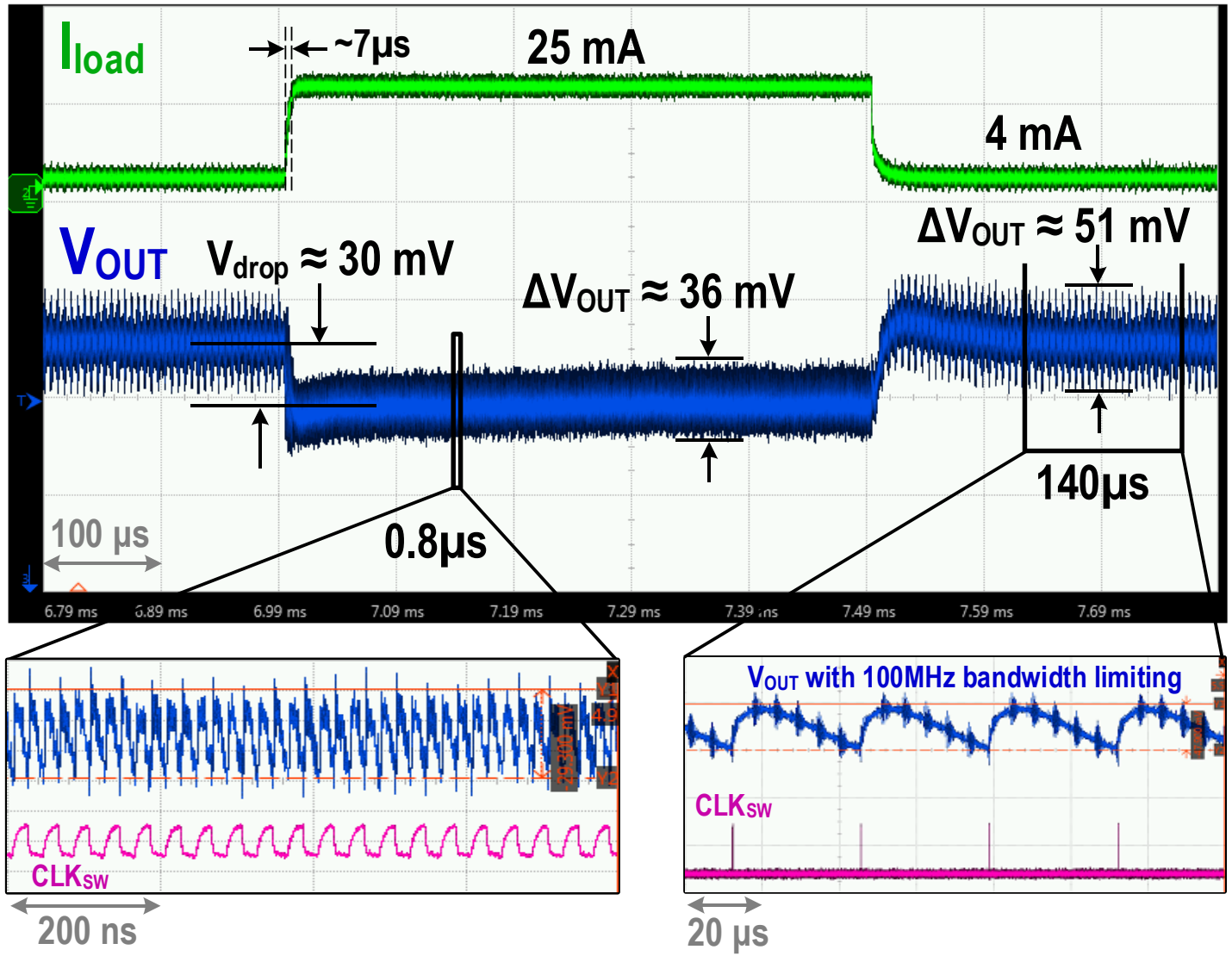
Measured Efficiency over Output Power Range



- Max. P_{OUT} > 80mW with buck 2:1

Measured Load Transient Waveforms

VCR = 6:5, f_S = 25MHz, V_{IN} = 1.32V, V_{OUT} > 1V, C_{L_EX} = 0µF



Performance Summary and Comparison

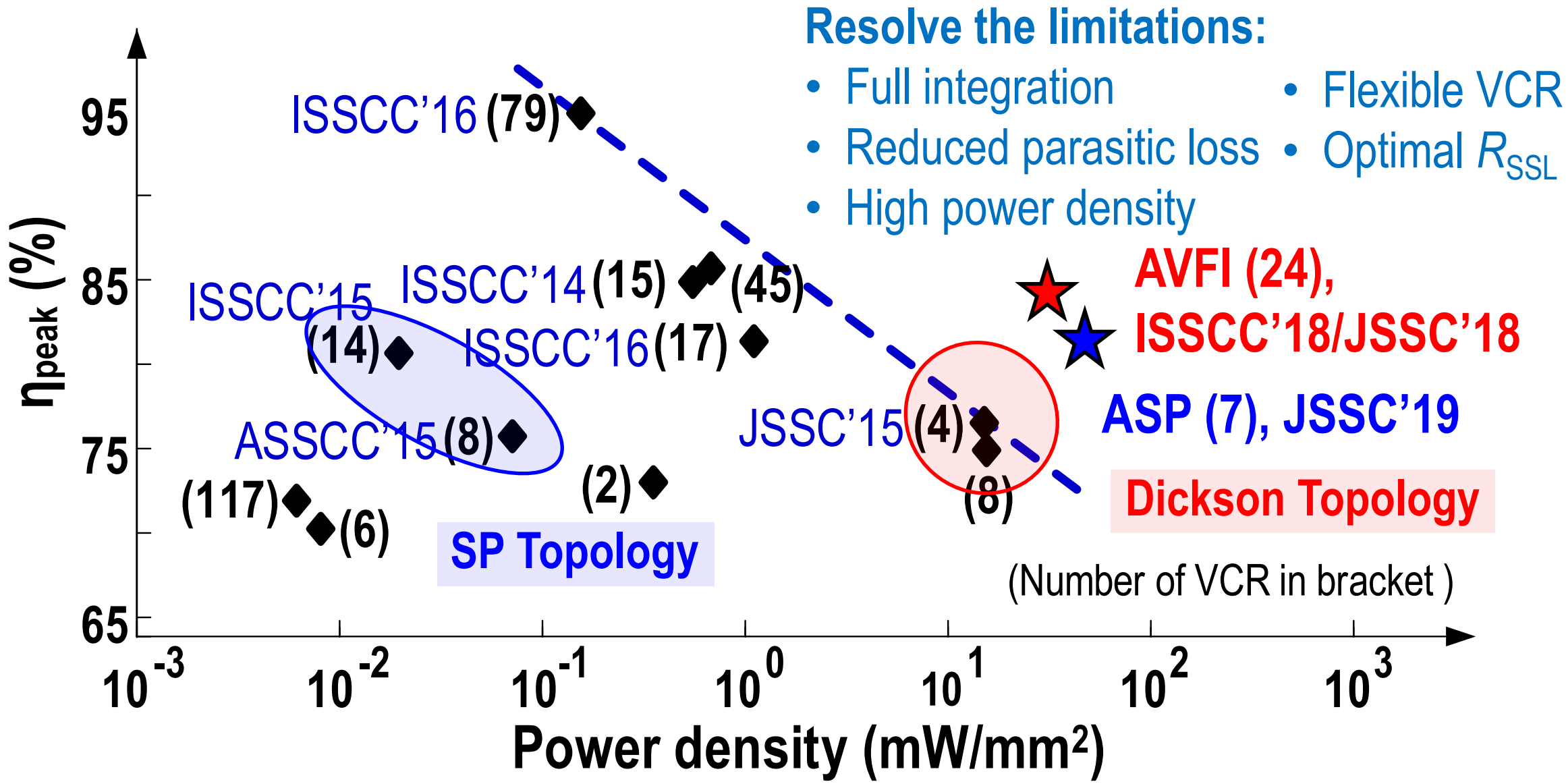
	This work	D. Lutz ISSCC'16	C. K. Teh ISSCC'16	M. Saadat ASSCC'15	X. Hua CICC'15	J. Jiang JSSC'17
Technology	**65nm CMOS**	0.35μm HVCMOS	65nm CMOS	0.25μm CMOS	65nm CMOS	130nm CMOS
Conv. type	**Buck-Boost**	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck
No. of VCR	**11 buck + 13 boost**	8 buck + 9 boost	5 buck + 1 boost	4 buck + 4 boost	3 buck + 3 boost	6 buck
Integrated C_{fly}	**MOS + MIM**	MIM	MOS + off-chip 1μF	MIM	N/R	Off-chip 4μF
V_{IN} [V]	**0.22 ~ 2.4**	2 ~ 13	0.85 ~ 3.6	0.6 ~ 2.4	0.5 ~ 3.3	1.6 ~ 3.3
V_{OUT} [V]	**0.85 ~ 1.2**	5	0.1 ~ 1.9	1.2 ~ 1.5	1	0.5 ~ 3
I_{OUT_MAX} [mA]	**80.1**	4	10	0.1	0.0033	120
η_{peak} [%]	**Buck: 84.1** **Boost: 83.2**	Buck: 81.5 Boost: 70.9	Buck: 95.8 Boost: 90.5	76	70.4	91
P-den@η_{peak} [mW/mm^2]	**Buck: 13.2** **Boost: 10.2**	*Buck: 0.96 *Boost: 0.15	N/R	*0.062	*0.0069	N/A

*Estimated from the corresponding literature

Outline

- Background and Motivation
- Algebraic Series-Parallel (ASP)-based Boost Topology
- Algorithmic Voltage-Feed-In (AVFI) Buck/Boost Topology
- Summary

Summary


Resolve the limitations:
• Full integration
• Reduced parasitic loss
• High power density
• Flexible VCR
• Optimal R_{SSL}
ISSCC'16 (79)
ISSCC'15 (14)
ISSCC'14 (15)
(45)
ISSCC'16 (17)
ASSCC'15 (8)
(117)
(6)
(2)
JSSC'15 (4)
(8)
AVFI (24), ISSCC'18/JSSC'18
ASP (7), JSSC'19
Dickson Topology
SP Topology
(Number of VCR in bracket)
η_{peak} (%)
95
85
75
65
10^{-3}
10^{-2}
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
Power density (mW/mm²)

Acknowledgement

- Macau Science and Technology Fund (FDCT)
- Research Committee of University of Macau

科學技術發展基金
F | D | C | T

UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

Thank you for your attention!

Man-Kay Law (MKLaw@um.edu.mo)