55nm DDC Subthreshold MCU 2.5µA/MHz

Talk IEEE - Switzerland – SSCS
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CSEM is the «Centre Suisse d'Electronique et Microtechnique»

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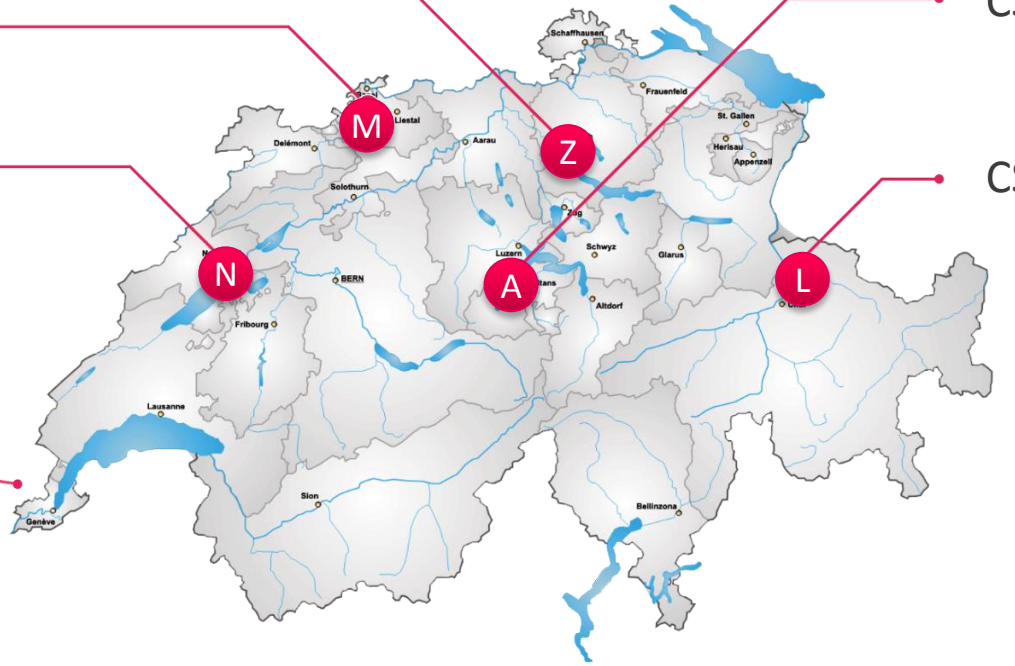

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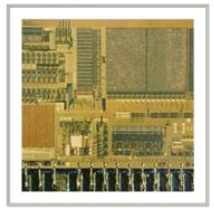
Our mission is to develop and transfer microtechnologies to industry

Disruptive developments – a story of "firsts"

1967 — The first electronic watch in the world: Beta1

1982 — The first watch micro-processor



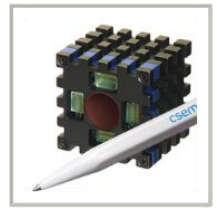
1991 — The first commercial standalone AFM in Europe

1993 — The first optical mouse in the world

1997 — The very first fully integrated convolutional NN chip

1997 — The first UMTS (3G) demonstrator in the world

2003 — The first 3D TOF camera in the world



2007 — The first "Invar" out of silicon

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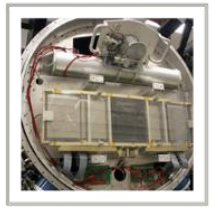
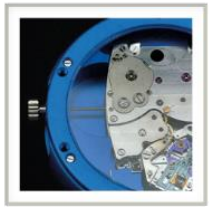
And since 2012?

2012 — Observation of the oldest galaxy



2014 — A revolution in the mechanical watch industry, a completely new movement principle



2014 — Colored photovoltaics panels

2014 — Landing of Philae on P67 the eyes of the scientists

2015 — Architectural integration of PV solar panels

2016 — First commercial solution for GPS-free geolocation of connected devices

2017 — Smallest BLE 5.0 chip of the market

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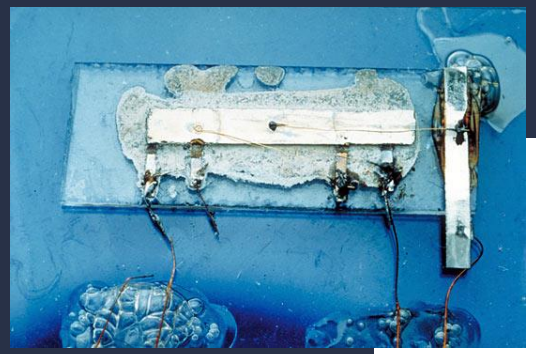
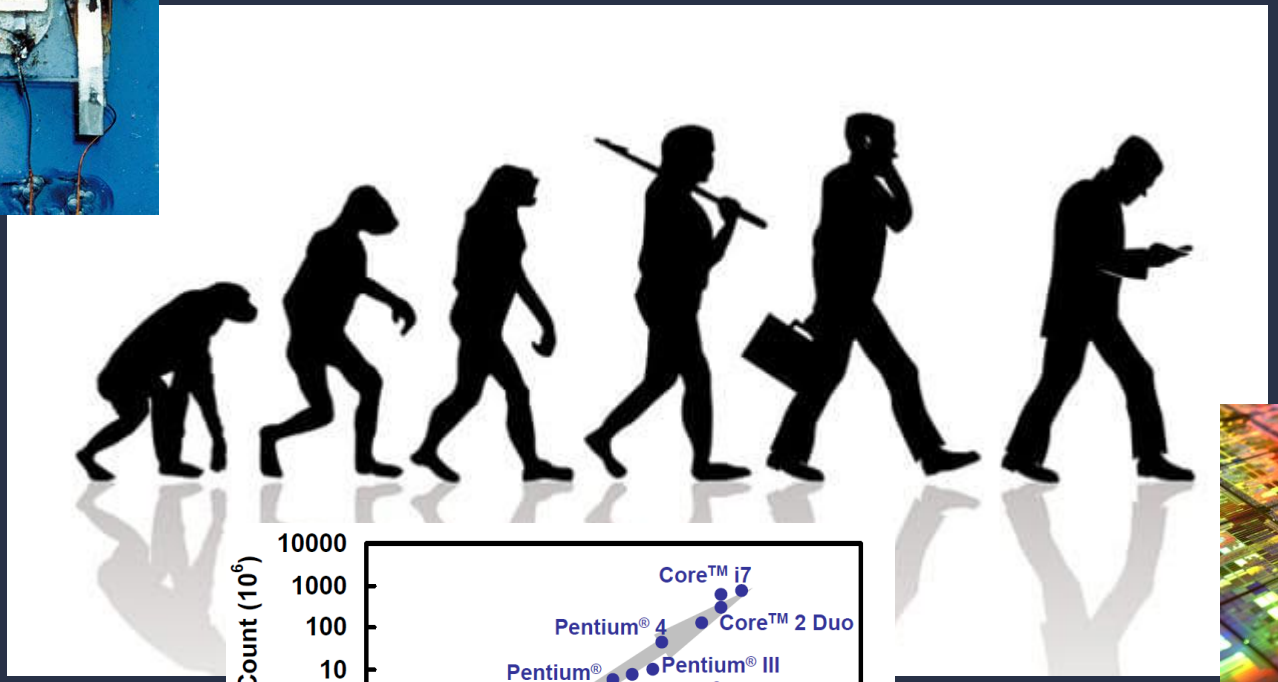
Outline

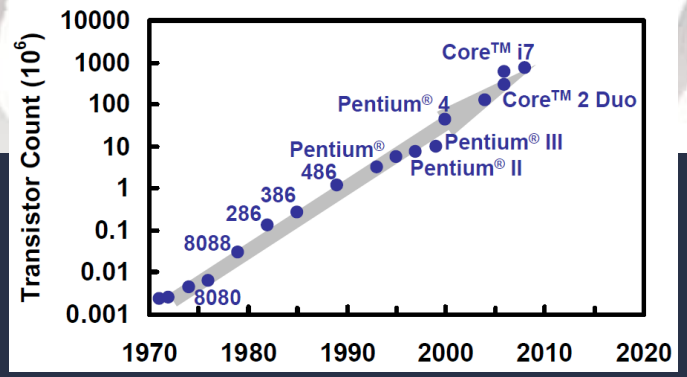
- Ultra low power challenge
- Low voltage approach
- 55nm DDC technology
- Body bias compensation
- MCU system
- Measurement results
- Conclusion

Technology has made a long way!

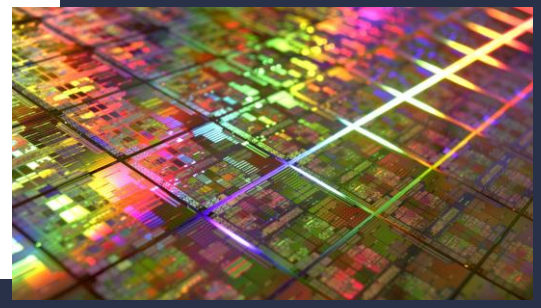


From Kilby's first circuit in 1958…





…following Moore's law…



…to nowadays integrated circuits!

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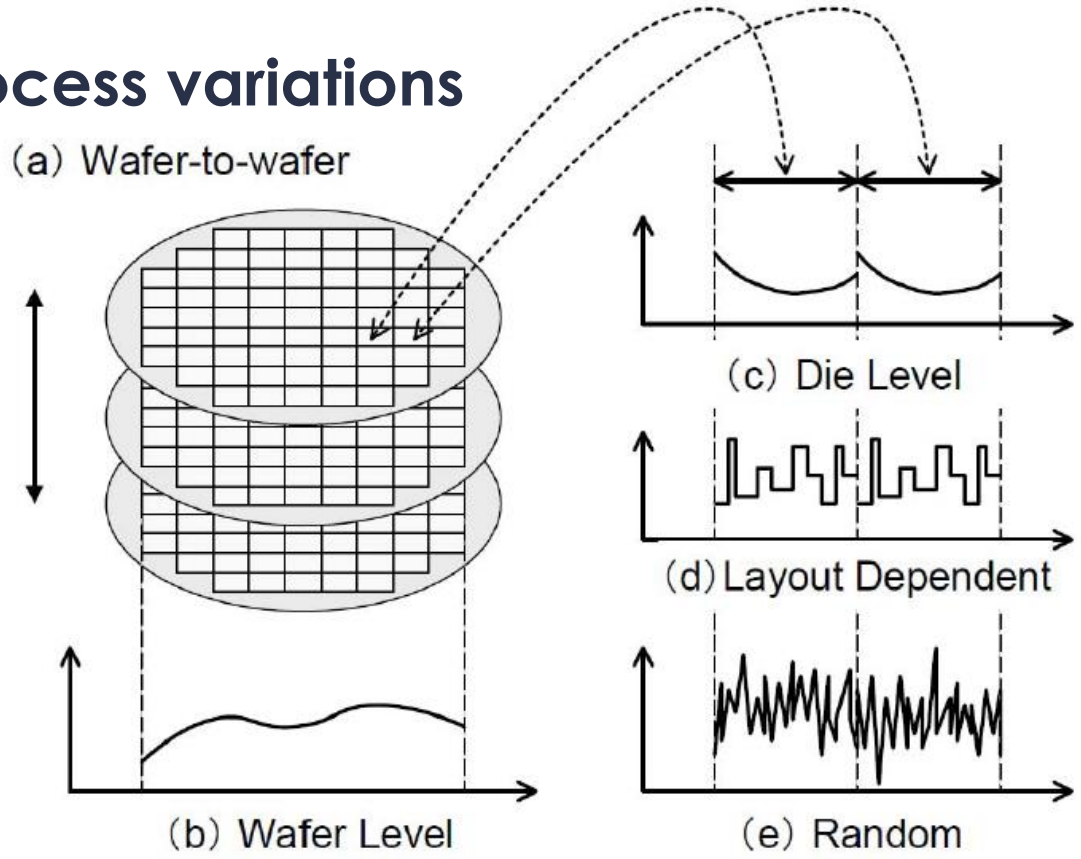
But the path is full of traps…

Process variations

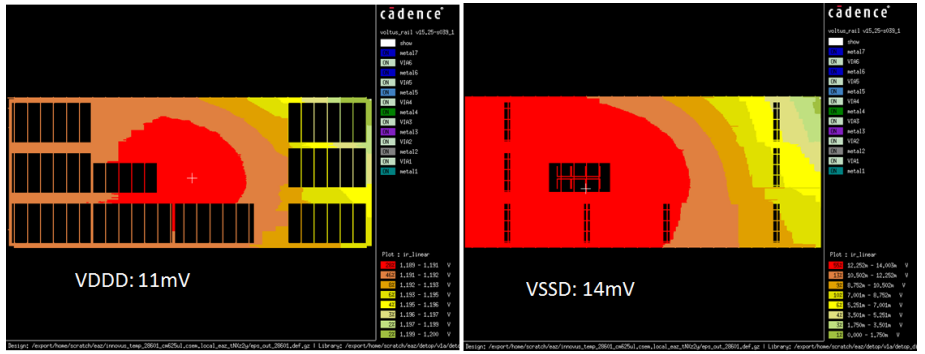


Temperature variations

$$V_{th}(T) = V_{th}(T_0) - k(T - T_0)$$

$$\mu(T) = \mu(T_0)\left(\frac{T_0}{T}\right)^m$$

Voltage variations



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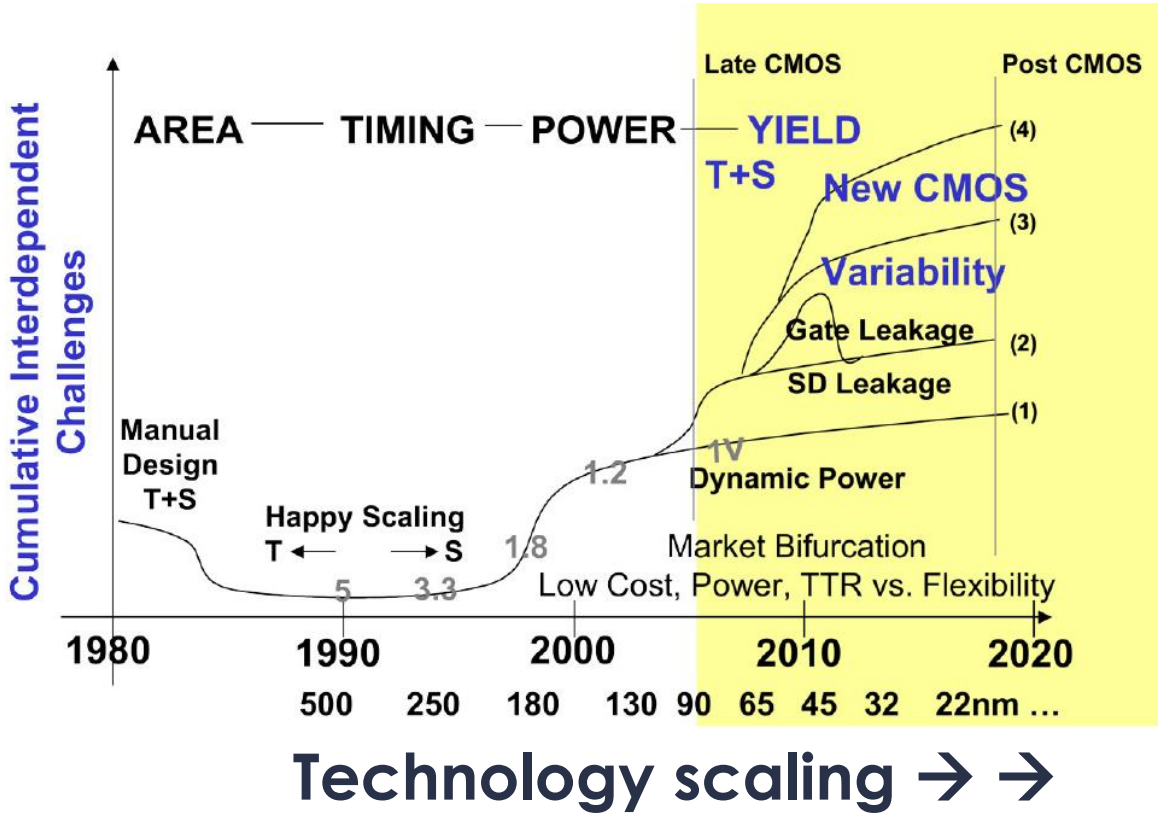
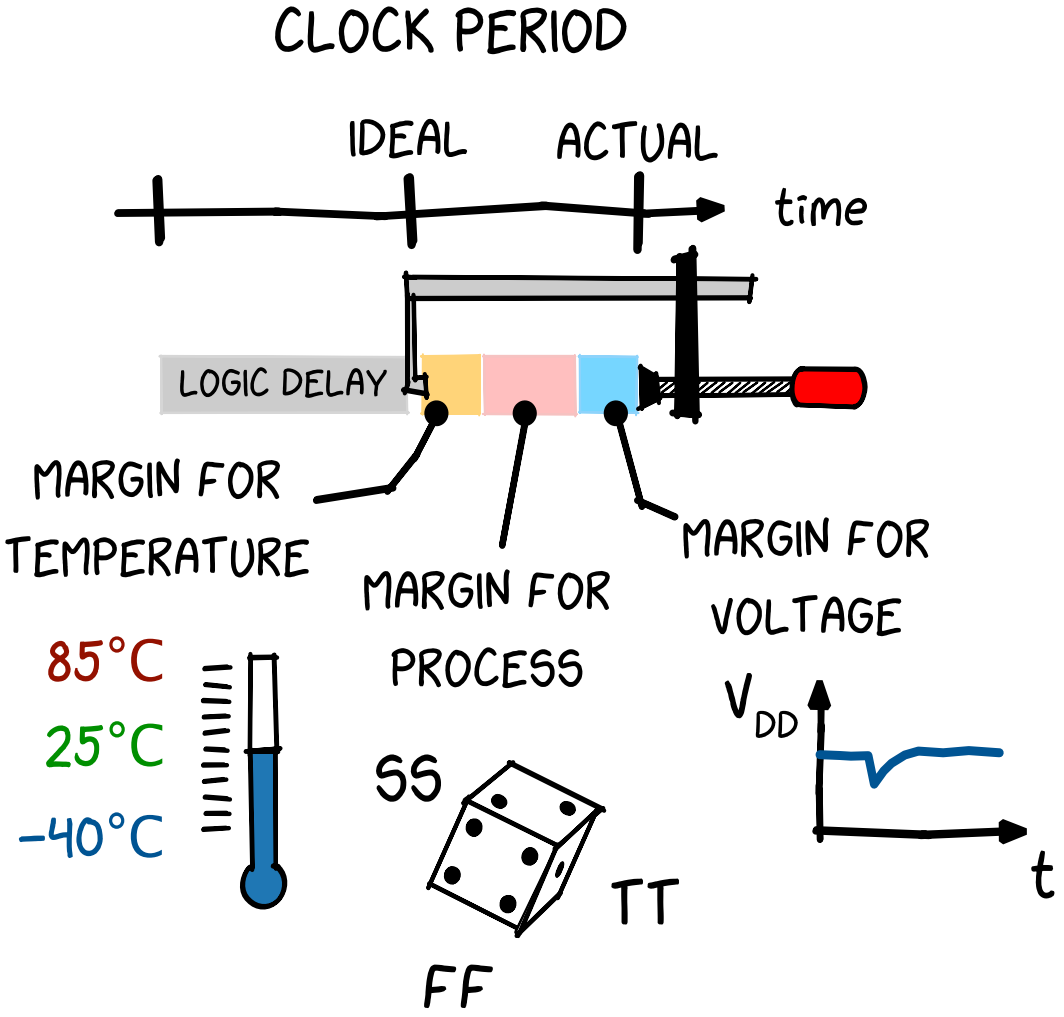
PVT variations to be considered for design's manufacturability and yield





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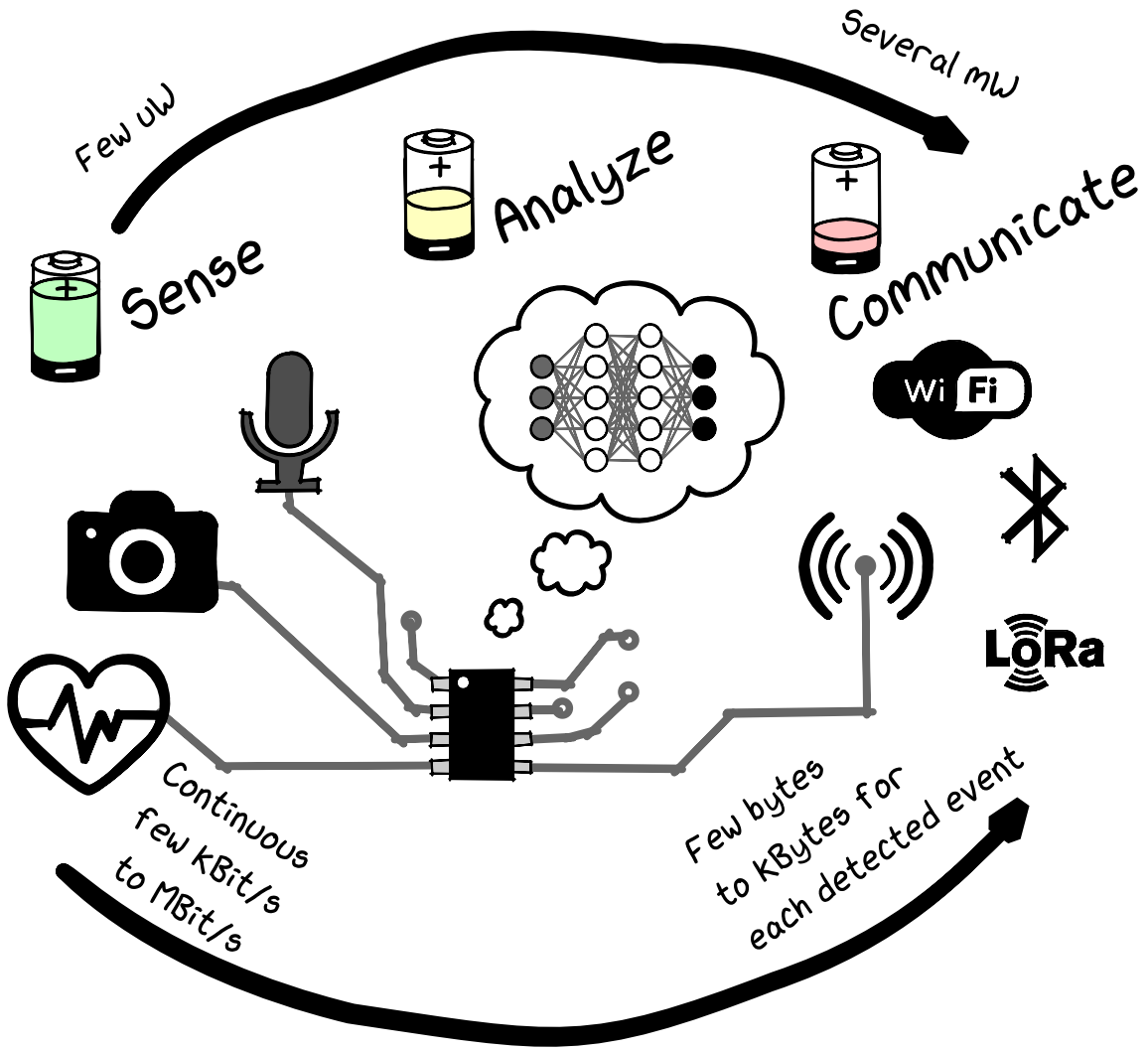
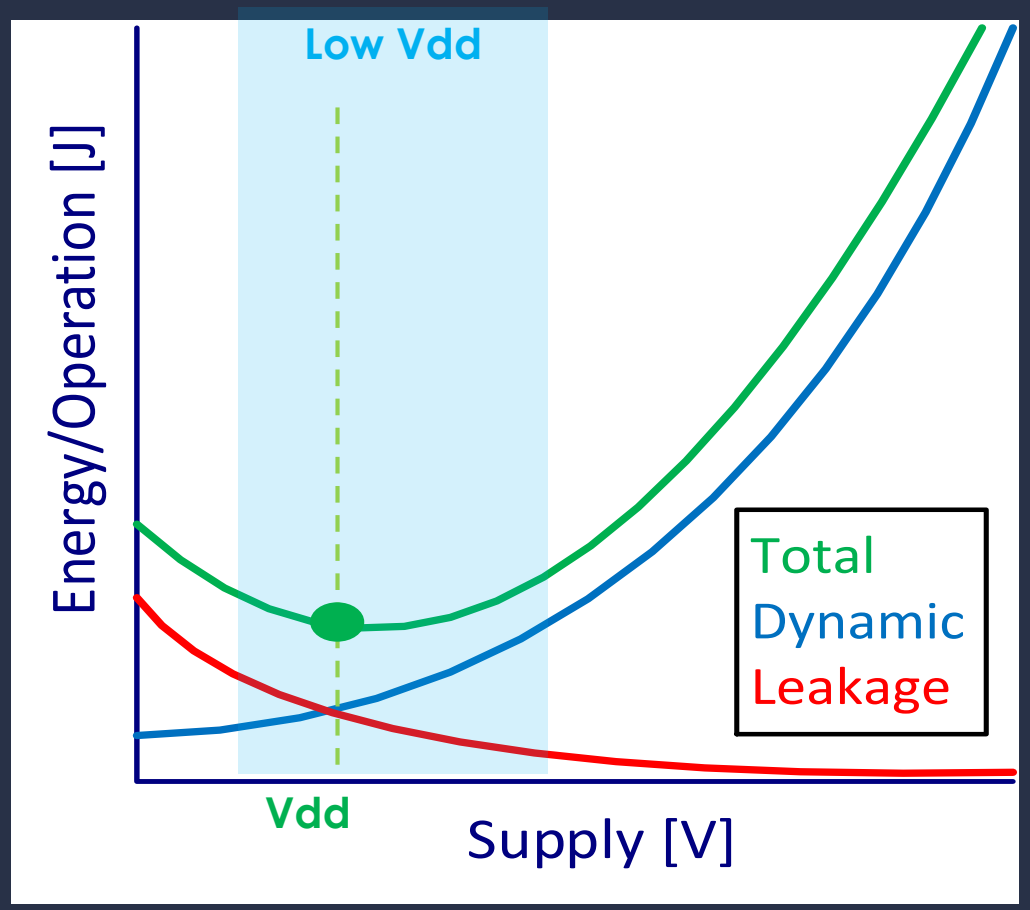
Then come ultra low power constraints!



- Constrained power budget
- Growing memory needs
- Connectivity
- Miniaturization

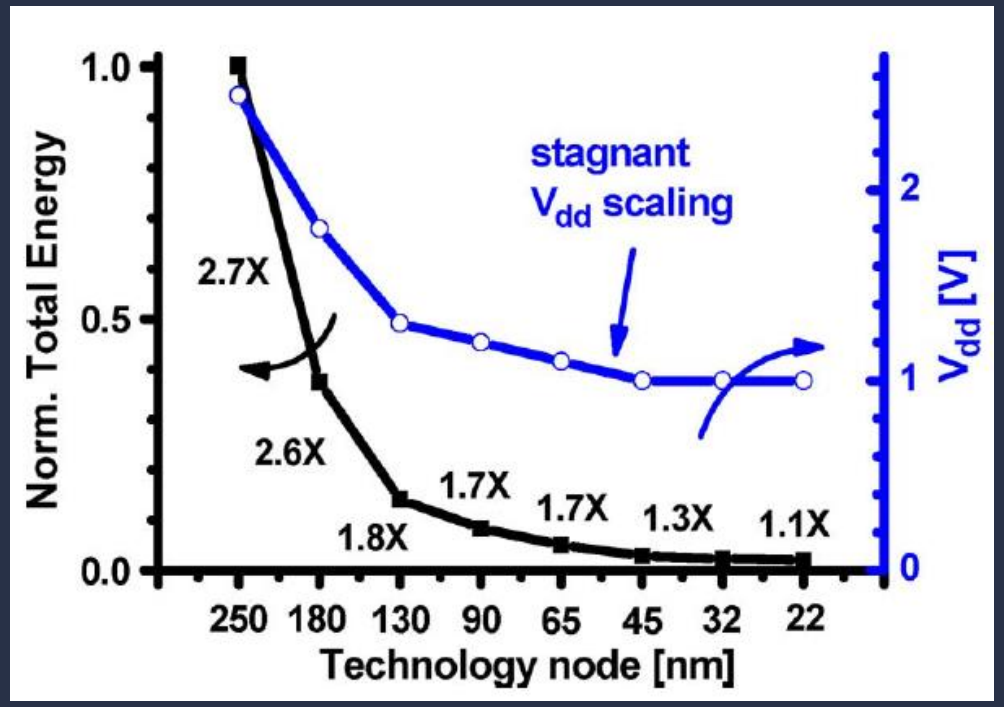
And subthreshold design comes to save the day…



$$E = \alpha \cdot C \cdot V_{dd}^2 + \frac{I_{off} \cdot V_{dd}}{f}$$

Minimum energy point obtained when reducing the voltage

But voltage scaling is challenging…



Technology scaling → →

Voltage scaling adds complexity to technology scaling!

The magic cycle!

Mature technology
- PVT under control
- Minimum energy point

Technology scaling

Voltage scaling

Standard technology
- PVT under control
- Energy constraints

Subthreshold techniques

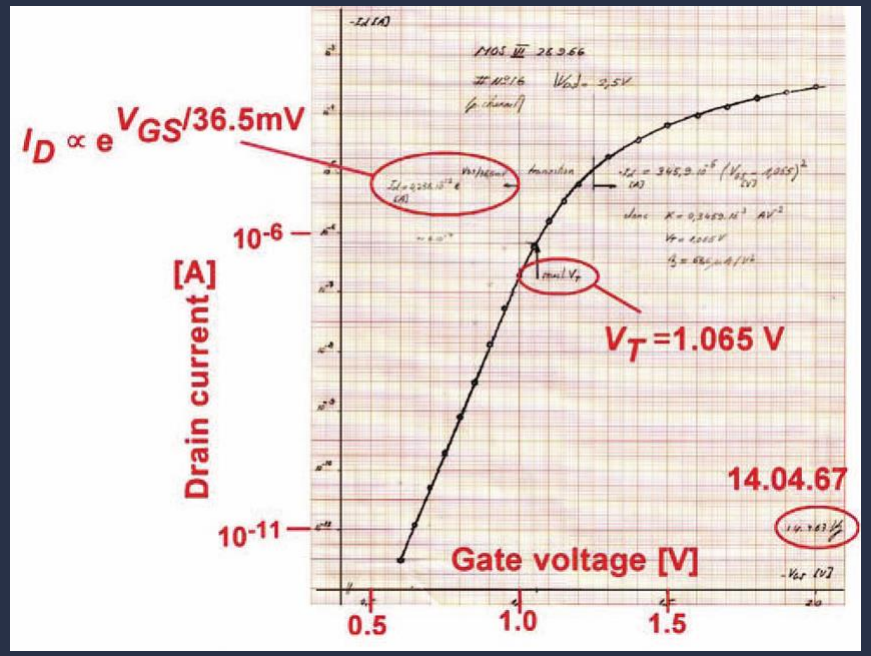
Standard techniques

Challenging technology
- PVT sensitivity

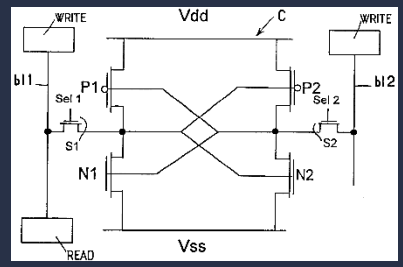
Challenging technology
- PVT sensitivity

CSEM's has a long history on subthreshold design

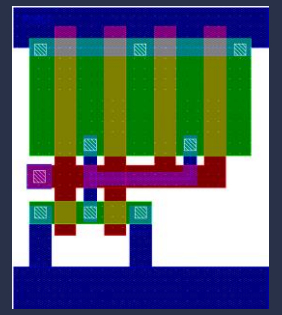
From Eric Vittoz first MOS meaurements in 1967…

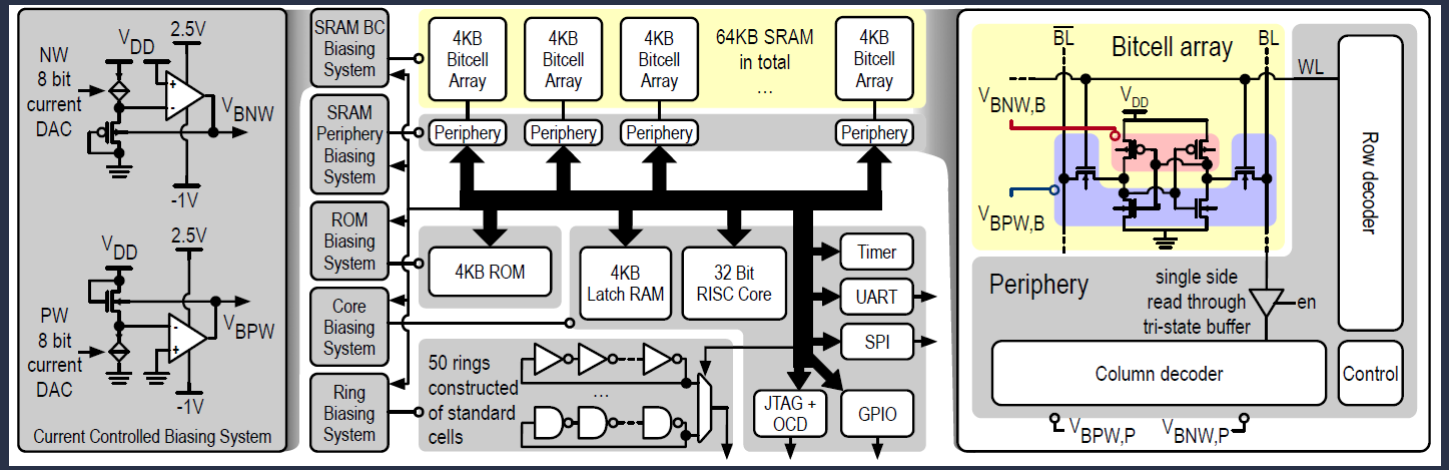


…through memory and standard cell design…



Patent: US 6,366,504 B1





…to nowadays subthreshold MCU

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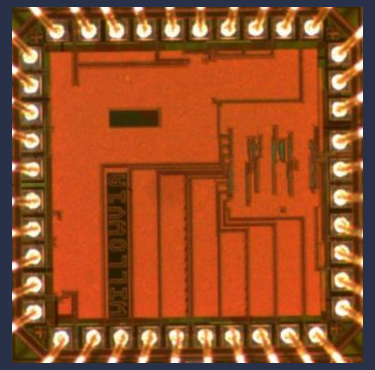
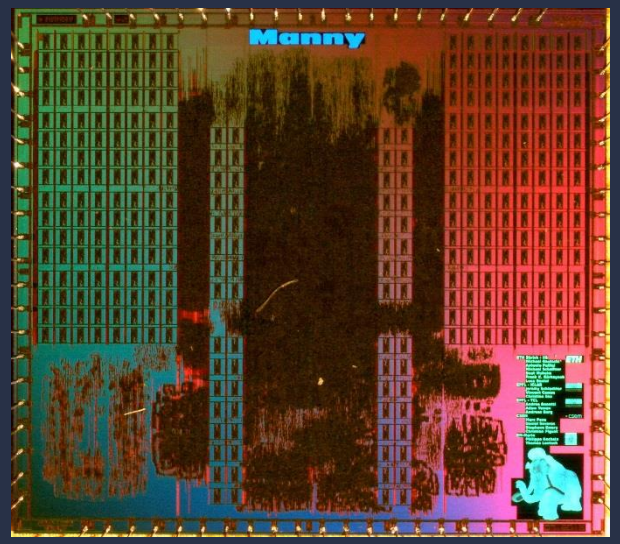
Subthreshold chips in the last years

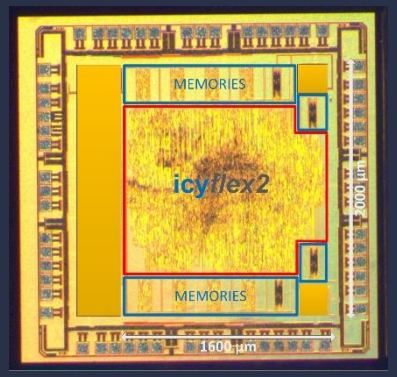


Willow
TSMC 180nm
0.4V

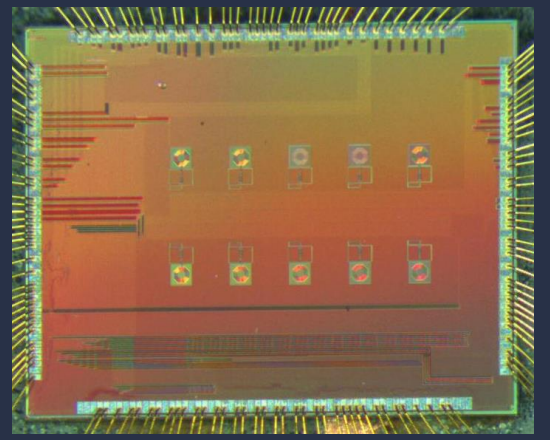


Manny
ALP 180nm
0.6V

Breithorn
TSMC 65nm
0.3V



Allalin
ALP 180nm
0.6V



Calanda
DDC 55nm
0.5V

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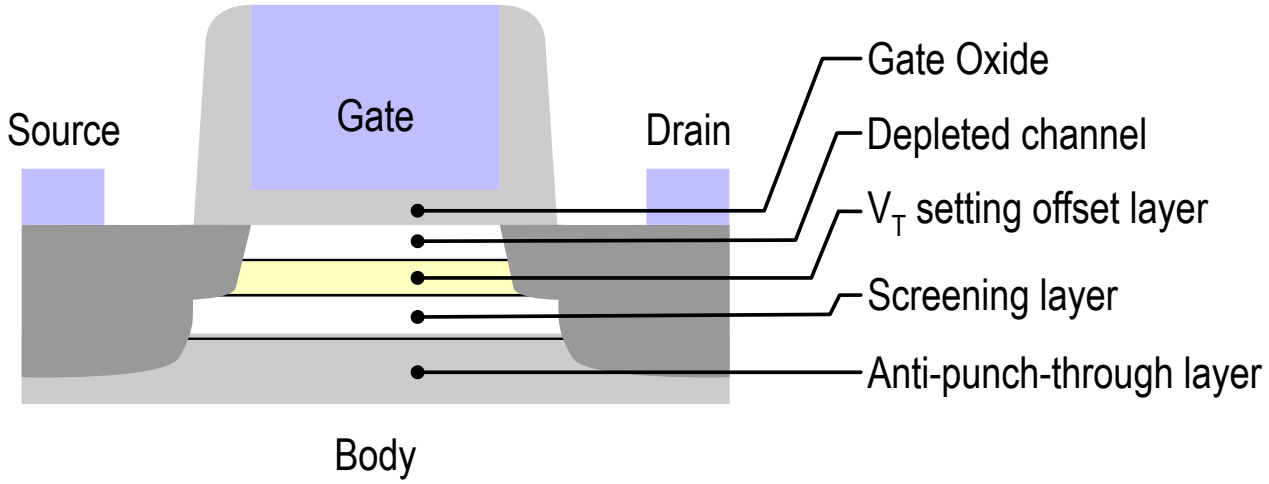
55nm DDC CMOS

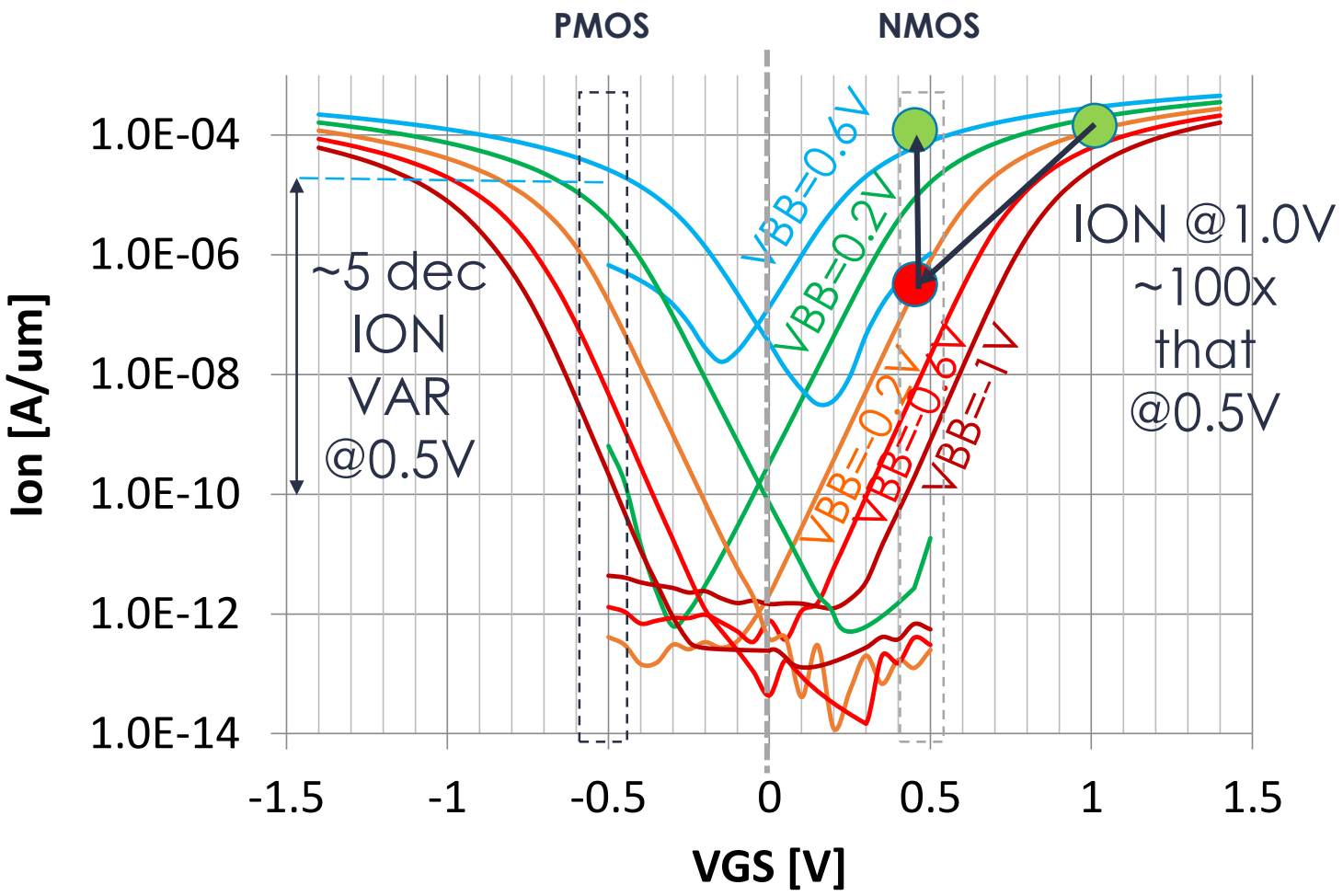
Strong body factor of 375 mV/V (FDSOI: 80mV/V)

Allows to scale V_{th} from 250mV to 850mV

Undoped depleted channel that does not suffer from random dopant fluctuations



DDC body bias control

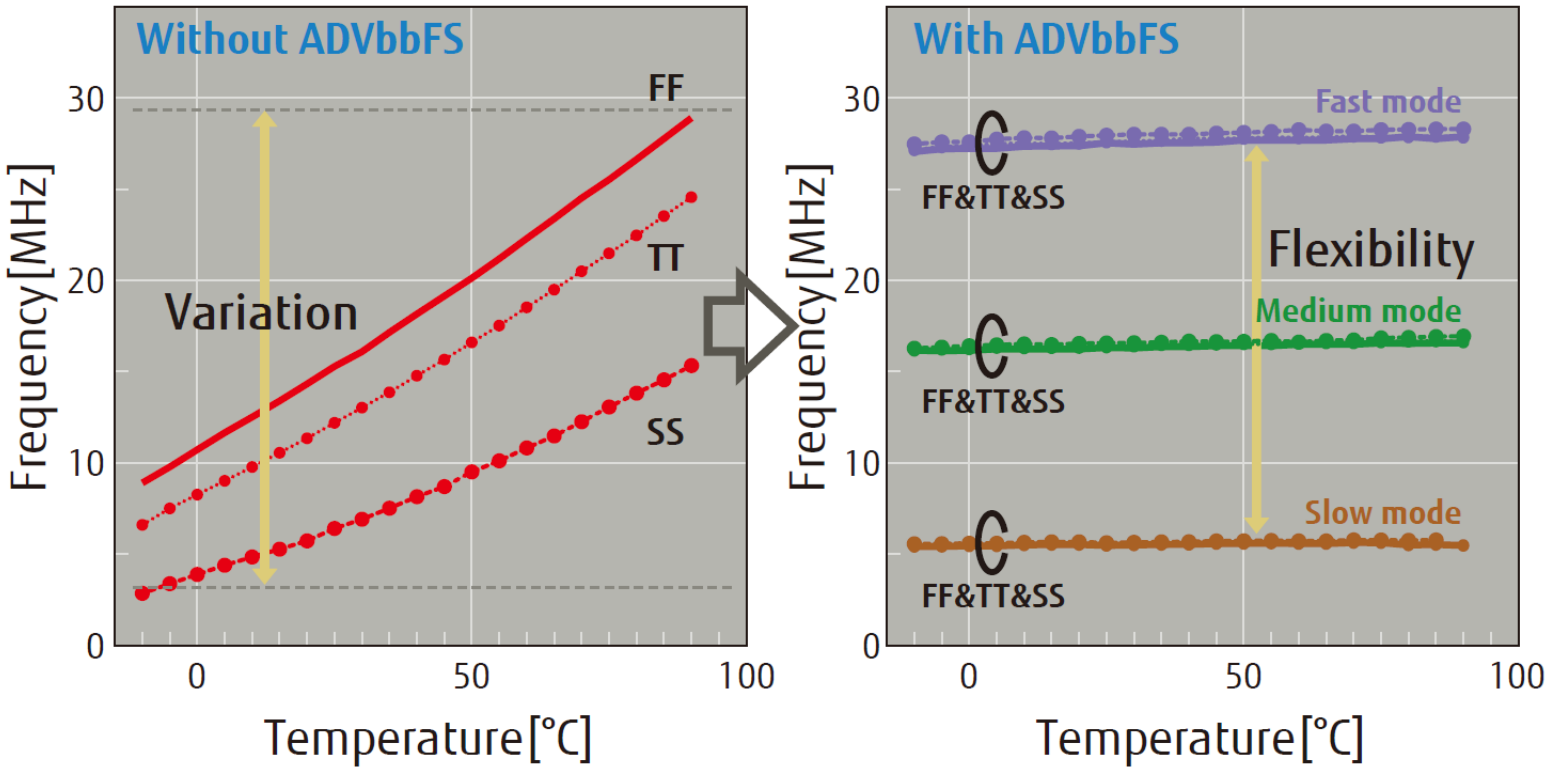


$$f \approx {}^{I_{ON}}/_{CV}$$

Almost same frequency at 0.5V compared to 1V with DDC !

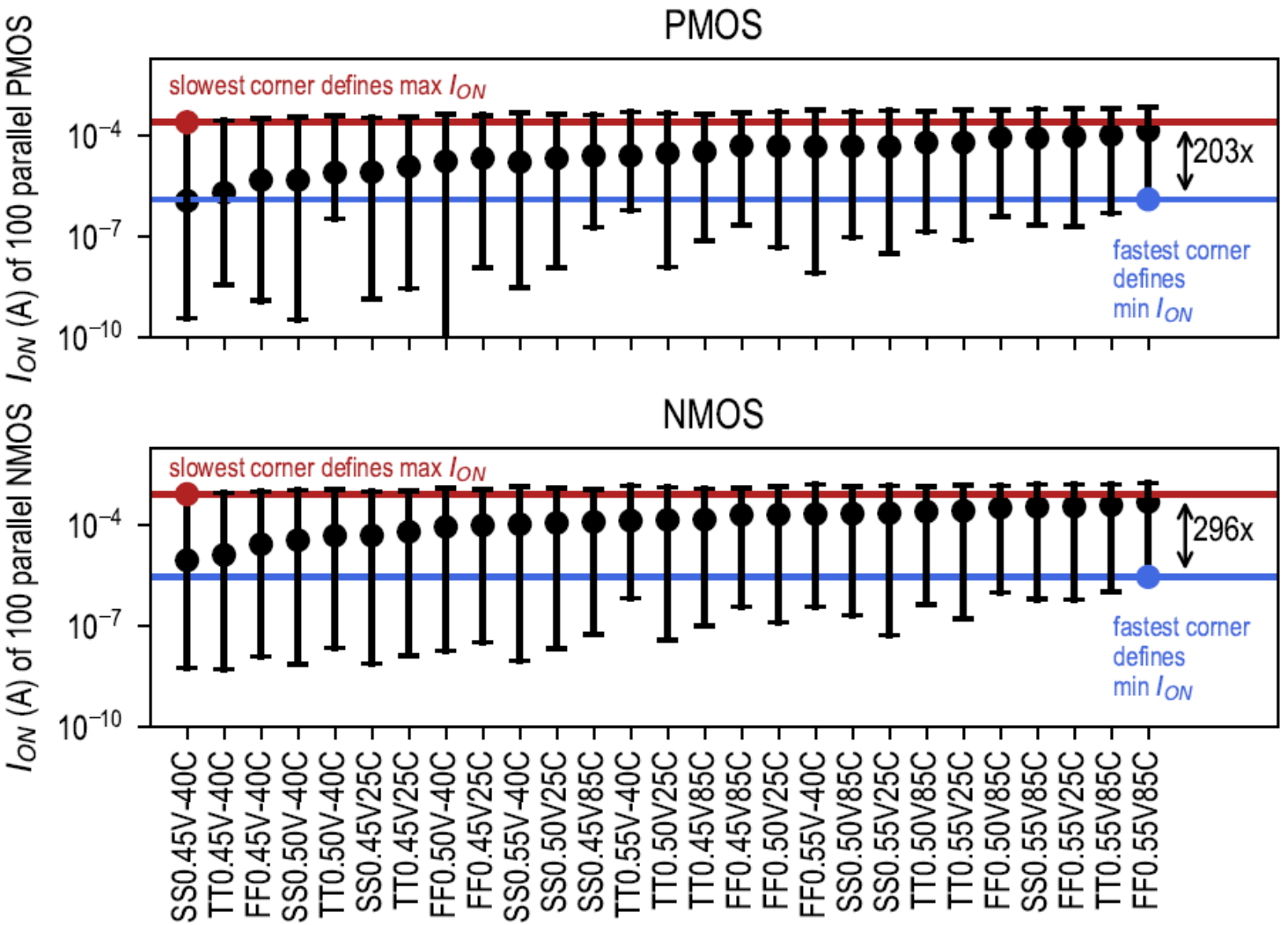
Huge frequency and leakage scaling capability

Frequency compensation principle



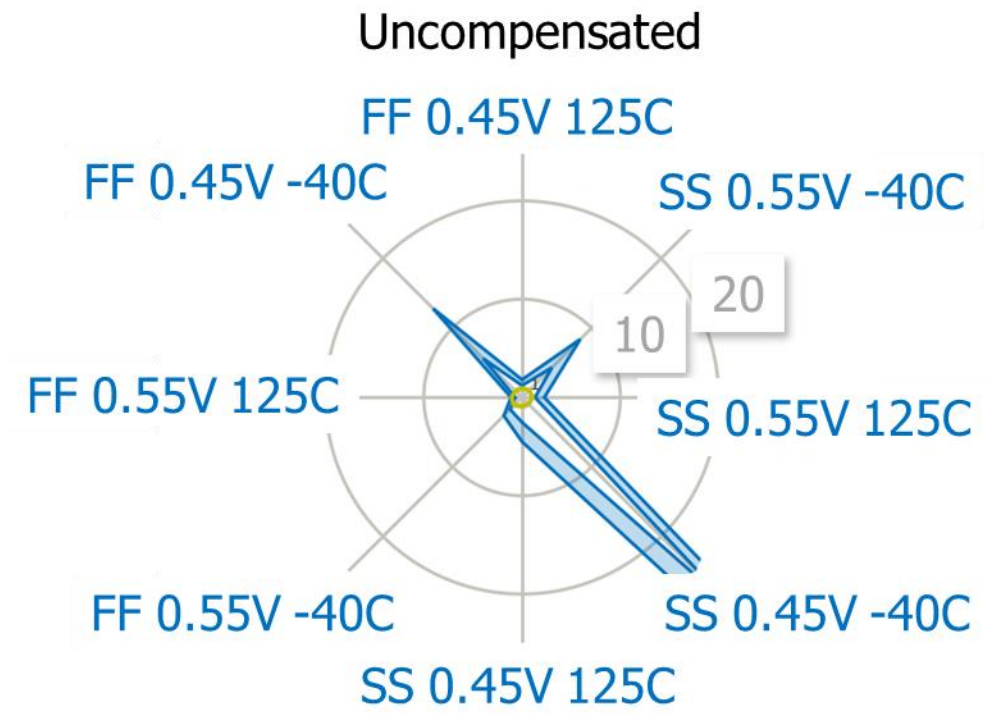
ADVbbFS stands for Adaptive Dynamic Body Bias Voltage Frequency Scaling

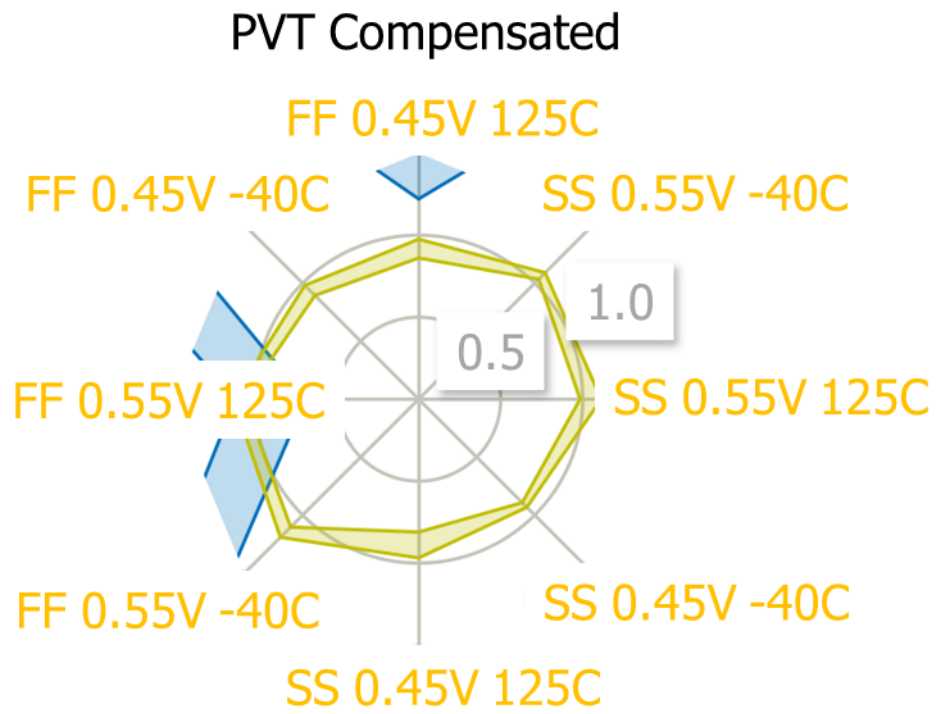
PVT spread



19

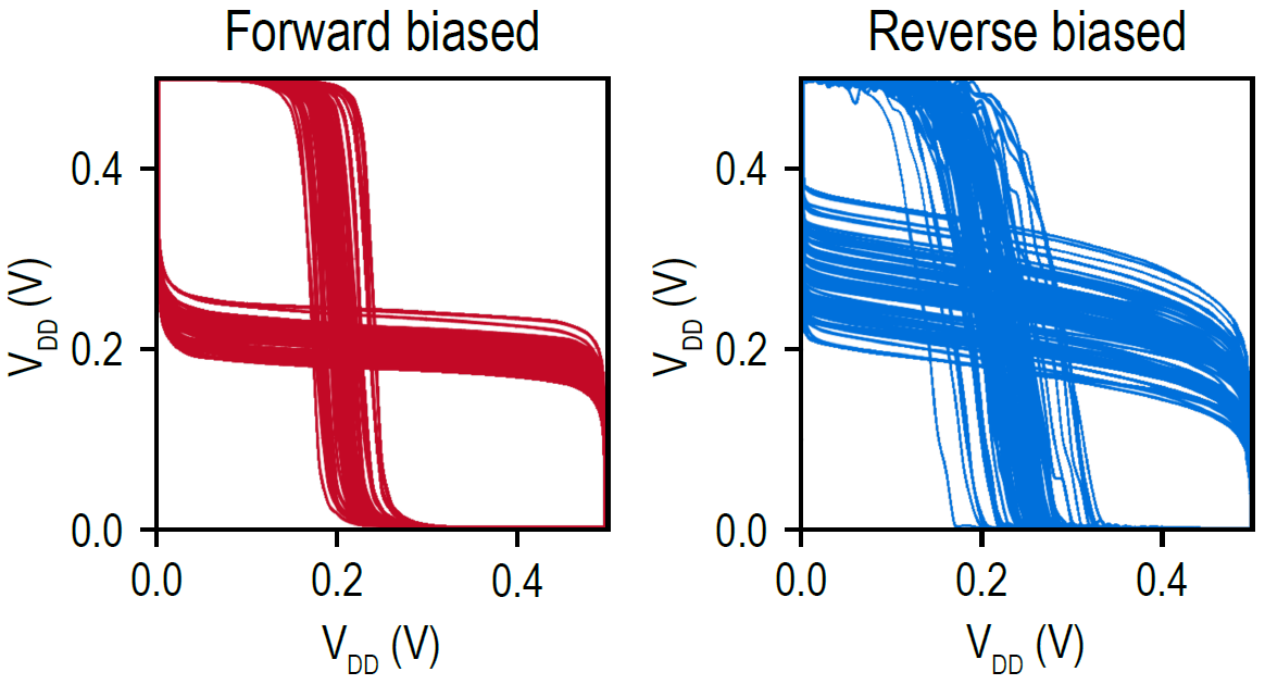
Standard cells frequency compensation

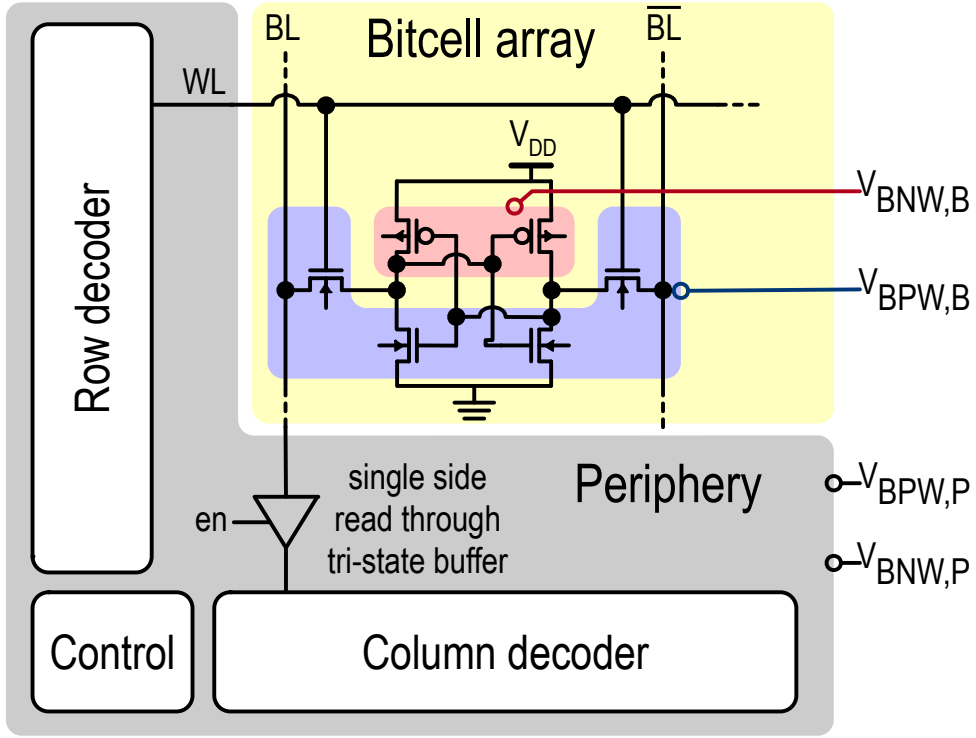




6T SRAM frequency compensation

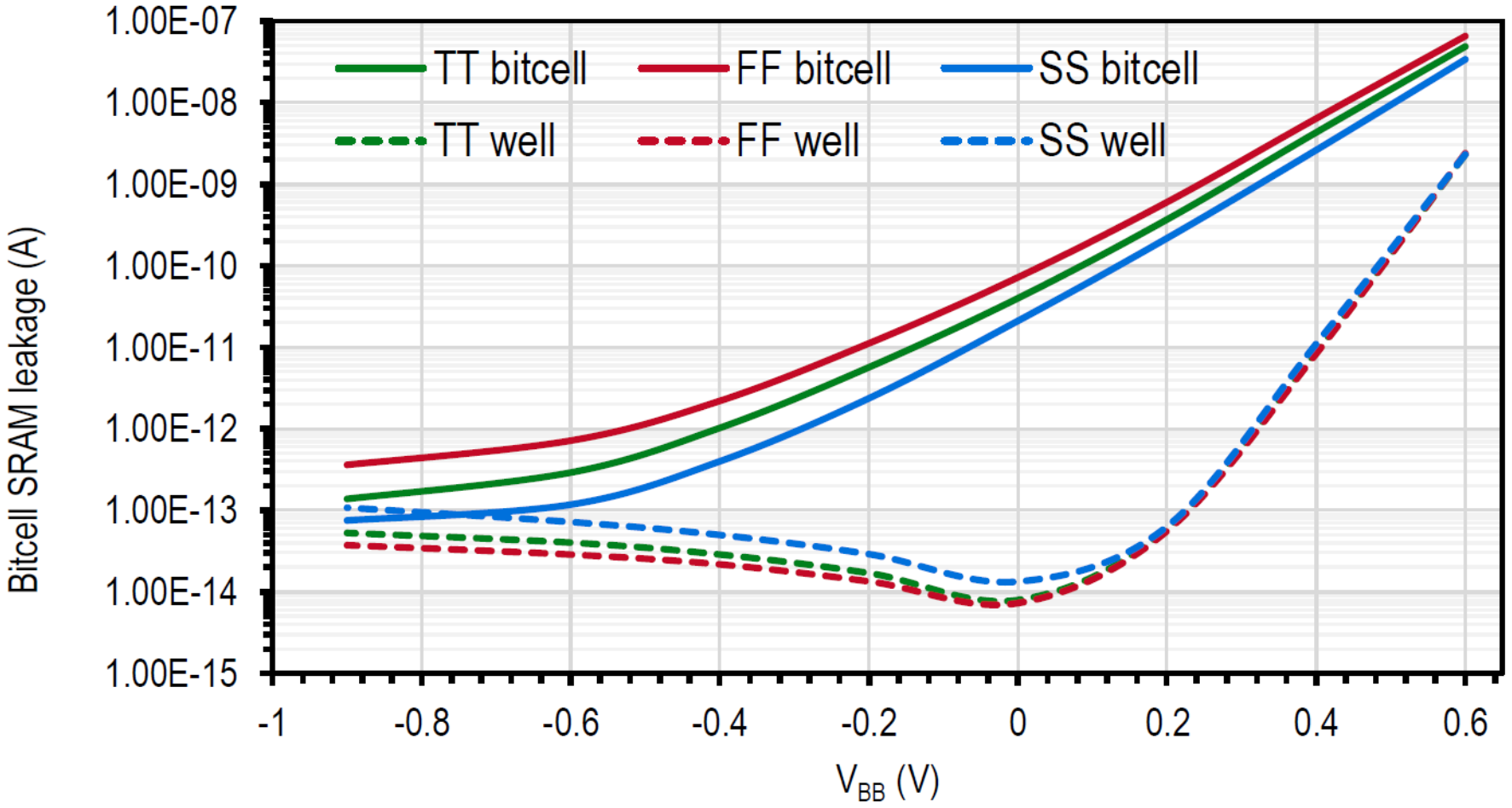
Static noise margin in the whole bias range



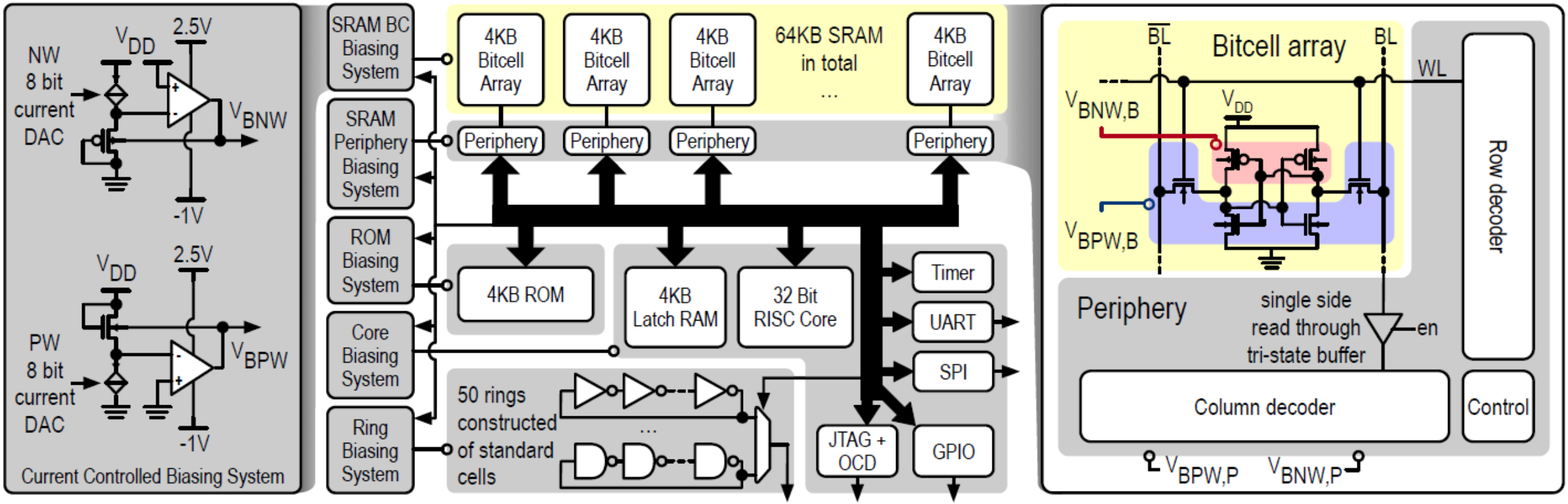


21

Well currents are far below Ion currents



System block diagram



32 bit Microcontroller + 64kB SRAM + Analog-Assisted Adaptive Body Bias PVT Compensation

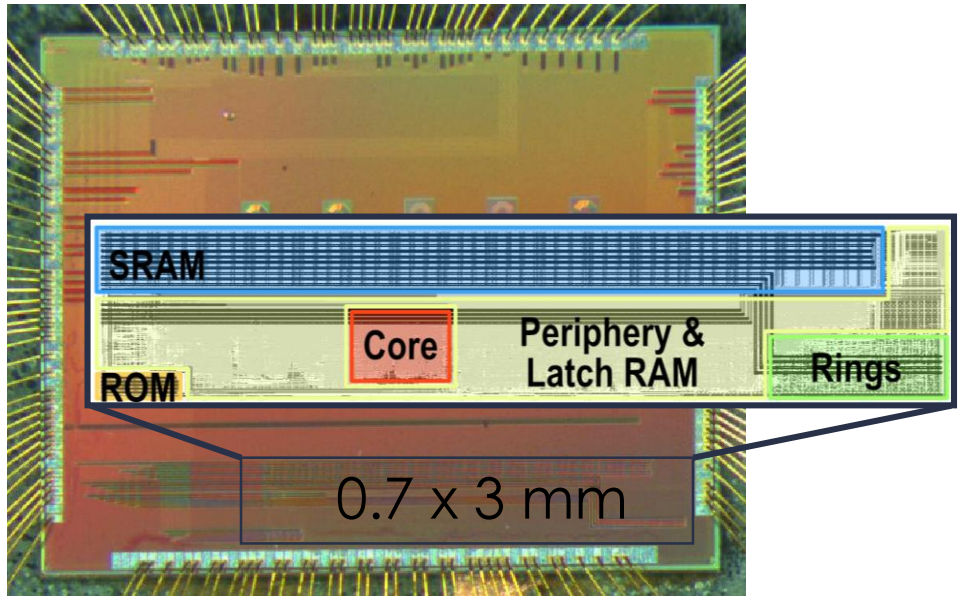
Measurement conditions

Process: 55nm DDC SS, TT, FF

Voltage: 0.5 V ±10%

Temperature: -40°C to 85°C

Frequency (mode): 0.31 to 10 MHz



32 bit RISC Core measurement

	Leakage			
Frequency	FF 0.55V 85°C	TT 0.5V 25°C	SS 0.45V -40°C	Dynamic
0.31 MHz	0.25 µA	54 nA	14 nA	2.56 µW/MHz
10 MHz	4.08 µA	1.19 µA	0.24 µA	

25

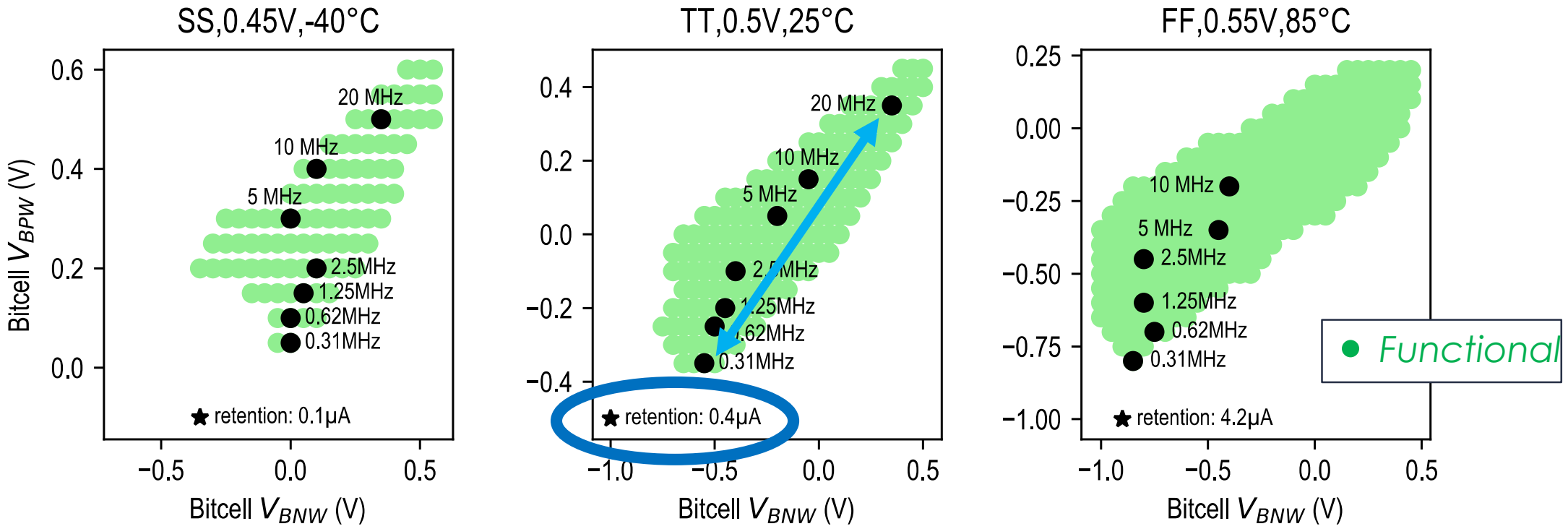
Frequency	Frequency variation over PVT
0.31 MHz	± 21%
10 MHz	± 6%

In typical conditions

- *> 30x frequency scaling*
- *> 20x leakage scaling*

Variation increases in sub-threshold operation (use of reverse bias for low frequency)

64kB SRAM measurements



26

Dynamic 2.5 µW/MHz

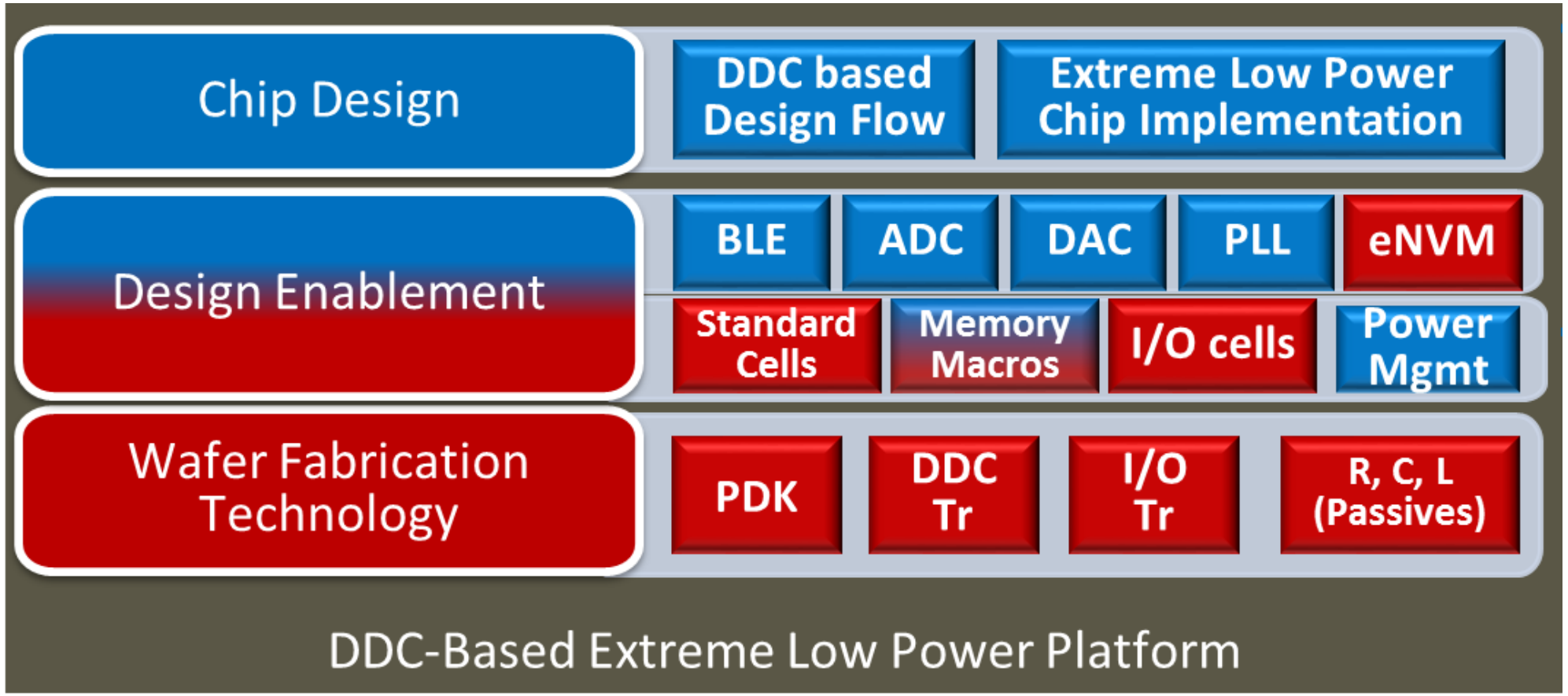
In typical conditions

- *> 60x frequency scaling*
- *3.13 nW/kB retention*

Conclusion

- Combination of DDC 55 nm CMOS with a novel analog-assisted current-based adaptive body bias for low voltage
- 32 bit Microcontroller system with 64kB 6T SRAM at 0.5V
- 30x frequency scaling, 20x leakage scaling at fixed voltage
- Down to ±6 % frequency variation over PVT
- 32 bit RISC 2.56 µW/MHz, 27 nW leakage
- 6T SRAM 2.5 µW/MHz, 3.13 nW/kB retention

Deeply-Depleted Channel (DDC) ecosystem



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IEEE papers

[ISLPED 2019-accepted] Energy-Autonomous MCU Operating in sub-VT Regime with Tightly-Integrated Energy-Harvester

[CICC 2019] A 0.5V 2.5 µW/MHz Microcontroller with Analog-Assisted Adaptive Body Bias PVT Compensation with 3.13 nW/kB SRAM Retention in 55 nm Deeply-Depleted Channel CMOS

[ICSEE 2018] PVT Compensation and Performance Scaling with Adaptive Body Bias in Fujitsu 55nm DDC

[S3S 2017] PVT Compensation in Mie Fujitsu 55 nm DDC: A Standard-Cell Library Based Comparison

[S3S 2017] SNM Analytical Approach to Robust Subthreshold SRAM Operation based on the 55nm DDC Technology

[ESSCIRC 2016] Sub-Threshold Latch-Based icyflex2 32-bit Processor with Wide Supply Range Operation

[S3S 2015] A 10 kgates sub-threshold stream cipher in 180 nm with 6.1 kHz frequency 70 nA total current and 46 nA leakage at 0.33 V

[S3S 2015] A 1kb single-side read 6T sub-threshold SRAM in 180 nm with 530 Hz frequency 3.1 nA total current and 2.4 nA leakage at 0.27 V

[ISVLSI 2015] Sub-Threshold Design and Architectural Choices

[PATMOS 2013] Ultra Low-Power Standard Cell Design using Planar Bulk CMOS in Subthreshold Operation

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