ESD Design in High Voltage Smart Power Technologies

Lorenzo Cerati

ESD Design Solutions Technical Director
STMicroelectronics

Acknowledgments

Part of the following presentation has been extracted by a tutorial presented in the past years at the EOS/ESD Symposium and jointly prepared by STMicroelectronics and Infineon Technologies ESD experts.

I would like to thank our colleagues for supporting the preparation this tutorial:

- Infineon Technologies :
  - Filippo Magrini, Yiqin Cao, Joost Willemen, Michael Mayerhofer, Ulrich Glaser, Andreas Rupp, Werner Simbürger and Ralf Rudolf
- STMicroelectronics:
  - Antonio Andreini, Eleonora Gevinti, Leonardo Di Biccari, Luca Cecchetto, Riccardo Depetro, and Damiano Riccardi

Instructor's biography

Lorenzo Cerati is ESD Senior Principal Engineer and senior member of the Technical Staff at STMicroelectronics. Lorenzo received his M.Sc. degree in telecommunication engineering at the "Politecnico di Milano" Technical University in 1998, discussing a thesis on a CdZnTe cross-connect for optical networks. Since 2000, he has been working in STMicroelectronics in the ESD protections development team for Smart power technologies and now he is the manager of the group responsible for ESD protections development, Latch-up immunity and bipolar parasitic analysis in BCD processes. He is also in charge of design teams support to define, implement and debug complex ESD architectures in BCD ICs.

Lorenzo represents STMicroelectronics in the ESDA standardization committees and is member of JWG HBM, JWG CDM, WG5.4, WG 5.5 (where he is acting as vice-chairman), WG 5.6, and WG 14. Starting from 2016 he also has been serving as member of the Technical and Advisory Support Committee (TAS). Lorenzo served multiple times as a member of the ESREF, ICICDT, IRPS, IEW, and EOS/ESD Symposium Technical Program Committees and authored several papers on ESD and EDA topics. Since 2015, Lorenzo is member of the EOS/ESD symposium steering committee and will be Vice General Chair at the 2019 EOS/ESD symposium. Lorenzo is member of the ESDA Board of Directors' since 2015.

Abstract

ESD design in High Voltage Smart Power is a very challenging task due to the peculiarities of these technology nodes. After a short introduction describing the status of the international standards and norms for the various application fields where these technologies are adopted, an overview of the process options and the typical device portfolios in the Smart Power world will be given. Different ESD protection concepts will be introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback, active clamps…). Finally, some examples of HV-technology and design-related challenges regarding ESD protections will be discussed, with a focus on parasitic bipolar formation and their impact on device performance.

Contents

- Part 1 - Introduction: International ESD standards and norms
- Part 2 - Introduction to Smart Power Technologies & device portfolio
- Part 3 - ESD Protection concepts in Smart Power technologies
- Part 4 - HV related ESD issues

Contents

What is an ESD?

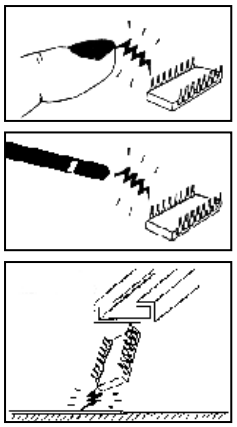
- An Electrostatic Discharge is a rapid discharge event that transfers a finite amount of charge between two bodies at different potentials
- The shape of the current is governed by the dynamic impedance of the two bodies
- The ESD discharge derives from an external event and is statistical in nature
- ESD events are one of the possible root causes for IC's failure on the field

How to face the problem

- In order to minimize ESD impact we can follow a twofold approach:
  - adopt static-safe practices to control charge build-up
  - produce robust ICs through process and circuit improvements

The ESD problem in IC

- ESD events can seriously damage ICs
- The charge transfer is due to:
  - Human handling (HBM)
  - Machine handling (MM)
  - Self-charging (CDM)

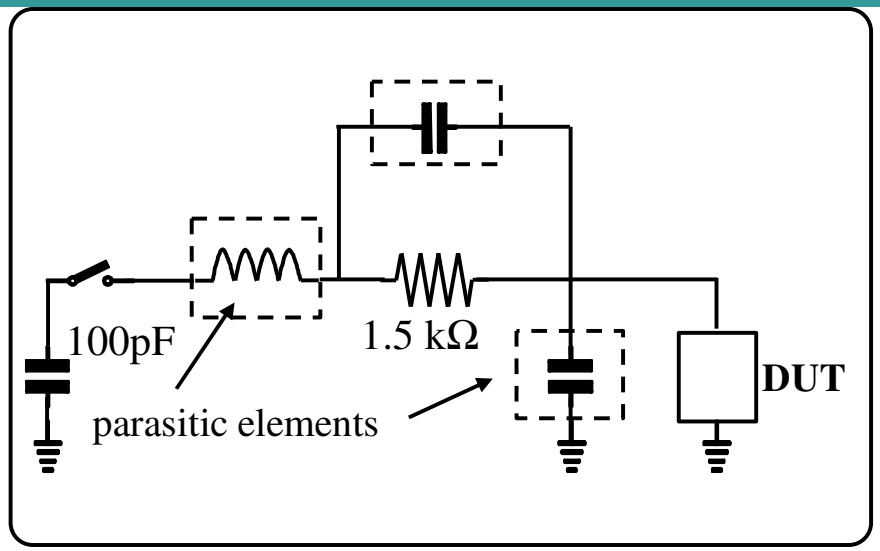


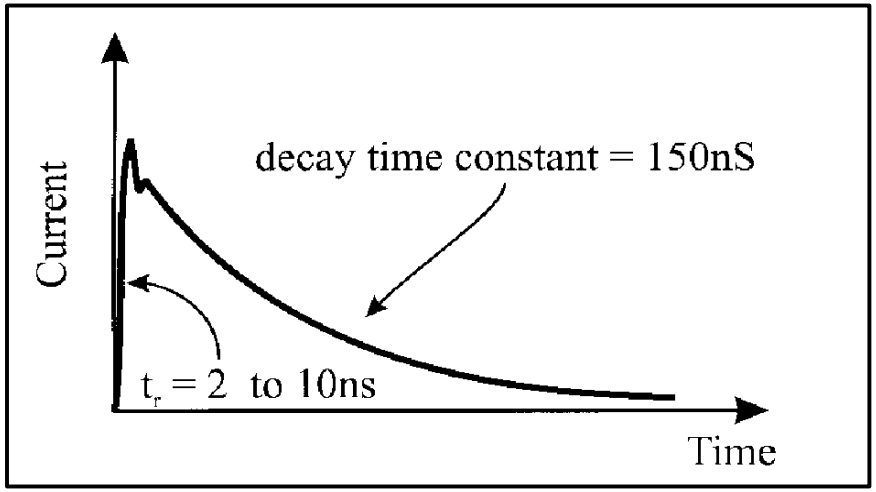
- High current and high voltage are typical for and ESD event
- On-chip protections are mandatory in order to preserve chip functionality

Charge transfer modeling

- ESD voltage levels vary drastically with atmospheric conditions
- A source of known and controlled ESD is needed in order to reproduce the discharge in lab → ESD simulator
- Stress level must be the same for any and all commercial ESD simulators
- ESD simulators should be able to reproduce the characteristics of the charge transfer processes which occurs in the real world
- Three different models have been developed
  - Human body model (HBM)
  - Machine Model (MM)
  - Charged device model (CDM)

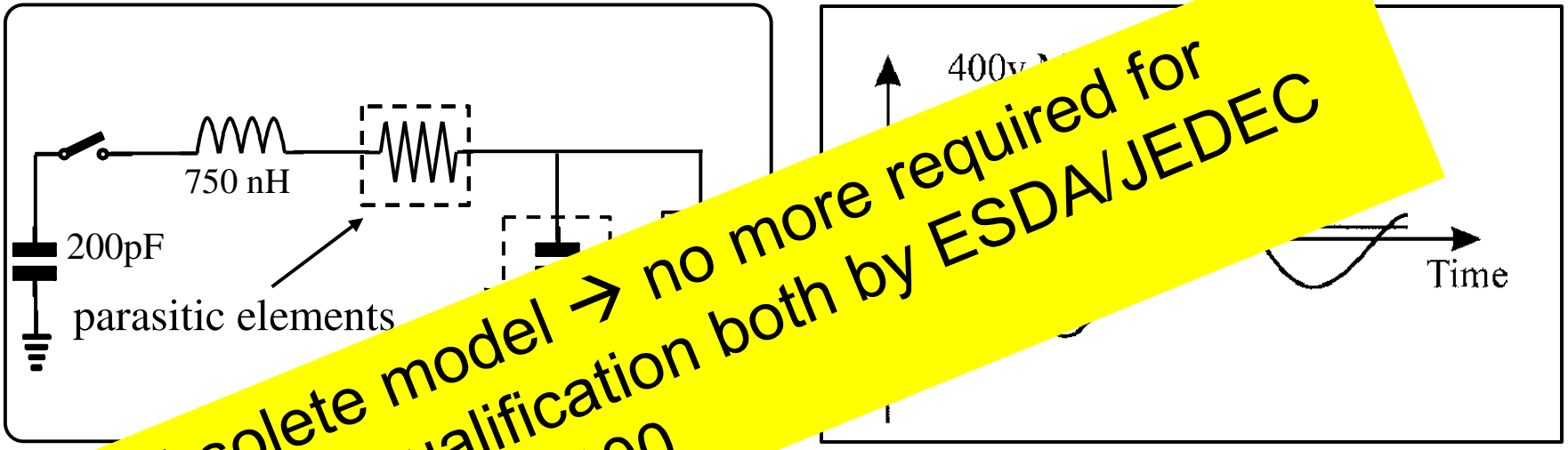
HBM: Human Body Model





- The Human Body Model attempts to reproduce an ESD waveform generated by the discharge of a human being through a low impedance path
- Rise time <10 ns, decay time @ 150 ns

MM: Machine model

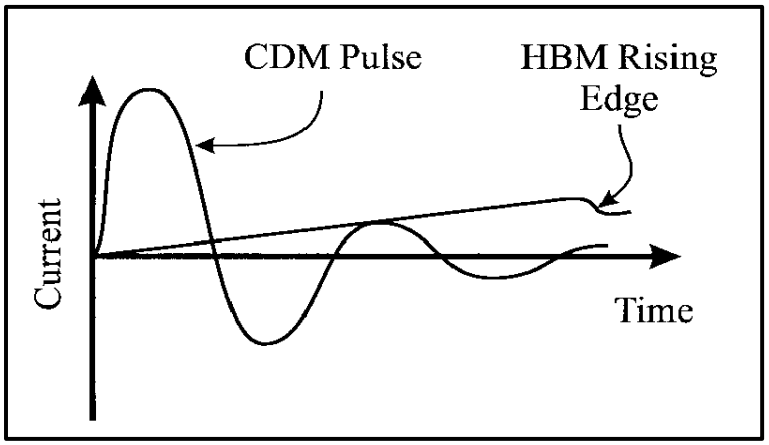


Obsolete model → no more required for product qualification both by ESDA/JEDEC and by AEC-Q100

- The model attempts to reproduce an ESD wave generated by the discharge of a charged machine
- It reaches higher current levels for a given discharge voltage compared to HBM

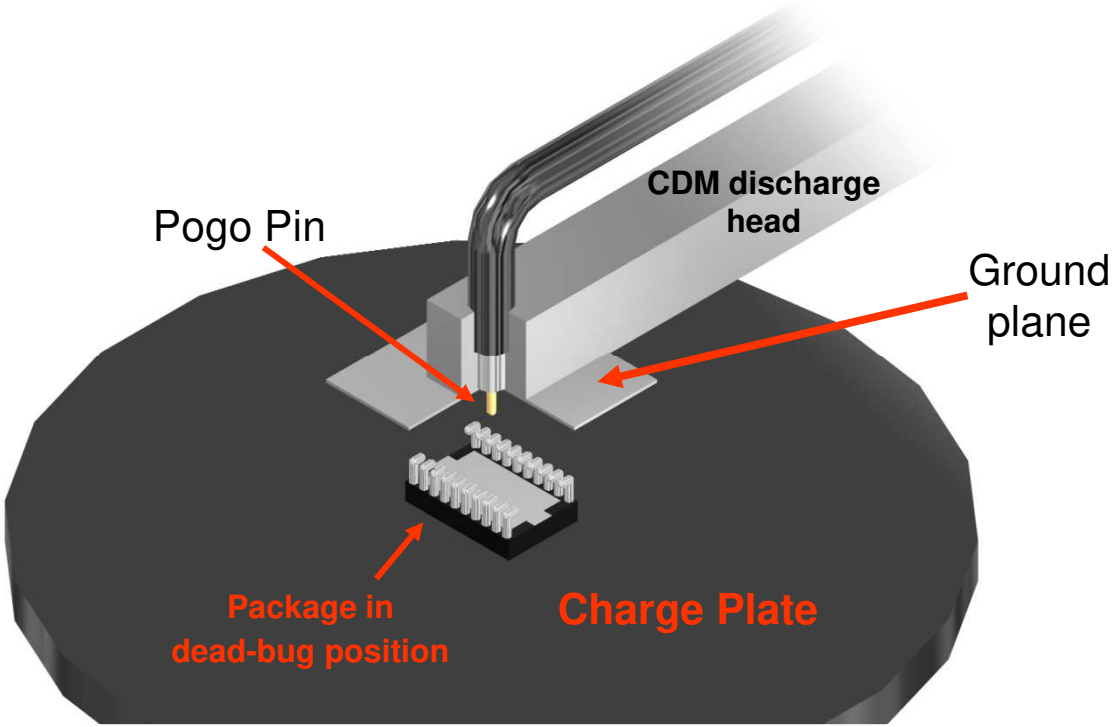
CDM: Main characteristics

- Discharge time: ≈ 0.5/1ns (tr ≈ 100/400ps)
- High current peak: till 20A for 1kV pre-charge
- Complete IC involved:
  - Full IC protection strategy must be implemented
  - Internal nodes could be critical (coupling capacitances)
- Stress dependent on parasitic elements
  - Package
  - Bond wires
  - Bond pads
  - Substrate
  - Well diodes



- High current injection phenomena → Forward recovery effect

CDM: tester description



- Package in dead bug position
- Pre-charged by charge plate induction
  → Mobile charges are on the device only
- To create the ESD event a probe touches down one pin of the device.
- Minimum RLC circuit simulating real word conditions.
- L & C of the device impact on the current waveform

Device vs. System level tests: two Worlds of ESD

Device level

- IC's can be exposed to ESD during assembly
- ESD on-chip protection is used to protect IC during manufacturing
- Qualification of IC by (JEDEC / ESDA / AEC) standards:
  - Human Body Model (HBM)
  - Machine Model (MM)
  - Charged Device Model (CDM)
- Stresses are applied to all pins of the IC

System level

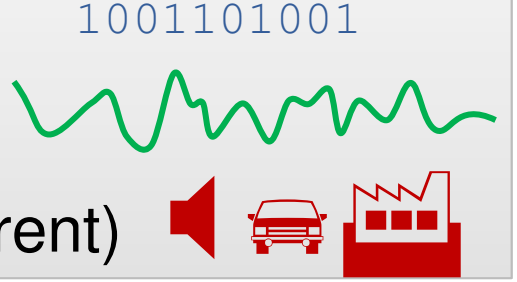
- ESD is also a threat for PCBs and (final) products
- Dedicated diodes are added on the PCB in order to survive such threats
- System level ESD standards:
  - IEC 61000-4-2
  - ISO 10605
- Stresses are applied to specified locations of the application,
  BUT: Stressing to component pins is prohibited!

Contents

Introduction to HV technologies

HV technologies combine:

- Digital signal processing
- Analog signal processing
- Power (high voltage and/or high current)

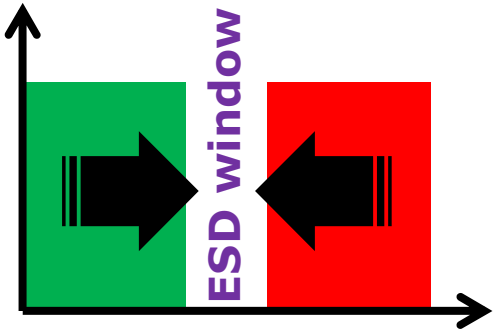


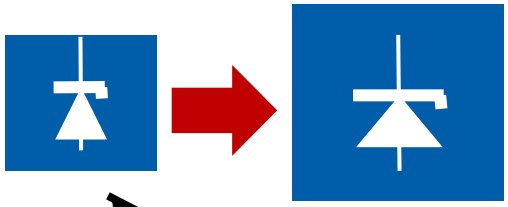
HV technologies are typically used for:

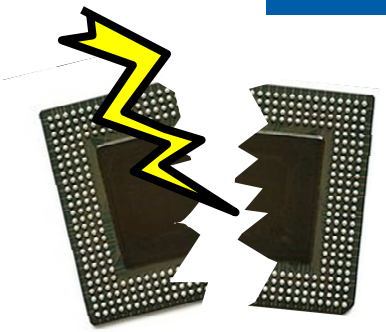
- Power control circuits
- Power conversion circuits
- Power drivers (LED, LCD, PDP, Audio)
- Automotive applications
- Sensor and actuators driving circuits

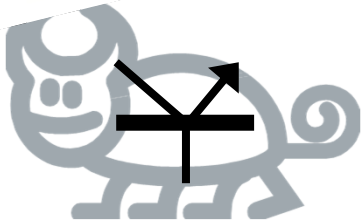
Challenges of HV design

- Main challenges typical of HV technologies
  - Narrow ESD Design Window
    → ESD window tends to vanish
  - Large Area Solutions
    → Higher clamping voltage requires larger device area
  - Fragility of typical HV devices
    → Ballasting is not effective like in CMOS technologies
  - Increased risk of parasitic BJT (both NPN & PNP) possibly inducing LU issues





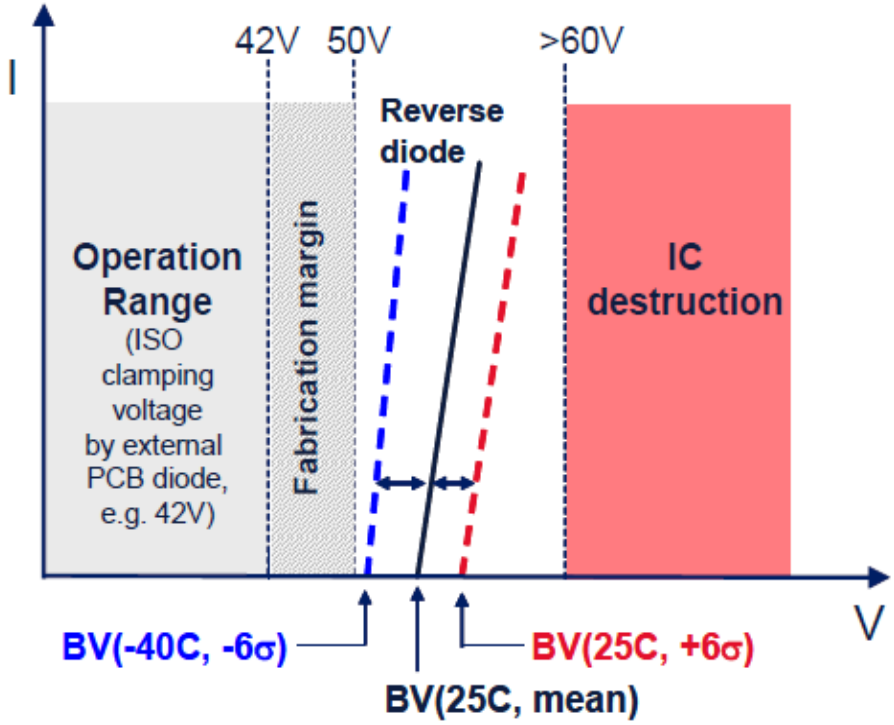




ESD window concept in HV technologies

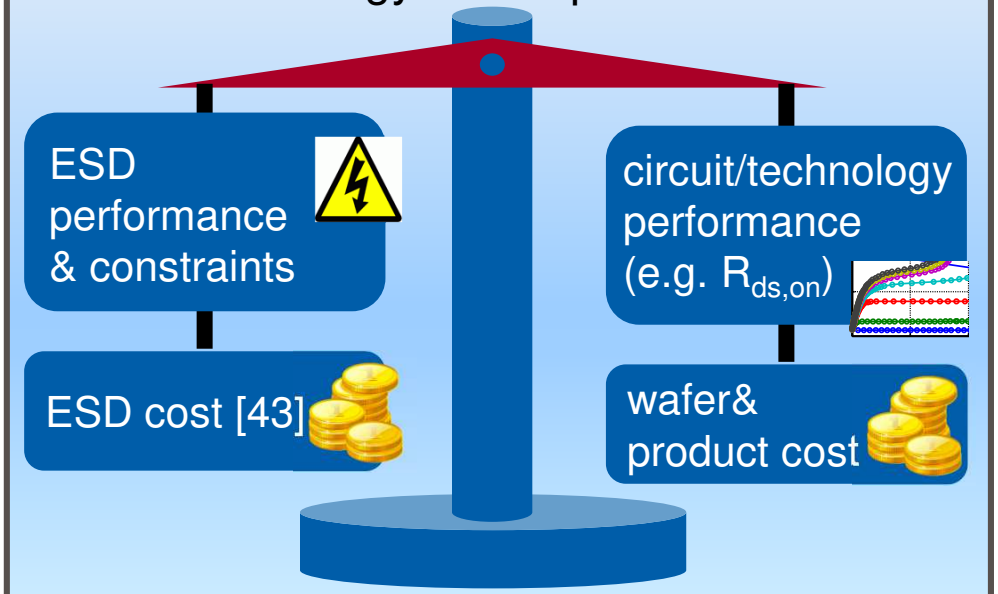
- Two concurrent trends in the HV world
  - Typical for HV MOS: trigger voltage ↓ , if V_{gs} ↑
  - External constraints ask for increasing voltage capability

→ **ESD window tends to vanish**

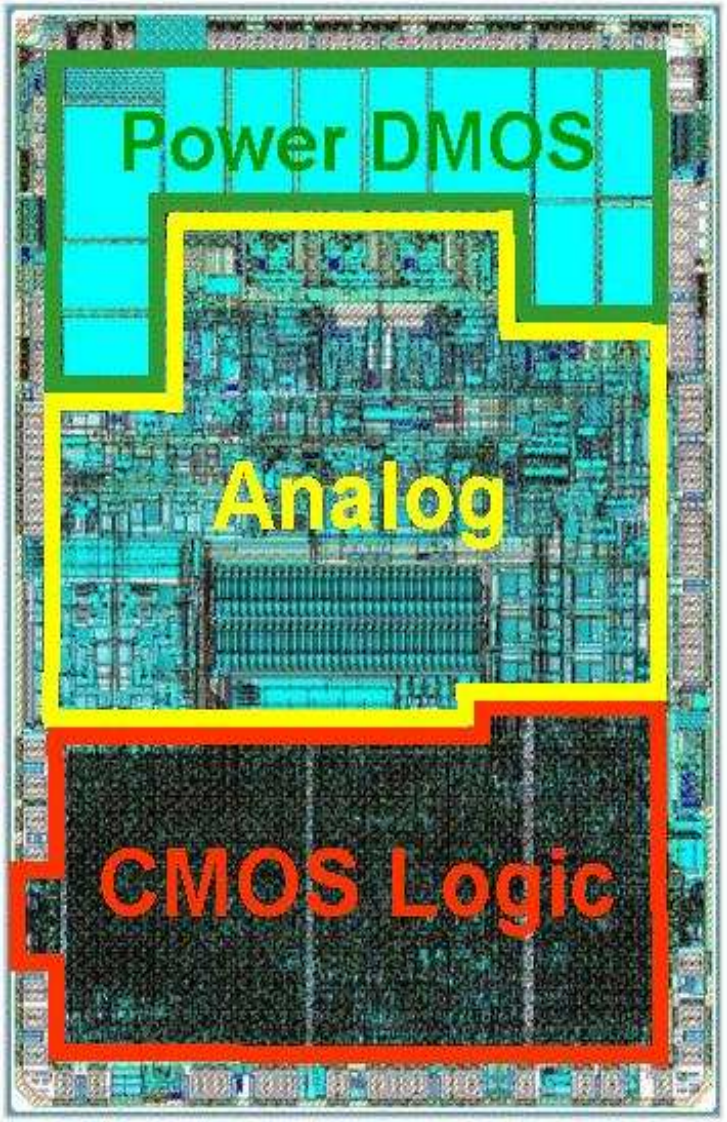


Important considerations:

- ESD protection development concurrent with technology development

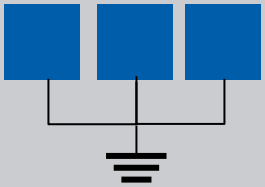
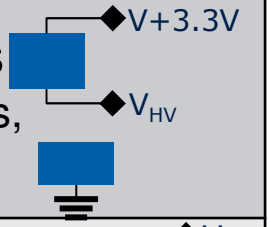
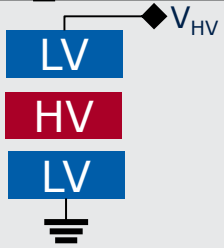


Example of chip partitioning



- DMOS:
  - Switches
  - Voltage regulator
- Analog:
  - Gate drivers
  - Diagnostics
  - Analog I/O
- CMOS:
  - Digital control
  - Digital I/O

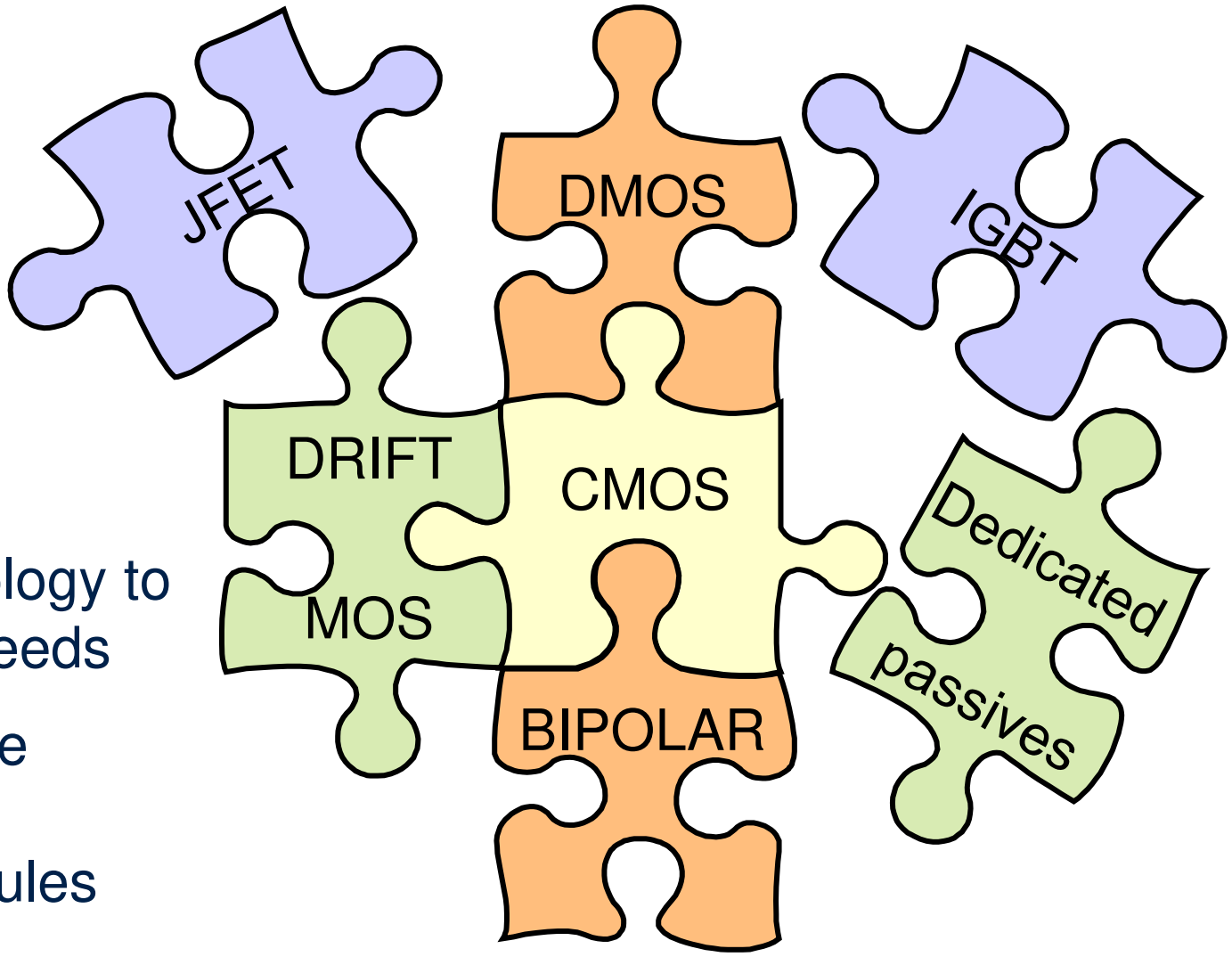
What is special for high voltage ICs?

CMOS Integrated Circuits	VERSUS	HV Integrated Circuits
Standard I/O cells & libraries 		Custom analog I/O cells 
Supply voltage of different domains in limited range V_{CC1}= 1.8V, V_{CC2}= 1.8V, V_{CCIO}= 3.3V		Supply & pin voltages of different domains vary largely V_{CC}= 3.3V, V_{sup}= 12-40V, V_{clamp}= 60V
All circuit blocks ground referenced 		Floating circuit blocks e.g. high side driver circuits, supply by charge pump 
		Analog circuits with LV devices in HV domain 

HV technologies: a flexible world

Modularity:

- Adapt technology to application needs
- Add & remove devices and process modules



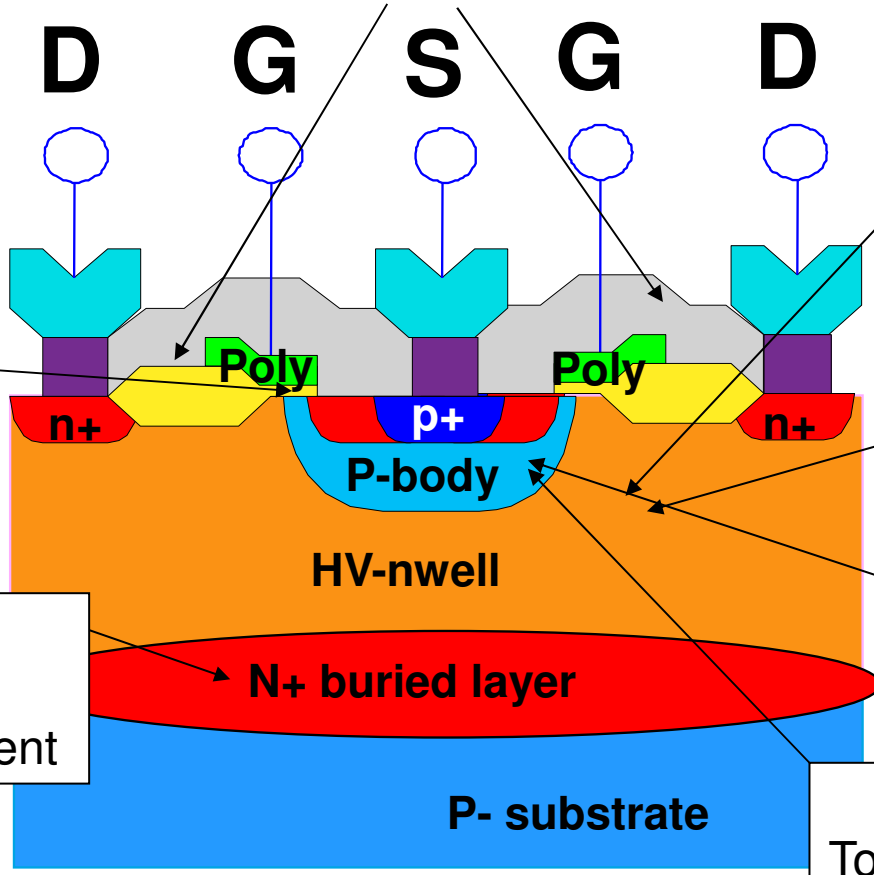
BCD – Definitions & Motivations

- High Voltage technologies → commonly referred to as Smart Power or BCD technologies
  - B = Bipolar
    → Typically used for precise analog blocks
  - C = CMOS
    → Typically used for digital blocks
  - D = DMOS
    → Typically used for HV & Power stages

- New challenges in the Smart Power world
  - Analog design at low voltage & power levels → ***Noise issues***
  - Power devices getting smaller → Increasing ***power dissipation*** by unit area

Power-MOS: architecture engineering

CMOS or Dedicated isolation:
(LOCOS vs. STI)
For Field-Plate realization



Gate oxide thickness:
CMOS (LV) or
Dedicated (HV)?

Drain engineering:
Doping of HV-Nwell

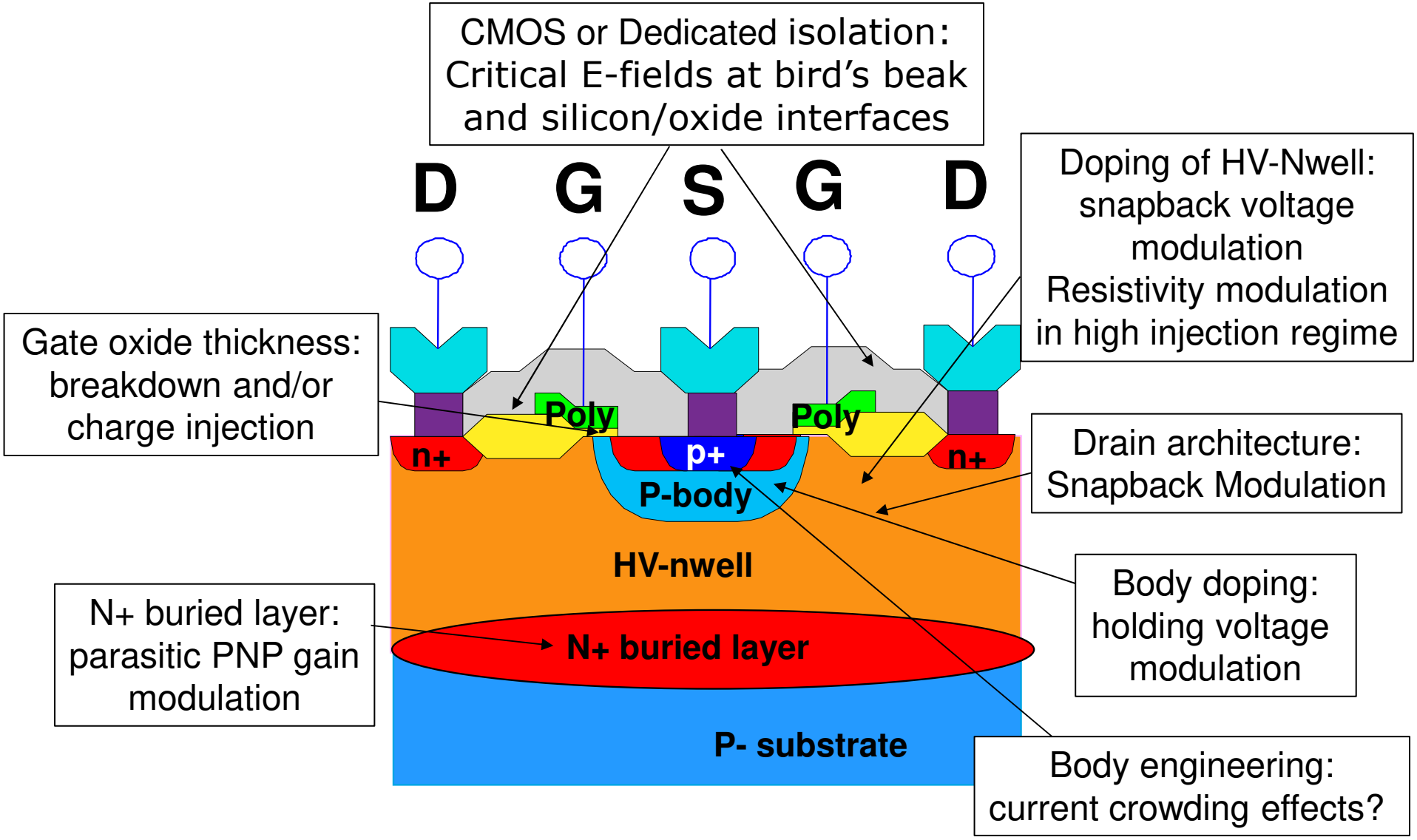
Drain engineering:
STD well or
RESURF on BL?

N+ buried layer:
Recommended for
High voltage/High current

Body realization:
Drift or DMOS?

Body engineering:
To improve ruggedness
Well doping or pocket?

Power-MOS: the ESD performances

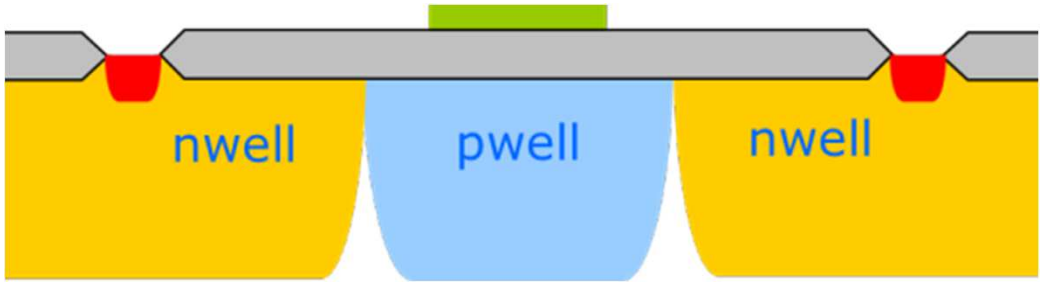


Junction vs. Deep Trench Isolations

- HV transistors need to have high Breakdown voltage vs. substrate

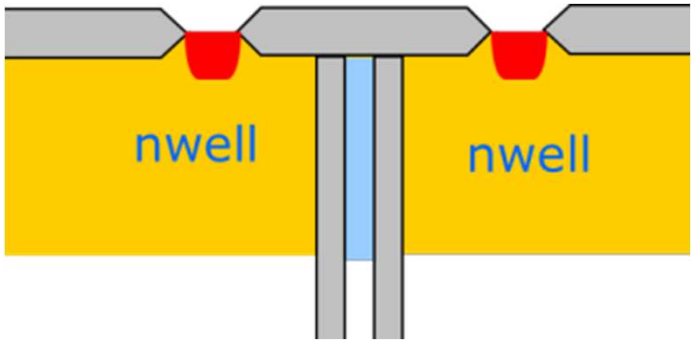
Junction Isolation

- Low doped region implemented to sustain the HV requirement
  - ↑ Pro: No extra-steps required
  - ↓ Con: Large area required
  - ↓ Con: Parasitic lateral bipolar & MOS transistors to be considered carefully



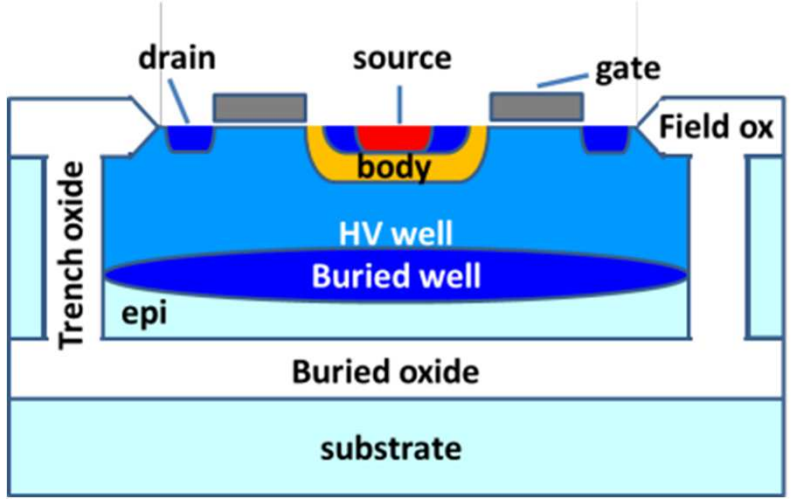
Deep Trench Isolation

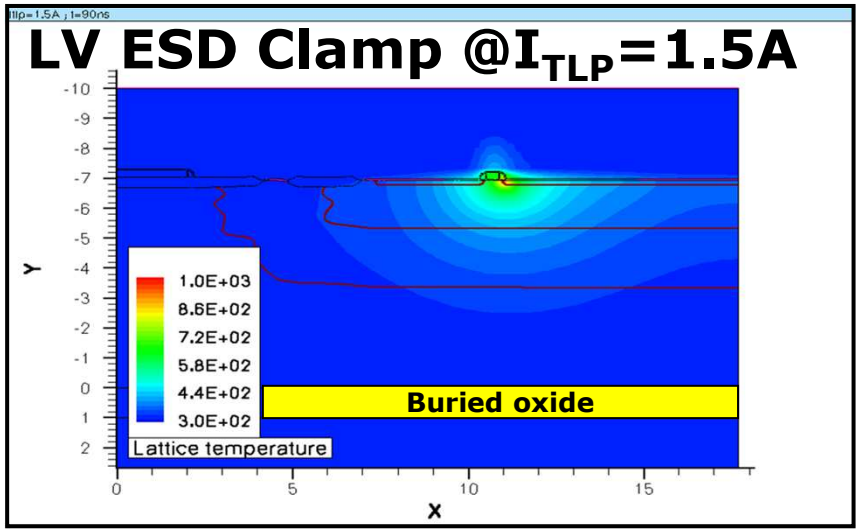
- High BV guaranteed by oxide-filled deep trench (depth ~ several um) surrounding the devices
  - ↓ Con: Dedicated etch required
  - ↑ Pro: More compact layout
  - ↑ Pro: Better LU performances expected due to inhibition of parasitic lateral bipolars



HV SOI: Pros & Cons

- Different SOI approach adopted compared to CMOS → much thicker active Si layer epitaxy (2-10um)
- Main pros
  - bipolar parasitic inhibition
  - HV devices (>100V) available



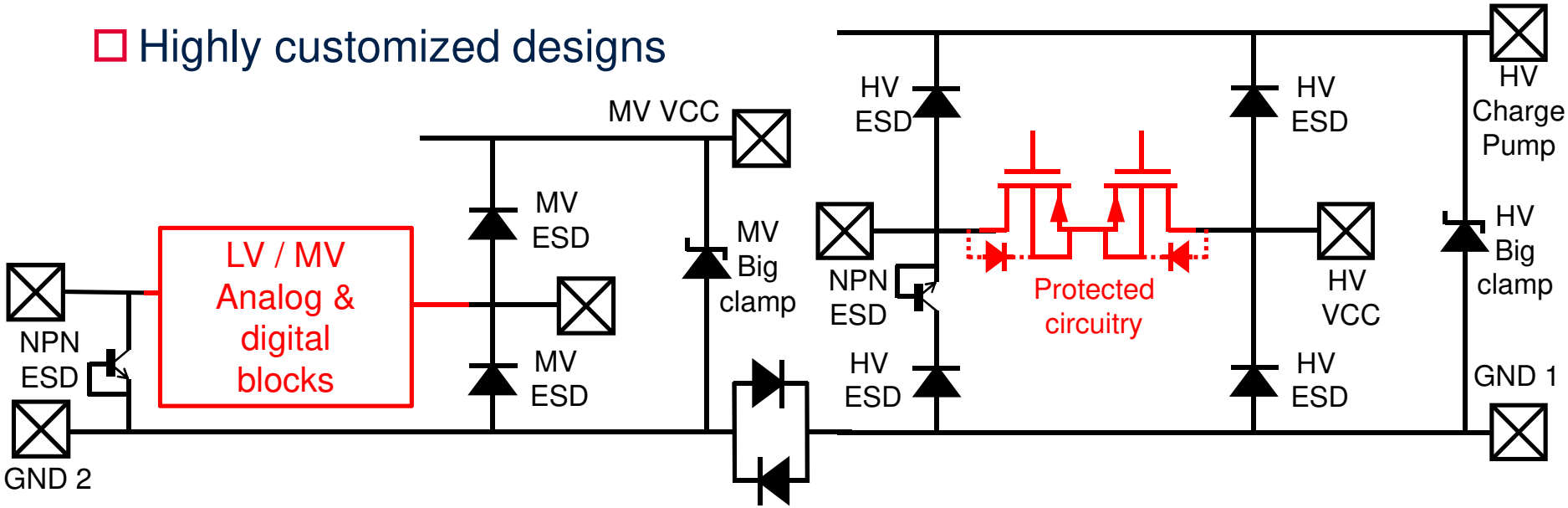


- ESD current flow and power dissipation confined in surface region → ESD performances not impacted
- EOS: increased power dissipation to be carefully considered

Contents

ESD networks in the HV world

- Typical complexity of an ESD network in the HV world: ***very high***
  - Different power domains (different voltage ratings) ***simultaneously*** present
  - Analog circuits → possible uncontrolled alternative ESD paths
  - LV transistors used in HV domains
  - Layout-dependent parasitic bipolar transistors
  - Highly customized designs

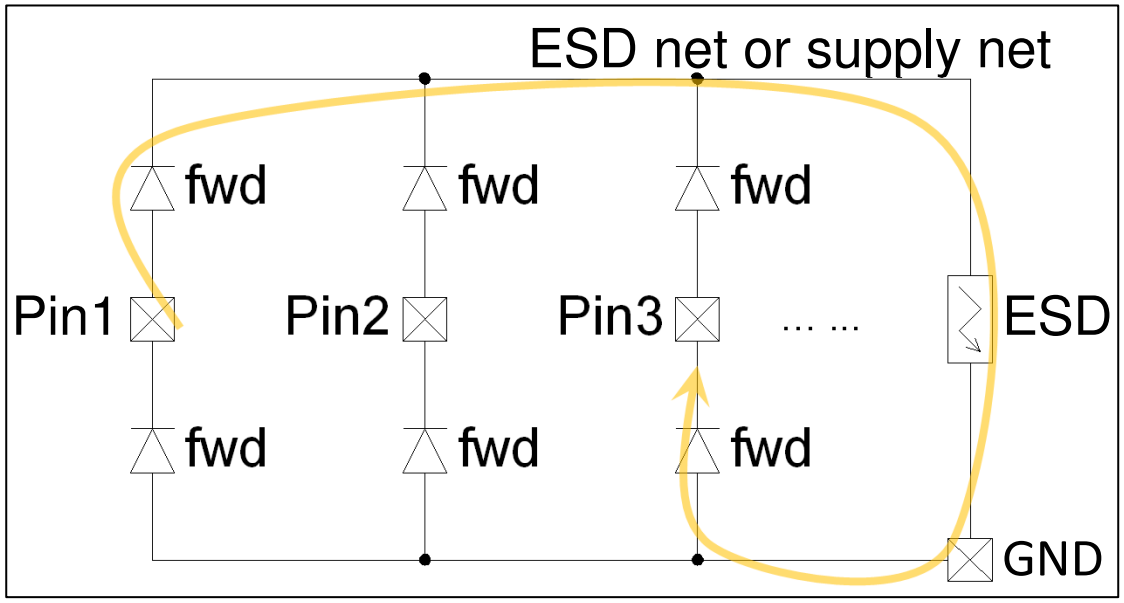


ESD-Robust design flow in Smart Power ICs

- Standardized protection schemes can be adopted for logic I/O pins only
- Analog stages, negative pins, power blocks require a customized approach with ad-hoc solutions inside the protection network general concept
  - Deep knowledge of sensitive circuits is mandatory
  - Strict control of internal nodes must be pursued
  - Self-protected circuit blocks can be identified
  - Tolerance vs. parasitic transistors must be always double-checked
- Circuit simulation as a tool for ESD robustness prediction
  - Reliable for HBM on I/O circuits
  - Far less consolidated for CDM
  - Key to implement a robust ESD network for System-Level ESD requirements

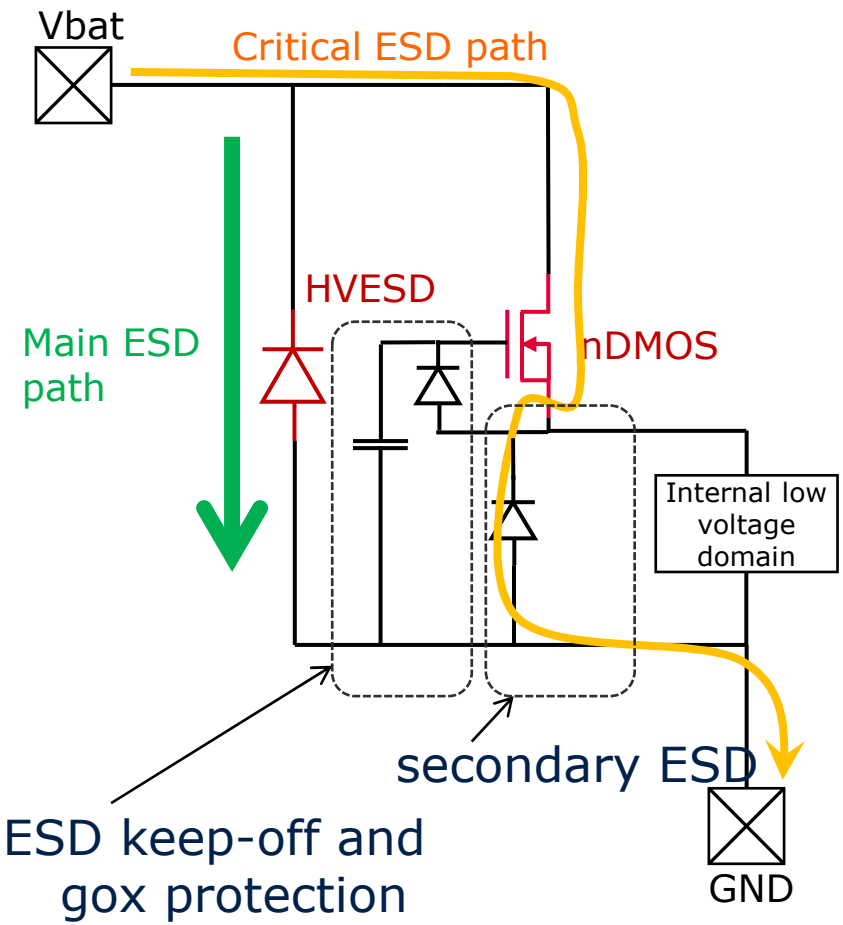
General HV ESD Concepts /1

- Basic ESD concepts and networks which optimize area efficiency
  - Be aware of forward recovery effect, low leakage floating node, metal interconnection routing, etc.



Dual-diode concept origin from CMOS can be also applied for HV ESD protection

General HV ESD Concepts /2



- Voltage regulator involving mixed voltage ESD design: stack LV and HV devices
  - nDMOS can pass significant ESD current to internal low voltage domain
  - ESD keep-off e.g. capacitor suppress dynamic turn-on of nDMOS
  - Secondary ESD protection required to protect internal domain

HV protections approaches: Bipolar-based

- Several approaches already presented to built effective ESD protections based on breakdown or bipolar actions
- Typical solutions: NPN, SCR, PNP, diodes
  - ↑ Pro: Area effective
  - ↑ Pro: Local clamping possible → reduced impact of parasitic metal resistances
  - ← May need dedicated steps
  - ← Tight process control required (esp. during process transfer to different fabs)
  - ↓ Con: Reduced ESD window
  - ↓ Con: Deeply impacted by conductivity modulation → difficult to obtain triggering uniformity

HV NPN & SCR /1

- Snapback-based (NPN & SCR) ESD protections show superior performances → higher area efficiency
- Main design issues of HV snapback protections
  - High conductivity modulation (Low doped regions)
  - High local E-field in singular points (e.g. bird's beak)
  - Isolated Body regions

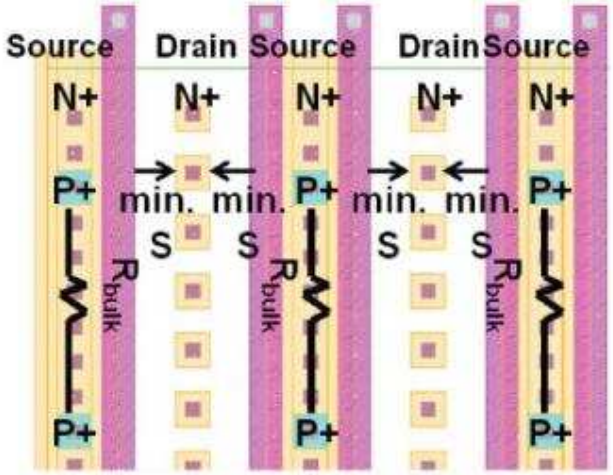
    → Risk of early filamentation (non-uniform current flow)
  - Triggering voltage engineering ***mandatory***

    → Risk of too high or unstable triggering (ineffective protection)
  - Holding voltage control

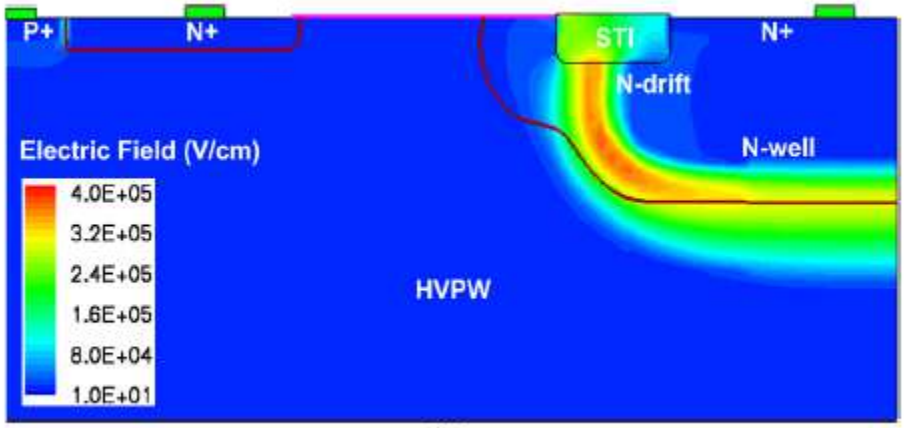
    → LU triggering risk if holding voltage < supply voltage (unacceptable in several application fields)

HV NPN & SCR /2

- Several techniques proposed to improve current uniformity and snapback control
  - Dedicated deep implants
  - Body resistance modulation

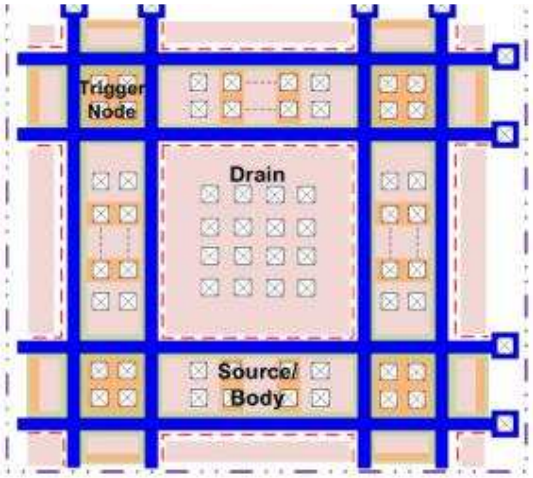


Courtesy of J. H. Lee [34]



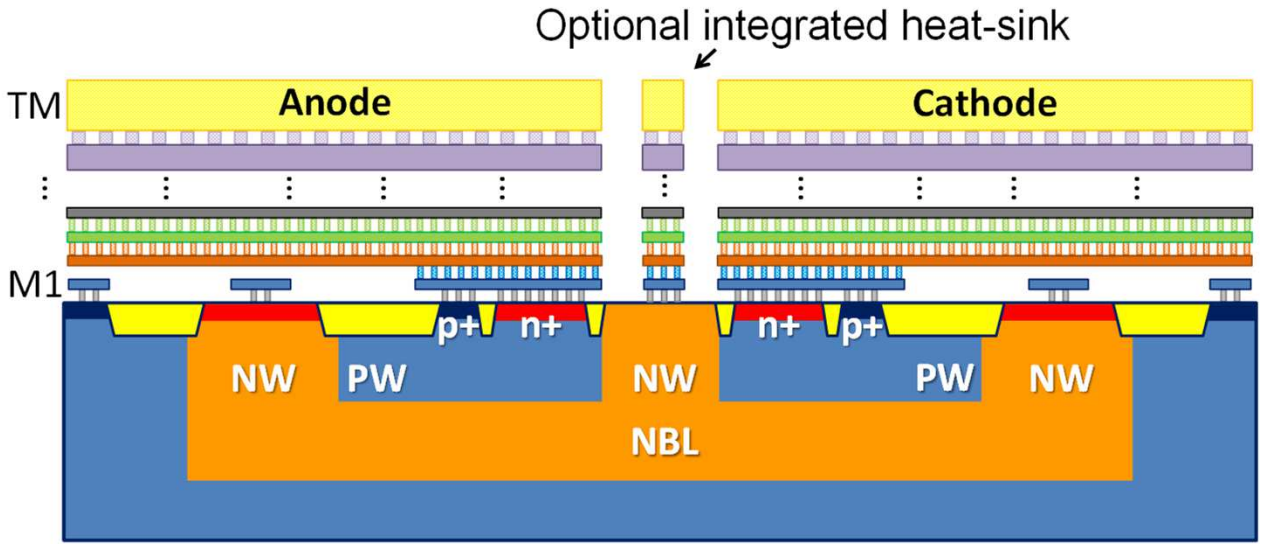
Courtesy of T. H. Lai [31]

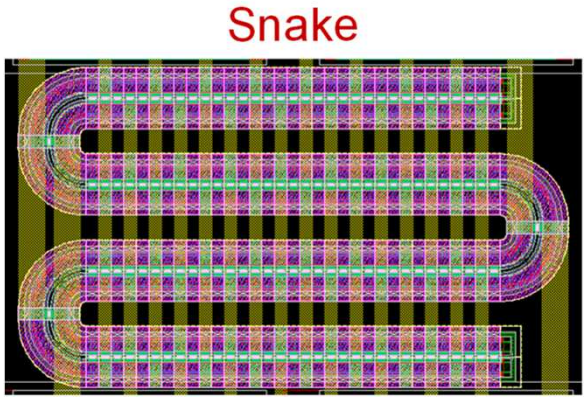
  - Triggering circuits embedding in HV transistor



Courtesy of W. Y. Chen [12]

BI-SCR - example



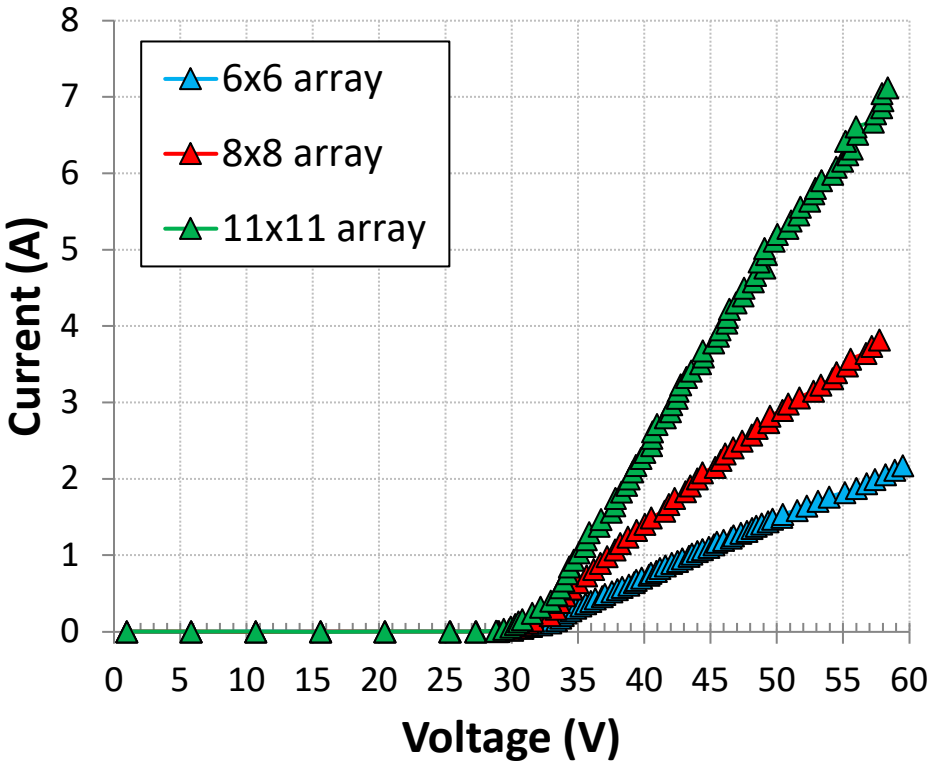


Courtesy of A. Tazzoli [73]

- Bi-directional SCR are often ad-hoc developed to implement on-chip system level protection cell
- Main characteristics and requirements:
  - Tunable Breakdown voltage
  - Low leakage (pA) & Low capacitance (pF)
  - Able to handle component- & system-level ESD stresses and also longer EOS (e.g. surge events)

HV PNP

- Specific concerns defined by safety-driven issues (e.g. automotive):
  - holding voltage must be higher than the application operating voltage and max rating
- Suitable alternative to standard NPN → ***PNP protections***
- Main advantages
  - No (or reduced) snapback
  - No ballast required
  - Matrix layout easily implementable
- Main limitations
  - Low Ron difficult to be obtained



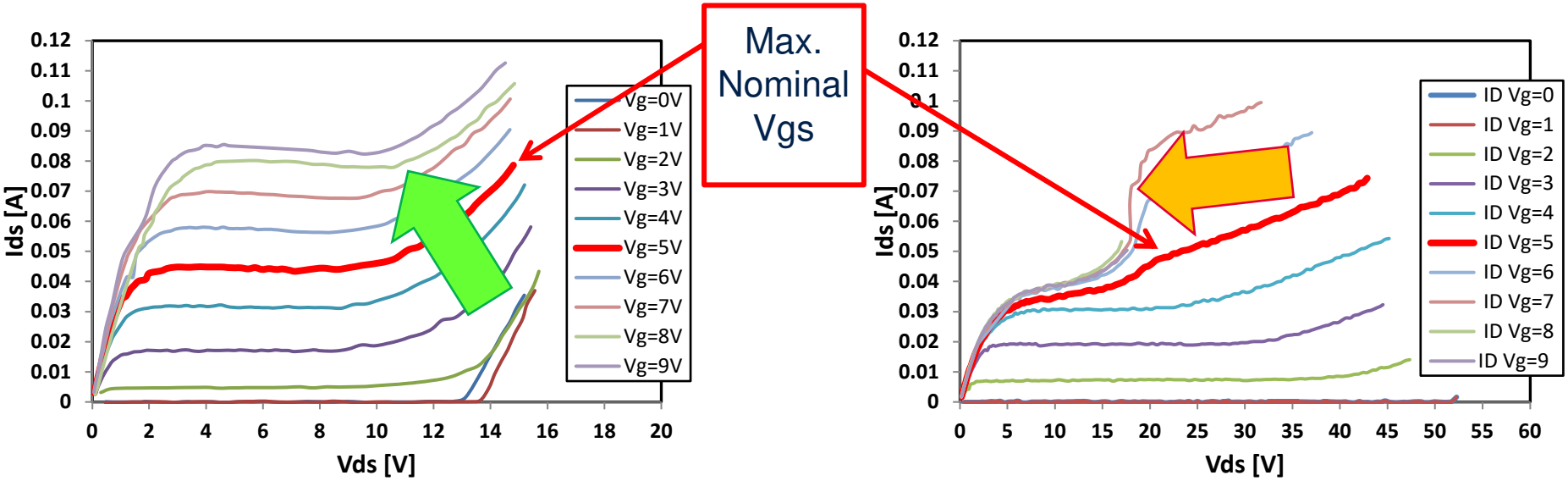
HV protections approaches: MOS-based

- High performing HV MOS already available in Physical Design Kit → suitable to build effective protections
- Two possible triggering mechanisms: dynamically- vs. statically-activated MOS
  - ↑ Pro: Standard components used (no extra development effort)
  - → Remote clamping implemented → parasitic metal resistances to be minimized
  - ↓ Con: Large area required

Dynamically-activated	Statically-activated
↑ Pro: less impacted by ESD window constraints	↑ Pro: not prone to mistriggering due to dV/dt effects
↓ Con: Possible interaction with device functionality and EMC testing	↓ Con: Reduced ESD window for statically triggered clamps

Active clamp Safe Operating Area

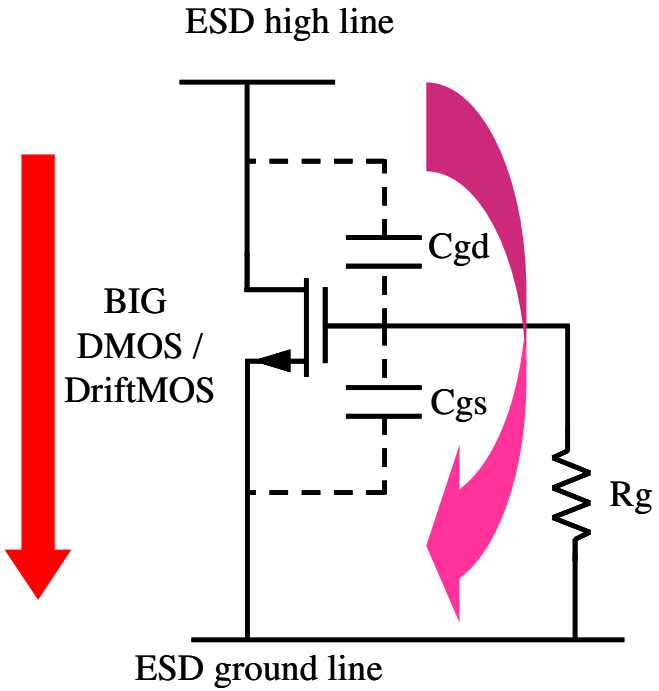
- HV MOS SOA data useful to optimize clamp performances
- Quasi-static IV curves at high Vgs & Vds (not impacted by thermal effects) obtained with 100ns-TLP
- Dedicated ESD SOA can be different from standard operating conditions (defined by reliability concerns)

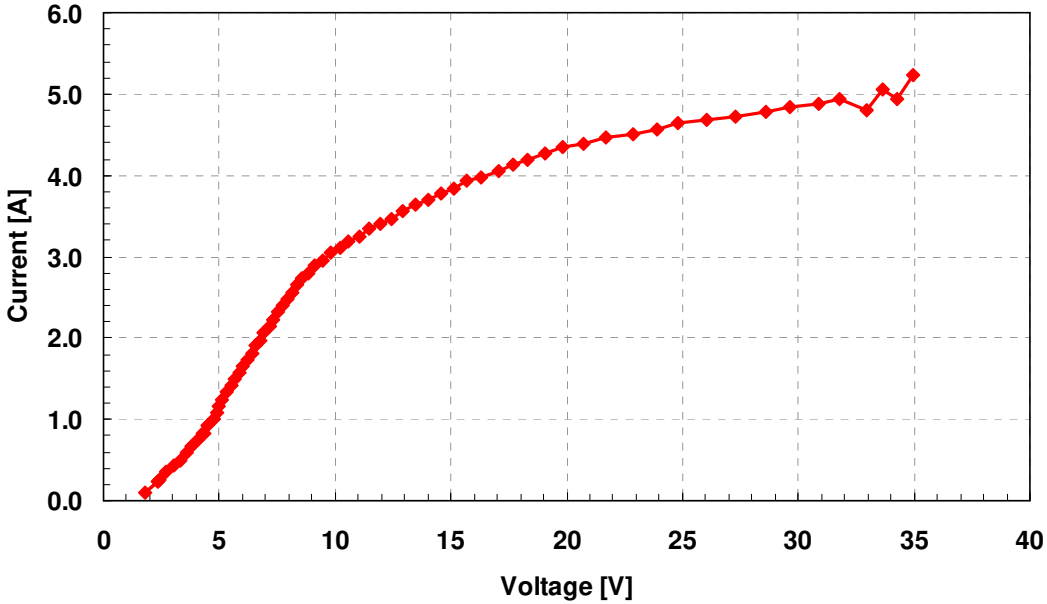


- Pro: overdrive beyond nominal condition can improve current capability
- Con: excessive gate voltage may induce premature snapback

Dynamically activated HV clamps

- High Drain/Gate capacitance of HV DMOS/DRIFT MOS allows to build efficient dynamic clamps





- Easily tunable clamping voltage → low values achievable
  - Gate coupling ratio dependent on HV-MOS implementation
    → Typical Vgs/Vds ratios (with pulsed Vds) in the range 1/15 – 1/5`

Dynamic clamps: design guidelines

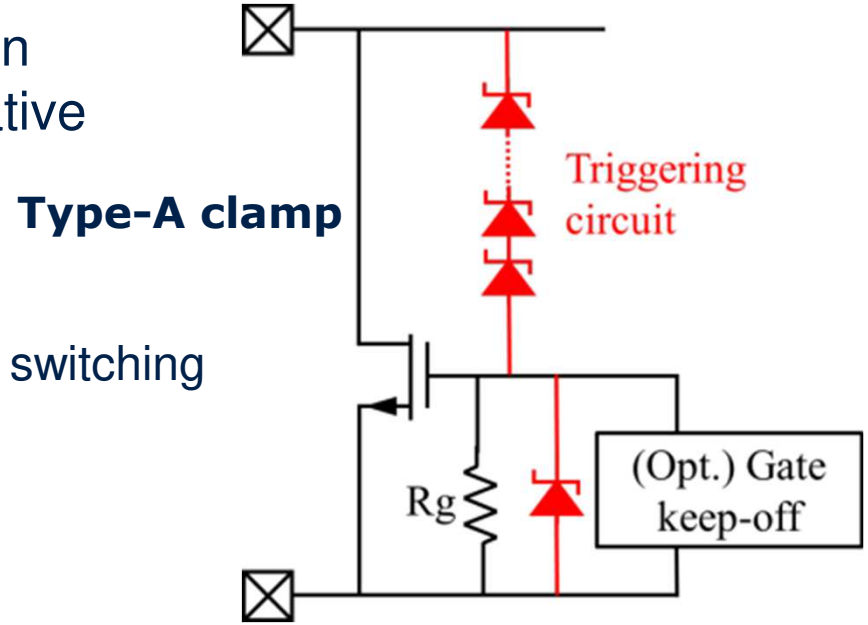
- **Development targets of dynamic clamps**

1. Limit drain ESD voltage (e.g. 70% of AMR)
   - To reduce IC voltage stress
   - To increase voltage margin for ESD network (diodes, parasitic metal resistance…)
2. Maximize ESD gate overdrive (> standard operating SOA)
   - High MOS current capability, minimized ESD area

- **Dynamic clamps reduce constraints on protected circuitry**
  - Strong optimization of active performances
  - Special transistors (IOMOS) may not be needed

Voltage triggering of active clamps

- Dynamically triggered active clamps main drawback: ***unintended turn-on*** in operative condition
- Main root causes:
  - Noisy supply lines caused by power stage switching
  - EMC coupling of disturbs
  - Hot plug of HV supply lines



- Statical trigger can be implemented with dedicated circuits (Zener chain…)
- Careful tailoring of the gate circuitry needed
  - Triggering circuit optimized to turn-on the clamp considering statistical process spread and voltage capability
  - Gate resistance → trade-off between disturb immunity (low Rg required) and suitably low current consumption (high Rg welcome)

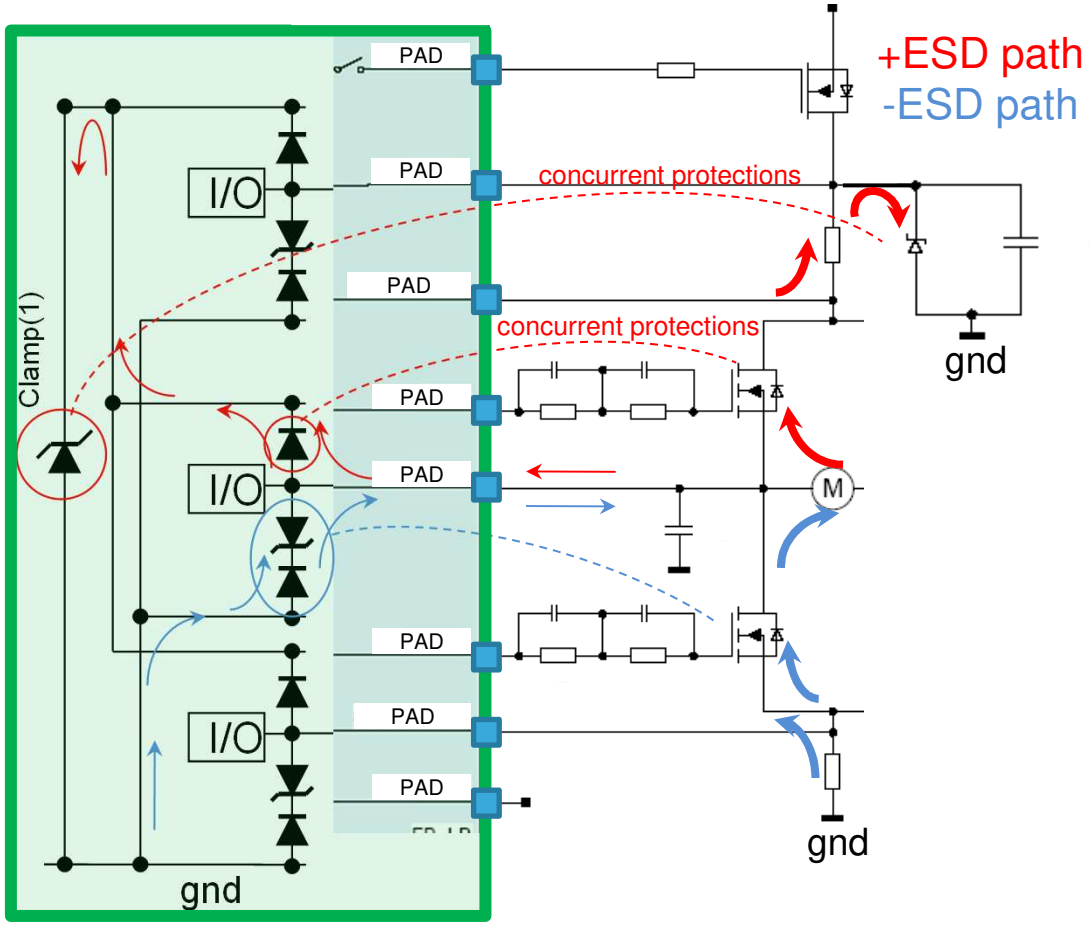
Simulations of HV active clamps

- Active clamps implemented with standard components
- No conduction in Breakdown and Snapback mode typically considered
- Two scenarios for circuit simulations:

- HV transistors are biased within the **standard operating conditions**
  - ↑ Pro: No dedicated models needed
  - ↑ Pro: No dedicated boundary conditions needed
  - ↓ Con: Safe and conservative clamp implementation is possible

- HV transistors are biased within the **ESD SOA**
  - ↓ Con: Dedicated models needed including multiplication regions
  - ↓ Con: Special boundary conditions needed to define safe regions
  - ↑ Pro: Strong area optimization is possible

Designing for System-Level ESD robustness /1



- External circuitry plays a major role
- ESD pulse may be clamped and/or distorted by external elements:
  - Discrete components (capacitors, PowerMOS…)
  - Board parasitics
- A simulation-based approach should be used to correctly design the best ESD solution for each pad

Designing for System-Level ESD robustness /2

- The choice of the right ESD protection approach is key factor to ensure the right system-level robustness
  - Each on-chip protection should not by-pass the off-chip elements
  - Off-chip devices should work in their most effective working points
  - Each ESD approach has specific drawbacks to be considered

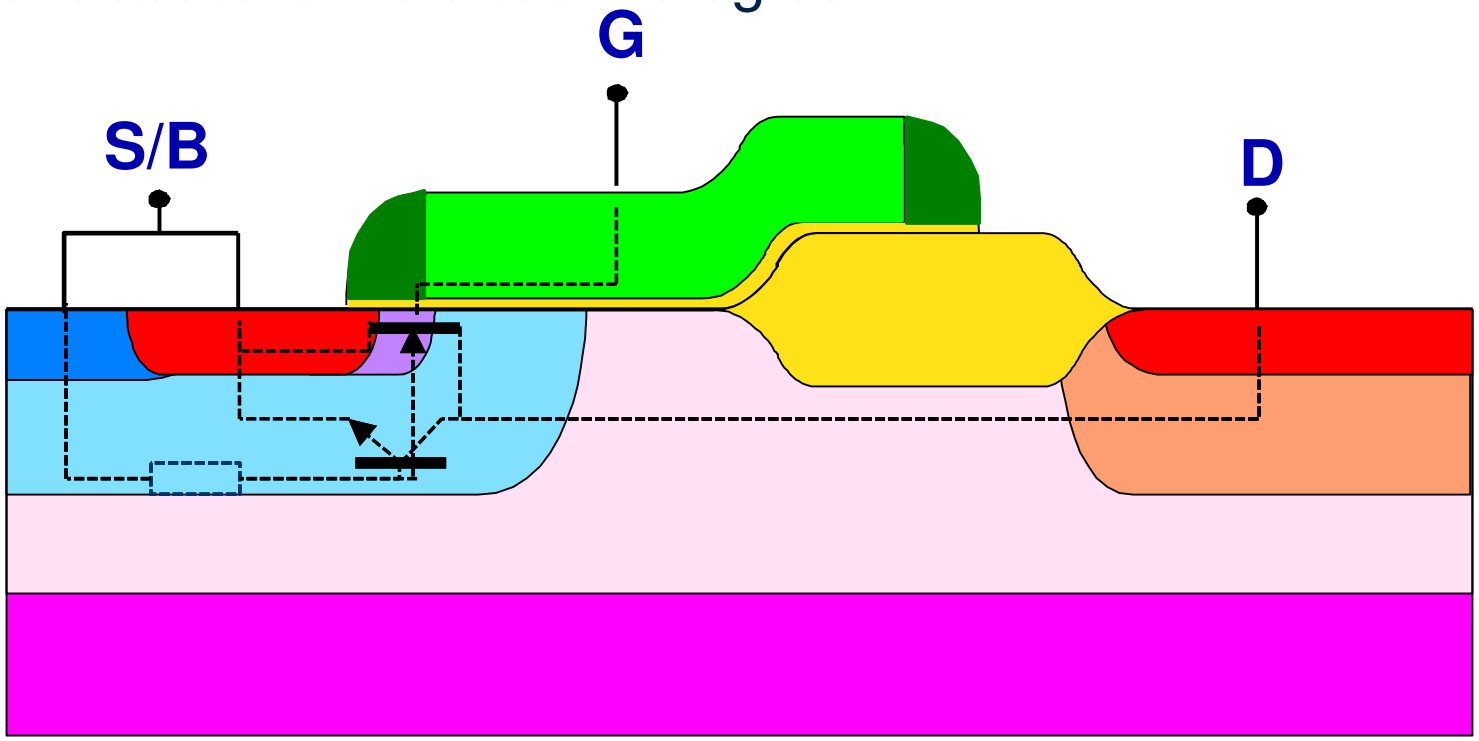
Static-MOS based	*Dynamic-MOS based*	*Snapback based*
■ High clamping voltage may impact voltage capability of protected stages	■ Low clamping voltage may impact off-chip protection (e.g. external capacitors show higher energy capability at high voltage)	■ Deep snapback may be risky for powered-on stresses

- There is no single and optimal solution fitting all requirements

Contents

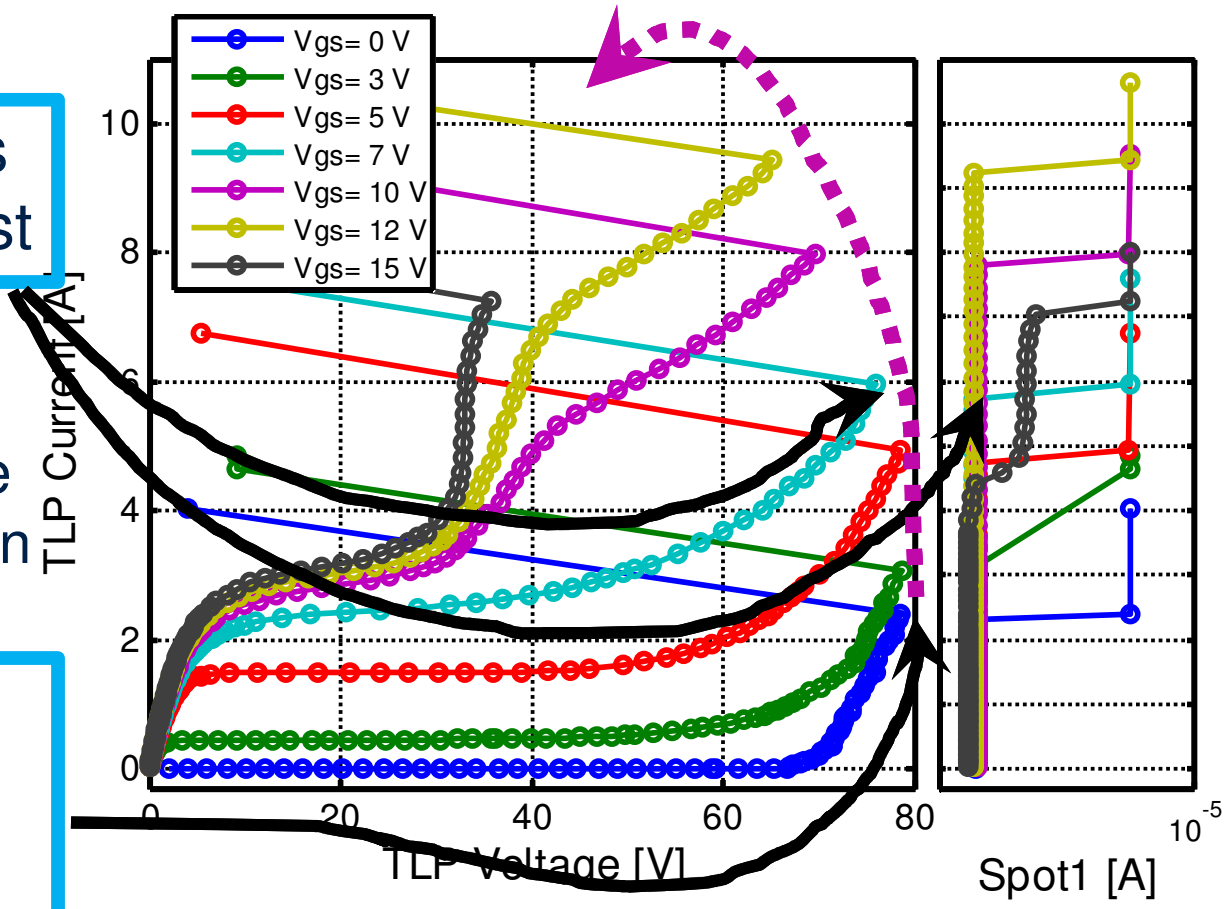
Bipolar parasitics (device internal) /1

- N-LDMOS includes a parasitic bipolar NPN
- Triggering of this bipolar usually destroys the device
- Ballasting (*drain-contact-to-gate-space*) is not effective in contrast to CMOS technologies



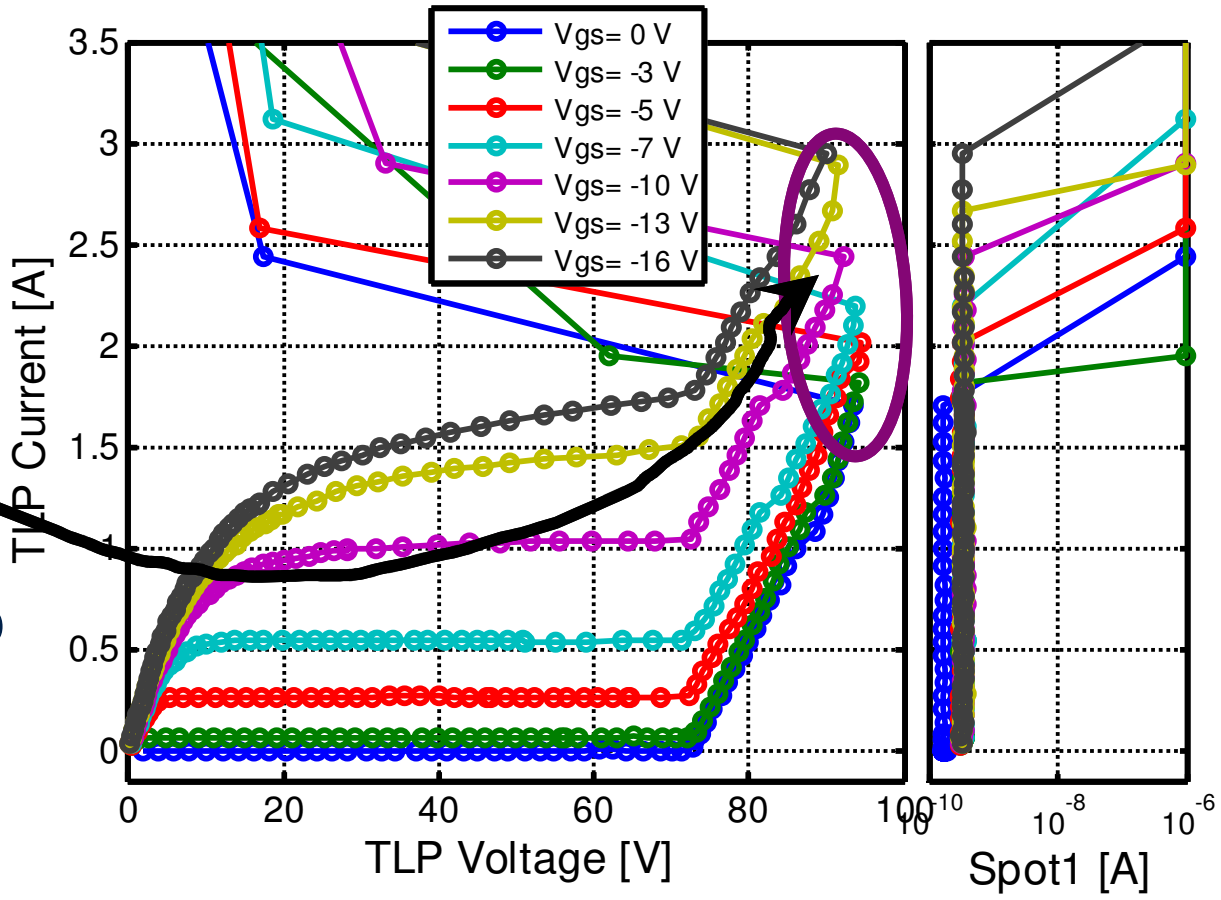
Bipolar parasitics (device internal) /2

- Triggering of bipolar NPN leads to snapback
- Usually nLDMOS is not snapback-robust
- Transient SOA characteristics: method to investigate device performance in detail
- Usually trigger point (V_{t2}, I_{t2}) depends on V_{gs}



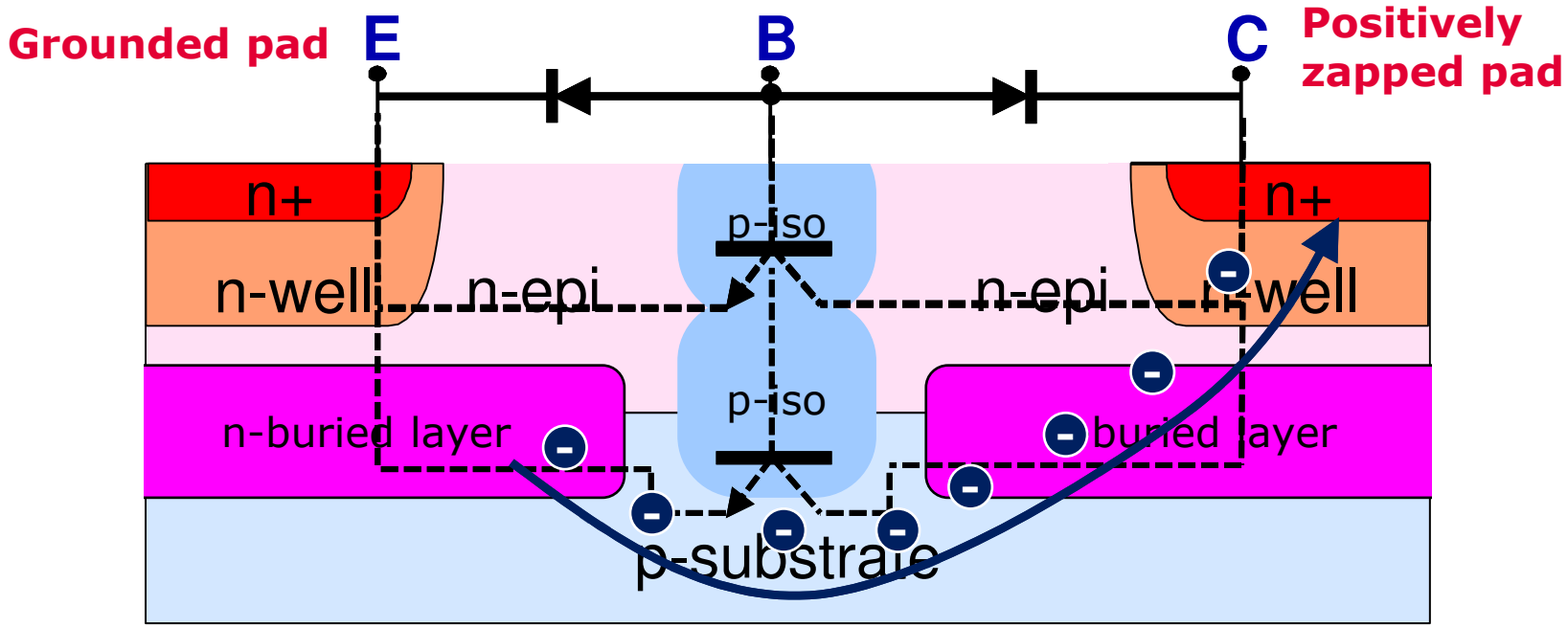
Bipolar parasitics (device internal) /3

- PMOS devices have parasitic PNP
- Parasitic PNP is usually much more robust than NPN
- Less dependence on V_{gs}
- PNP does not snap back as „easily“ as NPN



Bipolar parasitics (between devices) /1

- Cross-section of substrate NPN

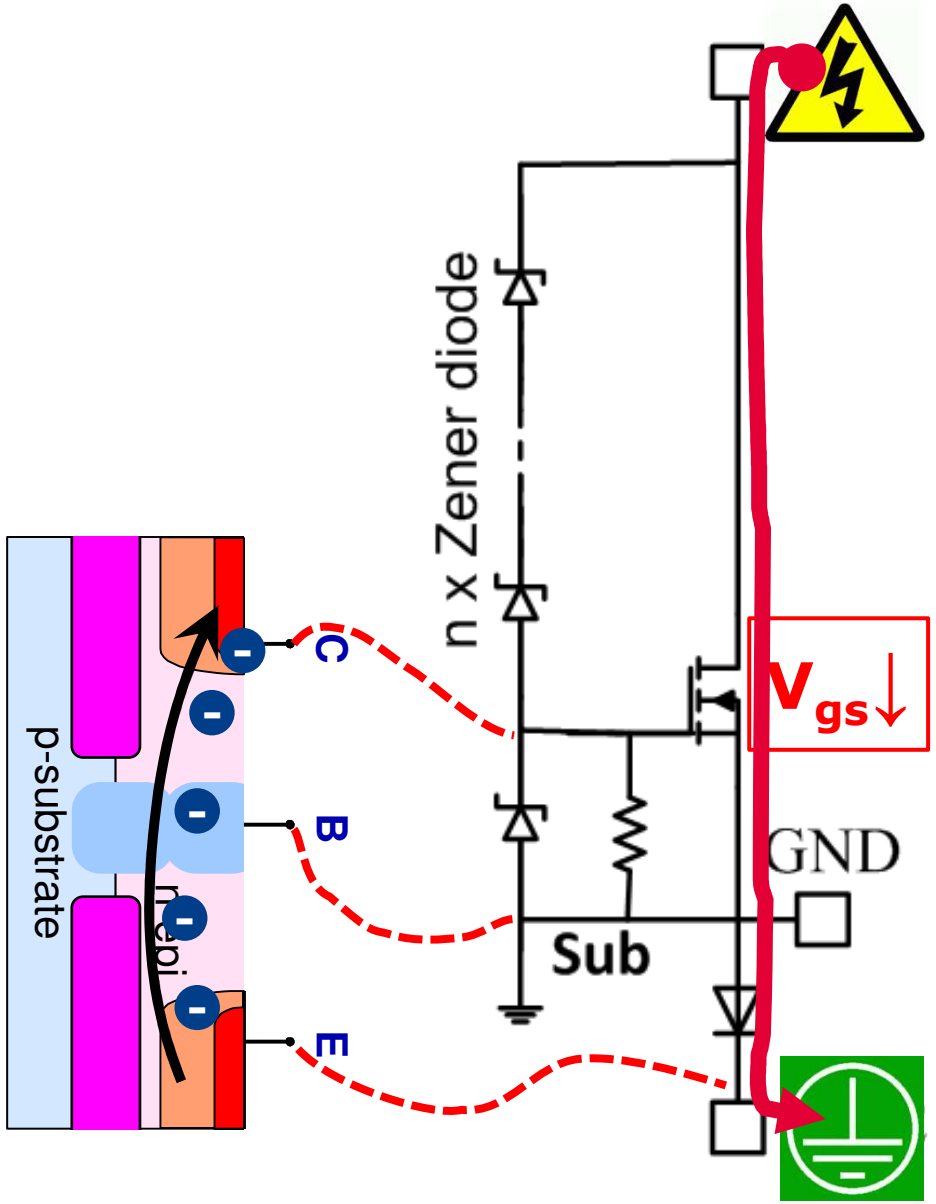


- Epi-well below Ground → emitter
  - Injection of minority carriers during ESD zap

- Epi well at high potential → collector
  - Usually multiple collectors
  - Snap-back risk of npn

Bipolar parasitics (between devices) /2

- E.g. risk with active clamps:
  - → Collector node is connected to gate of clamp device
  - → Gate may be pulled down during ESD zap
  - → ESD clamping function fails
- Majority carrier effects
  - → Substrate potential rise
  - → Active clamps may open due to forward bias of substrate / nwell diode (connected to gate) (unintended, in normal operation)



Thank you for your attention!

Now: Q & A time

References

1) G. Boselli et al., *Investigations on double-diffised MOS (DMOS) transistors under ESD zap conditions*, Proc. EOS/ESD Symp. Proc., 1999, pp. 19-27
2) G. Boselli et al., *Drain Extended NMOS High Current Behavior and ESD Protection Strategy for HV Applications in Sub-100nm CMOS Technologies*, IRPS Proc., 2007 pp. 342-347
3) Y. Cao et al., *On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD*, EOS/ESD Symp. Proc., 2010, pp. 283-292
4) Y. Cao et al., *ESD simulation with Wunsch-Bell based behavior modeling methodology*, EOS/ESD Symp. Proc., 2011, pp. 187-196
5) Y. Cao et al., *Statically triggered active ESD clamps for high-voltage applications* , EOS/ESD Symp Proc., 2012, pp. 353-362
6) Y. Cao et al., *Novel Active ESD Clamps for High-Voltage Applications*, IEEE Transactions on Device and Materials Reliability, Vol. 13, No. 2, pp. 388 - 397
7) L. Cerati et al., *Novel Technique to Reduce Latch-up Risk due to ESD Protection Devices in Smart Power Technologies*, EOS/ESD Symp. Proc., 2006, pp. 32-38
8) L. Cerati et al., *Power-to-Failure Investigation for PNP-Based ESD Protections: From ns to ms*, EOS/ESD Symp. Proc., 2013 (paper 3A.2)
9) W. J. Chang et al., *The Impact of Drift Implant and Layout Parameters on ESD Robustness for On-Chip ESD Protection Devices in 40-V CMOS Technology*, IEEE Transactions on Device and Materials Reliability, Vol. 7, No. 2, June 2007, pp. 324-332
10) S. L. Chen et al., *To Achieve a Novel Weak Snapback Characteristic in the High Voltage nLDMOS*, ISNE Proc., 2010, pp. 182-185
11) W. Y. Chen et al., *High-voltage NLDMOS in waffle-layout style with body-injected technique for ESD protection*, IEEE Electron Device Lett., Vol. 30, No. 4, April 2009, pp. 389–391

References

12) W. Y. Chen et al. , *Improvement on ESD Robustness of Lateral DMOS in High-Voltage CMOS ICs by Body Current Injection*, ISCAS Proc., 2009, pp. 385-388

13) W. Y. Chen et al., *Circuit and Layout Co-Design for ESD Protection in Bipolar-CMOS-DMOS (BCD) High-Voltage Process*, IEEE Transactions on Circuits and Systems, Vol. 57, No. 5, May 2010, pp. 1039-1047

14) V. De Heyn et al., *Design And Analysis of New Protection Structures for Smart Power Technology with Controlled Trigger and Holding Voltage*, IRPS Proc., 2001, pp. 253-258

15) A. Delmas et al., *Transient voltage overshoots of high voltage ESD protections based on bipolar transistors in smart power technology*, BCTM Proc., 2010, pp 253-256

16) H. Fujii et al., *A novel 80V-class HV-MOS platform technology featuring high-side capable 30Vgate- voltage drift-NMOSFET and a trigger controllable ESD protection BJT*, ISPSD Proc., 2009, pp. 323-326

17) A. Gendron et al., *Deep Trench NPN Transistor for Low-Ron ESD Protection of High-Voltage I/Os in Advanced Smart Power Technology*, IEEE BCTM, 2006

18) A. Gendron et al., *Area-Efficient, Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology*, EOS/ESD Symp. Proc., 2006, pp. 69-76

19) A. Gendron et al., *Techniques to Prevent Substrate Injection Induced Failure During ESD Events in Automotive Applications*, ISPSD Proc., 2011, pp. 192-195

20) A. Gendron et al., *New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications*, EOS/ESD Symp. Proc., 2011, pp. 1-10

21) E. Gevinti et al., *Novel 190V LIGBT-based ESD Protection for 0.35mm Smart Power Technology realized on SOI Substrate*, EOS/ESD Symp. Proc., 2008, pp. 211-220

22) H. Gossner et al., *Wide Range Control of the Sustaining Voltage of ESD Protection Elements Realized in a Smart PowerTechnology*, EOS/ESD Symp. Proc., 1999, pp. 19-27

References

23) A. Goyal et al., *Unique ESD Failure Mechanism of High Voltage LDMOS Transistors For Very Fast Transients*, IRPS Proc., 2008 pp. 673-674

24) M. Heer et al., *Analysis of the triggering behavior of low voltage BCD single and multi-finger gc-NMOS ESD protection devices*, EOS/ESD Symp. Proc., 2006, pp. 275-284

25) C. T. Hsu, *Cumulative Electrostatic Discharge Induced Degradation of Power-Rail ESD Clamp Device in High-Voltage CMOS/DMOS Technologies*, APCCAS Proc. , 2008, pp. 49-52

26) R. Ida et al., *A Method for Characterizing the DPI Immunity of an ESD Clamp*, IEW Proc., 2011, pp. 261-272

27) T. Imoto et al., *A Novel ESD Protection Device Structure for HV-MOS ICs*, IRPS Proc., 2009, pp. 663-668

28) D. Johnsson et al., *Avalanche Breakdown Delay in ESD Protection Diodes*, IEEE Transactions on Electron Devices, Vol. 57, No. 10, October 2010, pp. 2470-2476

29) D. Johnsson et al., *Avalanche Breakdown Delay in High-Voltage p-n Junctions Caused by Pre-Pulse Voltage From IEC 61000-4-2 ESD Generators*, IEEE Transactions on Device and Materials Reliability, Vol. 9, No. 3, September 2009, pp. 412-418

30) B. Keppens et al., *ESD protection solutions for high voltage technologies*, EOS/ESD Symp. Proc., 2004, pp. 289–298

31) T. H. Lai et al., *Design of Modified ESD Protection Structure with Low-Trigger and High-Holding Voltage in Embedded High-Voltage CMOS Process*, IRPS Proc., 2011, pp. 392-395

32) J.-H. Lee et al., *Novel ESD protection structure with embedded SCR LDMOS for smart power technology*, IRPS Proc., 2002, pp. 156–161

33) J. H Lee et al., *The Influence of NBL Layout and LOCOS Space on Component ESD and System Level ESD for HV-LDMOS*, ISPSD Proc., 2007, pp. 173-176

34) J. H Lee et al., *The Influence of The Layout On The ESD Performance Of HV-LDMOS*, ISPSD Proc., 2010, pp. 303-306

35) D. Linten et al., *Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD stress*,EOS/ESD Symp. Proc., 2008, pp. 204-210

References

36) Z. Liu et al., Novel Silicon-Controlled Rectifier (SCR) for High-Voltage Electrostatic Discharge (ESD) Applications, IEEE Electron Device Letters, Vol. 29 , No. 7, July 2008, pp. 753-757

37) A.W. Ludikhuize et al., *Improved device ruggedness by floating buffer ring*, ISPSD Proc., 2000, pp. 153-156

38) K. Kawamoto et al., *A no-snapback LDMOSFET with automotive ESD endurance*, IEEE Transactions on Electron Devices, Vol. 49, No. 11, November 2002, pp. 2047–2053

39) M. Mayerhofer et al., *ESD Review Methodology using Transient Simulations on Circuit Level and its Application for JEDEC/ESDA HBM and IEC 61000-4-2 Pulses in Automotive Circuits*, Proceedings 11. German ESD-Forum, 2011

40) G. Meneghesso et al., *ESD robustness of smart power protection structures evaluated by means of HBM and TLP tests*, IRPS Proc., 2000, pp. 270-275

41) G. Meneghesso et al., *Overstress and Electrostatic Discharge in CMOS and BCD Integrated Circuits*, Microelectronic Reliability, Vol. 40, pp. 1739-1746, 2000

42) M. Mergens et al., *Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions*, EOS/ESD Symp. Proc. , 1999, pp. 1-10

43) M. Mergens et al., *ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive*, EOS/ESD Symp. Proc., 2006, pp. 54-63

44) G. Notermans et al., *Designing HV active clamps for HBM robustness*, EOS/ESD Symp. Proc. , 2007, pp. 47–52

45) O. Quittard et al., *ESD Protection for High-Voltage CMOS Technologies*, EOS/ESD Symp. Proc., 2006, pp. 77-86

46) P. Renaud et al., *High robustness PNP-based structure for the ESD protection of high voltage I/Os in an advanced smart power technology*, IEEE BCTM, 2007, pp. 226-229

47) R. Rudolf, et al., *Automotive 130 nm Smart-Power-Technology including embedded Flash Functionality*, ISPSD, 2011.

48) C. Salaméro et al., *TCAD Methodology for ESD Robustness Prediction of Smart Power ESD Devices*, IEEE Transactions on Device and Materials Reliability, Vol. 6, No. 3, September 2006, pp. 399-407

References

49) L. Sponton et al., *ESD protection structures for BCD5 smart power technologies*, Microelectronics Reliability, Volume 41, Number 9, September 2001 , pp. 1683-1687

50) L. Sponton et al., *ESD protection structures for 20 V and 40 V power supply suitable for BCD6 smart power technology*, Microelectronics Reliability, Volume 42, Number 9, September 2002 , pp. 1303-1306

51) A. Tazzoli et al., *Development of ESD protection structures for BULK and SOI BCD6 technology*, ISPSD Proc., 2006, pp. 361-264

52) V. Vashchenko et al., *Implementation of dual-direction SCR devices in analog CMOS process*, EOS/ESD Symp. Proc., 2007, pp. 75-79

53) V. Vashchenko et al., *Comparison of ESD protection capability of lateral BJT, SCR and bidirectional SCR for high-voltage BiCMOS circuits*, BCTM Proc., 2002, pp. 181-184

54) S. J. Wang et al., *Analysis and Optimization of HV ESD Protection*, EDSSC Proc., 2010, pp. 1-4

55) S. Y. Wang et al., *An EOS-Free PNP-Enhanced Cascoded NMOSFET Structure for High Voltage Application*, IRPS Proc., 2011, pp. 396-400

56) P. Wessels, *Smart Power Technologies on SOI*, VLSI-TSA Proc., 2011, pp. 1-2

57) P. Wessels et al., *Advanced 100V 0.13 mm BCD process for next generation automotive applications*, ISPSD 2006, pp. 1-4

58) J. Willemen et al., *Characterization and Modeling of Transient Device Behavior under CDM ESD Stress,* EOS/ESD Symp. Proc., 2003.

59) J. Willemen et al., *A TLP-based characterization method for transient gate biasing of MOS devices in high-voltage technologies*, EOS/ESD Symp. Proc., 2010, pp. 1-10

60) J. Willemen et al., *Photon Accelerated Turn-on of High-Voltage ESD Diode Breakdown*, EOS/ESD Symp. Proc., 2013 (paper 5B.3)

References

61) E. Gevinti et al., *HBM ESD EDA Check Method Applied to Complete Smart Power ICs - Functional Initialization and Implementation*, EOS/ESD Symp. Proc., 2013 (paper 4A.1)

62) B. Aliaj et al., *Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting*, EOS/ESD Symp. Proc., 2014 (paper 7B.2)

63) Y. F. Chang, *High Flexibility SCR Clamp for ESD Protection in BCD Power Technology*, EOS/ESD Symp. Proc., 2014 (paper 7B.3)

64) L. Di Biccari et al., *Thin Copper Metal Interconnections Thermomigration Analysis in ESD Regime*, EOS/ESD Symp. Proc., 2014 (paper 3A.2)

65) U. Glaser et al., *TLP Failure Level Extraction Despite Reflected Waves*, EOS/ESD Symp. Proc., 2014 (paper 5B.3)

66) W. Y. Hsu, *A High-Reliable Self-Isolation Current-Mode Transmitter (CM-Tx) Design for +/-60V Automotive Interface with Bulk-BCD Technology*, EOS/ESD Symp. Proc., 2014 (paper 7B.4)

67) F. Magrini, *Advanced Wunsch-Bell based Application for Automotive Pulse Robustness Sizing*, EOS/ESD Symp. Proc., 2014 (paper 9A.5)

68) A. Tazzoli et al., *Effect of process technology variation on ESD clamp parameters*, EOS/ESD Symp. Proc., 2014 (paper 3A.1)

69) V. Vashchenko et al., *Pseudo p-i-n Avalanche Diode Clamp*, EOS/ESD Symp. Proc., 2014 (paper 3A.4)

70) Z. Chen et al., *Design and Optimization on ESD Self-Protection Schemes for 700V LDMOS in High Voltage Power IC*, EOS/ESD Symp. Proc., 2015 (paper 7A.1)

71) E. Gevinti et al., *Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC's - Initialization and Implementation*, EOS/ESD Symp. Proc., 2015 (paper 3A.2)

72) A. Rupp et al., *Active clamp design for on-chip GUN protection*, EOS/ESD Symp. Proc., 2015 (paper 7A.4)

73) A. Tazzoli et al., *Engineering of Dual-Direction SCR Cells for Component and System Level ESD, Surge, and Longer EOS Events*, EOS/ESD Symp. Proc., 2015 (paper 7A.2)

References

74) M. F. Tsai et al., *Investigation and solution to the early failure of parasitic NPN triggered by the adjacent PNP ESD clamps*, EOS/ESD Symp. Proc., 2015 (paper 7A.3)

75) V. Vashchenko et al., *Active Clamps with Hybrid BIT -CMOS Operation Mode*, EOS/ESD Symp. Proc., 2015 (paper 4A.3)

76) Y. Xiao et al., *HBM Failures Induced by ESD Cell Turn-Off and Circuit Interaction with ESD Protection*, EOS/ESD Symp. Proc., 2015 (paper 3B.1)

77) L. Di Biccari et al., *HV ESD diodes investigation under vf-TLP stresses: TCAD approach*, EOS/ESD Symp. Proc., 2016 (paper 2A.1)

78) L. Cliff et al., *A Simple Power Diode Model with Forwards and Reverse Recovery*, IEEE Transaction on Power Electronics, Vol. 8, No. 4, 1993, pp 342-346

79) R. Rudolf et al., *Automotive 130 nm Smart-Power-Technology including embedded Flash Functionality*, ISPSD Proc., 2011

80) H. Marquardt et al., *Topology-Aware ESD Checking: A New Approach to ESD Protection*, EOS/ESD Symp. Proc., 2012 (paper 2A.3)

81) Y. Cao, *ESD Troubleshooting Using Multi-level TLP*, EOS/ESD Symp. Proc., 2014 (paper 7A.3)