ESD Design in High Voltage Smart Power Technologies

Lorenzo CERATI
Fellow of the Technical Staff

STMicroelectronics

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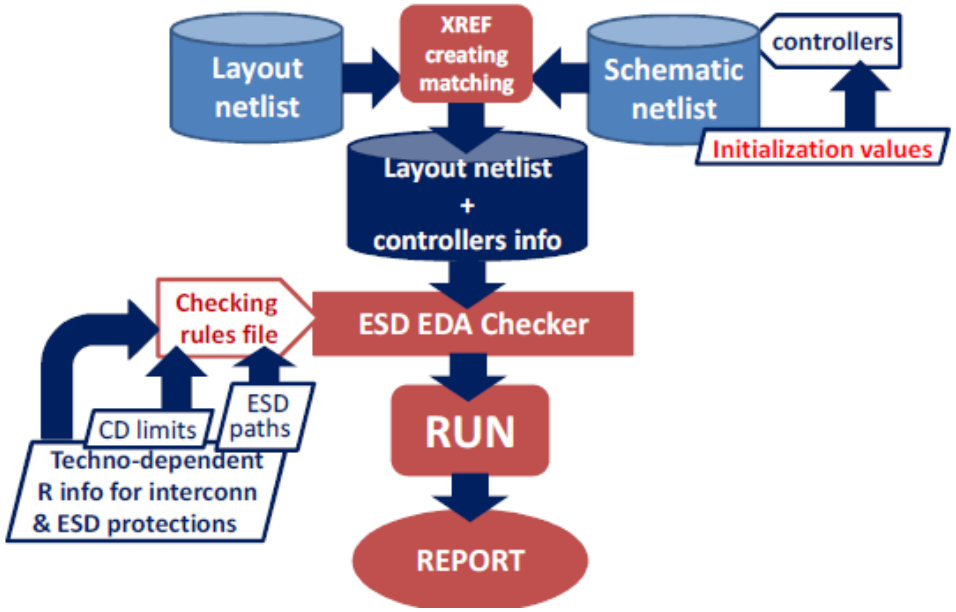
About Lorenzo CERATI

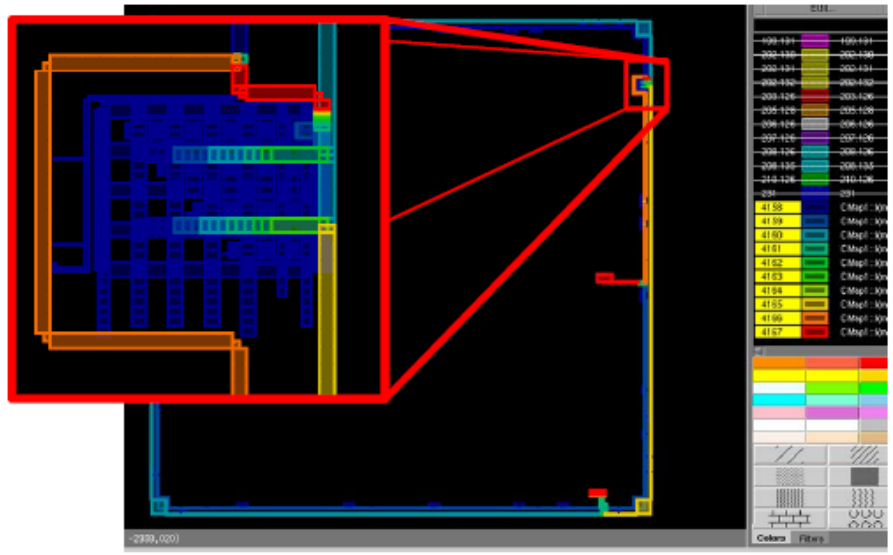
1. 1998 M.Sc. Degree in from
   - ✓ Telecommunication engineering
   - ✓ "Politecnico di Milano".
   - ✓ Thesis "cadmium zinc tellurid (CdZnTe) cross-connect for optical networks"

2. 2000 -Now, With ST Microelectronics,
   - ✓ leading the team developing ESD protection architectures in Smart Power technologies (e.g BCD)

3. Society contributions:
   - ✓ Dozens of peer reviewed publication within IEEE
   - ✓ ESDA Board of Directors since 2015.
   - ✓ Symposium Technical Program Committees ESREF, ICICDT, IRPS, IEW, and EOS/ESD Gently
   - ✓ Accepted to present us

Layout Level checks





References

[1] Eleonora. Gevinti, Lorenzo Cerati *et al*., "Schematic-Level and Layout-Level ESD EDA check methodology applied to smart power IC's - initialization and implementation," *2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, 2015, pp. 1-10, doi: 10.1109/EOSESD.2015.7314770

Eleonora. Gevinti, Lorenzo Cerati et al., "Schematic-Level and Layout-Level ESD EDA check methodology applied to smart power IC's - initialization and implementation," 2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2015, pp. 1-10, doi: 10.1109/EOSESD.2015.7314770.