

# **75 Years of Transistor and Its Impact on Humanity** **Birth and Evolution of Semiconductor Devices**

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IEEE EDS Distinguished Lecture  
IEEE EDS Northern Virginia / Washington DC Chapter,  
Region 1  
22 March, 2022  
(Virtual Talk)

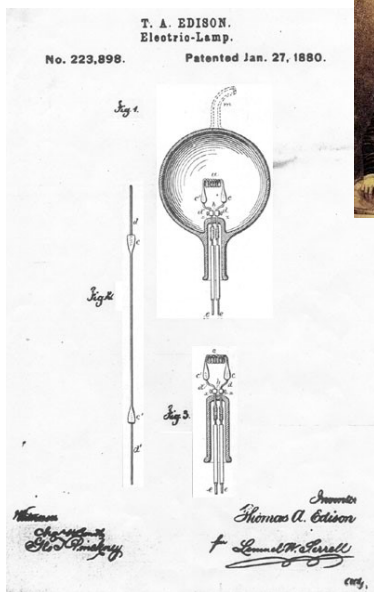
1

## **OUTLINE**

- **Electronics Evolution (devices)**
  - Prior History and Birth of Transistor
    - Patents 755,840 ; 1,900,018 ; 2,524,035 ; 2,569,347
  - Concept to Reality - MOSFET - Birth of Modern Technology
    - Invention to Industry / Room at the Bottom
  - Fifty, Trillion & 0.0001 – and goes on
- **Veracity in Device Progression**
  - Challenges continues / What becomes Important
- **Technology Impacts in Society and Humanity**
  - Extended Research, Application
  - Transistors & Neurons – a number game
  - Advancements in Society and Human Interactions

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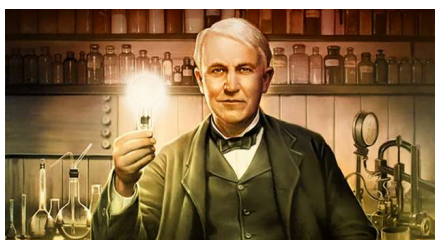
## Electronics Evolution – the Beginning



William Gilbert (English Scientist) in late 1500s coined the word **Electricity** from Greek word **ELEKTRON** meaning *like amber*. He showed static electricity from friction - occurs in materials



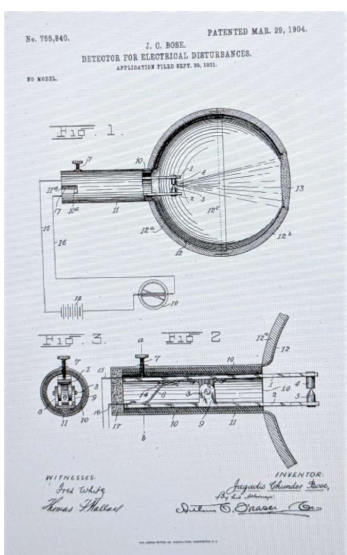
Thomas Edison's first successful model of light bulb, used in public demonstration - December 1879 ([https://en.wikipedia.org/wiki/Thomas\\_Edison](https://en.wikipedia.org/wiki/Thomas_Edison))



US Patent 223898 - Edison in 1878

## Electronics Evolution – Prior History

### 120 Years of Solid State Diode



First patent for **solid-state diode** (to receive electromagnetic waves)

J.C. Bose demonstrated his wireless millimetre wave (microwave) experiments at the Royal Institution, London in **January 1897**.

(This predates the wireless experiments at Salisbury Plain by Guglielmo Marconi in **May 1897**).

Bose was an authority with many pioneering works on reflection, refraction, polarization and absorption of millimeter waves and its application to wireless communication.

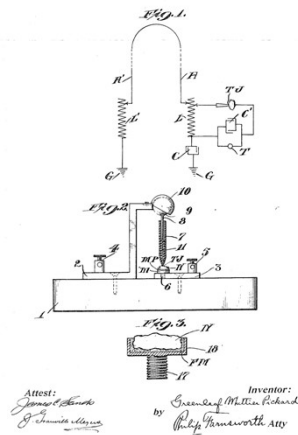
"Detector for electrical disturbances," **U. S. Patent 755,840 - J.C. Bose**, (Filed September 30, 1901. Issued March 29, 1904).

Based on his contributions **IEEE recognized JC Bose in 1997 as the Father of Radio Sciences**.

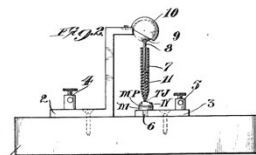
## Electronics Evolution – Prior History

(1901 to 1910)

No. 836,531. PATENTED NOV. 20, 1906.  
G. W. PICKARD.  
MEANS FOR RECEIVING INTELLIGENCE COMMUNICATED BY ELECTRIC WAVES.  
APPLICATION FILED APR. 30, 1906.



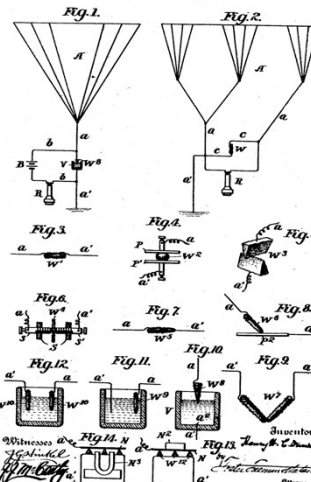
**G W Pickard  
(1906)**



**US Patent 836531**

Detector for receiving intelligence communicated by electric waves.

No. 837,616. PATENTED DEC. 4, 1906.  
H. H. C. DUNWOODY.  
WIRELESS TELEGRAPH SYSTEM.  
APPLICATION FILED MAR. 22, 1906.



**H H C Dunwoody  
(1906)**

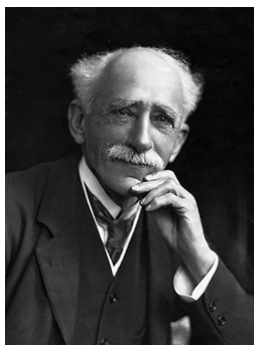


**US Patent 837616**

invented the carborundum radio detector.

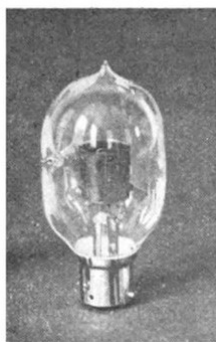
## Electronics Evolution – Prior History

(1901 to 1910)



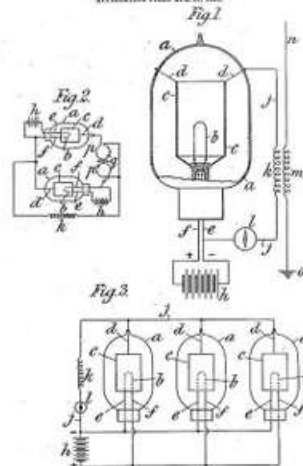
**John Ambros Fleming – 1904 – Vacuum Diode  
British Patent : 24850**

**John Ambrose Fleming invented the two-electrode vacuum tube rectifier**



Fleming's valve

No. 302,486. PATENTED NOV. 7, 1905.  
J. A. FLEMING.  
INSTRUMENT FOR CONVERTING ALTERNATING ELECTRIC CURRENTS INTO CONTINUOUS CURRENTS.  
APPLICATION FILED APR. 11, 1905.



Witnesses  
William T. Davis  
James G. Mason  
Inventor  
John Ambrose Fleming  
By his attorney  
Theodore D. Safford

## Electronics Evolution – Prior History (1901 to 1910)



Le De Forest



Vacuum Tube (Triode) -1906

(US Patent : 841,386 - Wireless Telegraphy)

No. 841,386. L. DE FOREST. PATENTED JAN. 15, 1907.  
WIRELESS TELEGRAPHY.  
APPLICATOR FILED APR. 21, 1906. 2 SHEETS-SHEET 1.

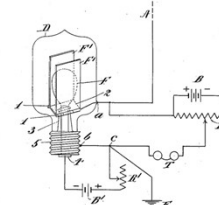


FIG. 1.

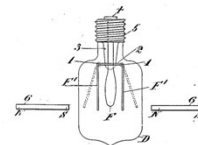


FIG. 2.

WITNESSES:  
*Frank G. Parker*  
*John R. ...*

INVENTOR:  
*Le de Forest*  
By *Lucy Woodcock*  
ATTORNEY

## 94 Years of MOSFET

### MOSFET Patent - 1928

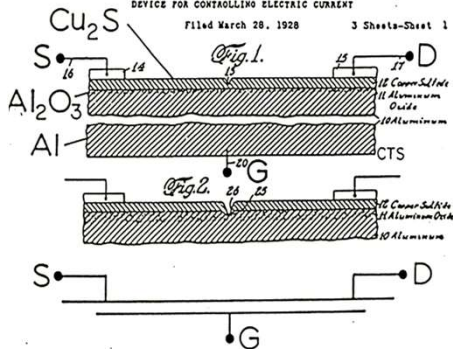
Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENTHAL, OF BROOKLYN, NEW YORK  
DEVICE FOR CONTROLLING ELECTRIC CURRENT

Applicant filed March 28, 1928. Serial No. 243,374.

J. E. LILIENTHAL  
DEVICE FOR CONTROLLING ELECTRIC CURRENT  
Filed March 28, 1928 3 Sheets-Sheet 1



DEVICES FOR CONTROLLING ELECTRIC CURRENT

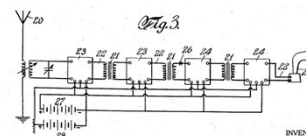
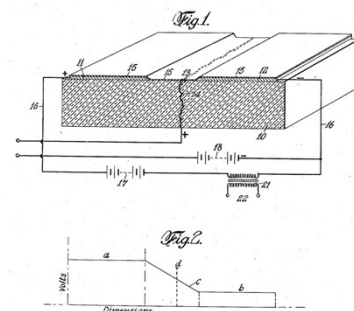
8 Patent filed on March 28, 1928



J. E. LILIENTHAL

### MESFET Patent - 1926

Jan. 28, 1930. J. E. LILIENTHAL 1,745,175  
METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS  
Filed Oct. 8, 1926



INVENTOR  
*Julius Edgar Lilienthal*  
BY *Frank ...*  
ATTORNEY

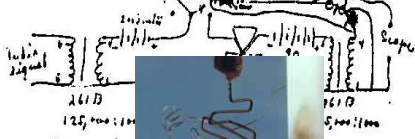


# Birth of Transistor

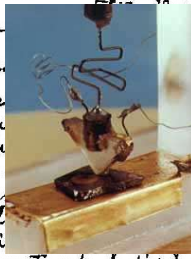
DATE Dec 24 1947  
CASE No 38177-7

We attained the following A.C. values at 1000 cycles.  
 $E_p = .016 \text{ V}$ ,  $I_p = 1.5 \text{ mA}$ ,  $E_o = 1.5 \text{ V}$ ,  $I_o = 1.5 \text{ mA}$   
 $P_o = 2.25 \times 10^{-5} \text{ W}$   
 Voltage gain 100 Power gain 40  
 Current  $\frac{1}{2.5}$

This unit was then connected in the following circuit



This circuit was then connected in the following circuit when power was applied the device showed a gain in current and power. The gain was measured at the peak frequency.

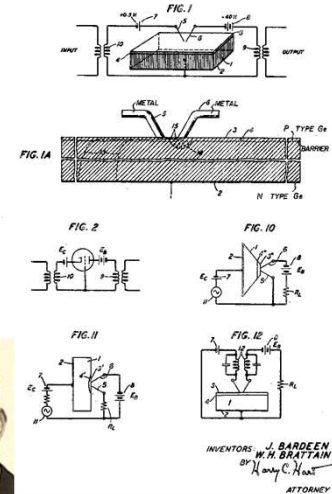


It was determined that the power gain was the order of magnitude of 18 on quartz. Various points witnessed this test and nature of whom some were the following: R.B. Jidney, H. N. Moore, J. Bardeen, G. N. Pearson, W. Shockley, H. Fletcher, R. Brown. Mr. H. N. Moore assisted in setting up the circuit and the demonstration occurred on the afternoon of Dec 27 1947

Redesigned by  
S. L. Brown  
H. N. Moore on 12/27/47



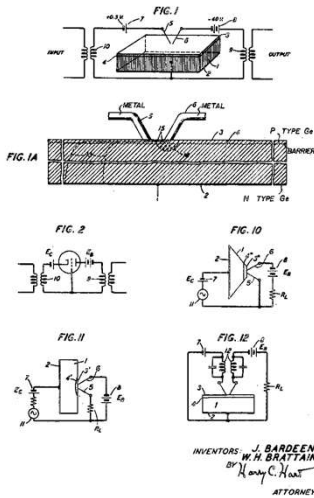
Oct. 3, 1950  
Filed June 17, 1948



INVENTORS: J. BARDEEN  
W. H. BRATTAIN  
BY: H. C. HOUSTON  
ATTORNEY

# P-N Junction Transistor

Oct. 3, 1950  
Filed June 17, 1948



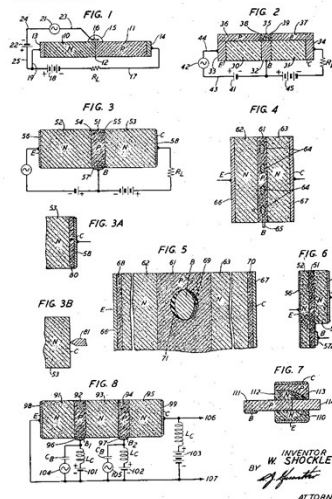
INVENTORS: J. BARDEEN  
W. H. BRATTAIN  
BY: H. C. HOUSTON  
ATTORNEY

Patent 2524035 filed June 17, 1948



William Shockley

Sept. 25, 1951  
Filed June 26, 1948



INVENTOR: W. SHOCKLEY  
BY: J. F. HUNTER  
ATTORNEY

Patent 2569347 filed June 26, 1948

# 75 Years of Transistor

We obtained values at-  
 $k_p = .015$   
 $P_g = 5.4 \times 10^{-5}$   
 Voltage gain  
 Current  
 This circuit in the lab

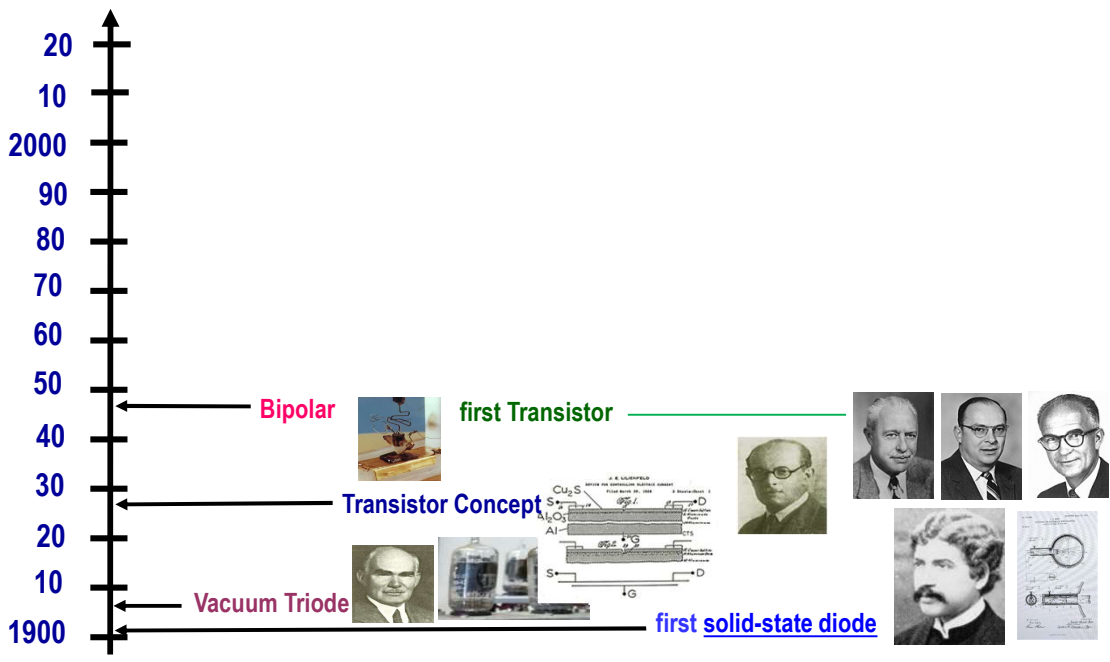
This circuit was actually spoken up and by switching the device in and out a distinct gain was observed.

has determined that the gain was the order of 10 to 20. Various people, this fact and nature same were the following: H. N. Mease, J. Bardeen, W. Shockley, H. Flat. Mr. H. D. Mease acting up the circuit as a demonstration secured on Dec 27 1947

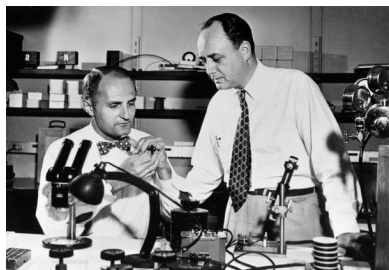
But is understood by J. Bardeen & H.N. Mease!

**Birth Certificate of Our Era**

## Devices Evolution



## First grown Si Junction Transistor

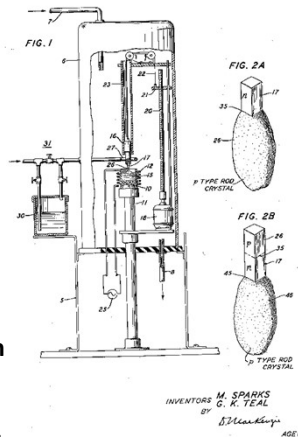


Morgan Sparks & Gordon Teal

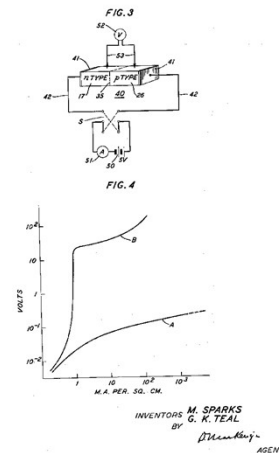


Czochralski grown semiconductor material used for making P-N junctions (1951-53)

March 17, 1953 M. SPARKS ET AL 2,631,356  
 METHOD OF MAKING P-N JUNCTIONS IN SEMICONDUCTOR MATERIALS  
 Filed June 15, 1950 2 Sheets-Sheet 1

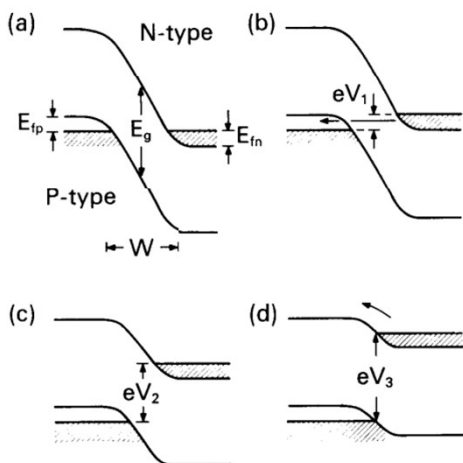


March 17, 1953 M. SPARKS ET AL 2,631,356  
 METHOD OF MAKING P-N JUNCTIONS IN SEMICONDUCTOR MATERIALS  
 Filed June 15, 1950 3 Sheets-Sheet 2



First Grown Silicon Junction Transistor (1953)  
 (M Sparks & G Teal - US Patent : 2631356)

## Tunneling phenomenon in Semiconductors



Energy band diagrams of heavily doped semiconductor P-N junctions at varied bias voltages depicting interband tunneling (L. Esaki, Phys. Rev., 109, 1958)

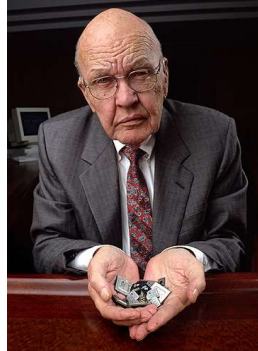
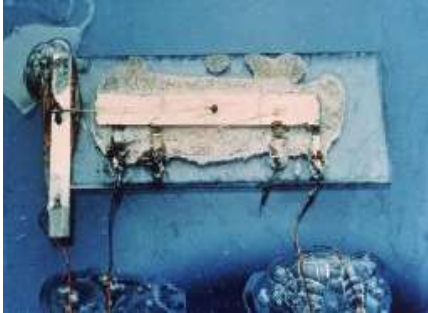


Leo Esaki (1973 Nobel Prize) demonstrated band-to-band Tunneling in semiconductors experimentally in 1958

I would like to point out that many high barriers exist in this world: Barriers between nations, races and creeds. Unfortunately, some barriers are thick and strong. But I hope, with determination, we will find a way to tunnel through these barriers easily and freely, to bring the world together so that everyone can share in the legacy of Alfred Nobel.

(from Leo Esaki, Nobel Lecture, 1973)

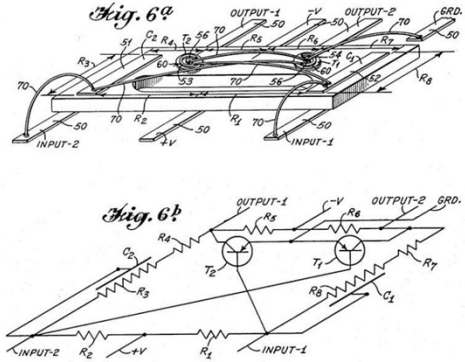
# 1958: 1<sup>st</sup> Integrated Circuit



Jack S. Kilby

“The innovation and development that has followed in the past 40 years has been remarkable and far more rapid than all the developments in the prior 400 years after William Gilbert coined the term ‘electricity’”  
 - from Jack Kilby’s Nobel Lecture 2000

June 23, 1964 J. S. KILBY 3,138,743  
 MINIATURIZED ELECTRONIC CIRCUITS  
 Filed Feb. 6, 1959 4 Sheets-Sheet 2



INVENTOR  
 Jack S. Kilby

BY *Edwards, Davis, Pellier & Prosser*  
 ATTORNEYS

US Patent 3138743

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# 32 Years for Concept to Reality

1960: First MOSFET by D. Kahng and M. Atalla



Aug. 27, 1963 DAWON KAHNG 3,102,230  
 ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE  
 Filed May 31, 1960

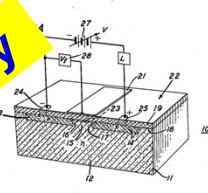
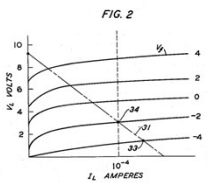
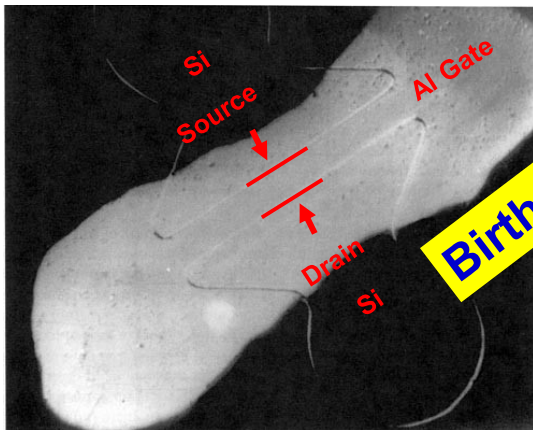


FIG. 1B

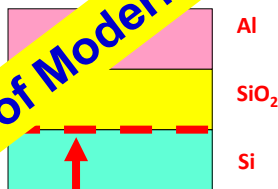


INVENTOR  
 D. KAHNG  
 BY *W. J. ...*  
 ATTORNEY

Top View



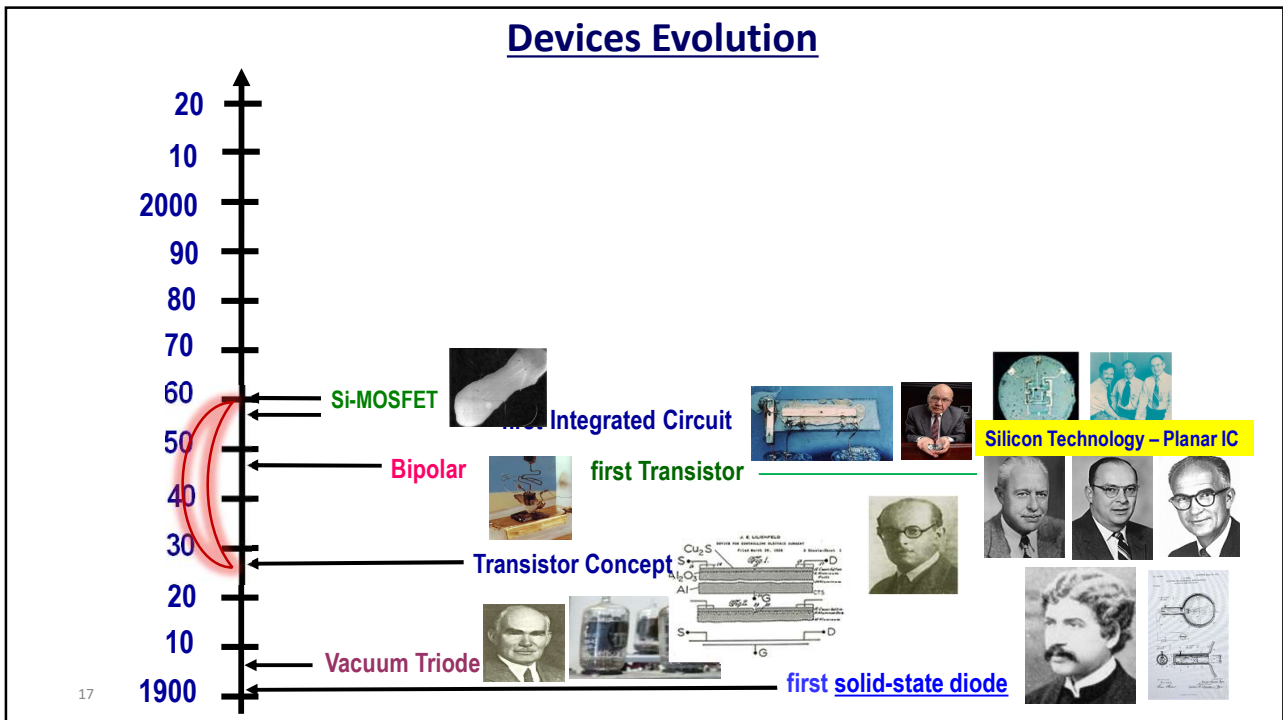
Cross-section



Exceptionally good interface!

**Birth of Modern Technology**



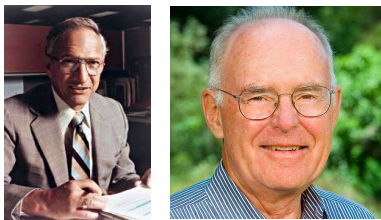


## Integrated Circuits – Invention to Industry

First Semiconductor company

**FAIRCHILD**  
SEMICONDUCTOR® in 1957 in San Jose, CA

by a team including  
Robert Noyce and Gordon Moore



Both Noyce and Moore left Fairchild in 1968 and started a company **NM Electronics** which later changed the name to **Intel**

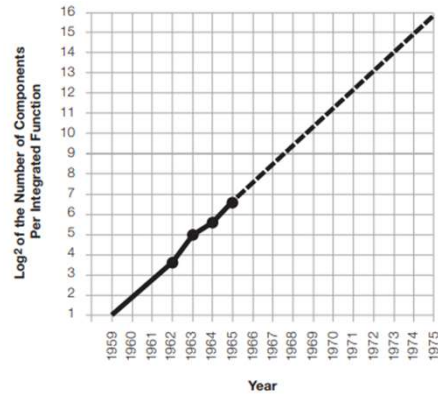
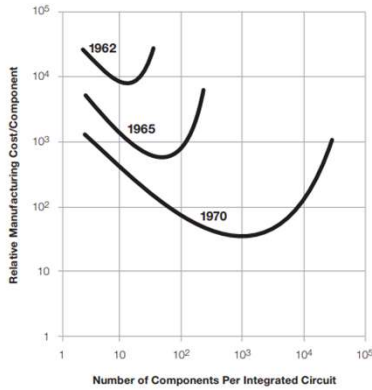


Gordon Moore, Robert Noyce & Andrew Grove

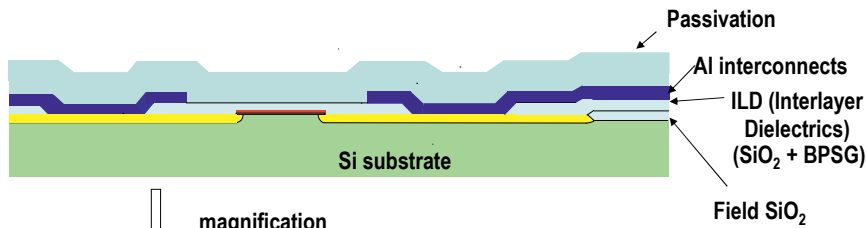
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## Invention to Industry – Moore’s Law

Gordon Moore, “Cramming more components onto integrated circuits”  
 Electronics, Vol 38, Number 8, April 19, 1965



## NMOS LSI in Early 1970s



- Layers**
- Si substrate
  - Field oxide
  - Gate oxide
  - Poly Si gate electrode
  - Source/Drain diffusion
  - Interlayer dielectrics
  - Aluminum interconnects
  - Passivation

## Device Evolution LSI to VLSI

### Major Stages in Process

1970 - 10-12 um device (1971 - Intel 4004)

1979 - Polycide Gate

1981 - Salicide Process

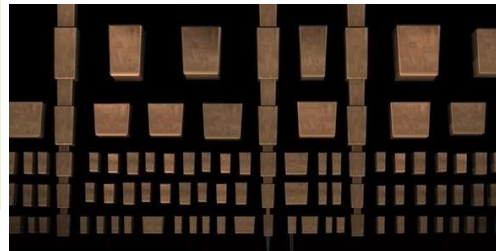
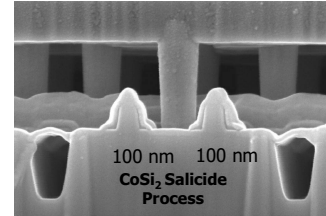
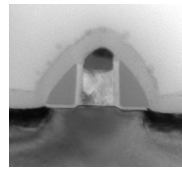
1995 - Shallow Trench Isolation (STI)

1997 } Cu Metallization / Low K ILD

} SiON / High K Gate Dielectrics

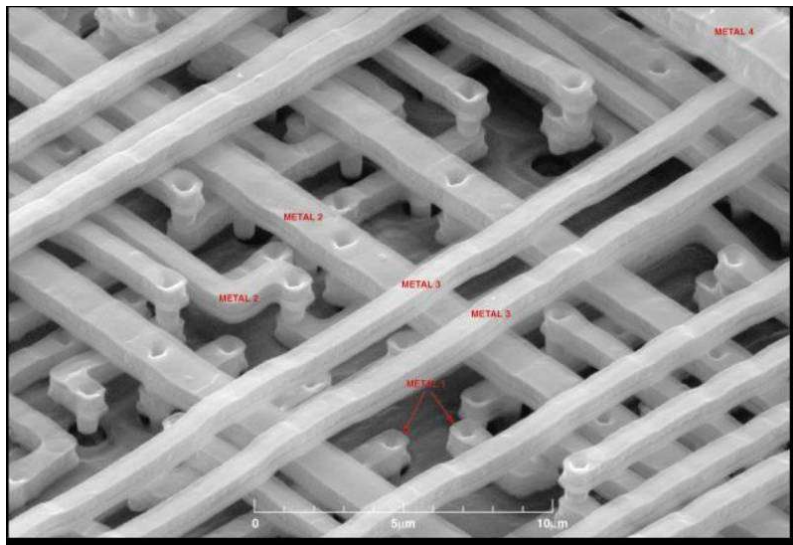
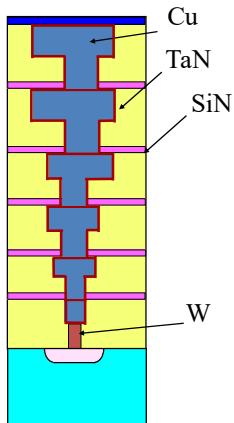
2007 } Metal gate Structures

Gate Length - from 10um to 65-45nm



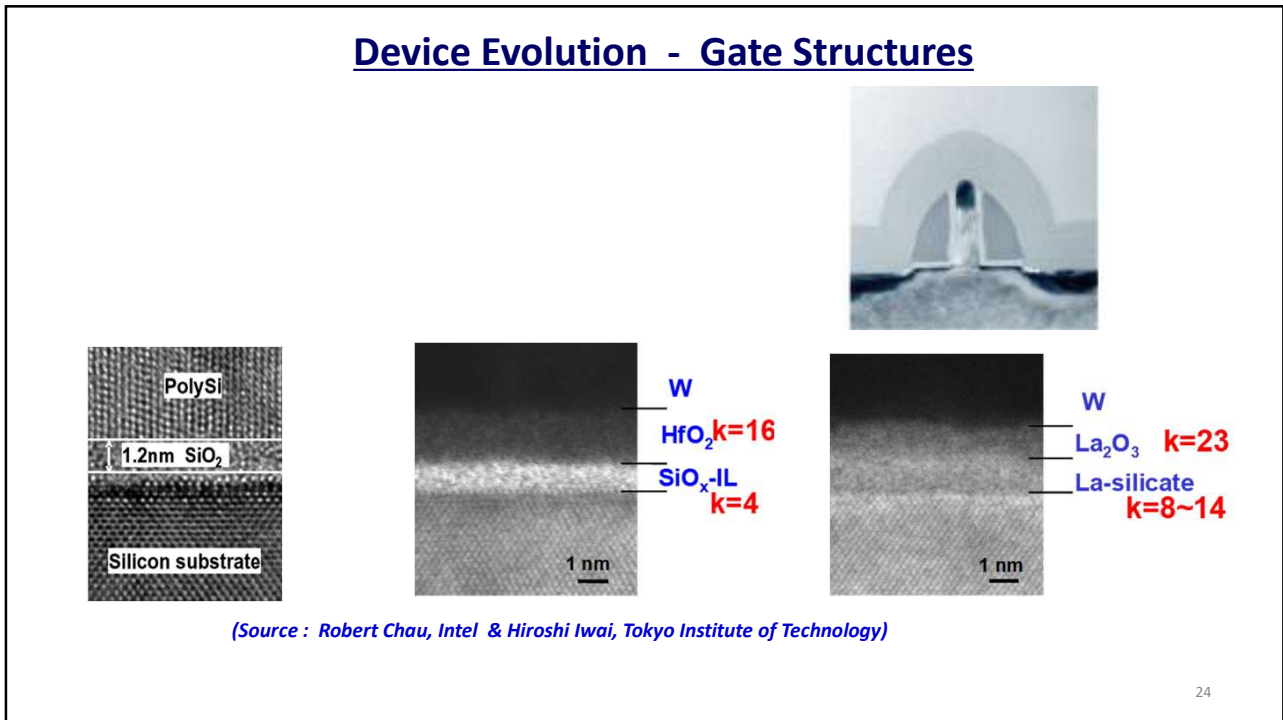
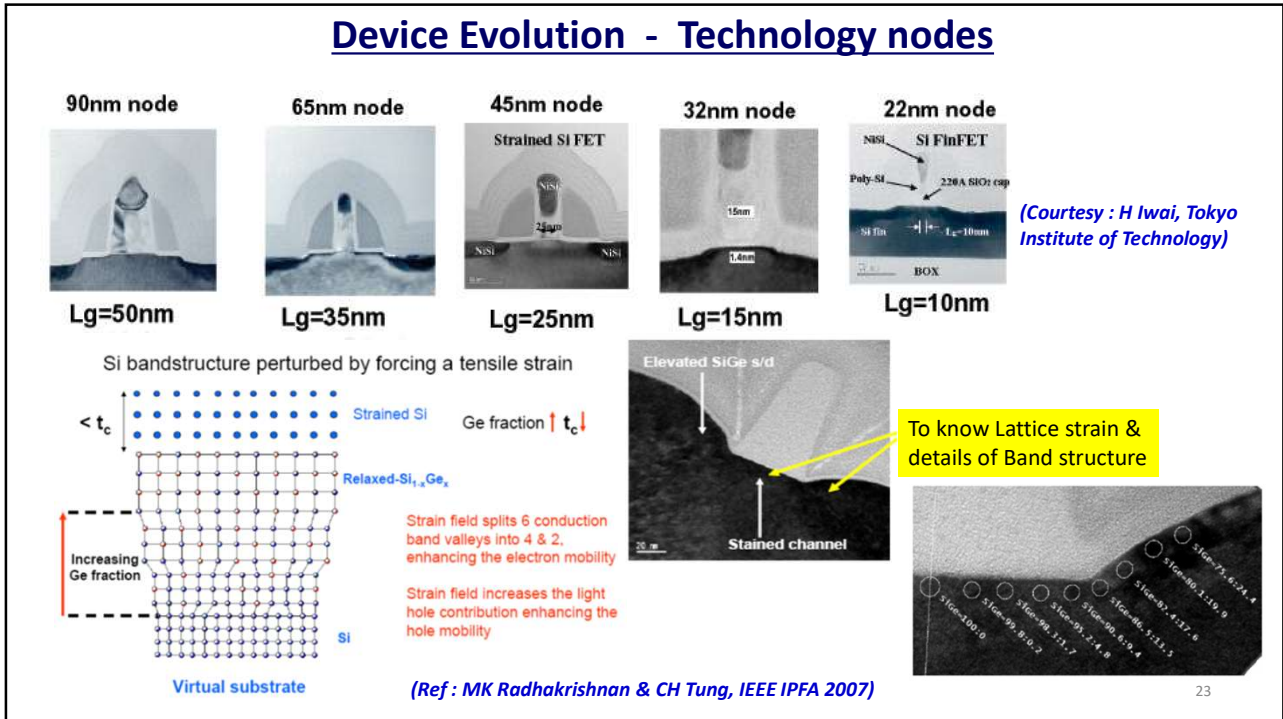
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## Device Evolution - Interconnects



(Courtesy : Jeff Gambino, IBM)

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The image contains three diagrams and one micrograph. On the left is a cross-section of FDSOI (Fully Depleted Silicon-On-Insulator) showing an Inversion Layer, Gate, Gate Oxide, Source, Drain, Buried Oxide, and Silicon Substrate. Below it is the text: "Floating body eliminated - fully depleted FDSOI". In the center is a cross-section of a FinFET showing Gate Oxide, Inversion Layer, Fin, Gate, Oxide, and Silicon Substrate. Below it is the text: "Gate on three side - fully depleted". On the right is a scanning electron micrograph (SEM) of a FinFET fin. Below the SEM is the text: "1998 - FinFET UC Berkley, TSMC". At the bottom center is a 3D block diagram of a FinFET with Source, Gate, Drain, and Fin labels.

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The image contains three micrographs. The left one is labeled "Gate Stack". The middle one is labeled "SOI" and shows a cross-section with red arrows for "Transverse", "Longitudinal", and "Vertical" directions, and a label for  $I_{ds}$ . Below the SOI micrograph are the labels "Si (7nm)", "BOX (10nm)", and "Si sub.". The right one is labeled "Fin / Tri Gate" and is a scanning electron micrograph of a fin. Below the SOI and Fin / Tri Gate micrographs are the labels "Gate Stack", "SOI", and "Fin / Tri Gate".



*“ Why cannot we write the entire 24 volumes of Encyclopedia Britannica on the head of a pin ”*


**“There is plenty of room at the bottom”**

**Richard Feynman**  
1959

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## 10 Million Transistors Fit in 1 mm<sup>2</sup>

1 mm




Ball Point Pen

10,000 x

→

0.1 μm

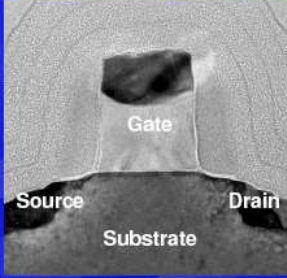


SRAM Cell  
Top View

10 x

→

10 nm

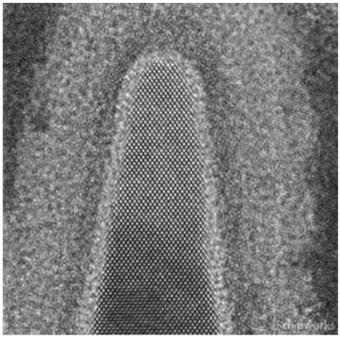


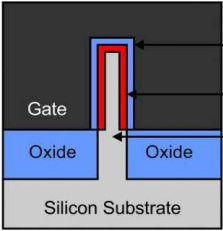
Transistor  
Side View

**10 million transistors fit in 1 mm<sup>2</sup>, roughly the size of the tip of a ball point pen**

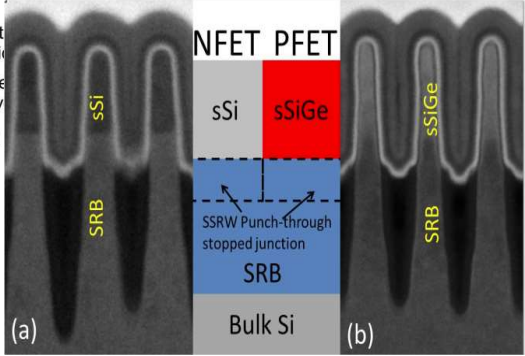
(Source : Intel Developer's Forum)

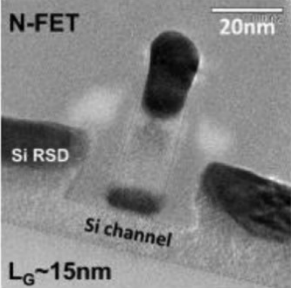
27



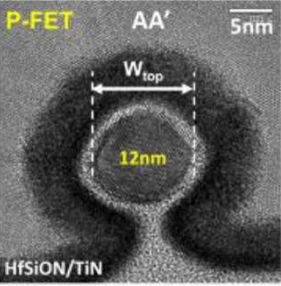


Gate on three side - fully depleted





N-FET  
20nm  
Si RSD  
Si channel  
L<sub>G</sub> ~ 15nm



P-FET  
AA'  
5nm  
W<sub>top</sub>  
12nm  
HfSiON/TiN

SiGe FETs – different approaches

**7 nm FinFET : Dual-stressed channel materials on the strain-relaxed buffer (SRB) with a super-steep retrograde well (SSRW)**

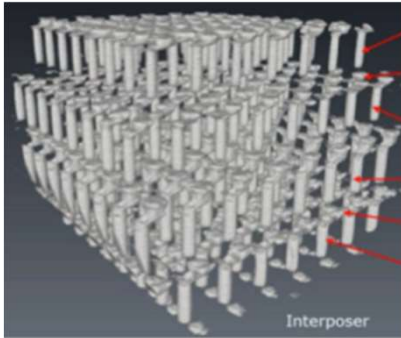
(a) TEM image of tensile strained silicon fin  
 (b) TEM image of compressively strained SiGe fin on a common SRB

(source : IBM/Globalfoundries/Samsung – 2016) 28

(P. Nguyen et al., IEDM 2014)

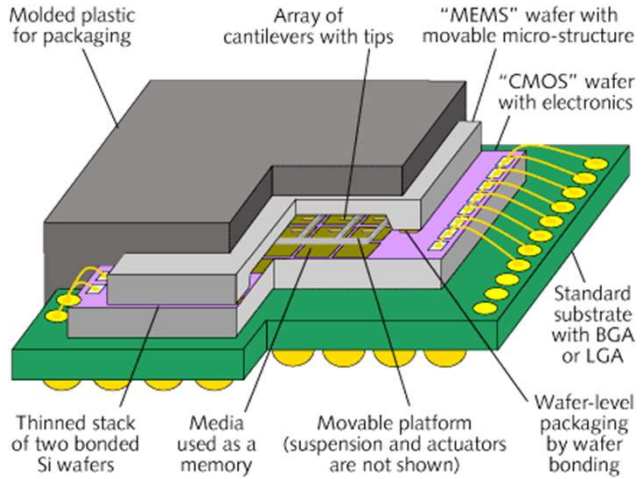
### 3D Integration and Super Chips

3D hetero-integration technology opens up the possibility to assemble various functional blocks - processors, memory, sensors, logic, analog, photonic, and power ICs into one stacked chip



X-ray CT scan image measured from TSV array areas in the 4-layer stacked 3-D multicore processor chip

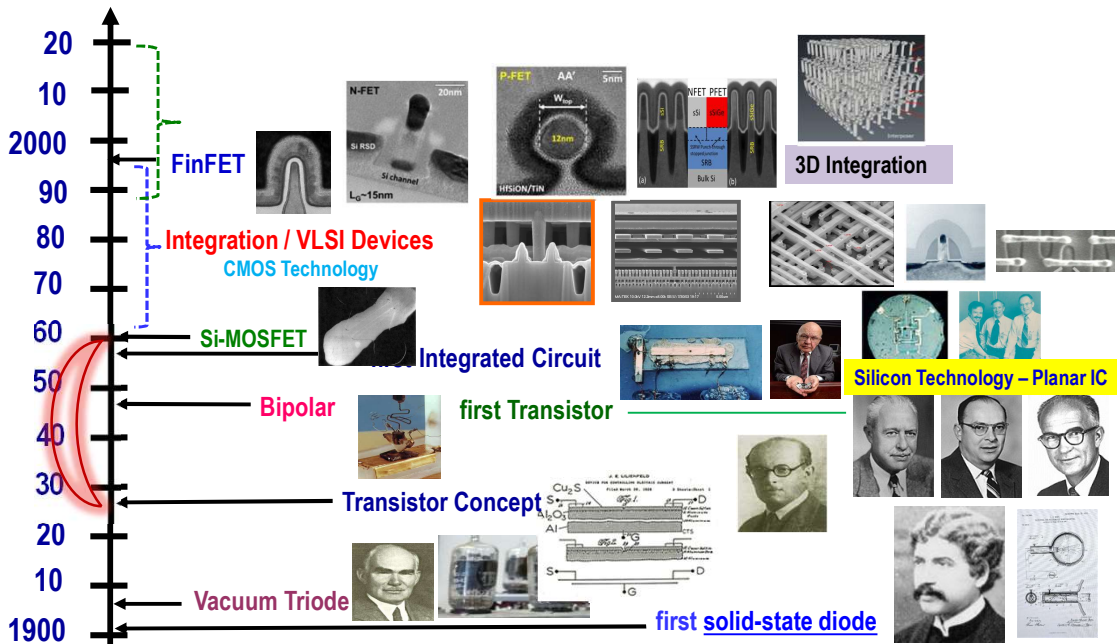
(K.-W. Lee et al, IEDM 2014)



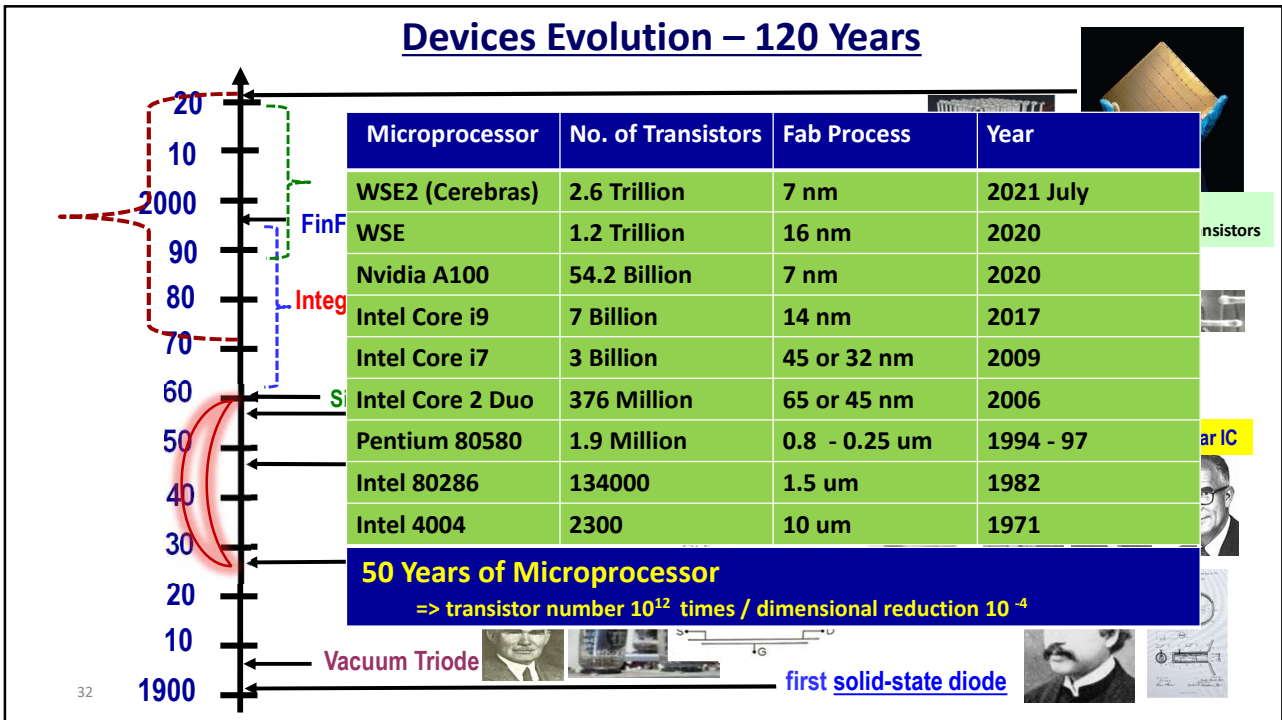
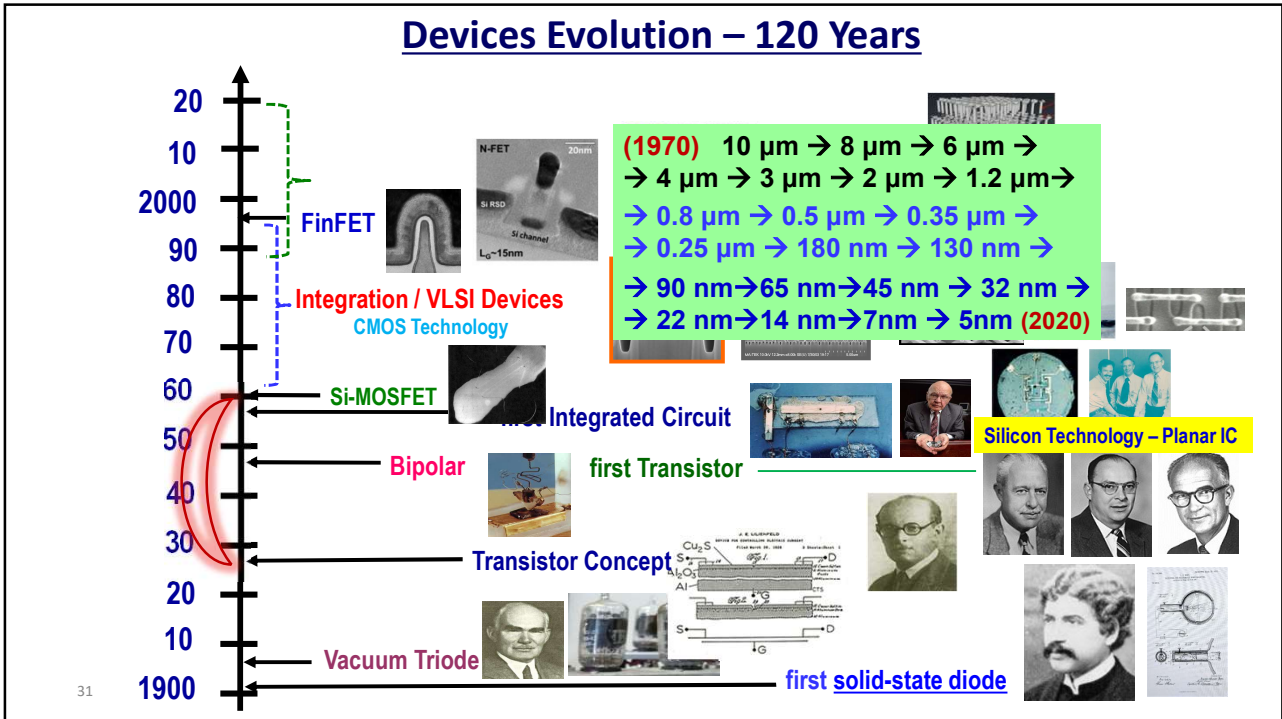
A vision of Super Chips (Source : Solid State Technology)

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### Devices Evolution

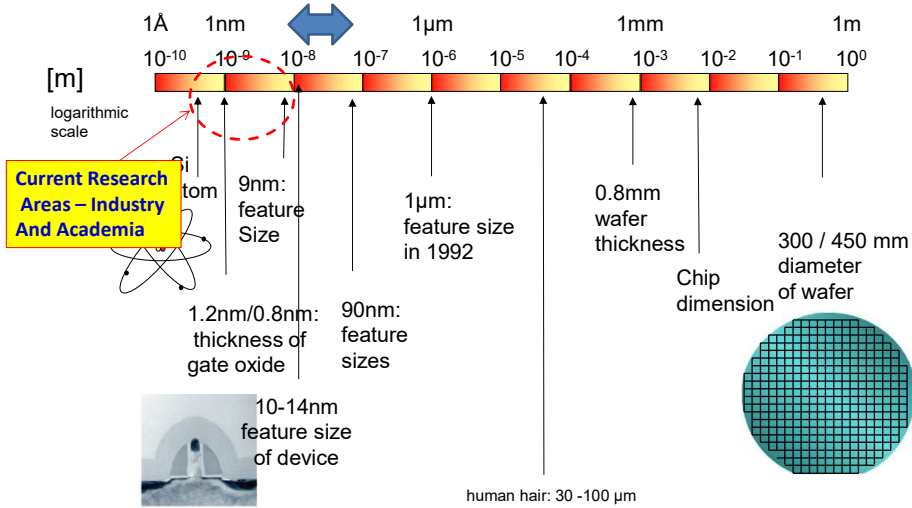


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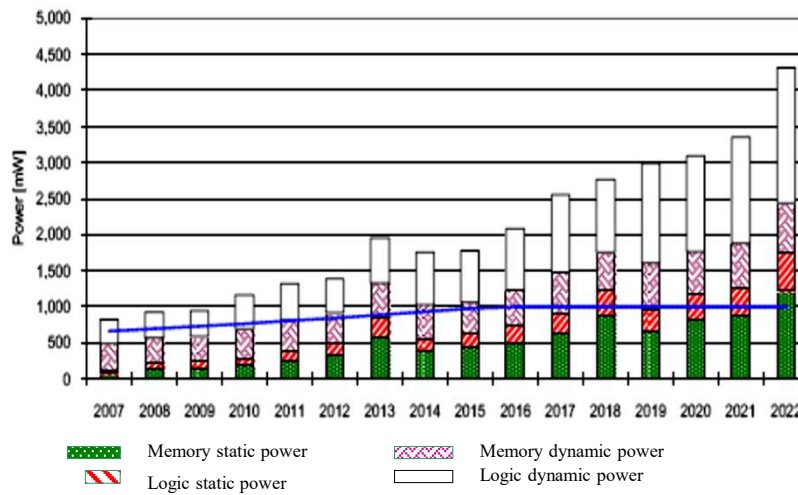


## Present Day Semiconductor (Si) Status



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## Power Consumption Trends



*(courtesy : ITRS 2008).*

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**Interaction between the channel carriers and interfaces**  
 The interaction becomes stronger as  $d$  becomes smaller with decrease in  $t_{ox}$  and  $t_{Si}$ .

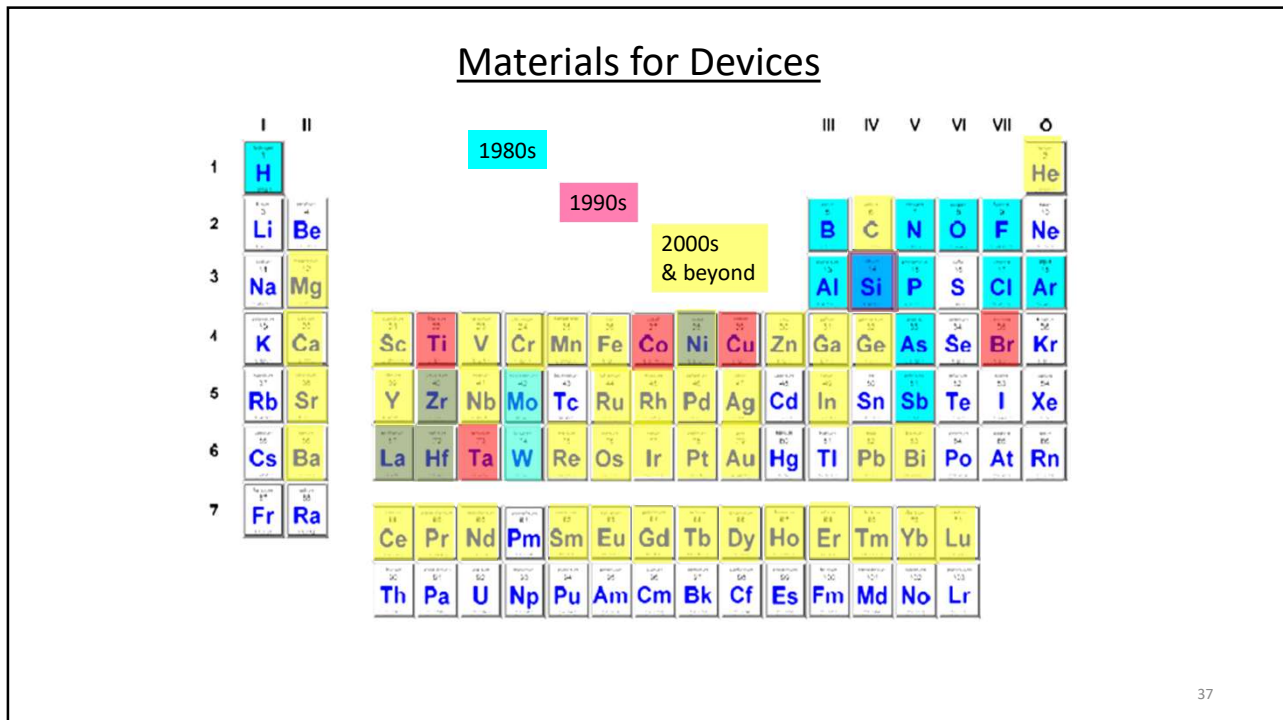
## What becomes Important ?

1928 – J E Lilienfeld

Exceptionally good interface!

1960: D. Kahng and M. Atalla

(Ref: C.H. Tung & M.K. Radhakrishnan, IEEE IPFA, 2002)



### Si Devices : Reliability Challenges - in decades

- **Major Efforts - Reliability Physics Studies (1980 – 1990)**
  - Models for *EM / SM / TDDB / HC* *( $\mu\text{m}$  devices)*
  - ESD Protection & Corrosion and Related Issues
- **Major Efforts - Process/Device Engineering(1990 - 2000)**
  - Approaches based on *WLR / DFR , etc* *(sub- $\mu\text{m}$  devices)*
  - SPC, 6-Sigma, etc – in process lines
- **New Material Challenges (2000 – 2010)**
  - High-K gate dielectrics / Cu & lowK) *(sub-100nm devices)*
  - Material Interactions / new structures
- **Interface Physics / Tools Limitations (2010 onwards)**
  - Interfaces & new failure mechanisms *(nano devices)*
  - Physical analysis challenges & tools

## OUTLINE

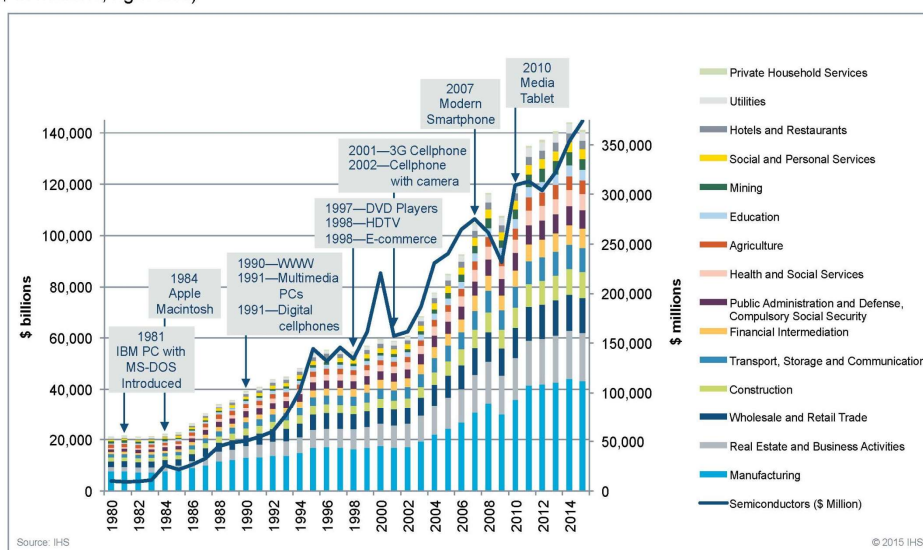
- **Electronics Evolution (devices)**
  - **Prior History and Birth of Transistor**
    - Patents 755,840 ; 1,900,018 ; 2,524,035 ; 2,569,347
  - **Concept to Reality - MOSFET - Birth of Technology**
    - Invention to Industry / Room at the Bottom
  - **Fifty, Trillion & 0.0001 – and goes on**
- **Veracity in Device Progression**
  - **Challenges continues / What becomes Important**
- ➔ • **Technology Impacts in Society and Humanity**
  - **Extended Research, Application**
  - **Transistors & Neurons – a number game**
  - **Advancements in Society and Human Interactions**

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## Moore and Impact of Devices

### Semiconductor growth tracks global output

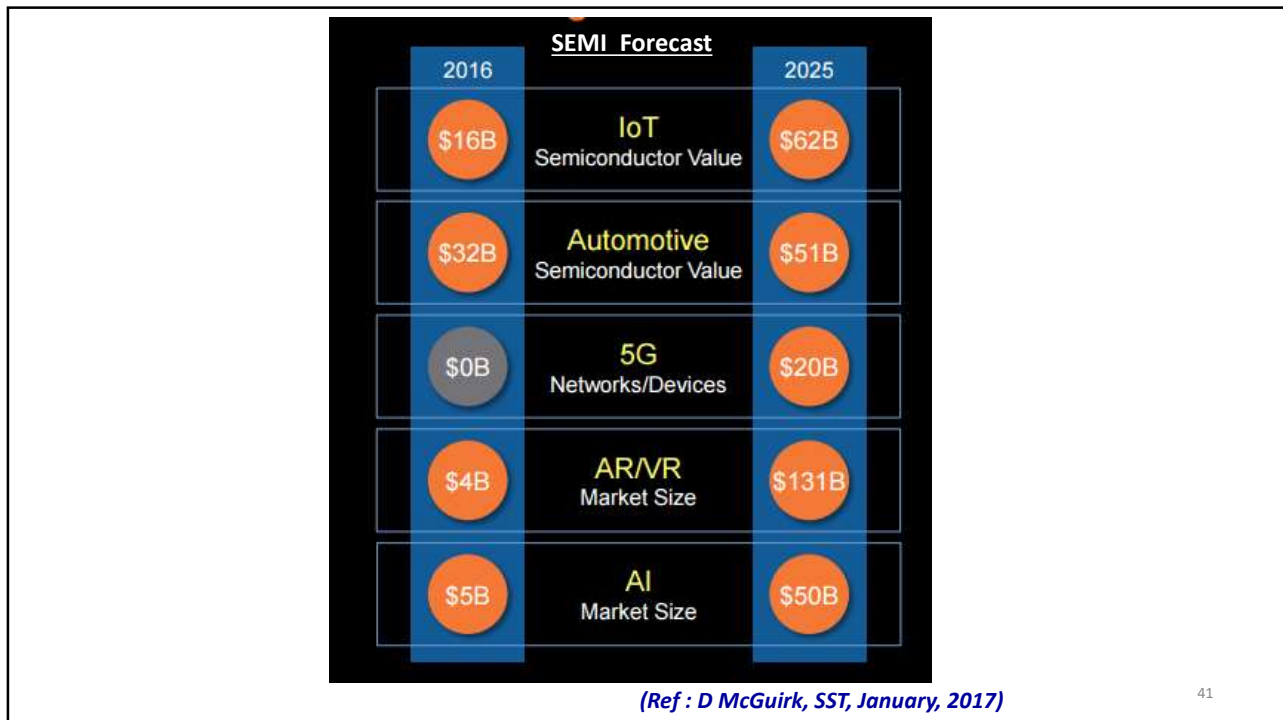
Worldwide gross output by industry (\$ in billions, left axis) and semiconductor sales (\$ in millions, right axis)



**(Source : Solid State Technology, June 2015 : 50 Years of Moore's Law)**

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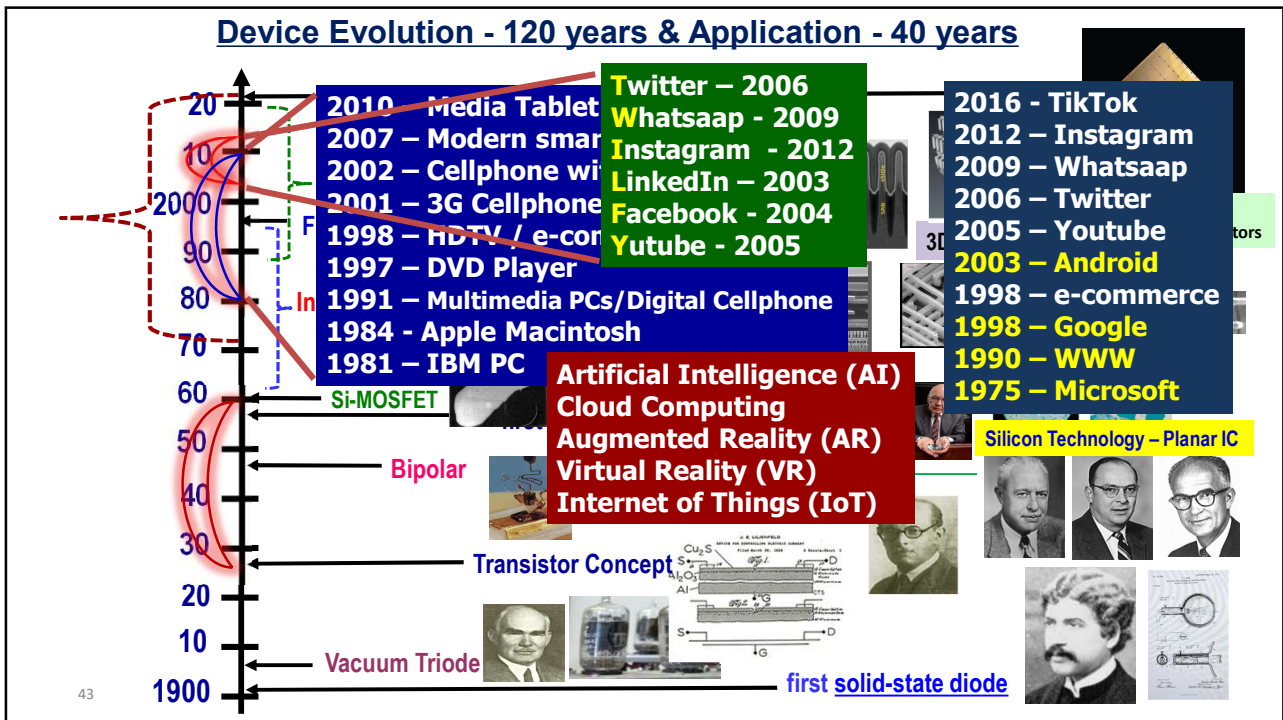




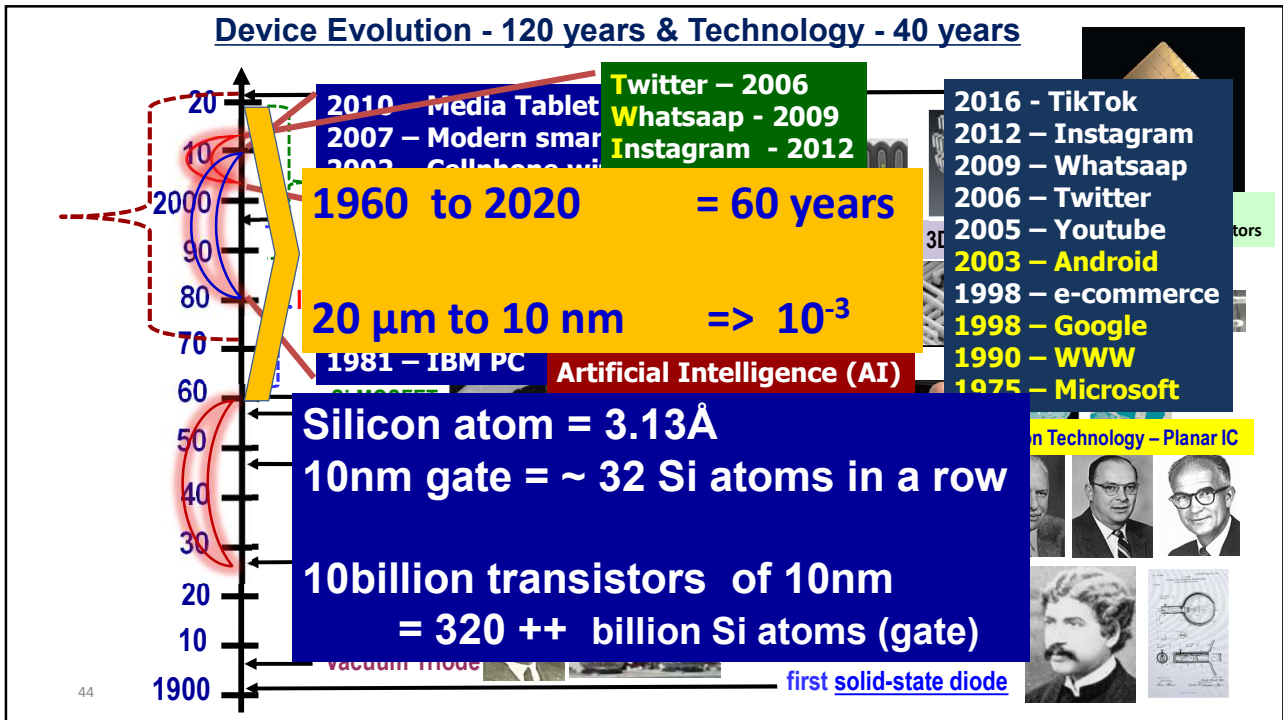
**FAB is a multidisciplinary conglomerate of**  
**Physics / Chemistry / Mathematics**  
**Economics / Commerce**  
**Engineering : Electrical / Civil / Mechanical / Electronics**  
**/Computer, etc**  
**Psychology / Physiology, etc, etc**

**Every aspect of Science & Engineering**  
**& its impact in human physiology**  
**Extended Research**  
**“Outside the Conventional Programs”**

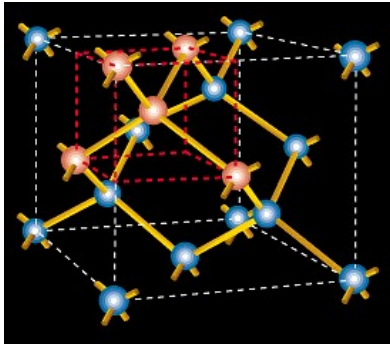
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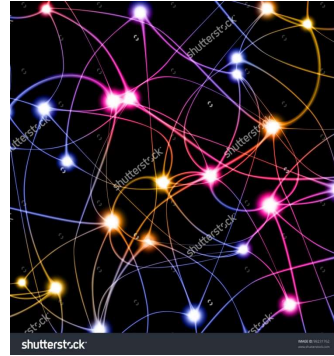
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Si Lattice structure  
Lattice Constant = 5.431Å  
Silicon Atom - 3.13Å



Digital illustration of neuron  
(Courtesy : [http://www.123rf.com/photo\\_14580711\\_digital-illustration-of-neuron.html](http://www.123rf.com/photo_14580711_digital-illustration-of-neuron.html))

**Human brain has about 100 billion neurons**  
**10nm gate IC with 10 billion transistors**

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## How Effectively the Technology is being Utilized ?

Technology advancements = > Progress

(Advancements in living conditions)

- Environment
- Empathy – towards fellow beings
- Expansion of knowledge
- Equity in living
- Excellence

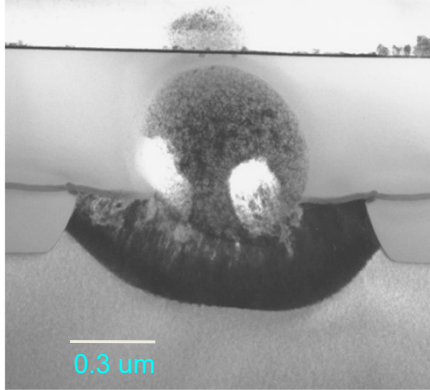
**Are we really owe all these ?**

Technology advancements also led **us** (*human beings*)

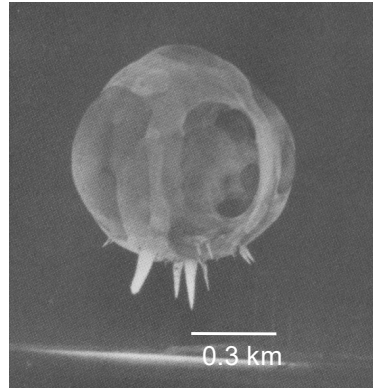
- In dwindling the **power of “observation” & “Awareness”**
- Gradual alteration from a **Social Being**
- Decline in social responsibility == > **Selfish**

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**Nature has its own game – whether Micro or Macro**



**fireball of a polyicide gate burned  
(a few days after explosion)**  
*(C H Tung & MK Radhakrishnan, 2000)*



**fireball of a 2nd generation A-bomb  
(0.006 sec after explosion)**  
*(Courtesy ; US Defence)*

***An exploding polygate burnt out location due to ESD, strikingly resembles to an atomic bomb exploding fireball.***

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**Thank You  
for  
Attending**

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