SSCS Switzerland Chapter lecture at ETH Zurich on ‘’A 55nm DDC Subthreshold MCU 2.5µA/MHz” by Dr. Marc Pons

The IEEE Solid-State Circuits Society (SSCS) Switzerland Chapter Organized a Lecture on 55nm DDC Subthreshold MCU 2.5µA/MHz at ETH Zurich on 26st June 2019 from 5:30pm to 6:30 pm.

Dr. Pons, engineer at the Swiss Center for Electronics and Microtechnology (CSEM) offered the chapter with a Lecture on sub-threshold techniques.

Figure 1 Prof. Taekwang Jang Introducing Dr. Pons

The meeting started by Prof. Taekwang Jang, the chair of Switzerland Solid-State Circuits Chapter, introducing the lecturer to the audience. The audience included students and engineers from the hosting university, local companies and research centers forming a friendly group of 16 attendees.

Figure 2 : Audience attending the lecture

The lecture started with an introduction about CSEM experience and on the various issues appearing with subthreshold circuit design such as process, voltage and temperature variation. As well as the die to die variability.

Having motivated these aspects, CSEM has been investigating on subthreshold techniques for a long time [1, 2]. The voltage scaling set the subthreshold circuit supply voltage in a range between the minimum energy point and about 500mV.

Nevertheless, CMOS Technology did not stand still. Today's FinFet, Fully-depleted Silicon-on-Insulator, or deeply-depleted channel (DDC) which offers improved opportunities such as the strong body factor. The architecture presented in [3] shows the Adaptive Dynamic Body Bias Voltage Frequency Scaling (ADVbbFS). This is applied to a 32 Bits RISC-Core alongside with RAM. The target is to operate permanently at 0.5V and take advantage of the body effect to compensate frequency over PVT to ±6%, achieving 30x frequency and 20x leakage scaling. The dynamic power consumption reaches 2.56uW/MHz for the MCU and similar for the SRAM also the leakage is 3.13nW/kB. The whole system offer Frequency-leakage configurability implemented by current-controlled adaptive body bias at a fixed supply voltage.

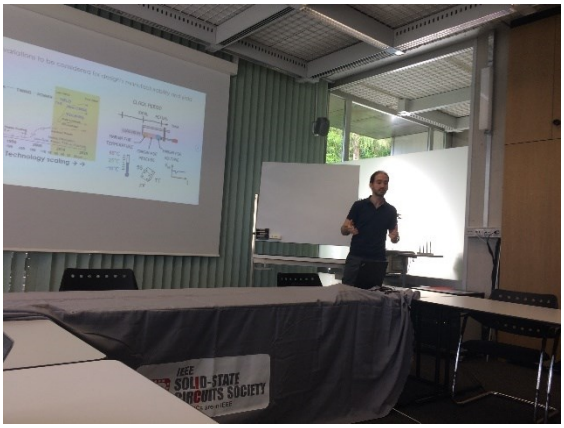

Figure 3 : Dr. Pons Conducing his lecture

The meeting was closed after fruitful round of questions and more at a round of beer after the talk. The audience was captivated by the technology aspect, and circuit techniques such as the library and memory point modification. Various aspect of the power management unit were also discussed.

REFERENCES

[1] E. Vittoz, “Weak Inversion for Ultimate Low-Power Logic,” in Low-Power CMOS Circuits, CRC Press, 2005

[2] P. Macken, M. Degrauwe, M. Van Paemel, and H. Oguey, “A voltage reduction technique for digital systems,” in 1990 37th IEEE International Conference on Solid-State Circuits, 1990

[3] A 0.5 V 2.5 uW/MHz Microcontroller with Analog-Assisted Adaptive Body Bias PVT Compensation with 3.13 nW/kB SRAM Retention in 55 nm Deeply-Depleted Channel CMOS, Marc Pons et al.

Taekwang Jang, Michel Bron, and Mathieu Coustans, For IEEE SSCS Switzerland Chapter.