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Virtual Mini Colloquia (MQ) on "75th Anniversary of Transistor Invention"

Organized by IEEE EDS Delhi Chapter (New Delhi, India)

Final Technical Program Schedule

August 22, 2022 @ 06:30 pm IST

Integrating Nanoelectronics and Optoelectronics for Healthcare Applications

Professor M. Jamal Deen

Distinguished University Professor, Senior Canada Research Chair in Information Technology
Director, Micro- and Nano-Systems Lab., President - Academy of Science, Royal Society of Canada (2015-17) &
https://www.ece.mcmaster.ca/~jamal/

August 23, 2022 @ 09:00 pm IST

Evolution of Semiconductor Devices Enabling Smart Environments and Integrated Ecosystems

Professor Samar Saha

2016-2017 President of the IEEE Electron Devices Society (EDS) and currently serving as the Senior Past President

August 24, 2022 @ 06:00 pm IST

Memory Modeling for Neuromorphic Computing

Professor Mansun Chan

Dept. of Electronic & Computer Engineering,
Hong Kong University of Science & Tech., Kowloon, Hong Kong

August 25, 2022 @ 06:00 pm IST

SOI nano-devices: Novel concepts and dimensional effects

Professor Sorin Cristoloveanu

Director of Research CNRS & Editor, Solid-State Electronics
IMEP - INP Grenoble MINATEC - 3, Parvis Louis Néel, Grenoble Cedex 1, France
https://imep-lahc.grenoble-inp.fr/fr/recherche/cristoloveanu-sorin

August 26, 2022 @ 06:00 pm IST

The Discovery of Third Breakdown: Its physical origin and Applications on Further Development of Transistor and Memory in High-k Metal-gate CMOS Generations

Prof. Steve S. Chung, *IEEE Fellow/Distinguished Lecturer*

Chair Professor, National Yang-Ming Chiao Tung University (NYCU), Taiwan

August 27, 2022 @ 06:00 pm IST

Transistor Evolution From Micro to Nano Era

Professor Joao Antonio Martino

University of Sao Paulo, LSI/PSI/USP, Sao Paulo,Brazil

August 29, 2022 @ 06:30 pm IST

Evolution of MOSFETs toward Nanoelectronic

Professor Adelmo Ortiz-Conde

https://publons.com/researcher/1201109/adelmo-ortiz-conde/metrics/

For further details kindly contact:

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Organized by IEEE EDS Delhi Chapter (New Delhi, India)

IEEE EDS Delhi Chapter organized Virtual Mini Colloquia (MQ) on "75th Anniversary of Transistor Invention" during August 22-29, 2022. Professor M. Jamal Deen, Distinguished University Professor, Senior Canada Research Chair in Information Technology delivered the inaugural talk on Integrating Nanoelectronics and Optoelectronics for Healthcare Applications. On August 23, 2022, Professor Samar Saha, 2016-2017 President of the IEEE Electron Devices Society (EDS) and currently serving as the Senior Past President delivered DL talk on Evolution of Semiconductor Devices Enabling Smart Environments and Integrated Ecosystems. On August 24, 2022, Professor Mansun Chan, Dept. of Electronic & Computer Engineering, Hong Kong University of Science & Tech., Kowloon, Hong Konggave DL talk on Memory Modeling for Neuromorphic Computing. Professor Sorin Cristoloveanu, Director of Research CNRS, IMEP - INP Grenoble MINATEC - 3, France gave a DL talk on August 25, 2022on the topic - SOI nano-devices: Novel concepts and dimensional effects. On August 26, 2022,DL talk on The Discovery of Third Breakdown: Its physical origin and Applications on Further Development of Transistor and Memory in High-k Metal-gate CMOS Generations was delivered by Prof. Steve S. Chung, Chair Professor, National Yang-Ming Chiao Tung University (NYCU), Taiwan. On August 27, 2022, DL talk on Transistor Evolution from Micro to Nano Era was delivered by Professor Joao Antonio Martino, University of Sao Paulo, LSI/PSI/USP, Sao Paulo, Brazil. Professor Adelmo Ortiz-Conde, Solid State Electronics Laboratory, Simón Bolívar University, Caracas, Venezuela delivered DL talk on August 29, 2022 on the topic - Evolution of MOSFETs toward Nanoelectronics. In all 282 delegates (IEEE Member: 68, Non Member: 214) from23 countries participated (i.e. Bangladesh, Bhutan, Brazil, Canada, China, Denmark, Egypt, France, Germany, Hong Kong SAR, India, Italy, Malaysia, Russia, Singapore, Spain, Sweden, Switzerland, Taiwan, Uganda, United Arab Emirates, United Kingdom and United States)

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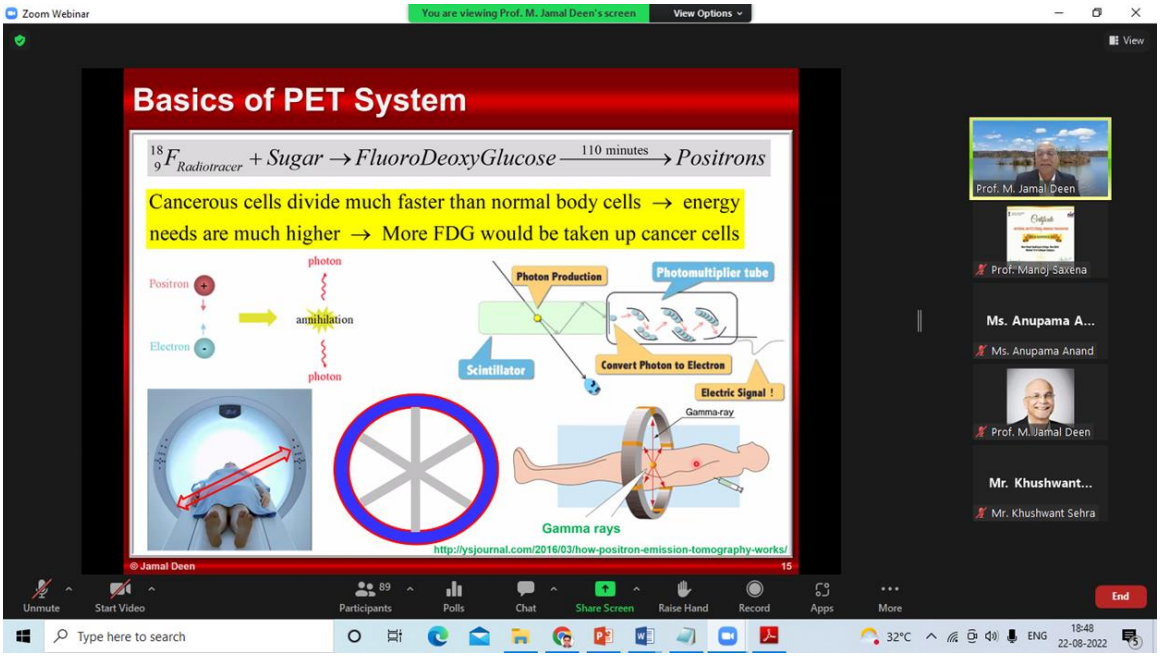

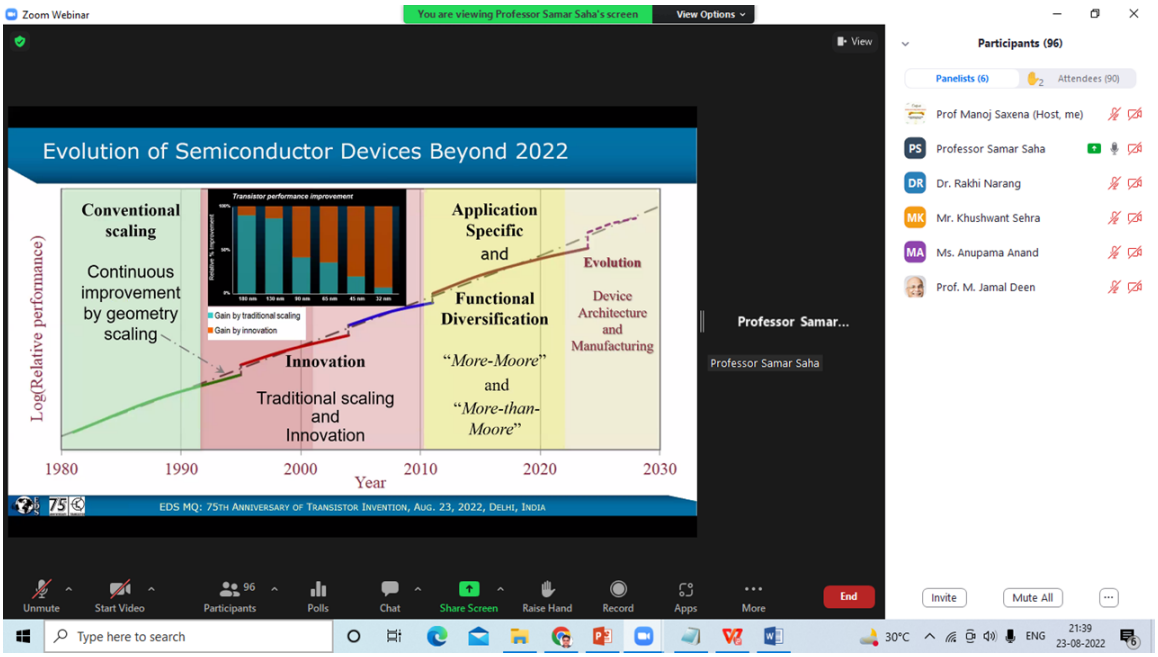

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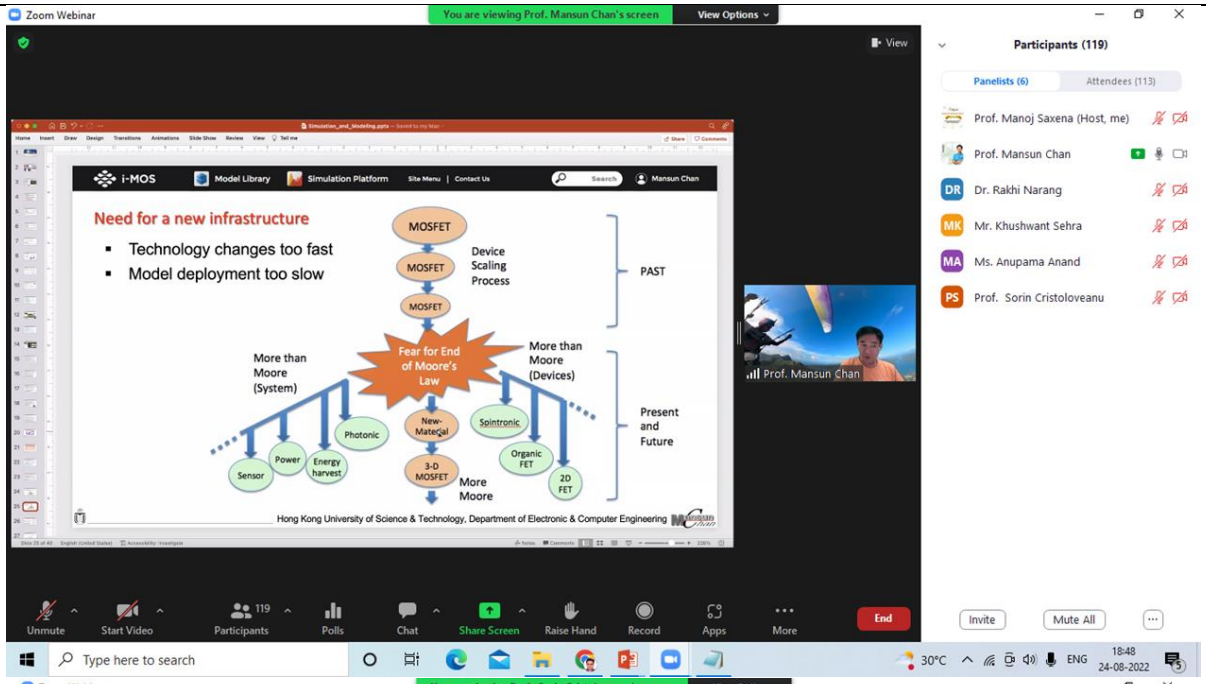

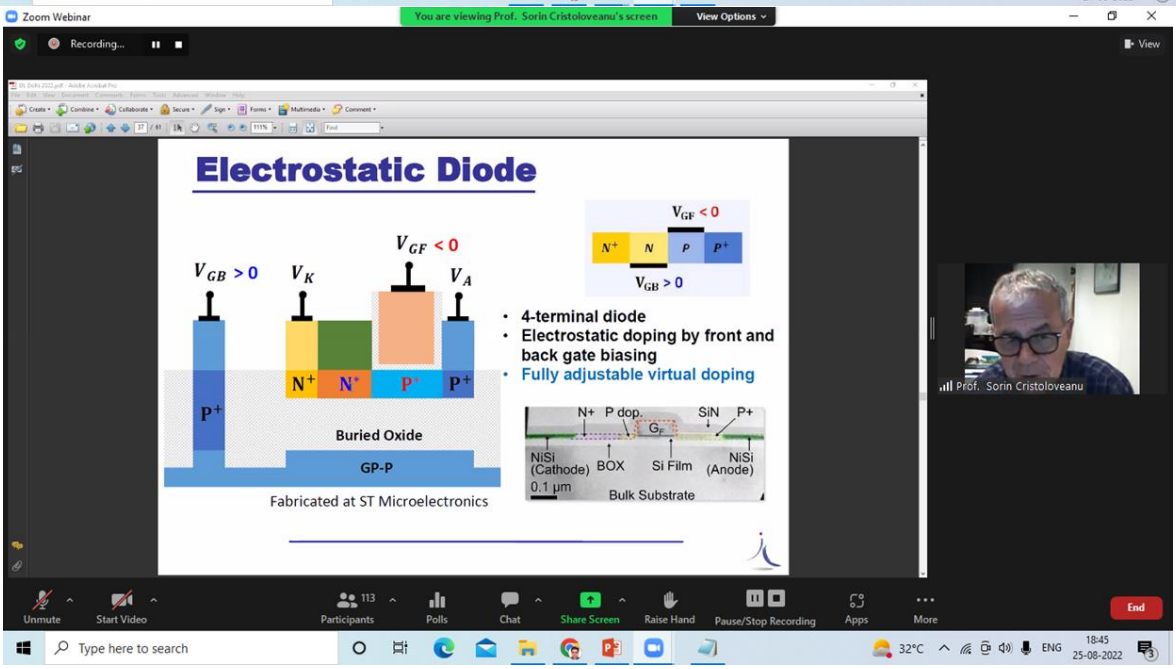

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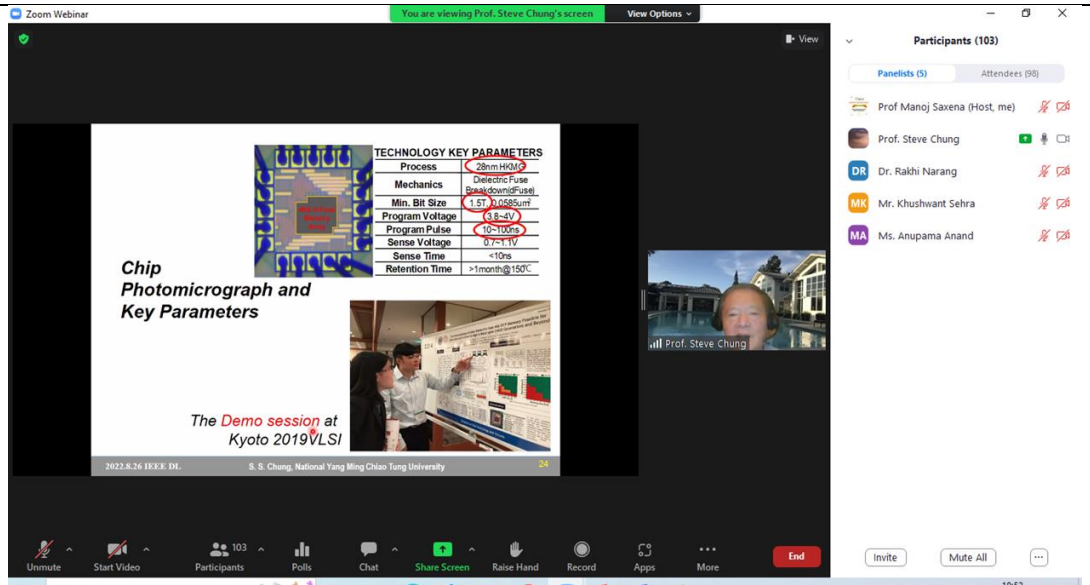

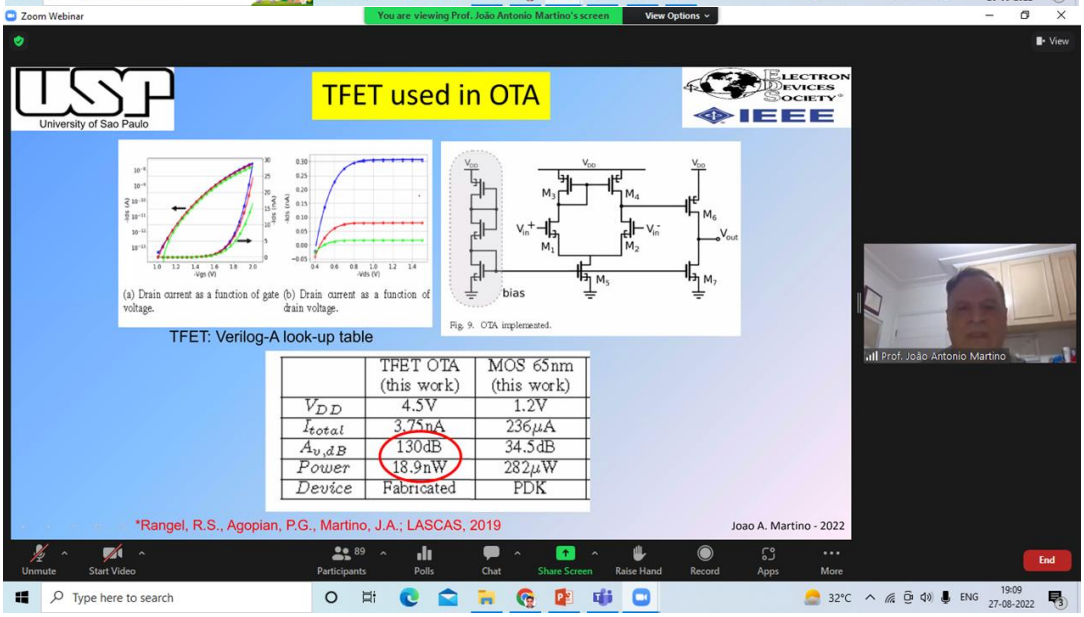

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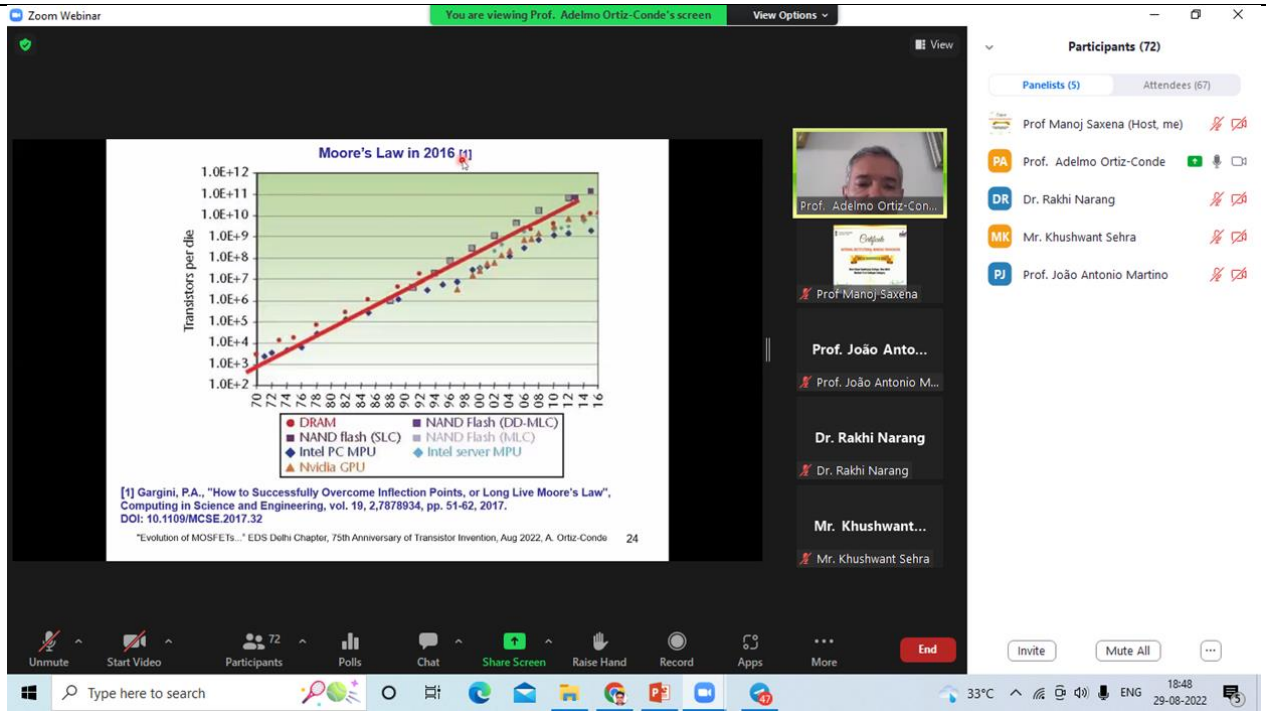

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August 22, 2022 @ 06:00 pm IST

Integrating Nanoelectronics and Optoelectronics for Healthcare Applications

M. Jamal Deen

Distinguished University Professor and Director of the Micro- and Nano-Systems Laboratory
Electrical and Computer Engineering Department & School of Biomedical Engineering
McMaster University, Hamilton, Ontario CANADA. E-mail: jamal@mcmaster.ca

Some of the grand challenges in engineering for current and future societal needs require smart sensors, many of which are constructed using nanoelectronics and optoelectronic technologies. For example, in the healthcare area, smart sensing systems are required for screening, diagnostics and monitoring of a variety of diseases and illnesses for the health of well-being of individuals. Among the diseases, cancer is one of the leading causes of death globally. However, if the cancer can be detected in the very early stages of development, then the survival rate of the patients is significantly improved, and for some cancers such as breast or prostate cancer, the survival rate approaches 100%. Further, early detection translates into improved disease management, treatment plans, and treatment outcomes at significantly reduced costs. In particular, among the different imaging techniques, positron emission tomography (PET) is demonstrated to be an very valuable tool for screening and diagnosis of cancers since the PET system is able to generate functional images to observe biological processes in the body. These systems require high precision, high temporal resolution and high contrast medical images for more accurate diagnoses. In the early days, most commercial PET systems were based on bulky photomultiplier tubes (PMTs), which lack compatibility with multi-modal PET/MRI (magnetic resonance imaging) systems. A promising solution is the integration of single-photon avalanche diodes (SPADs) with time-to-digital converters (TDCs), integrated closely together on the same wafer to form digital silicon photomultipliers (dSiPMs). These dSiPMs are capable of achieving comparable gain and speed to PMTs, while maintaining full compatibility with strong magnetic fields, lower power consumption, compact size and low cost. Our work focusses on the design of SPAD-based image sensors implemented in standard silicon technology, as it provides the lowest cost alternative, compared to SPADs in custom processes. By improving the noise performance of standard silicon SPADs with guard ring and time-gating techniques, improving photon detection efficiency (PDE) through multi-junction SPAD structures, and producing higher resolution TDCs in compact areas, our work can help in making SPAD-based sensors a new gold-standard for biomedical imaging applications.

Dr. M. Jamal Deen is currently Distinguished University Professor and Director of the Micro- and Nano-Systems Laboratory at McMaster University. He served as the **elected President of the Academy of Science**, The Royal Society of Canada in 2015-2017. His current research interests are nanoelectronics, optoelectronics, nanotechnology, data analytics and their emerging applications to health and environmental sciences. Dr. Deen's research record includes more than 650 peer-reviewed articles (about 20% are invited), two textbooks on **"Silicon Photonics- Fundamentals and Devices"** and "**Fiber Optic Communications: Fundamentals and Applications",** 6 awarded patents that have been used in industry, and 21 best paper/poster/ presentation awards. As an educator, he won the Ham Education Medal from IEEE Canada, the McMaster University President's Award for Excellence in Graduate Supervision, and McMaster Student Union Macademics' Lifetime Achievement Award for his exceptional dedication to teaching and significant contribution to student life, the community at large, and

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academia. As an undergraduate student at the University of Guyana, Dr. Deen was the top ranked mathematics and physics student and the second ranked student at the university, winning the Chancellor's gold medal and the Irving Adler prize, respectively. As a graduate student, he was a Fulbright-Laspau Scholar and an American Vacuum Society Scholar. He is a Distinguished Lecturer of the IEEE Electron Device Society for two decades. His awards and honors include the Callinan Award as well as the Electronics and Photonics Award from the Electrochemical Society; a Humboldt Research Award from the Alexander von Humboldt Foundation; the Eadie Medal from the Royal Society of Canada; McNaughton Gold Medal (**highest award for engineers**), the Fessenden Medal, and the Gotlieb Computer Award, all from IEEE Canada. In addition, he was awarded the four honorary doctorate degrees in recognition of his exceptional research and scholarly accomplishments, exemplary professionalism and valued services. Dr. Deen has been elected by his peers as Fellow/Academician of twelve national academies and professional societies including The Royal Society of Canada (**FRSC**) - The Academies of Arts, Humanities and Sciences of Canada (**the highest honor for academics, scholars and artists in Canada**); Academician (Foreign Member) of The Chinese Academy of Sciences (A-CAS, **China's highest national honor in the area of science and technology and highest academic title**); The World Academy of Sciences (**FTWAS**), National Academy of Sciences India (**FNASI-Foreign**); The Institute of Electrical and Electronic Engineers (**FIEEE**); The American Physical Society (**FAPS**); and The Electrochemical Society (**FECS)**. In 2018, he was elected to the **Order of Canada, the highest civilian honor awarded by the Government of Canada**.

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August 23, 2022 @ 09:00 pm IST

Evolution of Semiconductor Devices Enabling Smart Environments and Integrated Ecosystems

Samar K. Saha

Prospicient Devices, Milpitas, CA 95035 USA

Abstract–The microelectronics device technology has made an unprecedented impact on modern society by continuous evolution of transistor architecture and disruptive innovation of integrated circuit (IC) fabrication processes. Since the mid-1970s, the global race to continuous miniaturization of silicon metal-oxide-semiconductor (MOS) field-effect-transistor (FET) devices along with innovative complementary MOS (CMOS) manufacturing technology led to high performance, low power, high density, and low-cost very large scale integrated (VLSI) circuits and systems. And for every new generation of scaled CMOS device technology, the performance of ICs continued to improve with decreasing manufacturing cost. The production of high performance and low-cost ICs led to the creation of the Internet to enabling wireless communications; online healthcare; smart-homes with digital security, energy-saving and self-service-call appliances, and infotainment and entertainment; mobile computing; autonomous vehicles; industrial automation, and so on. In this effort, the semiconductor devices have evolved from the point contact transistors to the state-of-the art ultra-thin-body FETs. And, the ability to fabricate billions of individual components on a few cm^2 area has enabled an integrated digital ecosystem with a shared user interface. This talk presents a brief overview of the continuous evolution of the IC device technology enabling smart environments and integrated ecosystems.

Samar Saha has served as the 2016-2017 President of the IEEE Electron Devices Society (EDS). Currently, he is the Chief Scientist at Prospicient Devices and an Adjunct Professor in the Electrical Engineering (EE) department, Santa Clara University, California, USA. Since 1984, he has worked in various technical and management positions at National Semiconductor, LSI Logic, Texas Instruments, Philips Semiconductors, Silicon Storage Technology, Synopsys, DSM Solutions, Silterra USA, and SuVolta. In academia, he was an EE faculty at Southern Illinois University, Carbondale, Illinois; Auburn University, Alabama; the University of Nevada at Las Vegas, Nevada; and the University of Colorado at Colorado Springs, Colorado. He has authored over 100 research papers; two (sole-authored) books entitled, *FinFET Devices for VLSI Circuits and Systems*, CRC Press, Florida (2020) and *Compact Models for Integrated Circuit Design*: *Conventional Transistors and Beyond*, CRC Press, Florida (2015); one book chapter on Technology Computer-Aided Design (TCAD); and holds 12 US patents. His book on FinFET has been translated in Chinese language with title, *Nanoscale integrated Circuits FinFET Device Physics and Modeling* and published in February 2022. Dr. Saha received the PhD degree in Physics from Gauhati University and an MS degree in Engineering Management from Stanford University. He is a distinguished Lecturer of IEEE EDS, an IEEE Life Fellow, and a Fellow of the Institution of Engineering and Technology (IET), UK. He is the recipient of 2021 IEEE EDS Distinguished Service Award.

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August 24, 2022 @ 06:00 pm IST

Memory Modeling for Neuromorphic Computing

Mansun Chan

Alex Wong Siu Wah Gigi Wong Fook Chi Professor of Engineering and Chair Professor

Dept. of ECE, Hong Kong University of Science & Technology,

Clear Water Bay, Kowloon, Hong Kong

E-mail: mchan@ust.hk

Abstract: The recent development in neuromorphic computing has generated a strong demand for memory array simulation. However, the conventional approach to simulate logic circuit is not memory friendly and memory models have to work around a number of fundamental limitations before they can be used in circuit simulator. Furthermore, there is a lot of confusion in the hardware requirement between deep-neural network versus neuromorphic computing. In this presentation, I will discuss the simulation infrastructure required for neuromorphic computing and the approach to develop memory models that can handle detail temporal variations with respect to in-coming signals and data.

Dr. Mansun Chan is the Alex Wong Siu Wah Gigi Wong Fook Chi Professor of Engineering and Chair Professor of the Department of Electronic and Computer Engineering at the Hong Kong University of Science and Technology. He received his PhD from the University of California at Berkeley and his expertise is in the area of emerging semiconductor devices. In addition to academic research, his has been actively involved in many entrepreneurship and educational activities. In 2015-2017, he was the Chairman the IEEE EDS Education Committee, and he started a series of electronic circuit construction training modules and competitions to primary and secondary school students. These activities have become the main vehicle for IEEE to reach out to young engineers. More recently, he has launched an animation based MOOC class on semiconductor devices, which has been widely received by learners around the world. As a result of his educational activities, he has received the teaching award three times from the Engineering School of HKUST, and the IEEE EDS Education Award “for pioneering innovative approaches in electronic engineering education”. He is a Distinguished Lecturer and Fellow of IEEE.

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August 25, 2022 @ 06:00 pm IST

SOI nano-devices: Novel concepts and dimensional effects

Sorin Cristoloveanu

IMEP-LAHC, Grenoble INP Minatec, UMR 5130,

3 parvis Louis Néel, CS 50257, 38016 Grenoble Cedex 1, France

Abstract

Down-scaling requires devices with sub-10 nm thickness which are naturally fully depleted. The operation of nanosize MOSFETs on SOI benefits from a number of intrinsic mechanisms – interface coupling, back-gate biasing, volume inversion, supercoupling – that will be briefly reviewed. The short-channel and thin-body effects add complexity. The 'electrostatic doping', also defined as gate-induced charge, is a unique feature of nano- structures. In an ultrathin SOI device, a positive gate voltage produces electrons that spread in the entire body such as the original undoped film suddenly behaves as an N-doped region. This volume inversion/accumulation effect is very different from the charge-sheet interface layer formed in bulk semiconductors. Changing the polarity of the gate bias turns the body into a P-type region, more or less doped according to the gate will. This fascinating doping metamorphosis enables novel and reconfigurable devices with unrivalled flexibility. For example, the band-modulation devices (FED, Z^2-FET, Z^3-FET) consist of successive N and P regions that are electrostatically doped to emulate a virtual NPNP thyristor. The operation of sharp-switching devices like tunneling FET (TFET), I-MOS and Electron-Hole Bilayer TFET also relies on electrostatic doping. Another interesting example is the Hocus-Pocus diode activated in ultrathin SOI films by simply biasing the front and back gates with opposite polarities. Adjacent electron and hole populations form a virtual P-N junction. The current-voltage characteristics reveal similarities and major differences with those of conventional P-N diodes with ion-implanted doping. A distinct merit of the virtual diode is the endless possibility of adjusting the concentration of electrostatic doping via the gates. An astonishing application is the dopingless Esaki diode with band-to-band tunneling. The physics, architecture and applications of the most promising devices with electrostatic doping will be discussed.

Sorin Cristoloveanu received the PhD (1976) in Electronics and the French Doctorat ès-Sciences in Physics (1981) from Grenoble Polytechnic Institute, France. He is currently Emeritus Director of Research CNRS. He also worked at JPL (Pasadena), Motorola (Phoenix), and the Universities of Maryland, Florida, Vanderbilt, Western Australia, Kyungpook (World Class University project, Korea), and Nanjing, China. He served as the director of the LPCS Laboratory and the Center for Advanced Projects in Microelectronics, initial seed of Minatec center. He authored more than 1,100 technical journal papers and communications at international conferences (including 170 invited contributions). He is the author or the editor of 36 books, and he has organized 35 international conferences. His expertise is in the area of the electrical characterization and modeling of semiconductor materials and devices, with special interest for silicon-on-insulator structures. He has supervised more than 110 PhD completions. With his students, he has received 17 Best Paper Awards, an Academy of Science Award (1995), and the Electronics Division Award of the Electrochemical Society (2002). He is a Life Fellow of IEEE, a Fellow of the Electrochemical Society, Doctor Honoris Causa of the University of Granada, and Editor of Solid-State Electronics. He is the recipient of the IEEE Andy Grove award 2017, the most prestigious distinction in the field of electronic components, for contributions to 'silicon-on-insulator technology and thin body devices'. This is actually the topic of his recent book https://www.sciencedirect.com/book/9780128196434/fully-depleted-silicon-on-insulator#book-info

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The Discovery of Third Breakdown: Its physical origin and Applications on Further Development of Transistor and Memory in High-k Metal-gate CMOS Generations

Steve S. Chung

Chair Professor, National Yang Ming Chiao Tung University

IEEE Fellow/EDS Distinguished Lecturer

Abstract- There are two major well known breakdowns in CMOS transistor's history. Not until 2015, a world first observation of the breakdown, different from soft- and hard-breakdown, named dielectric fuse breakdown, dFuse, was discovered when the CMOS technology was moving into HKMG era. In this talk, we will introduce from the inception of the Ig-RTN measurement on the understanding of breakdown in 2008 and briefly the describe the fundamentals of RTN technique. Recently, a 2.0 version of this Ig RTN measurement, named Ig-transient, was successfully developed to understand the breakdown path in HKMG transistors and the associated reliability, from which the first discovery of the third breakdown was unveiled. It was then directed towards the development of nonvolatile memory applications. In the end, we will use it to demonstrate how to use this technique to understand the filament formation in ReRAM.

Prof. Steve Chung received the Ph.D. degree in Electrical Engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA. His Ph. D. advisor is the world famous CMOS co-inventor, Prof. C. T. Sah. Currently, he is NYCU and UMC Chair Professor at National Yang-Ming Chiao-Tung University (NYCU). He has been the Dean of International Affairs Office and Executive Director of school level research center, (2007-2008). He was a visiting professor with Stanford University, University of California-Merced, giving course lectures successively. He has also been the consultant of two world largest IC foundries, TSMC and UMC. His current research interests include- nanoscale CMOS, flash memory, resistance Memory Technologies-from storage to AI applications. He was the first speaker (from Taiwan) to present the paper at VLSI Technology symposium in 1995, and has 35+ times presentations at IEDM/VLSI as corresponding author and with more than 300+ publications and also holds more than 40 patents. He is an IEEE Life Fellow, current IEEE Distinguished Lecturer, Senior Editor of Applied Physics-A (Springer), and with past involvements as IEEE EDS Board of Governor for more than 12 years, EDS Regions/Chapters Chair, and Editor of IEEE J-EDS, EDL, guest editor of TDMR. Among numerous awards, he has been a recipient of Three-time Outstanding Research Award (National Science Council), Pan Wen Yuan award (2013) to recognize outstanding researcher in Taiwan on semiconductors, Lifetime achievement award as National Inventors (2019) etc.

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Virtual Mini Colloquia (MQ) on "75th Anniversary of Transistor Invention"

Organized by IEEE EDS Delhi Chapter (New Delhi, India)

August 27, 2022 @ 06:00 pm IST

Transistor Evolution From Micro to Nano Era

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ABSTRACT

The Field Effect Transistor (FET) is the main device for the integrated circuits era. This presentation starts with an overview of the main progress steps of FET evolution and finish with a discussion of possible FET devices for future technologies. The starting point was the Lilienfeld patent filled in 1925 that was not fabricated due to the technological difficulties. Experimental Metal-Oxide-Semiconductor FET (MOSFET) was only obtained in 1960. The historical basic MOSFET was composed by Aluminum (Metal), silicon dioxide (Oxide) and Silicon (Semiconductor). In order to follow the Moore´s Law evolution and to avoid the short channel effects the basic MOSFET have to be upgraded using new materials and new device structures in order to improve the electrostatic control between gate and channel. The MOSFET has been upgraded with different gate electrode like polysilicon heavily doped, TiN and TaN. The gate oxide has also been replaced to high-k dielectrics like SiON, HfSiON and HfO_2 in order to avoid gate leakage current. Finally, the well-known silicon channel has also been modified to strained silicon (uniaxial and biaxial), SiGe, Ge, InGaAs in order to boost the carrier's mobility. The MOSFET structure has been improved from Bulk MOSFET to SOI (Silicon-on-Insulator) MOSFET and later from single gate to multiple-gate devices like FinFET, nanowire, nanosheet and forksheet devices for enhancing the electrostatic coupling. New type of device conduction mechanism like Tunnel-FET devices (TFETs) have been studied to replace the conventional drift-diffusion conduction mechanisms due to the benefits obtained by tunneling conduction. The analog behavior of these new devices will also be discussed.

Joao Antonio Martino (SM'07) was born in Sao Paulo, Brazil, in 1959, preserving both nationalities: Brazilian and Italian. He received the degree in electrical engineering from FEI University Center, in 1981, and starting on microelectronics field since 1982 on graduated program, when he received the Master (NMOS technology) and Ph.D (CMOS technology) degrees in 1984 and 1988, respectively, in electrical engineering (microelectronics area) from University of Sao Paulo (USP), Brazil. He worked as a post-doctoral researcher in joint collaboration between Imec (Interuniversity Microelectronic Center)/KU Leuven (Catholic University of Leuven), Belgium and University of Sao Paulo, from 1989 to 1994 in SOI technology and devices. In 1992, he joined the Department of Electronic Systems of University of Sao Paulo, Brazil, where he has been full Professor since 2005. He is also head of CMOS SOI group since 1990 and head of Laboratory of Integrated Systems since 2017, both from University of São Paulo. He was also the head of Department of Electronic Systems from University of Sao Paulo from 2009 to 2013. He is author and co-author of more than 600 technical journal papers and conference proceedings and author/editor of 7 books. He completed the supervision of 64 graduate students, 35 masters and 21 PhDs as main supervisor and 6 masters and 2 PhDs as co-supervisor. He introduced the study of SOI devices characterization and technology in Brazil in 1990. He was the head of the first 3D transistor (triple gate FinFET) fabricated in South America in 2012. His current research interests include electrical characterization and fabrication of SOI, multiple gate (FinFET, nanowire and nanosheet), Tunnel-FET, Reconfigurable FET and Bio-FET devices. The application of new transistors in basic analog circuits is also studied. He is Senior Member of IEEE, Member of Electrochemical Society. He was Vice-Chair of Region 9 Subcommittee for Regions/Chapters of IEEE Electron Device Society (EDS/IEEE) from 2013 to 2018. He has been Chapter Chair of South Brazil Session of EDS/IEEE since 2007 and Distinguished Lecturer of EDS/IEEE since 2008.

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August 29, 2022 @ 06:30 pm IST

Evolution of MOSFETs toward nanoelectronics

Adelmo Ortiz-Conde

Solid State Electronics Laboratory, Simón Bolívar University, Caracas, Venezuela

We review the origins, evolution and present status of MOSFETs, which has been the dominant semiconductor device in electronics applications for more than 4 decades. The conceptual invention of MOSFET, by Lilienfeld in 1928, and the end of World War II, in 1945, inspired Bell Labs to research into semiconductors. Bardeen and Brattain, who were working in the Semiconductor Sub-Group at Bell Labs, fabricated the first point contact transistor in December,1947. This achievement motivated Shockley, who was the group leader, to invent the bipolar junction transistor in January 1948. Bardeen, Brattain and Shockley received the Nobel Prize in 1956 “for their discovery of the transistor effect.” After solving oxide reliability problems, the MOSFET was fabricated in 1960 by Kahng and Atalla. The invention of CMOS, by Wanlass and Sah in 1963, made the MOSFET to be the most commonly used device in digital applications. The transistors have been miniaturized for more than fifty years, following Moore’s Law from 1965, and they are now approaching their final limits in the nanometer regime. Recent innovations, such as strained silicon and high-k metal gates are being used in modern MOSFETs. New device designs as FinFETS, Nanowire and Nanosheet are now being fabricated.

Adelmo Ortiz-Conde received the professional Electronics Engineer degree from Universidad Simón Bolívar (USB), Caracas, Venezuela, in 1979 and the M.E. and Ph.D. from the University of Florida, Gainesville, in 1982 and 1985, respectively. From 1979 to 1980, he served as an instructor in the Electronics Department at USB. In 1985, he joined the technical Staff of Bell Laboratories, Reading, PA, where he was engaged in the development of high voltage integrated circuits. In 1987, he returned to the Electronics Department at USB where he was promoted to Full Professor in 1995. He was on sabbatical leave at University of Central Florida (UCF), Orlando, from January to August 1994, and again from July to December 1998. He also was on sabbatical leave at “Centro de Investigaciones y Estudios Avanzados” (CINVESTAV) National Polytechnic Institute (IPN), Mexico City, Mexico, from October 2000 to February 2001. He has coauthored one textbook, Analysis and Design of MOSFETs: Modeling, Simulation and Parameter Extraction (2012 Springer reprint of the original 1st ed. 1998, http://dx.doi.org/10.1007/978-1-4615-5415-8), over 190 international technical journal and conference articles (including 20 invited review articles). His present research interests include the modeling and parameter extraction of semiconductor devices. Dr. Ortiz-Conde is an EDS Distinguished Lecturer and the Chair of IEEE’s CAS/ED Venezuelan Chapter. He was editor of IEEE Electron Device Letters in the area of Silicon Devices and Technology from 2009 to 2018. He was the Region 9 Editor of IEEE EDS Newsletter from 2000 to 2005. He is a Member of the Editorial Advisory Board of various technical journals: Microelectronics and Reliability, “Universidad Ciencia y Tecnología” and “Revista Ingeniería UC”. He regularly serves as reviewer of several international journals and conferences. He was one of the founders of the first IEEE International Caracas Conference on Devices, Circuits, and Systems (ICCDCS) in 1995. In order to make it more international, this conference changed its name to “International Caribbean Conference on Devices, Circuits, and Systems (ICCDCS)” in its sixth edition in 2006. Since 2019, this conference has been sponsored by the IEEE Electron Devices Society (EDS) under the name of “IEEE Latin America Electron Devices Conference (LAEDC)”.

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