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Digital RF PLLs for Wi-Fi: Present and Future

Francesco Brandonisio

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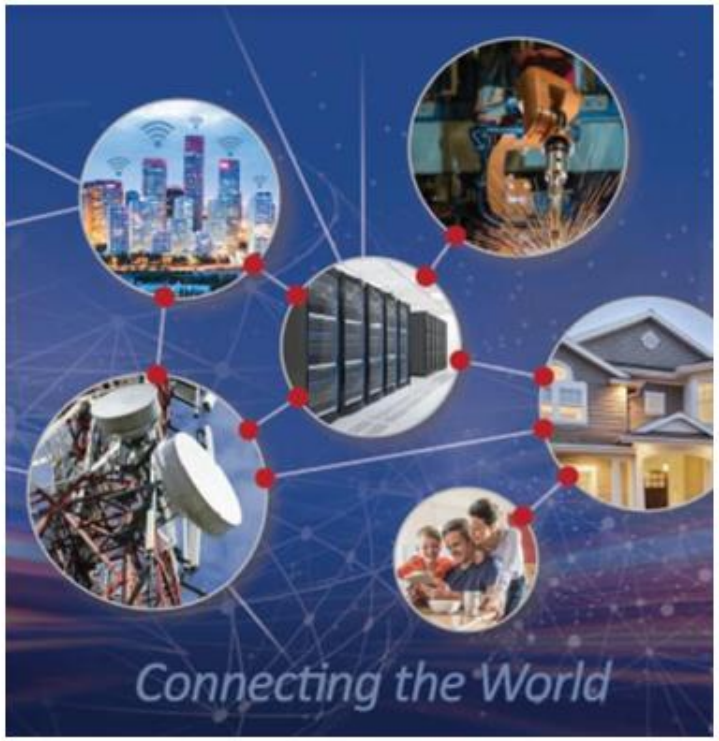
IEEE

Who are We?

- MaxLinear is a leading provider of highly integrated radio-frequency (RF), analog and mixed-signal semiconductor solutions for access and connectivity, wired and wireless infrastructure, and industrial and multi-market applications. The company's innovative solutions help shape the future of networking and communications technology



Founded
2003

NYSE
MXL

MAXLINEAR

Leading Semiconductor Supplier for the Broadband, Connectivity, and Infrastructure Markets

Global Scale for R&D, Operations and Customer Support

2003	2010	1500+	2500+	$1B+
Founded	IPO	Employees	Patents	2022 Est. Sales

MaxLinear Business Groups

Connectivity & Access

- AnyWAN Gateway Processors
- Cable Broadband
- PON
- xDSL/Copper
- Wi-Fi
- G.hn
- MoCA

Optical Interconnects

- Data Center Connectivity
- Optical Metro/Long Haul

Wireless Infrastructure

- Radio Head Transceivers
- Microwave & Millimeter Wave Modems
- Microwave Transceivers
- MaxLIN Linearization

High Performance Analog & Accelerators

- Power Management
- Interface
- Accelerators
- Ethernet
- Voice

MaxLinear Austria Overview

MaxLinear Austria GmbH

R&D

- System Engineering for RF/MS
- RF Design
- Analog/Mixed Signal Design
- Digital Systems
- CAD and IT Support

OPS

- Product Engineering
- Test Development

- MaxLinear acquired in August 2020 the Connected Home business from INTEL – the team in Austria was part of it
- MaxLinear Austria is represented by a team of 90 employees with excellent skills in CMOS IC design, verification and test
- Development focus is on communication systems, eg. Cable, Ethernet, PON, VoIP, WIFI, G.Fast

Content [1h and 40min]

Part 1: **Basics** [45 min]

- Background
- PLL Architectures
- Fundamental Design Considerations on Transfer-functions
- Design Considerations on PLL bandwidth and Fractional-N Spur

Break [10 min]

Part 2: **Wi-Fi** and **State-of-the-Art** [45 min]

- Wi-Fi Requirements
- State-of-the-Art
- Techniques to Advance the State-of-the-Art

Background

Application

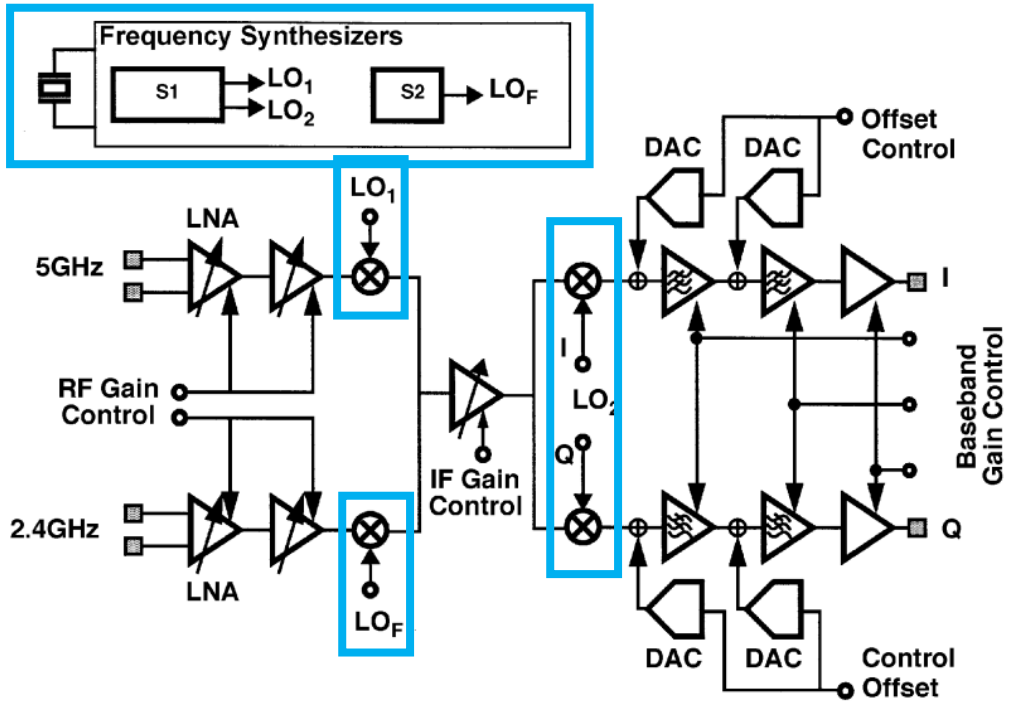


Fig. 3. Dual-band receiver block diagram.

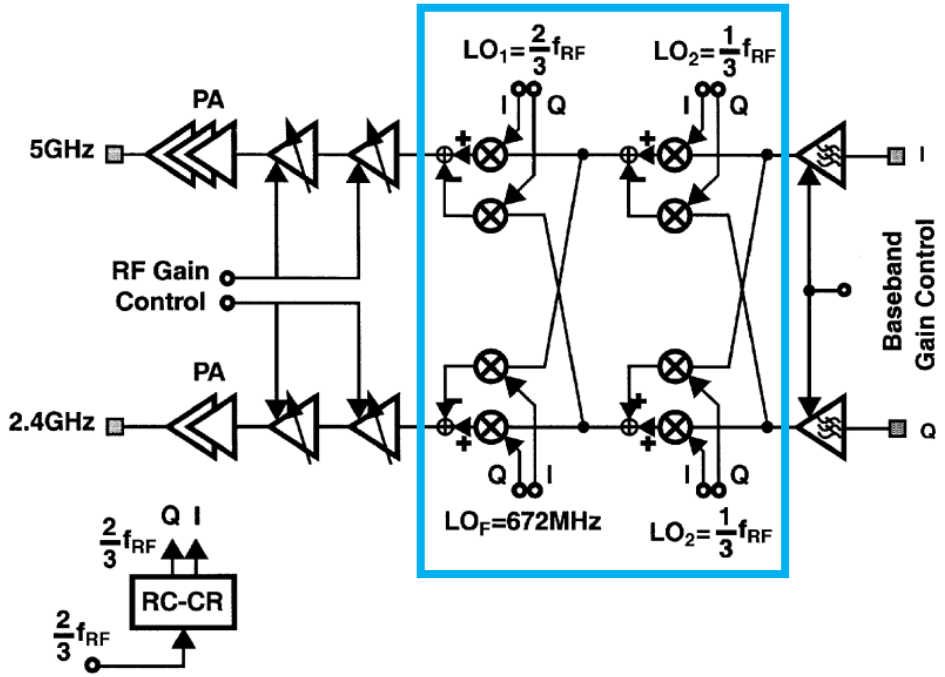


Fig. 7. Dual-band transmitter block diagram.

- A Phase-Locked-Loop (PLL) is used as a Local-Oscillator (LO) in a Wi-Fi transceiver [1]

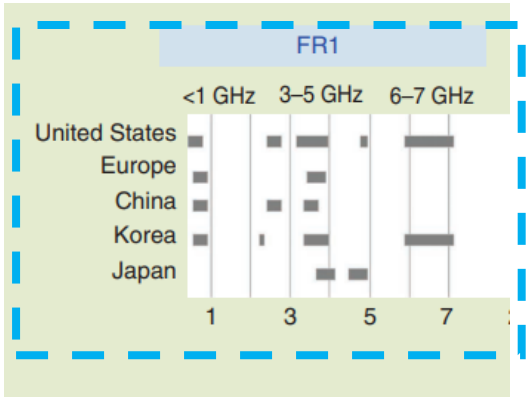
Wi-Fi 6 and 5G-Communication [2, 3]

Wi-Fi Generations

Generation	IEEE Standard	Maximum Linkrate (Mbit/s)	Adopted	Radio Frequency (GHz)[1]
Wi-Fi 7	802.11be	40000	TBA	2.4/5/6
Wi-Fi 6E	802.11ax	600 to 9608	2020	2.4/5/6
Wi-Fi 6			2019	2.4/5

Modulation and coding schemes

MCS index[i]	Modulation type	Coding rate	Data rate (Mbit/s)[ii]							
			20 MHz channels		40 MHz channels		80 MHz channels		160 MHz channels	
			1600 ns GI[iii]	800 ns GI	1600 ns GI	800 ns GI	1600 ns GI	800 ns GI	1600 ns GI	800 ns GI
0	BPSK	1/2	8	8.6	16	17.2	34	36.0	68	72
1	QPSK	1/2	16	17.2	33	34.4	68	72.1	136	144
2	QPSK	3/4	24	25.8	49	51.6	102	108.1	204	216
3	16-QAM	1/2	33	34.4	65	68.8	136	144.1	272	282
4	16-QAM	3/4	49	51.6	98	103.2	204	216.2	408	432



5G FR2 Band	Uplink/Downlink (GHz)	Channel Bandwidth (MHz)
N257	TDD 26.5 – 29.5	50, 100, 200, 400
N258	TDD 24.25 – 27.5	50, 100, 200, 400
N259	TDD 39.5 – 43.5	50, 100, 200, 400
N260	TDD 37.0 – 40.0	50, 100, 200, 400
N261	TDD 27.5 – 28.35	50, 100, 200, 400

- FR1 frequency ranges in 5G-Communication are **close** to those from the Wi-Fi 6 and 7
  - In the Literature, state-of-the-art PLLs can be seen as enablers both 5G-communications and Wi-Fi applications

- Frequency range 6 -7 GHz
  - Fractional-N operations are most-likely required

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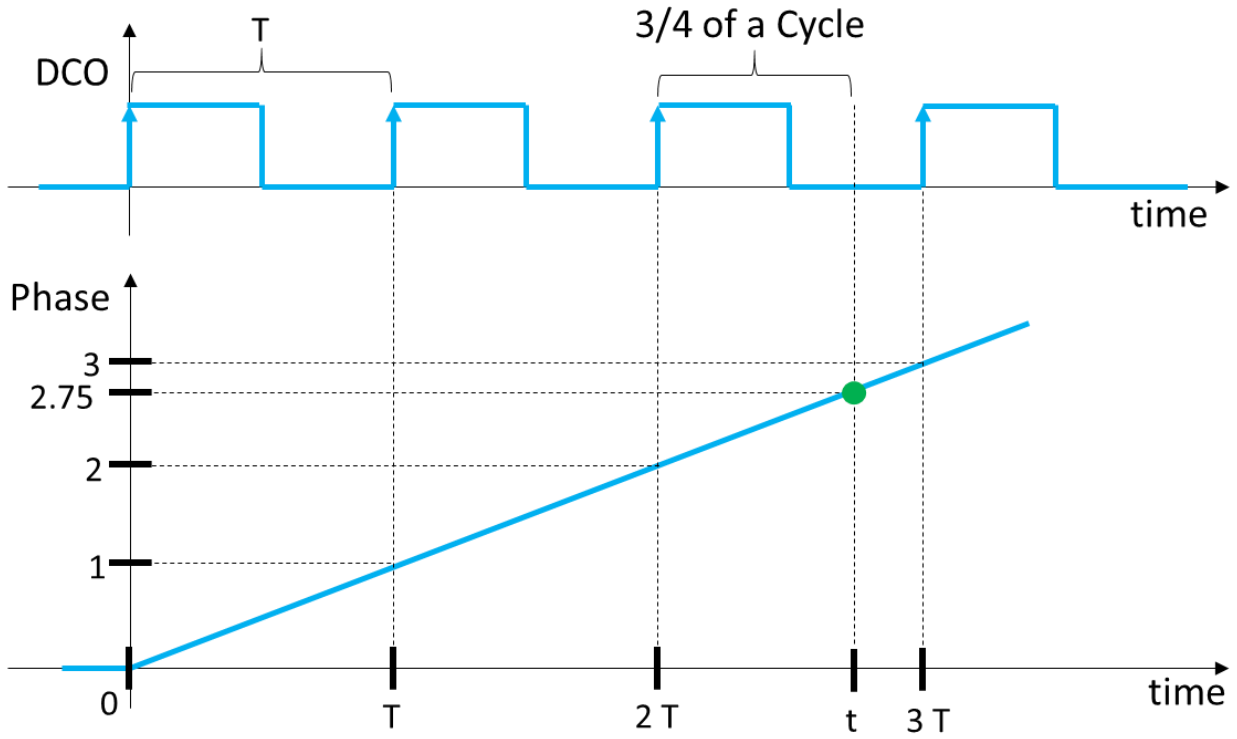
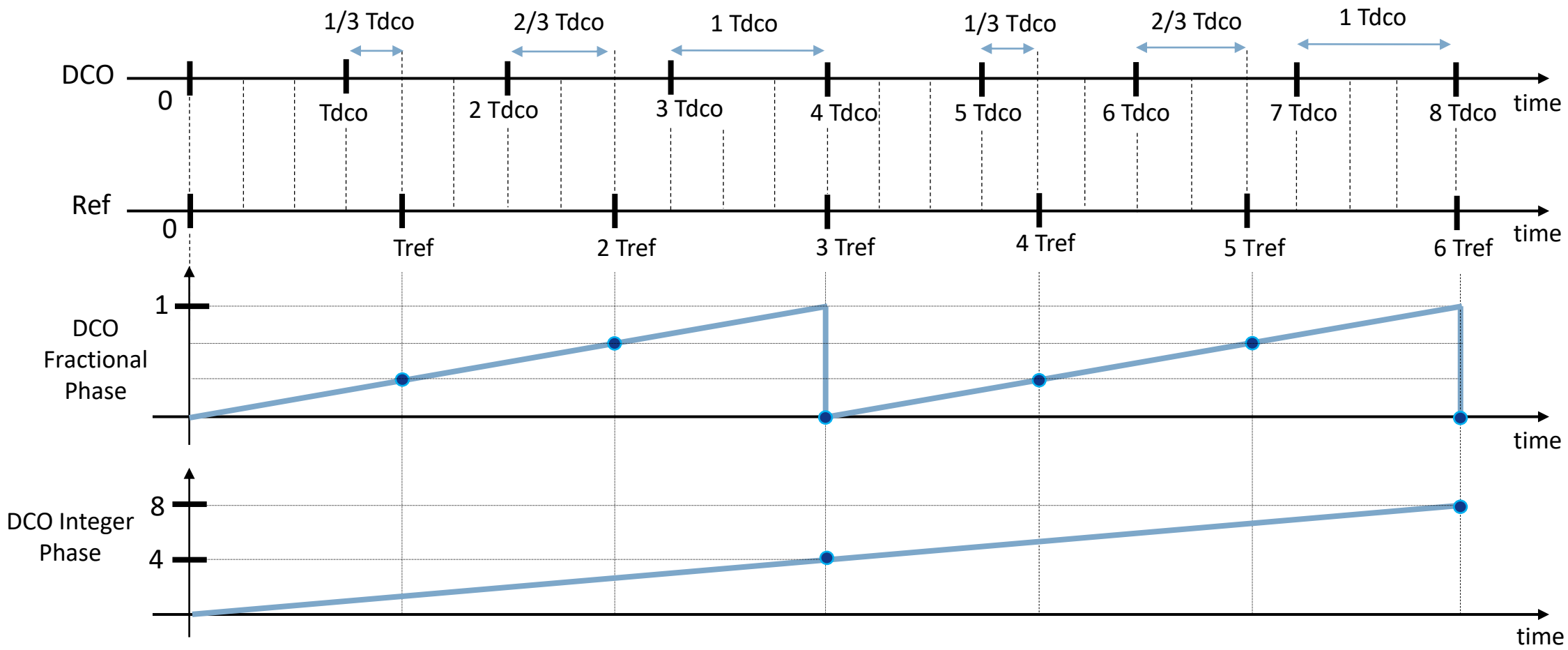
Let’s define “Phase”



Let’s define “Phase” as follows:

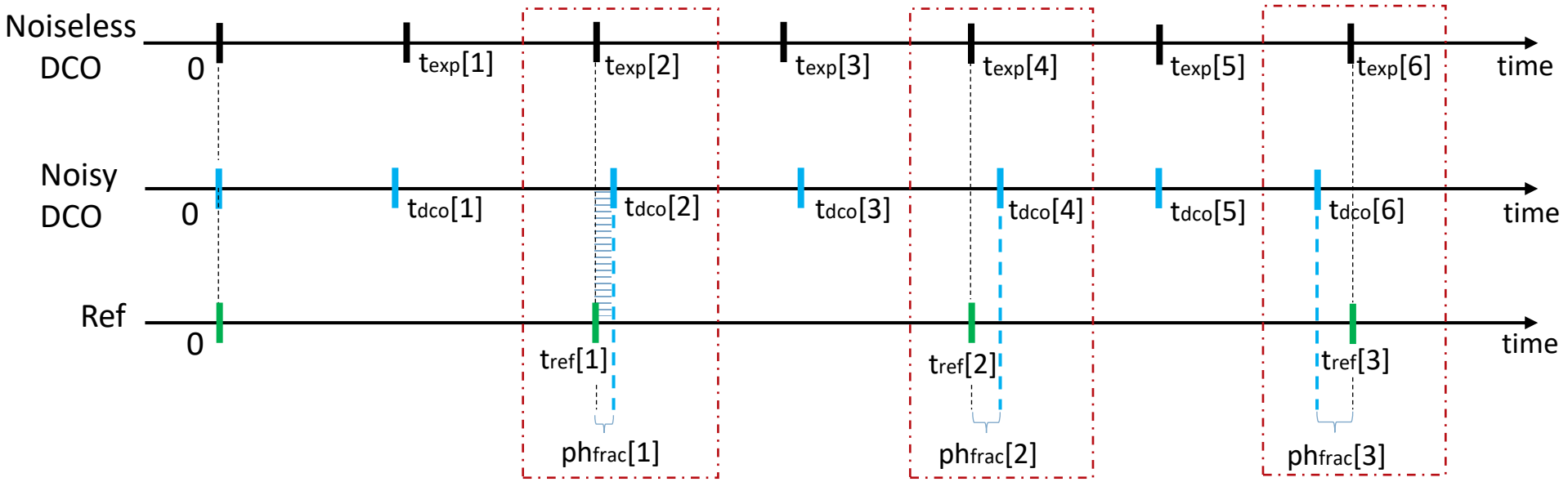
- Phase Integer-Part => Number of complete DCO clock cycles in the interval [0, t]
- Phase Fractional Part => Portion of the last DCO cycle that has been completed in the interval [0, t]
- Both Integer and Fractional parts are **normalized** to the DCO period

Example Phase in case of Fractional Ratio F_{DCO}/Fref



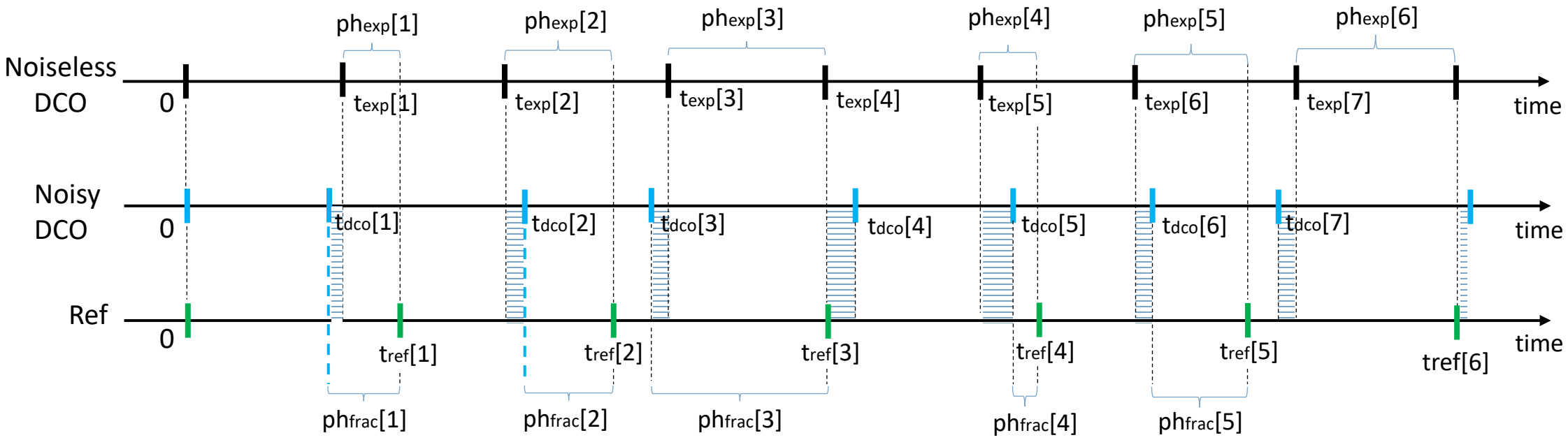
- Time stamps on x-axis = clock rising edges
- DCO Phase **evaluated** at Ref edges
- Tdco = 3/4 Tref => 4 completed DCO cycles every 3 completed Ref cycles (integer part of the DCO phase)
- Fractional part of the phase signal repeats in cumulative cycles: 1/3, 2/3, 0, 1/3, 2/3, 0, …
- Cumulative process plus wrapping can be seen as a case of “first order modulation”

Example Phase Difference when ratio F_{DCO}/Fref = 2



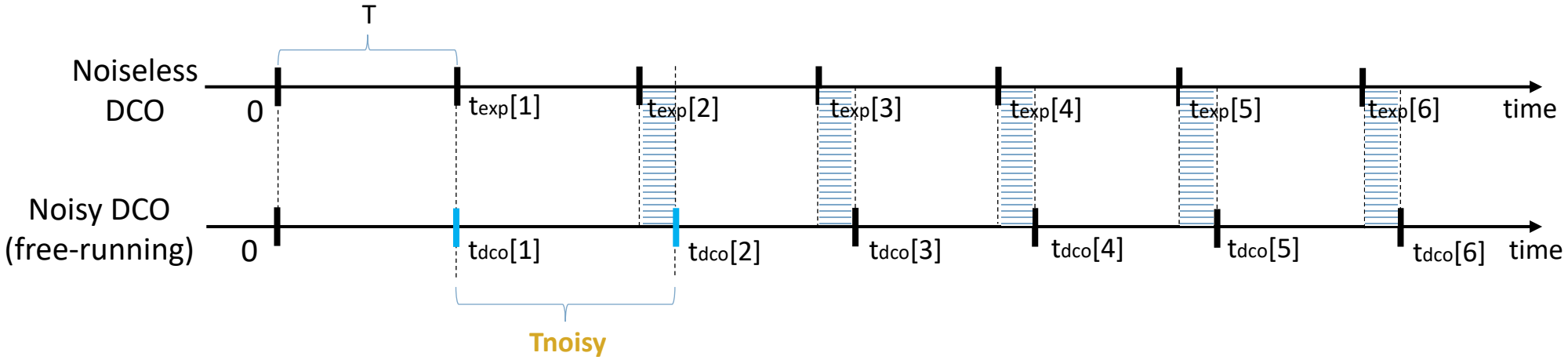
- We can calculate the "phase **difference**" in multiple ways:
  - (i) between Ref and noiseless DCO => not really "informative"
  - (ii) between noisy and noiseless DCO => we might calculate it
  - (iii) between Ref and noisy DCO => we can extract it with a circuit
- Integer part of the phase difference **can be ignored** when noise level in the DCO is small enough
- **Expected** fractional phase difference between Ref and noisy DCO is **zero** (or another **constant**)

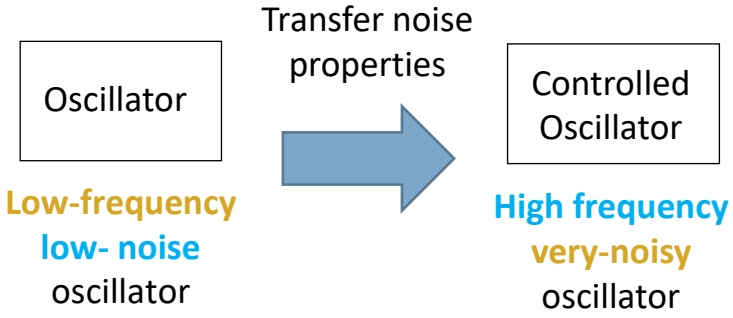
Example Phase Difference when ratio F_{DCO}/Fref is Fractional

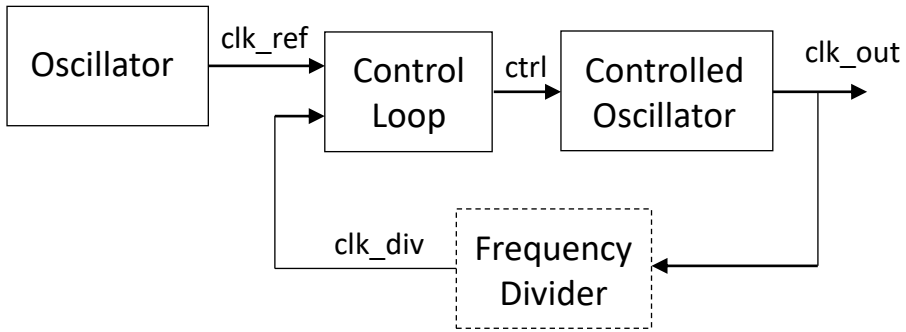


- **Expected** fractional phase difference between Ref and DCO is a **periodic pattern**

Phase Difference Accumulation and the Need for a Phase-Locked Loop



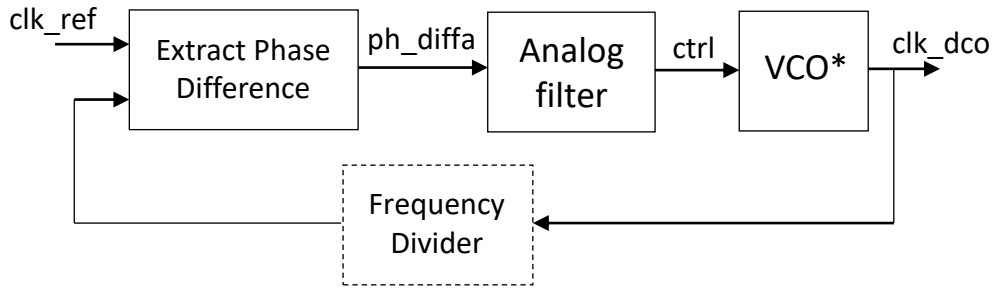




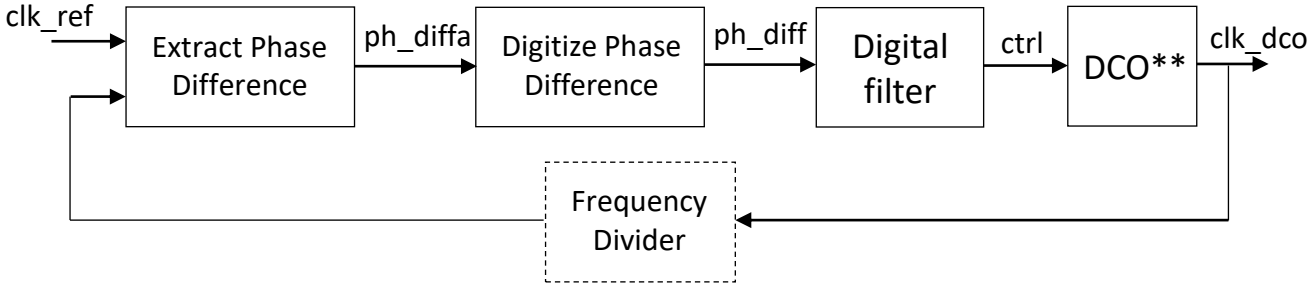
- In a **free-running** oscillator, a single cycle with perturbed duration produces a **constant** phase difference in all following cycles => phase difference (or phase noise) **accumulates**
- A phase-locked loop can be seen as a system to "transfer" the good phase noise properties of a low frequency oscillator (typically a crystal-based oscillator) to a high frequency noisier (typically integrated) oscillator.
- Introducing a frequency divider with division ratio Ndiv is a simple solution to have: fout = Ndiv fref

General Phase-Locked-Loop (PLL)

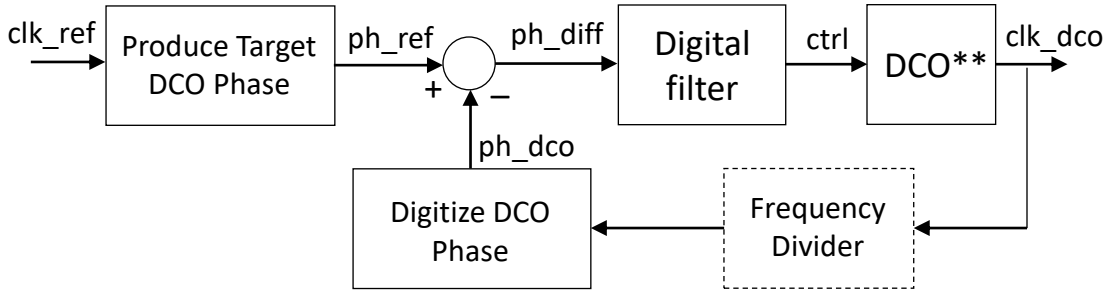
- PFD-CP PLL
- sampling PLL
- subsampling PLL



- PFD-plus-TDC-based PLL
- digital sampling PLL
- digital subsampling PLL



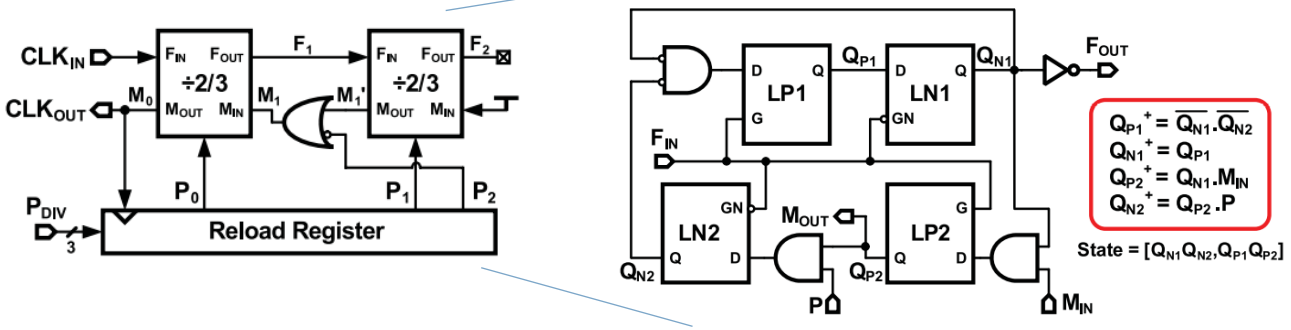
- TDC-plus-counter-based PLL



*VCO = Voltage Controlled Oscillator. It can be also a CCO = Current Controlled Oscillator
**DCO = Digitally Controlled Oscillator.

PLL Architectures

Programmable **Integer** Frequency Dividers [4]



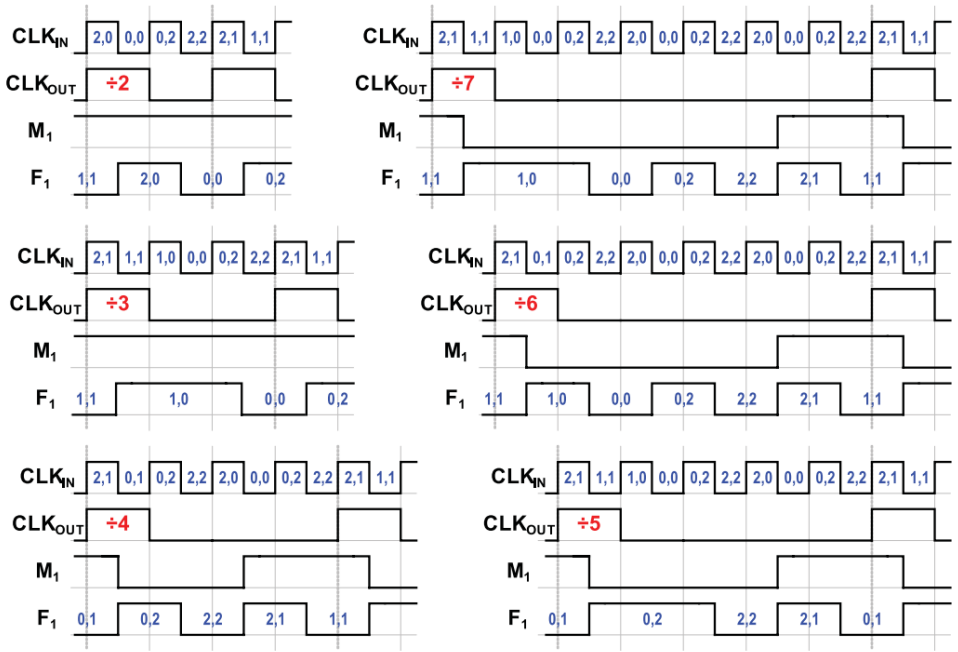
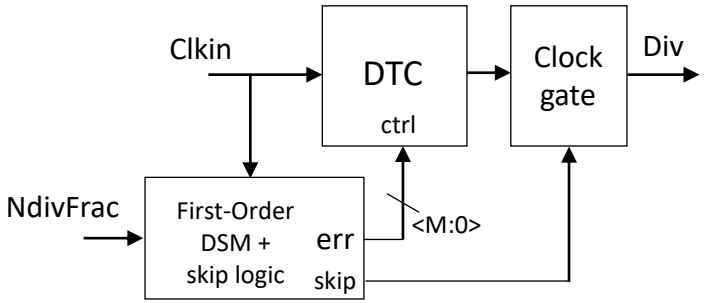
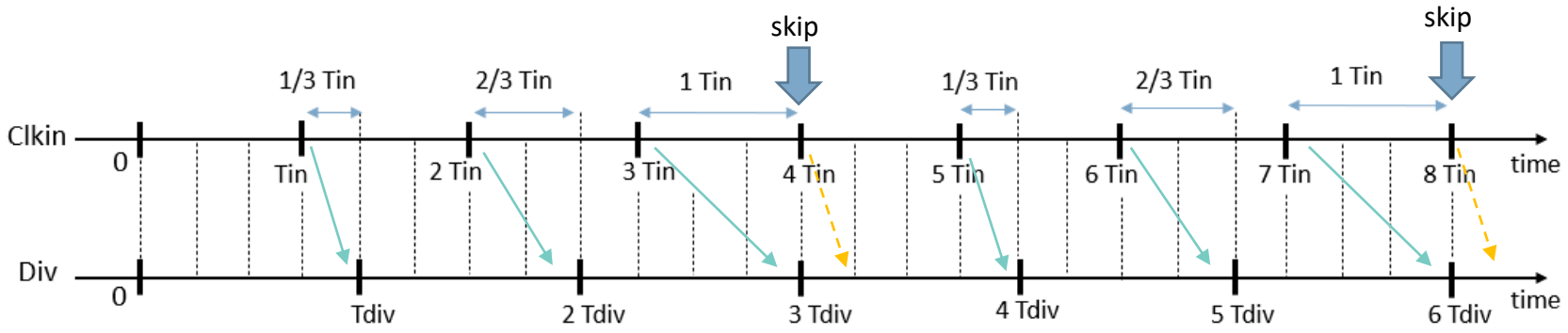


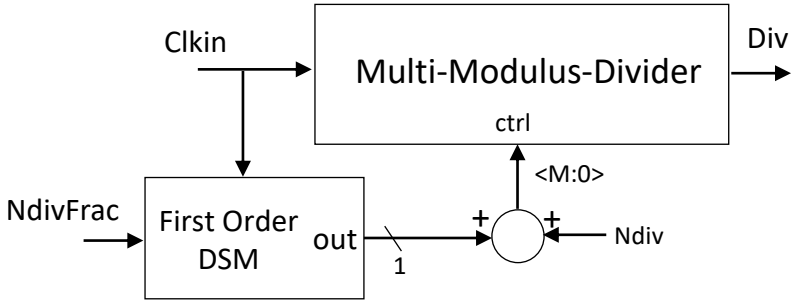
Fig. 10. Timing diagrams of the two-stage MMD for different division operations from 2 to 7.

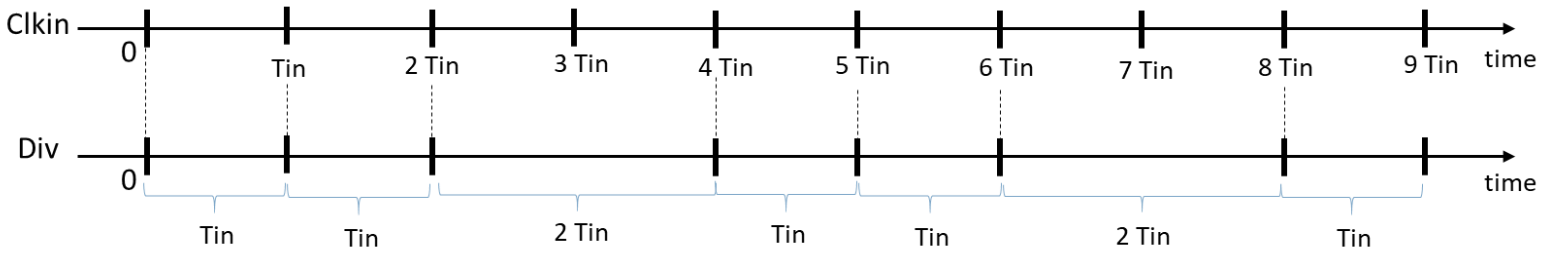
- Multi-Modulus-Dividers (MMDs) based on “Dividers by 2/3” are very popular
- Dividers by 2/3 are compact and suitable for RF-frequencies
- Alternative: Injection-locked frequency dividers with division by 2 or 3 [5]

Programmable **Fractional** Frequency Dividers (Examples)



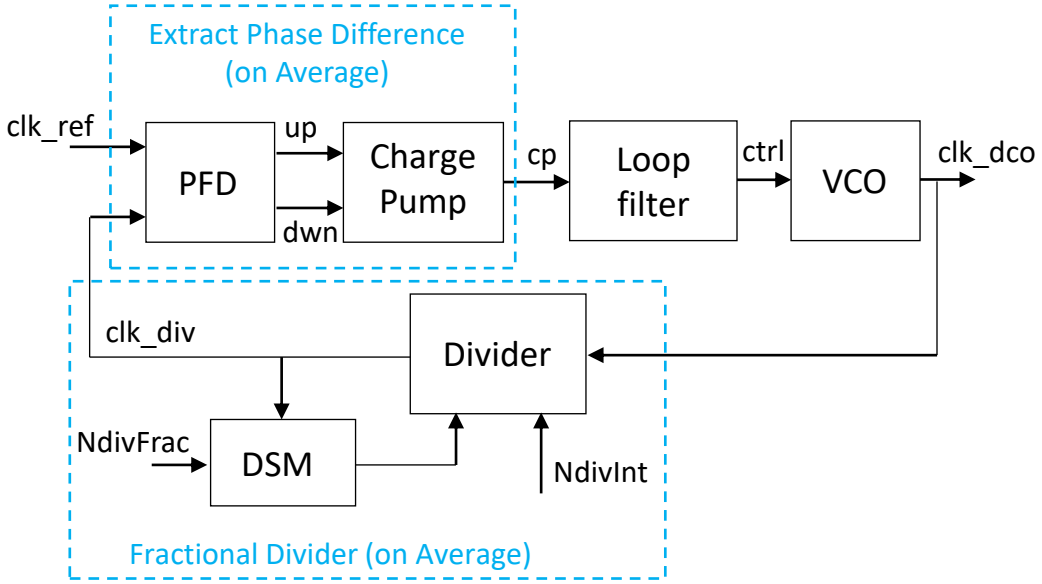


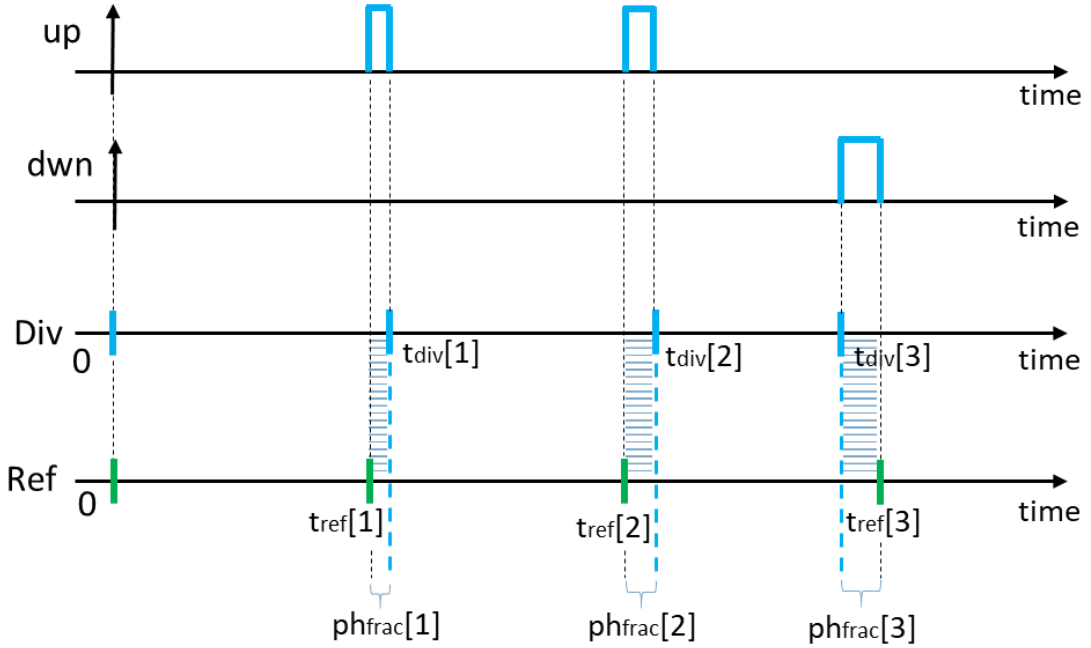




- DTC = Digitally-Controlled Delay; DSM = Delta-Sigma-Modulator
- Target ratio: Tin = 3/4 Tdiv => Tdiv = 4/3 Tdiv
- DTC-based Frequency Divider produces **exactly** the ratio Tdiv = 3/4 Tin
  - Fractional and integer phase definitions are obviously applicable
  - Duty cycle is distorted (typically)
- MMD-based Frequency Divider produces **on average** Tdiv = (Tin + Tin + 2Tin)/4 = 3/4 Tin

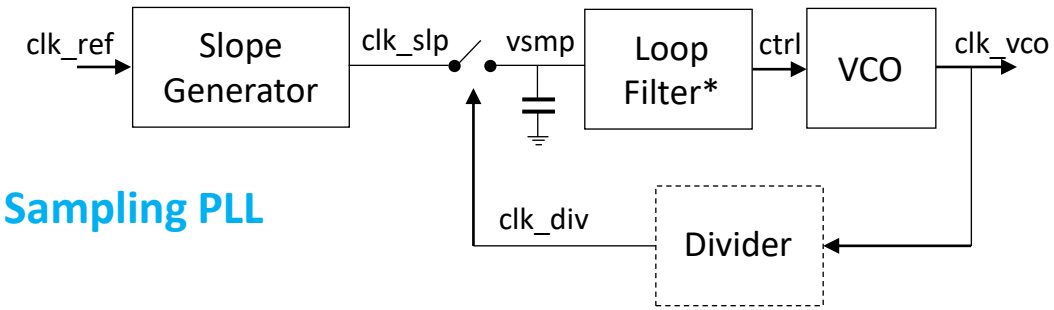
Architecture of a PFD-CP-based PLL



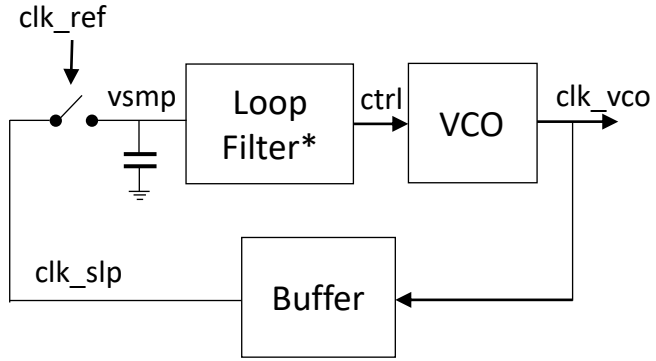


- Phase-Frequency-Detector (PFD) => extracts the phase difference => phase error encoded in average duration of up-dwn pulses
- Charge-Pump (CP) => converts the logic pulses into current pulses
- Loop filter => 1) extracts the average level from the current pulses and 2) defines loop noise transfer functions
- Voltage-Controlled Oscillator (VCO)
- DSM (Delta-Sigma-Modulator) + Divider = Fractional Frequency Divider “on average”

Architecture of Sampling/Subsampling PLLs

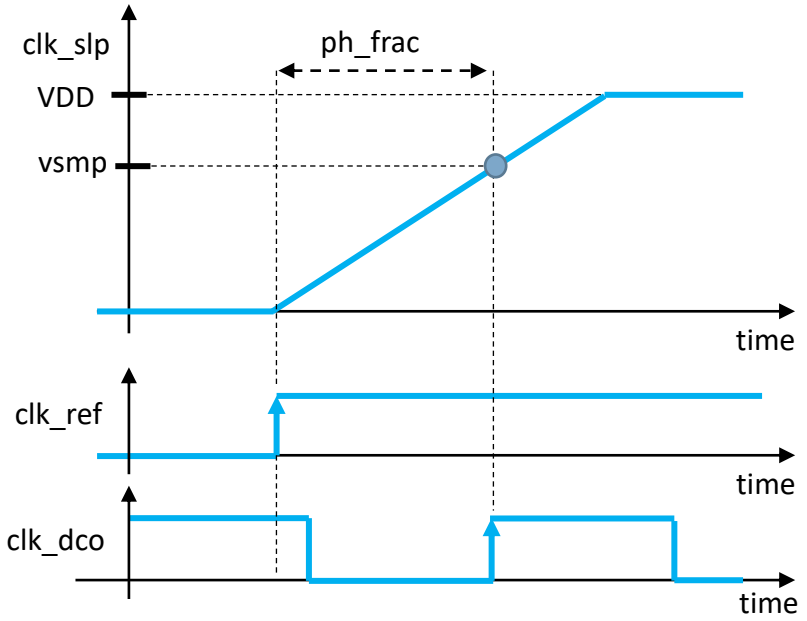


Sampling PLL



Subsampling PLL

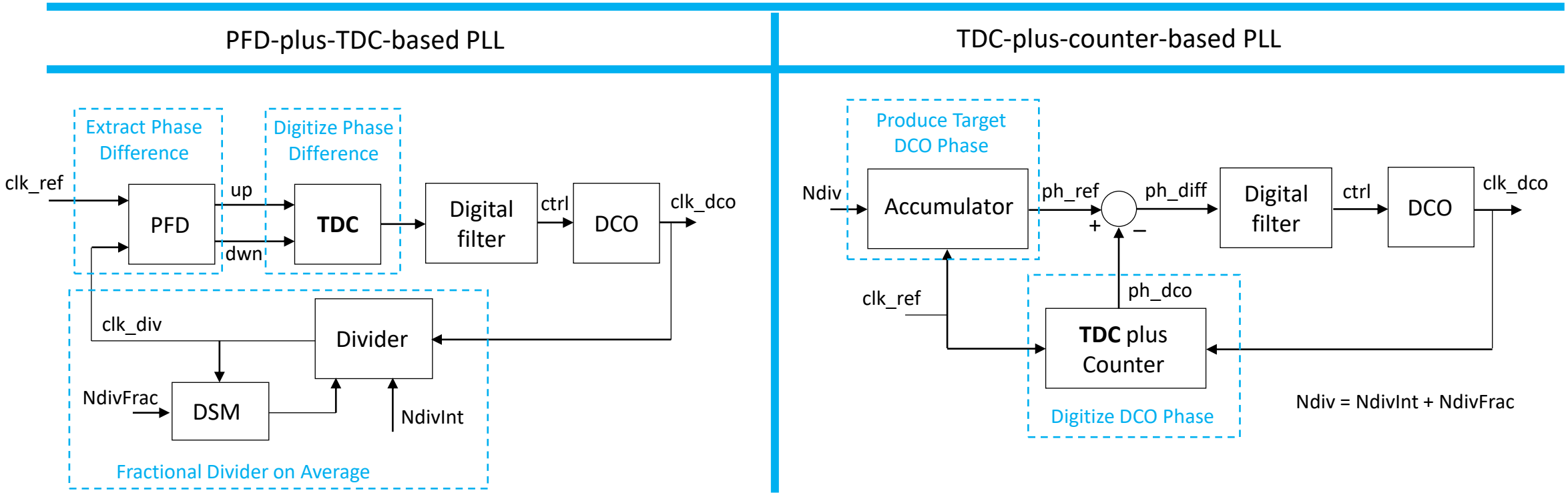
Operation of a sampling PLL



* In many cases, a Gm-stage is associated at the input of the Loop-filter

- The sampled voltage vsmp is proportional to the DCO fractional phase (and hence to the phase difference)
- Elegant, minimalistic PLL

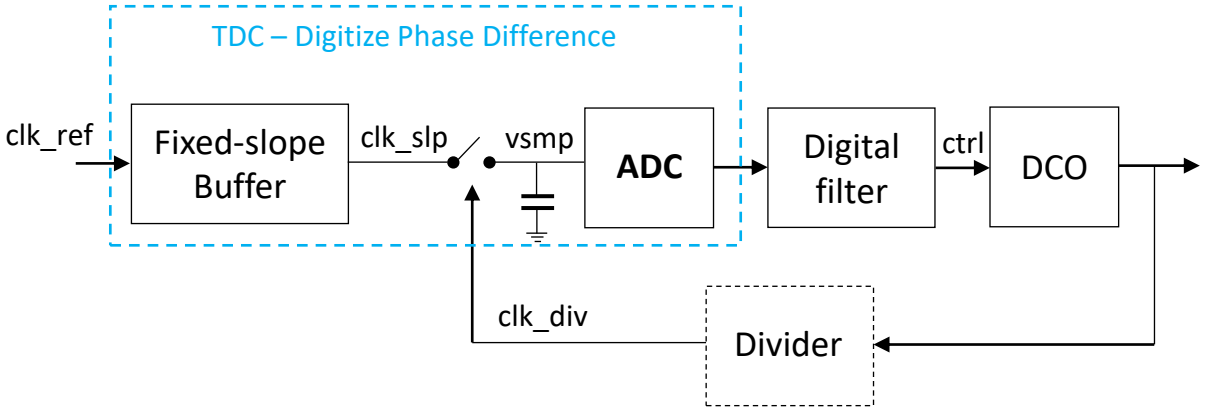
General Topologies of Digital PLLs



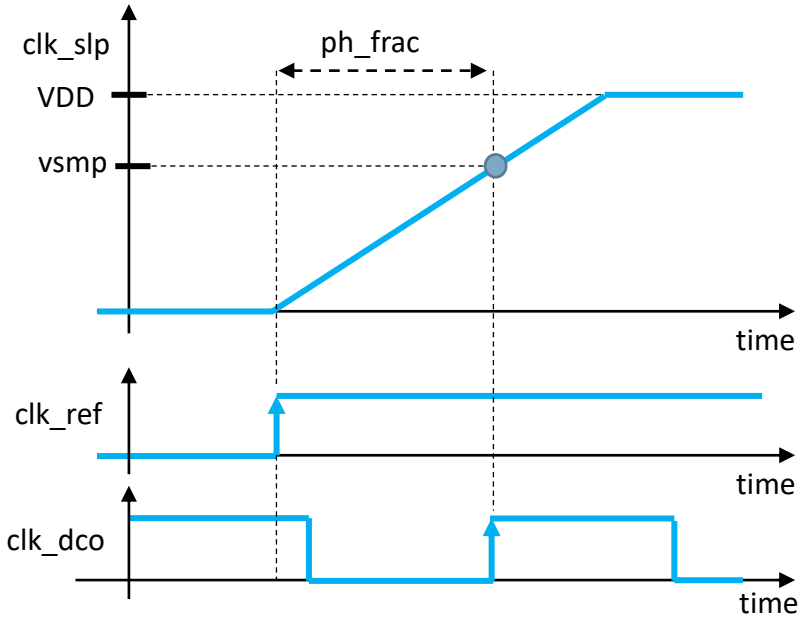
- In PFD-plus-TDC-based PLLs, the TDC (Time-to-Digital-Converter) digitizes the duration of the up/dwn pulses from the PFD => phase difference digitization

- In TDC-plus-counter-based PLLs, the signals ph_ref and ph_dco are **digital** phase signals.
  - The phase difference is calculated by means of a simple subtraction

Digital Sampling PLL or TDC-based PLL?

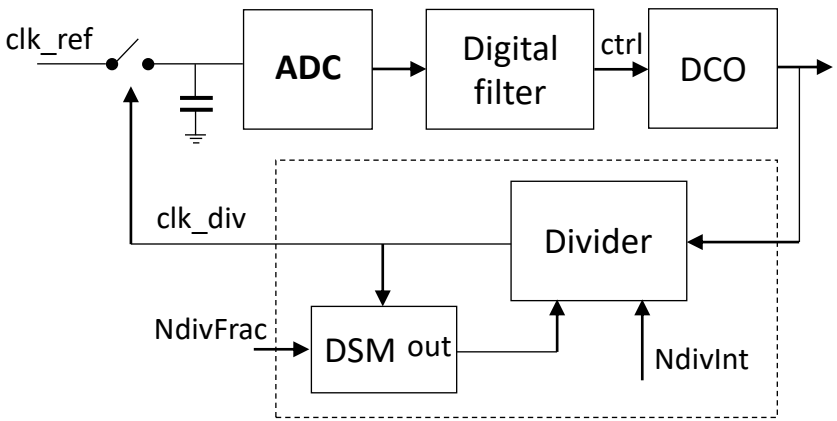


Just a particular case of a TDC

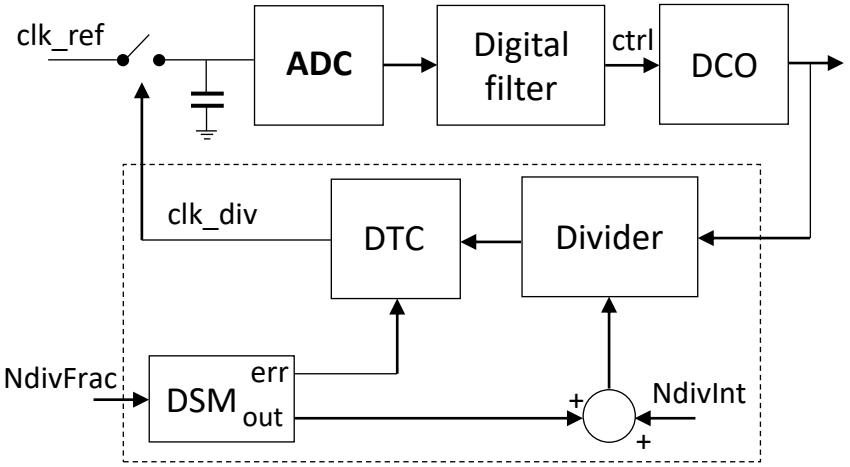


- A **digital** sampling/subsampling PLL can be seen as a case of a **TDC-based PLL**

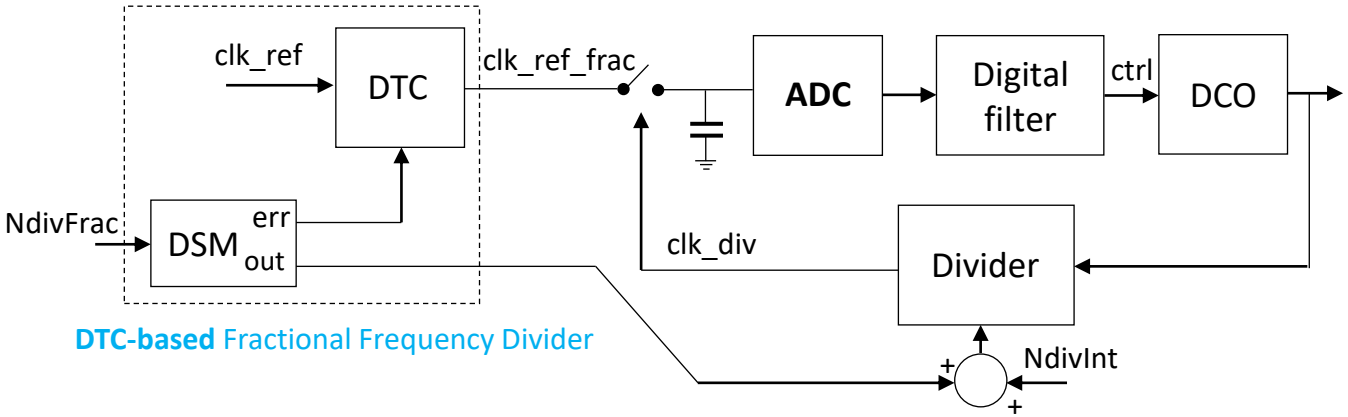
PLLs with DSM- and DTC-based Frequency Dividers



DSM-based Fractional Frequency Divider



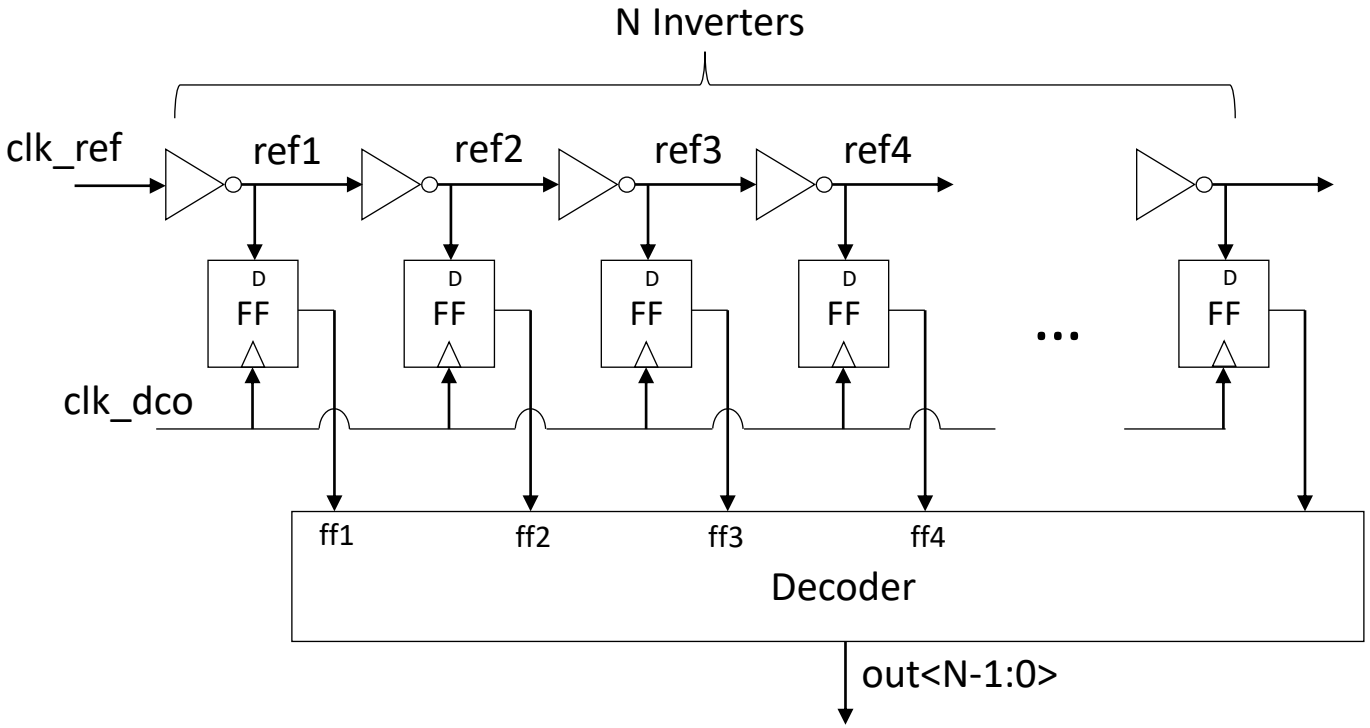
DTC-based Fractional Frequency Divider [4]



DTC-based Fractional Frequency Divider

- Both **analog and digital sampling/subsampling** PLLs often include DTC-based fractional dividers in order to build a Fractional-N PLL
- "DTC plus DSM error" can also be seen as a mechanism to "cancel" the quantization error from the sigma-delta modulation of the "Divider"

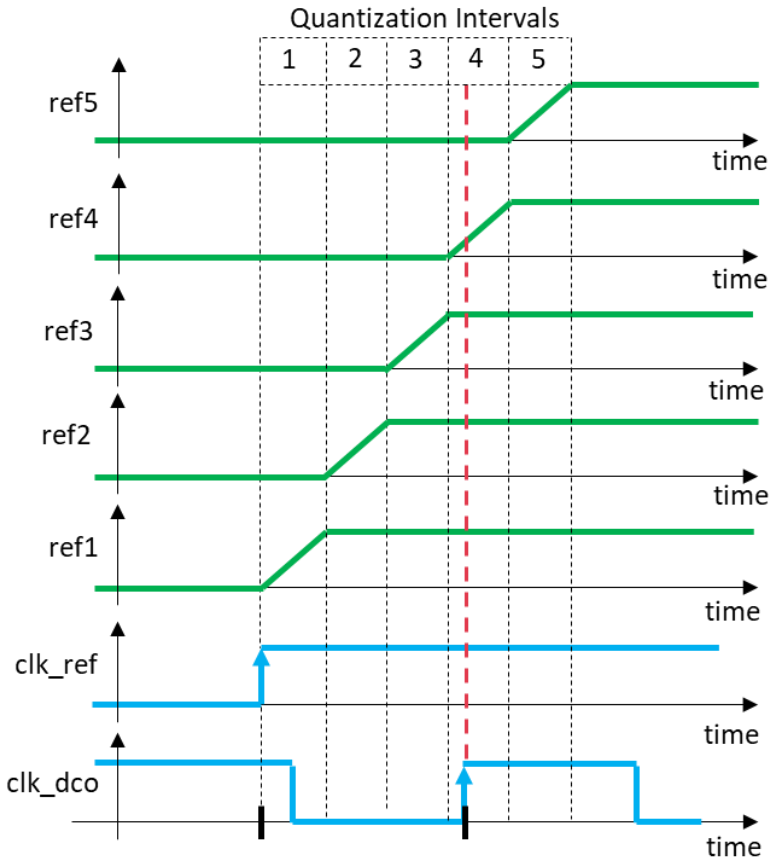
Simplest Delay-Line-based (Flash) TDC



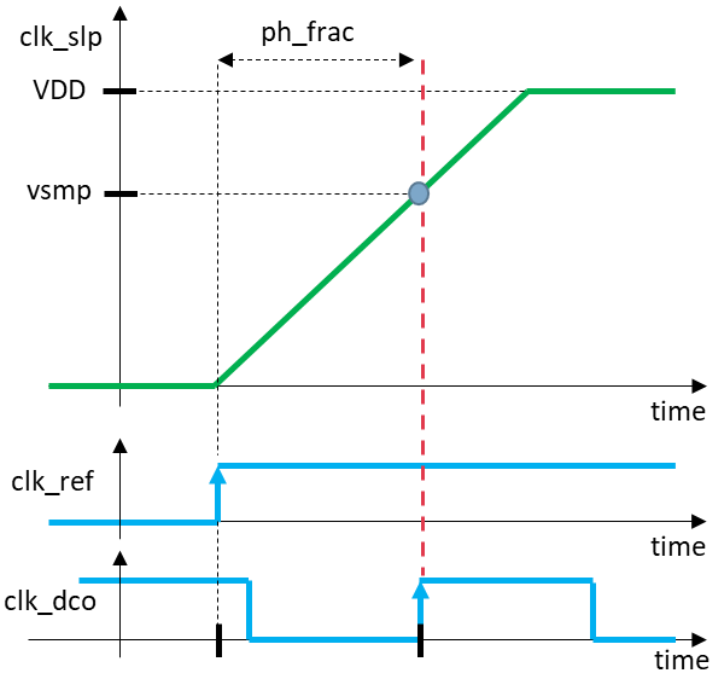
- Advantages:
  - Very simple implementation (digital-like circuit)
  - Fast conversion time
- Disadvantages:
  - Quantization step limited by fastest inverter
  - Large kick in the supply when many stages are used
  - Flip-flops are always clocked
- Note: clk_ref and clk_dco can be swapped

Delay-Line-based and “Slope-generator plus ADC”-based TDCs

Delay-Line-based TDC

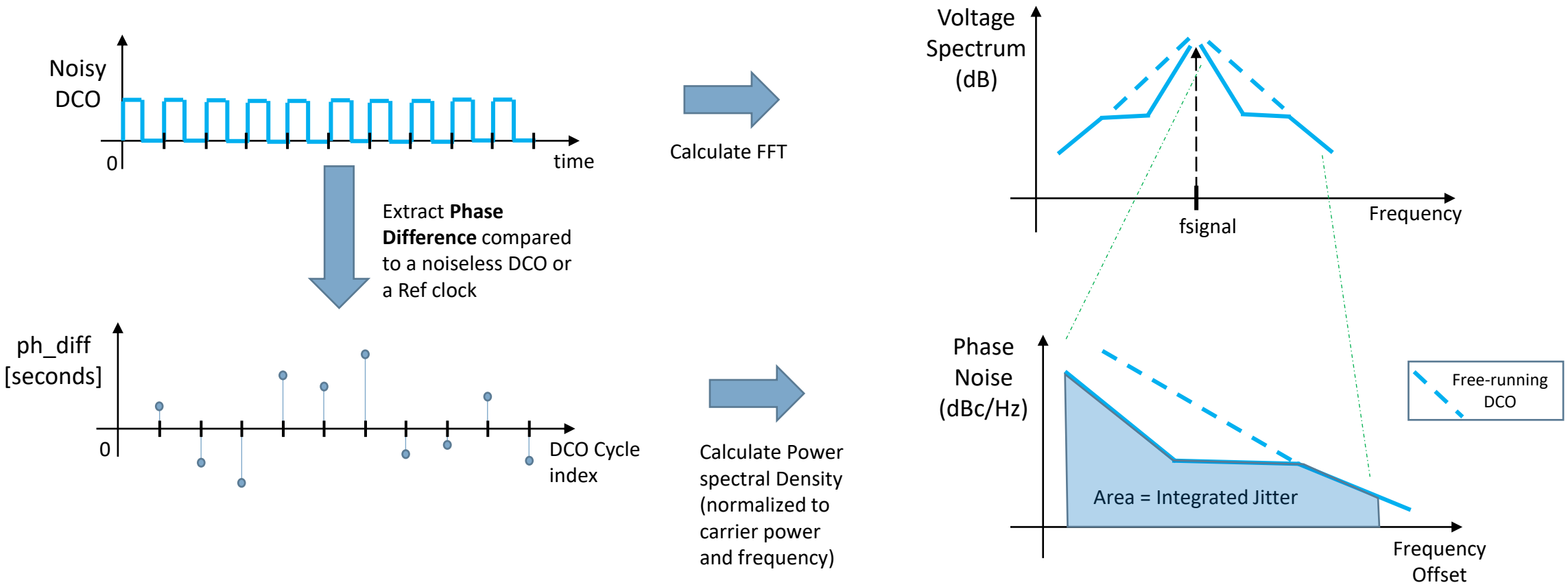


Slope-generator-plus-ADC



- In the sake of simplicity, ref1, ref2 … are the outputs of buffers (not inverters)
- Delay-Line-Based TDC => digitization process includes **many fast** charge/discharge consecutive processes
- Slope-generator-plus-ADC => digitization process includes a **single slow** charge/discharge process

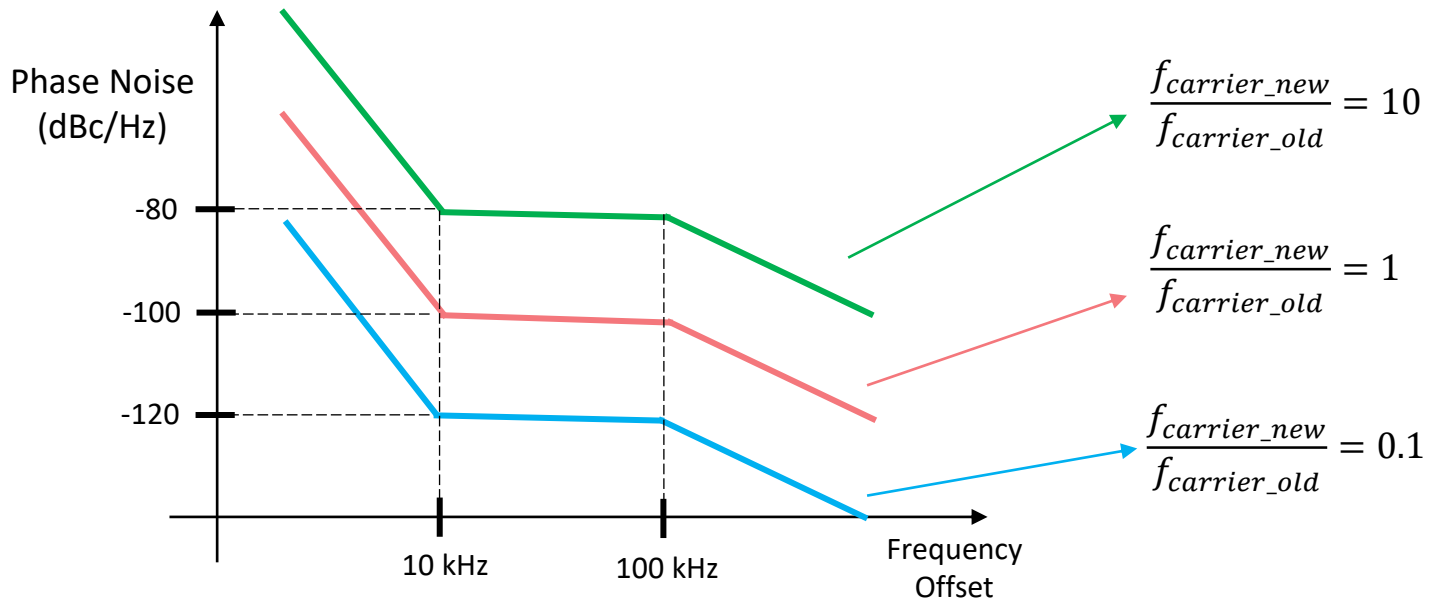
Phase difference, Phase Noise, Integrated Jitter



- Phase noise is the normalized Power-Spectral Density of the DCO phase difference signal calculated with respect to a noiseless DCO or a reference clock
- Phase noise is a measure of how much the **voltage spectrum** of a noisy voltage signal deviates from that of an ideal pulse
- Integrated jitter is obtained by integrating the phase noise over a given frequency range

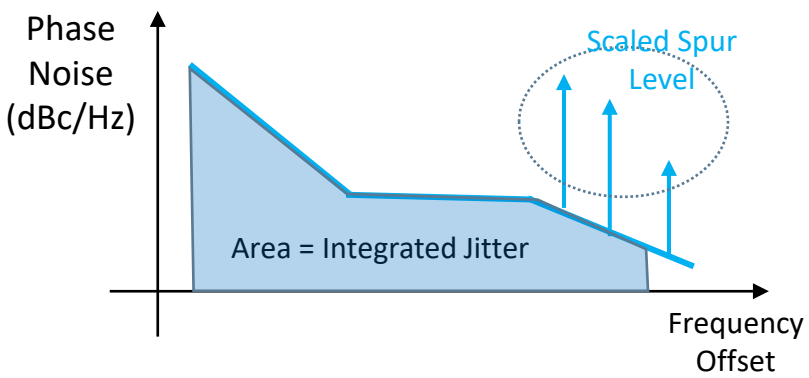
Referring Phase Noise to a given Carrier Frequency

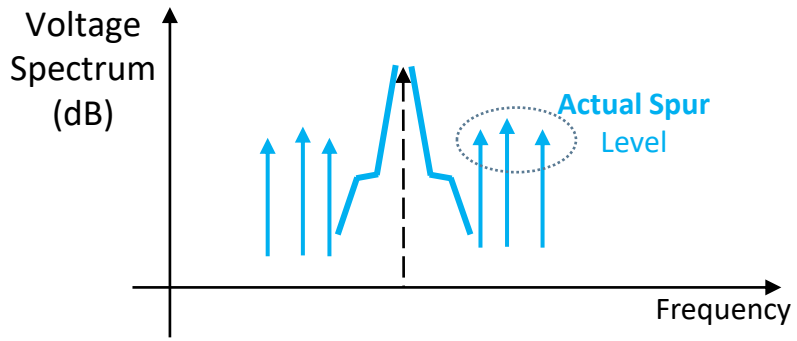
$$ScaleFactor = 10log_{10}\left(\frac{f_{carrier\_new}}{f_{carrier\_old}}\right)^2$$



- Phase noise is normalized to a carrier frequency
- In a PLL, the normalization frequency is often the DCO/VCO frequency
- Nevertheless, a phase noise can be normalized to **any** frequency
    - When the new carrier frequency decreases the phase noise decreases
- The integrated jitter is **independent** on the carrier frequency when the integration bandwidth is fixed

Short Introduction to Spurs





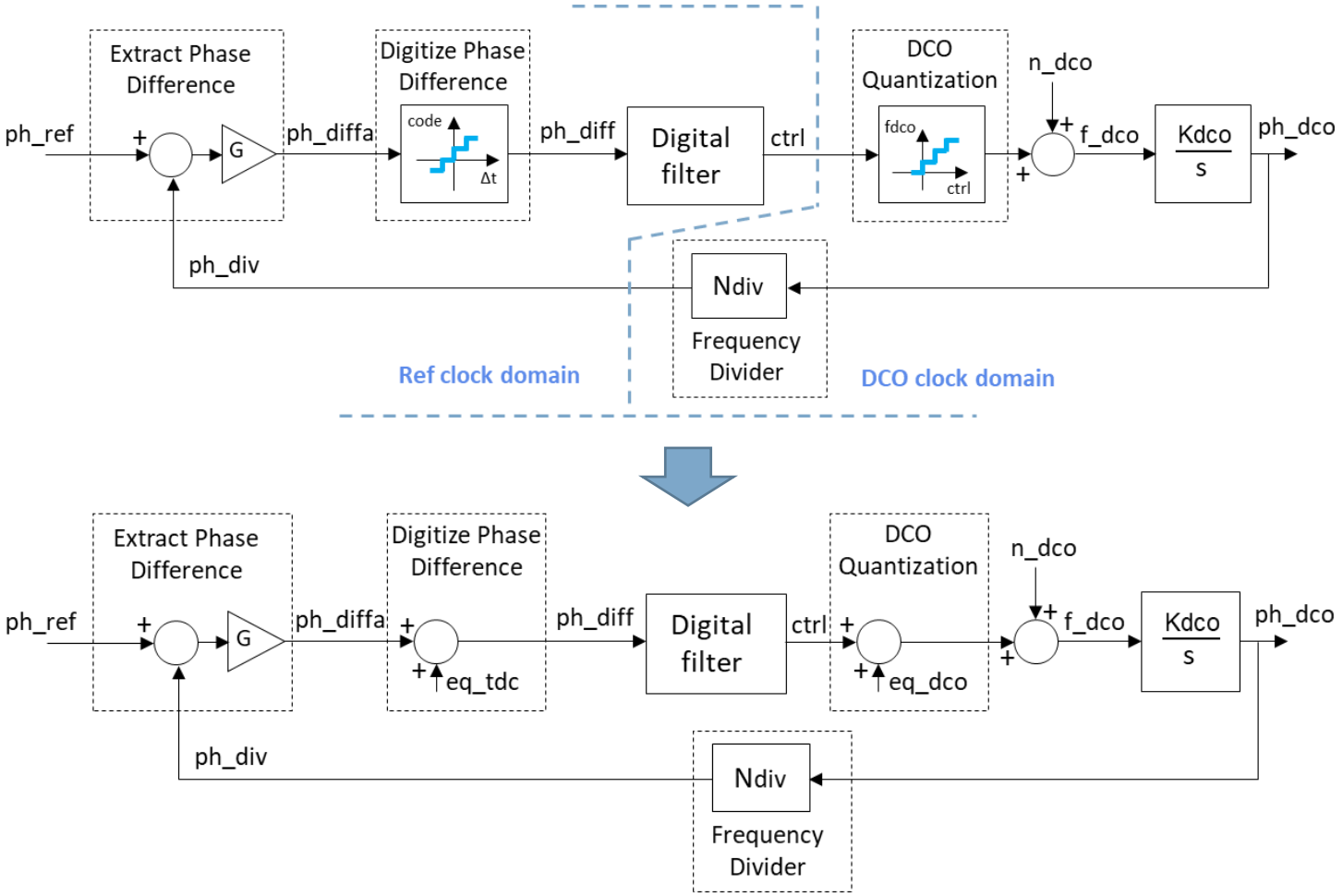
- Spurs are periodic perturbation in the frequency and phase of the VCO/DCO
- Spur actual level is obtained from the voltage spectrum of the VCO/DCO voltage signal

Main spurs:

- Reference spur => related to the activity of the PFD or the TDC at Fref (hence it appears at frequency Fref)
- Fractional-N spurs => related to nonlinearities in a Fractional-N PLL or to internal coupling
  1) Example nonlinearities: dead-zone and mismatch in PFD-CP, Differential- and Integral-Nonlinearities in a TDC
  2) Internal supply/ground spurs => related to coupling between internal PLL blocks => might become contributor to the reference spur
- Internal supply/ground spurs => related to coupling to circuitry external to the PLL
  - Example components in the output of DC-DC converters used to generate supplies

Fundamental Design Considerations on PLL noise Transfer Functions

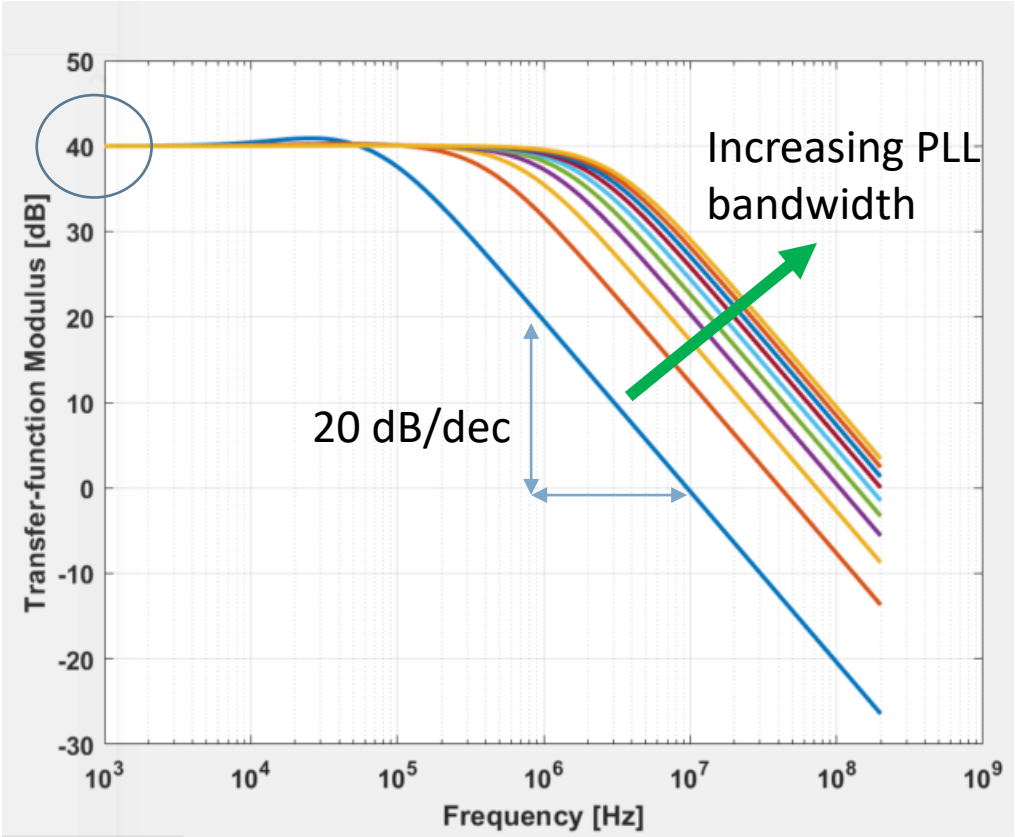
PLL Model with Quantization Errors from Phase Digitization



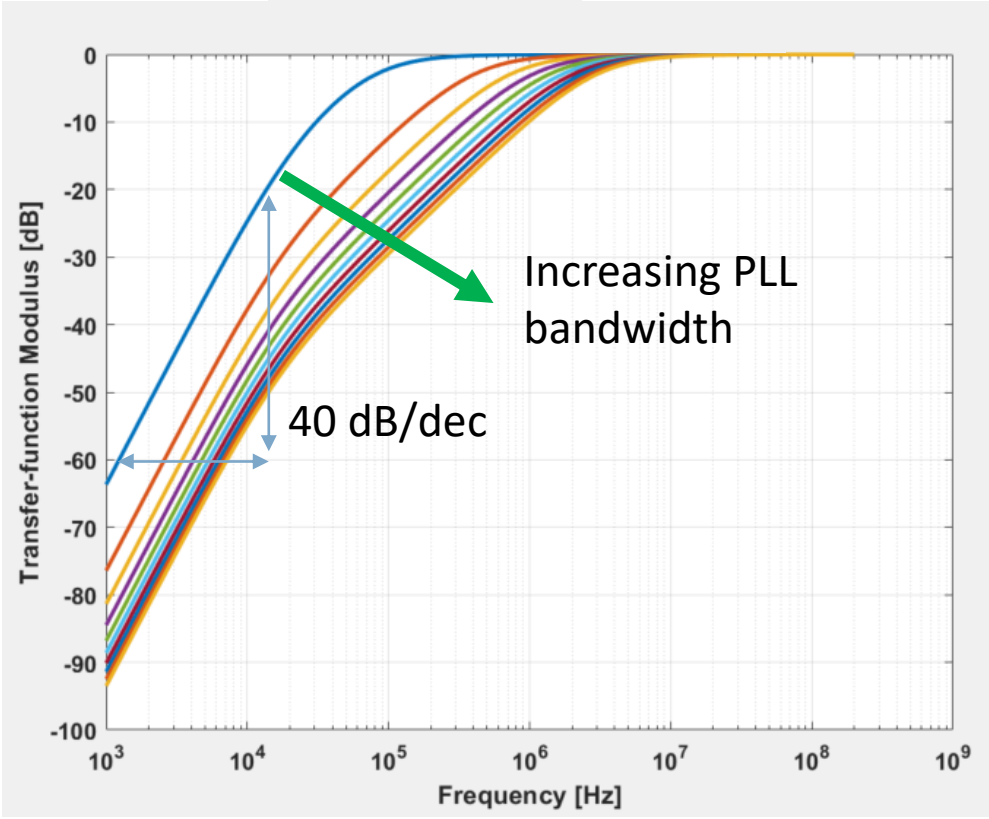
- eq_tdc and eq_dco => TDC and DCO quantization errors
- n_dco => random noise in the DCO (thermal plus flicker)

PLL Noise Transfer Functions (TFs)

PLL Reference-Noise Transfer Function



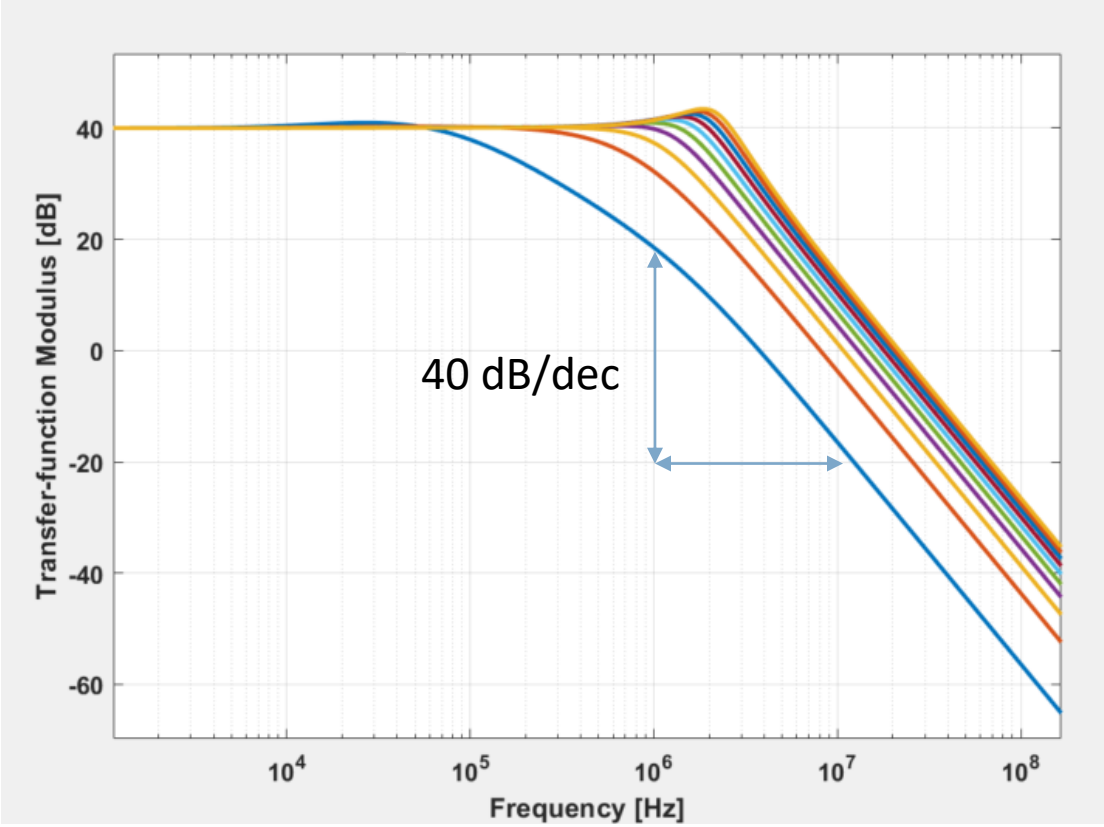
PLL DCO-Noise Transfer Function



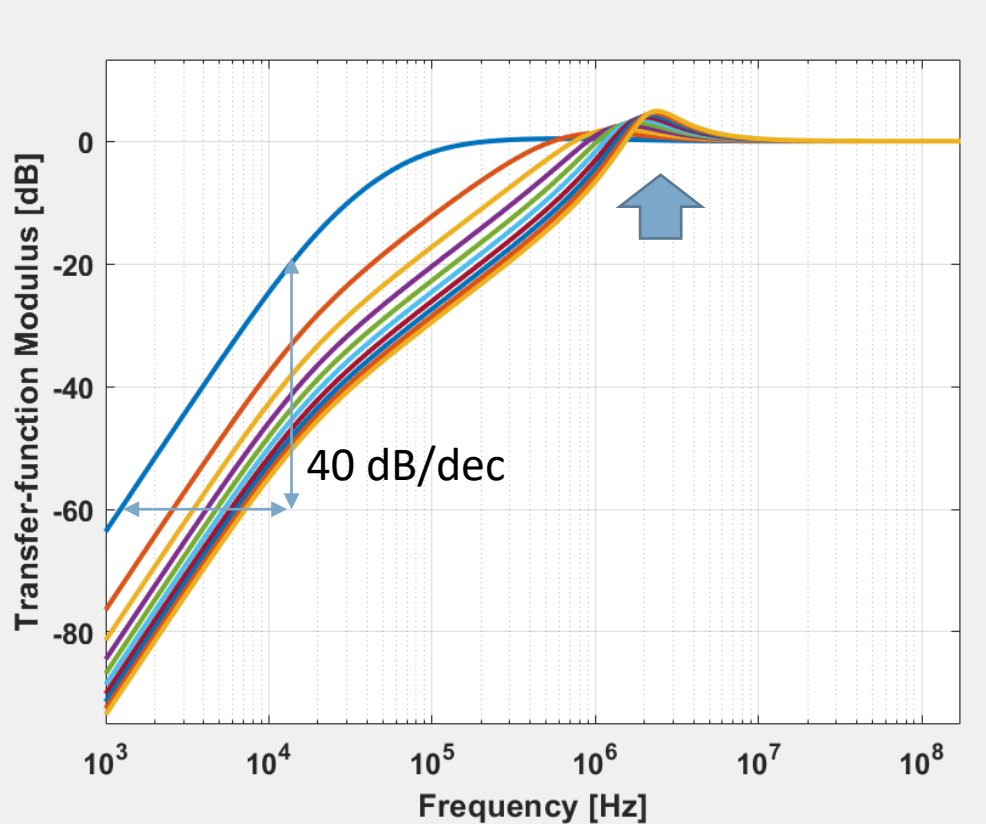
- **Design Trade off (PLL-bandwidth: in-band noise suppression vs VCO/DCO noise suppression)**
- In-band noise sources: TDC quantization, TDC random noise, PFD-CP random noise
- In this example, the loop filter includes a zero plus a pole at the origin

Trade off between Steeper Ref-noise Transfer Functions and Loop Stability

PLL Reference-Noise Transfer Function



PLL DCO-Noise Transfer Function



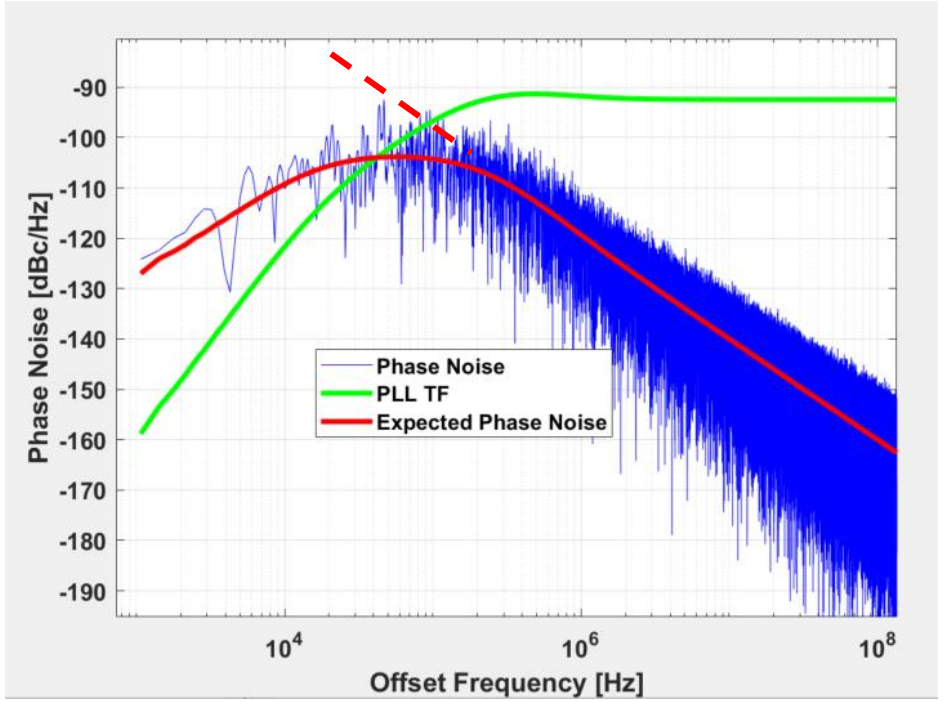
- **Design Trade off (extra-poles: extra-attenuation vs phase-margin)**: extra poles in the loop filter add extra attenuation in the ref-clock noise transfer function at the cost of lower phase margin

Approximations

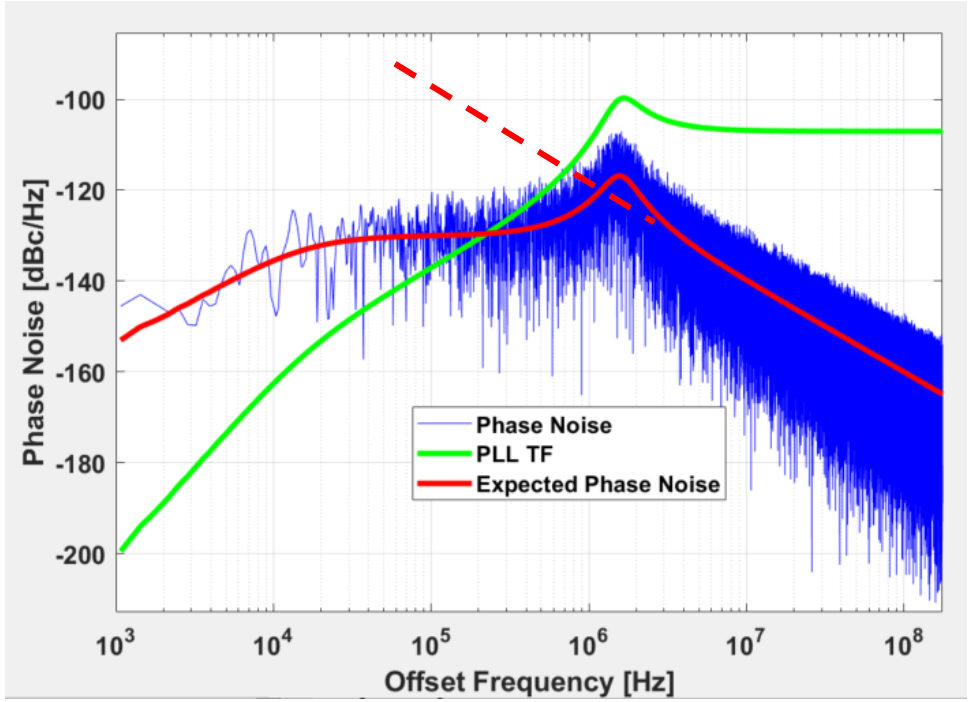
- Bilinear-transform in order to right transfer-functions from z- to s- domain
- Sampling from DCO-clock domain to Ref-clock domain is associated with an additional sinc(•) transfer function
- Loop latency can be modelled with transfer functions of the kind $e^{j\omega\varphi}$
- Interesting material available from M. H. Perrott's slides [6]

Example DCO Phase Noise after PLL noise Transfer Functions

Extra pole and good phase margin



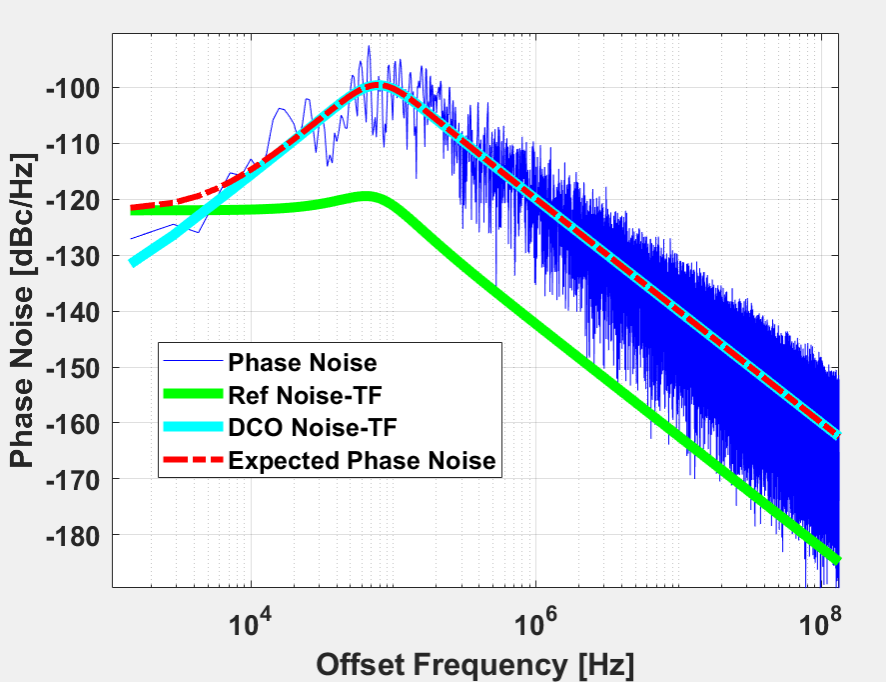
Extra pole and poor phase margin



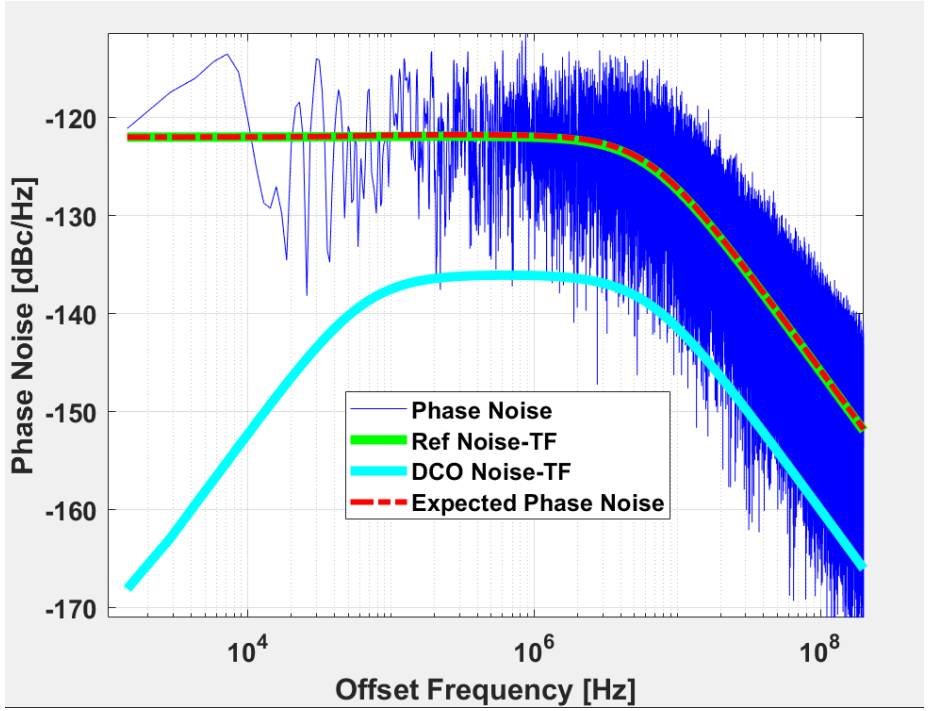
- Fcarrier = 6GHz
- Loop filter includes a zero, an integrator and an extra pole, in both figures
- The example transfer-function with the extra pole includes a peak of resonance => DCO noise is magnified by the resonance
- In both figure the dashed red line indicates the free-running DCO

Total Noise: Two Extreme Cases

Phase noise dominated by DCO noise

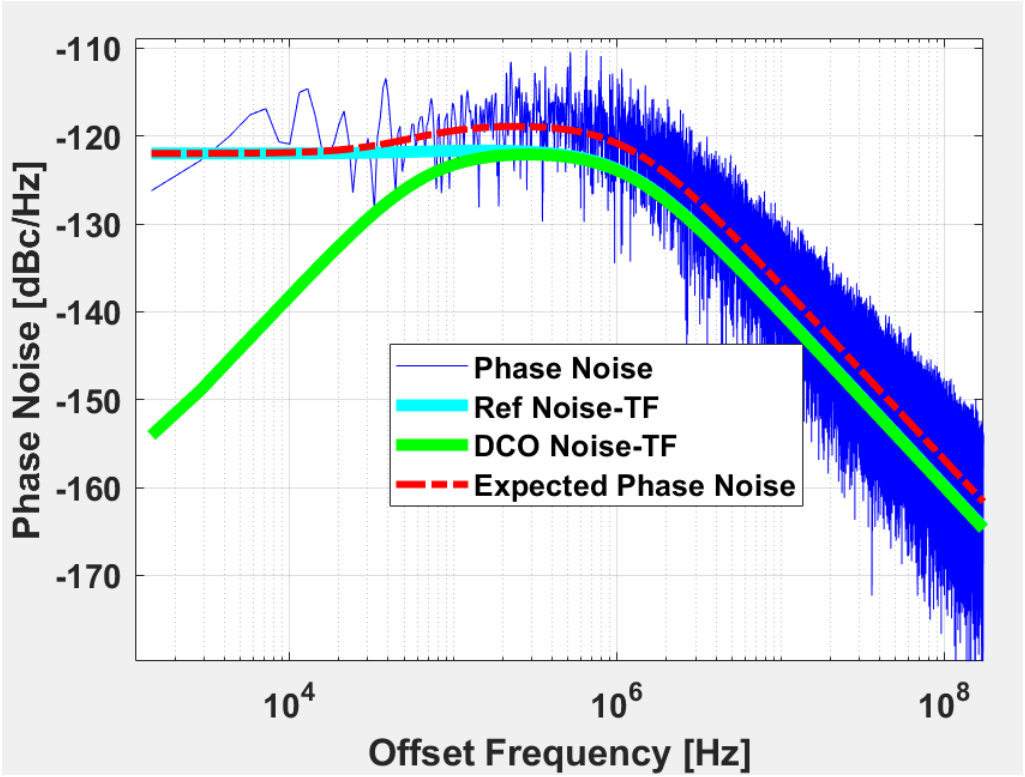


Phase noise dominated by in-band noise



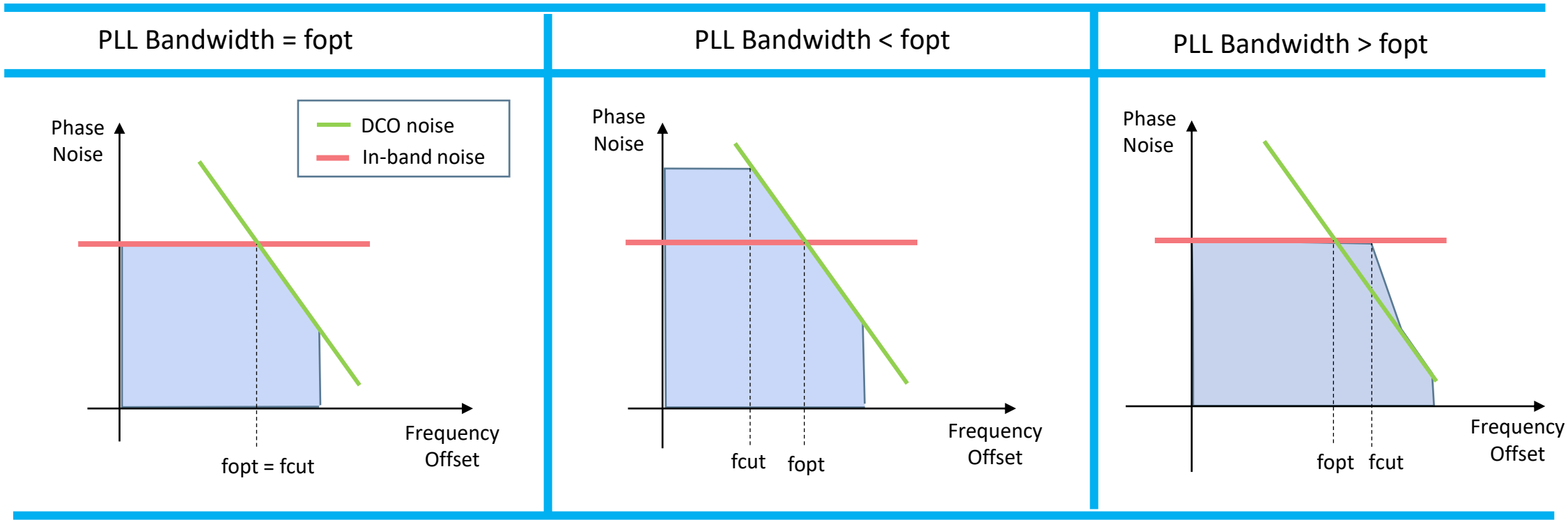
- Fcarrier = 6GHz
- Phase noise = low-pass-filtered in-band noise + high-pass-filtered DCO noise
- In extreme cases, only the low-pass-filtered in-band noise or the high-pass-filtered DCO noise dominate the PLL phase noise

Total Noise: a Balanced Example



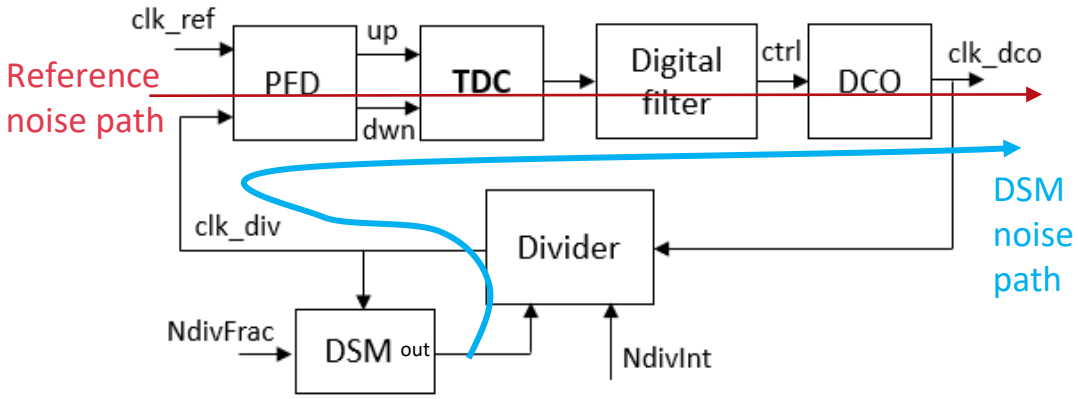
- Fcarrier = 6GHz
- Very common case: balanced phase noise with DCO noise dominating at higher frequencies and in-band noise dominating at low frequencies
- **Design Trade off (bandwidth: DCO-noise vs inband-noise)**: increasing the bandwidth reduces the impact of the DCO noise but increases that of the inband-noise

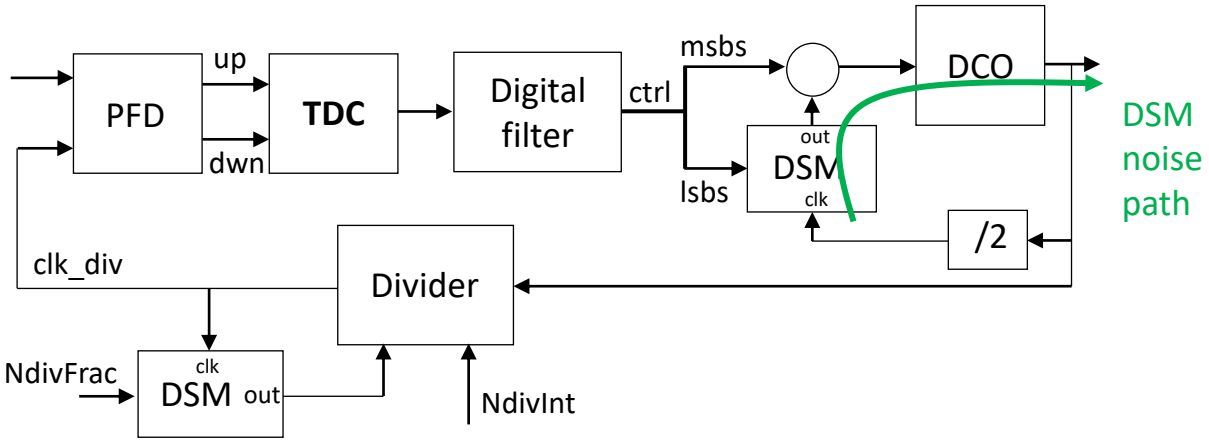
Oversimplified: Maximum Bandwidth for Integrated Jitter



- When the DCO noise and in-band noise floor are fixed, there's an optimum bandwidth for the lowest integrated jitter

Impact of DSM and Reference Noise





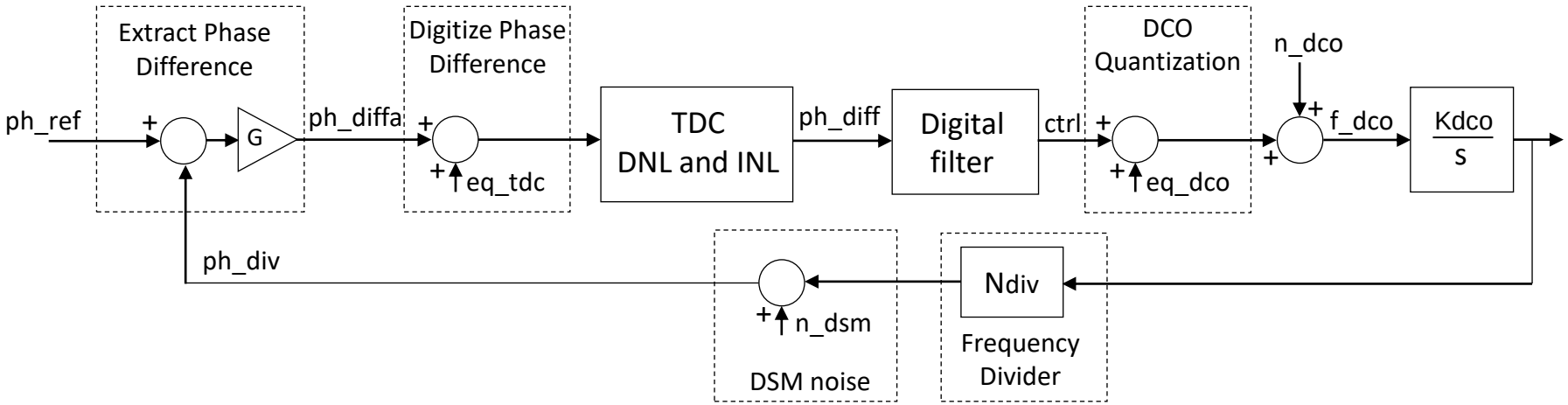
- DSM noise in “Divider plus DCM” are low pass filtered by the PLL ref-noise transfer function

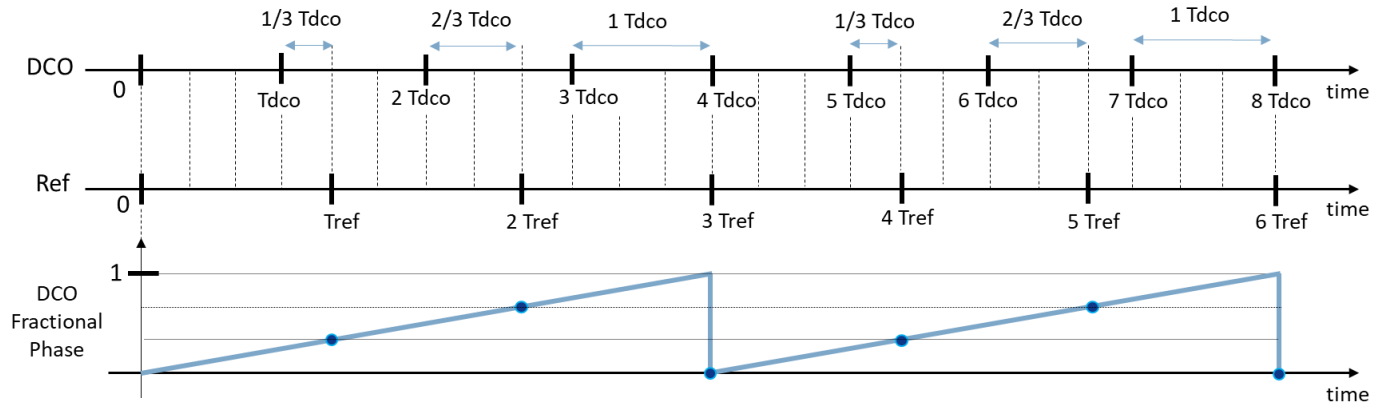
- When a DSM is added to the DCO input (in order to improve the DCO frequency accuracy on average) the DSM noise is integrated into phase noise and added directly to the PLL noise output (high pass)

- Reference noise is low-pass filtered by the PLL ref-noise transfer function (obviously)
    - In state-of-the-art PLLs the reference noise is actually a significant contributor to the PLL performance

Design Considerations on PLL bandwidth and Fractional-N Spur

Model of a Fractional-N PLL with TDC and a “Frequency Divider plus DSM”





- In a Fractional-N PLL, the DCO fractional phase is a periodic sawtooth-like signal (can have a more complex pattern compared to the example above)
  - The full TDC characteristic is “excited” when the PLL is locked => Fractional-N spurs related to TDC DNL and INL

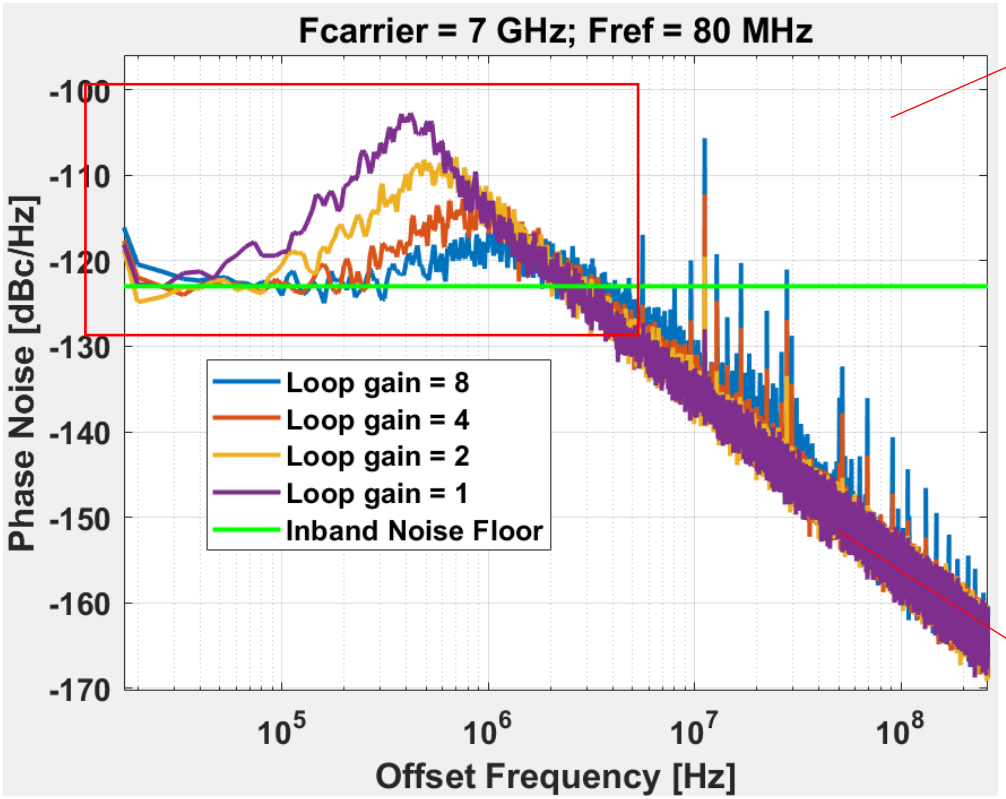
Spur level and Phase Noise

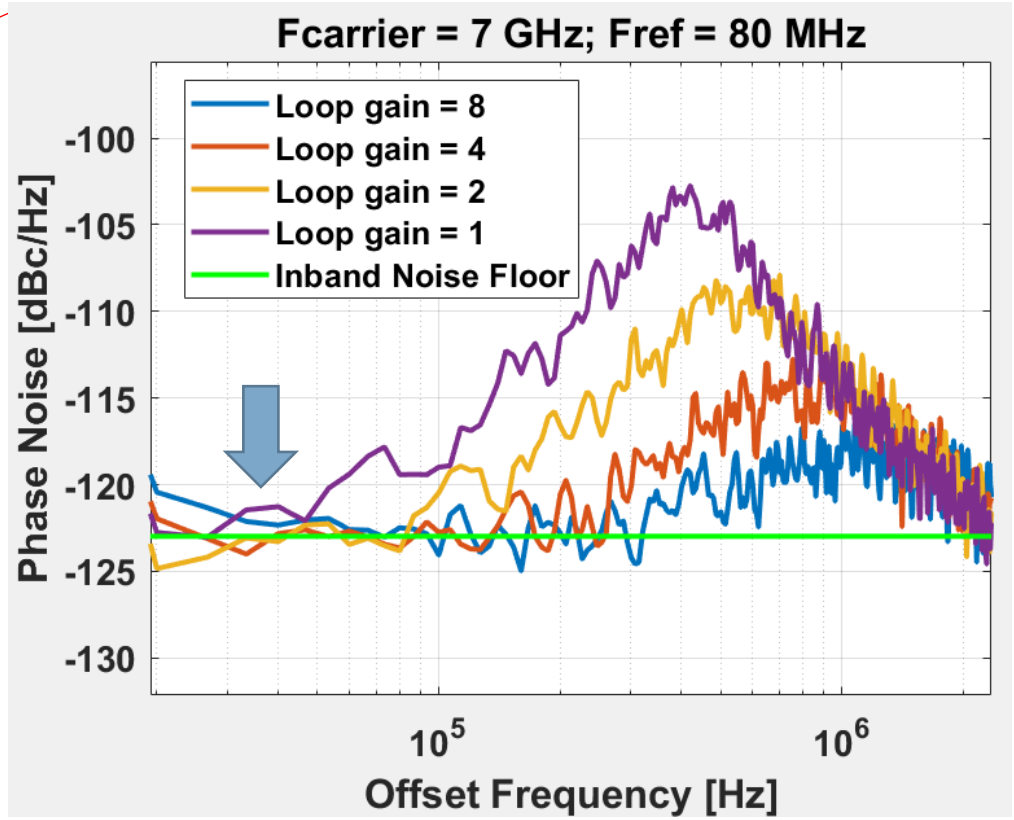
- Phase noise plots are not an accurate representation of the actual Fractional-spur level
    - Nevertheless, we can use the phase noise plots to assess variations in the spur level for different PLL bandwidth

- In order to estimate the spur level correctly, we should:
    1) Calculate or measure the spectrum of the clock signal
    or
    2) process the durations of the cycles of the clock signal and in particular:
        a) Extract amplitude of each periodic component in the DCO frequency
        b) Use standard modulation theory (Bessel's functions) to predict spur level

- In the sake of simplicity, we are only looking at the spurs in the phase noise plots in the following slides

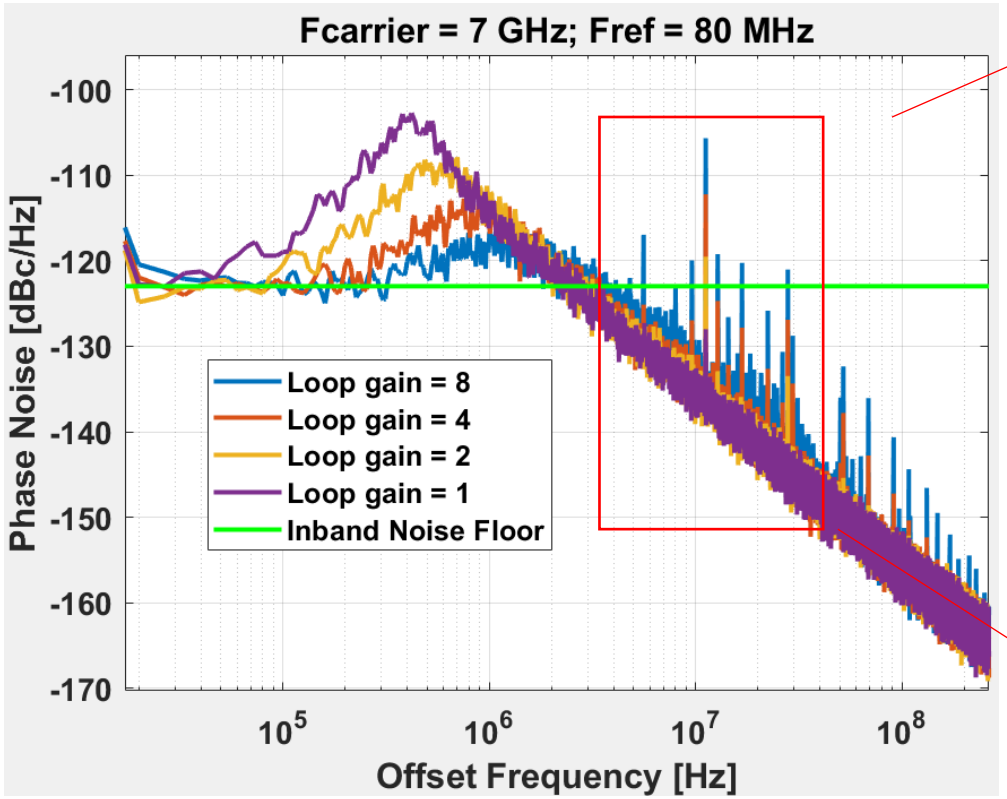
Example PLL Model with different Bandwidth: in-band-noise levels

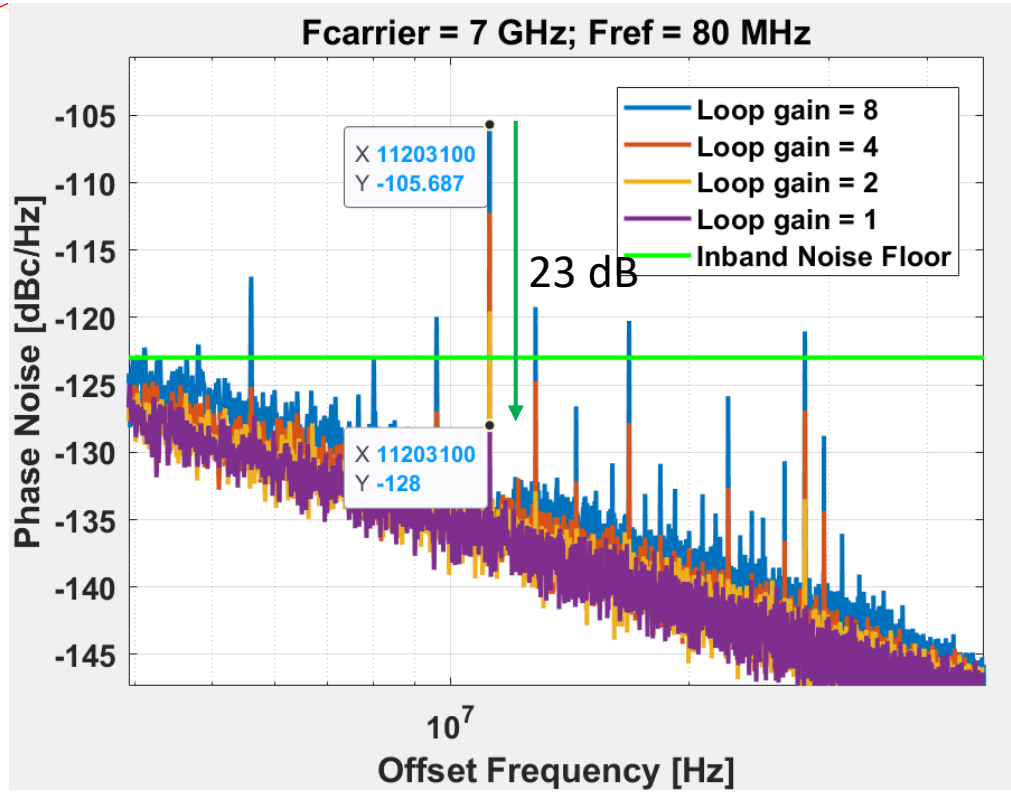




- TDC with 0.5 ps step
- Analytical predictions of the in-band-noise floor match simulations
- The results from the PLL model are consistent with the previous design considerations

Example PLL Model with different Bandwidth: spur levels



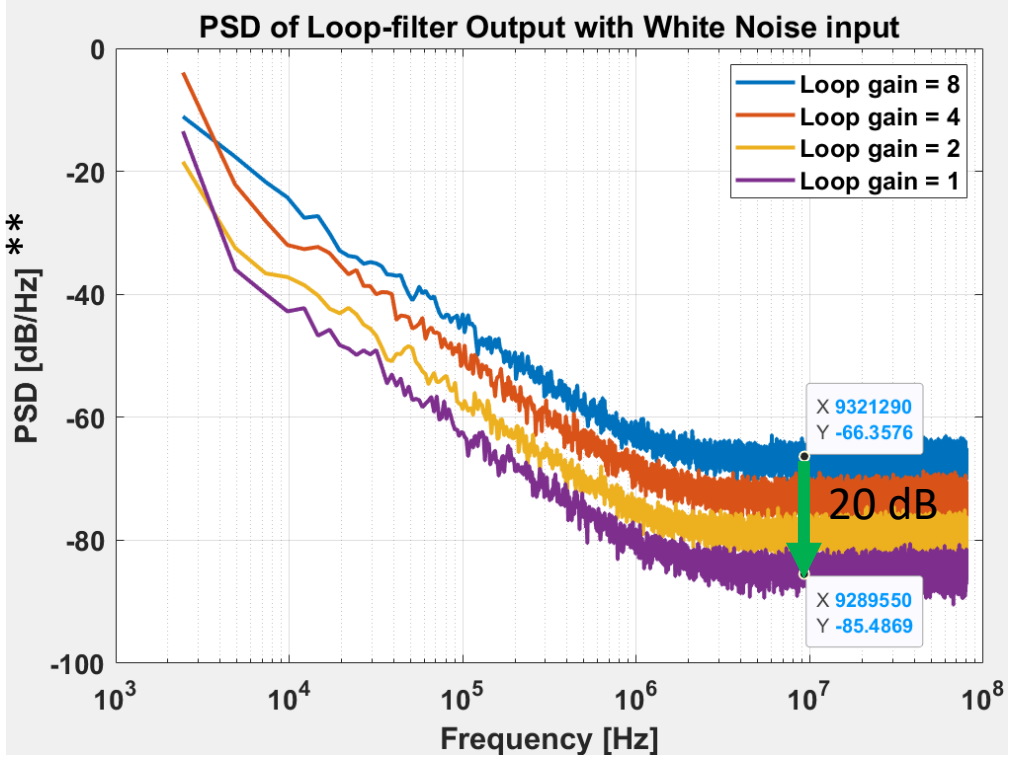


- **Design trade-off (bandwidth: integrated-jitter vs Frac-N-spur)**: when the PLL bandwidth reduces, the level of the fractional-N spurs decreases but the integrated jitter increases

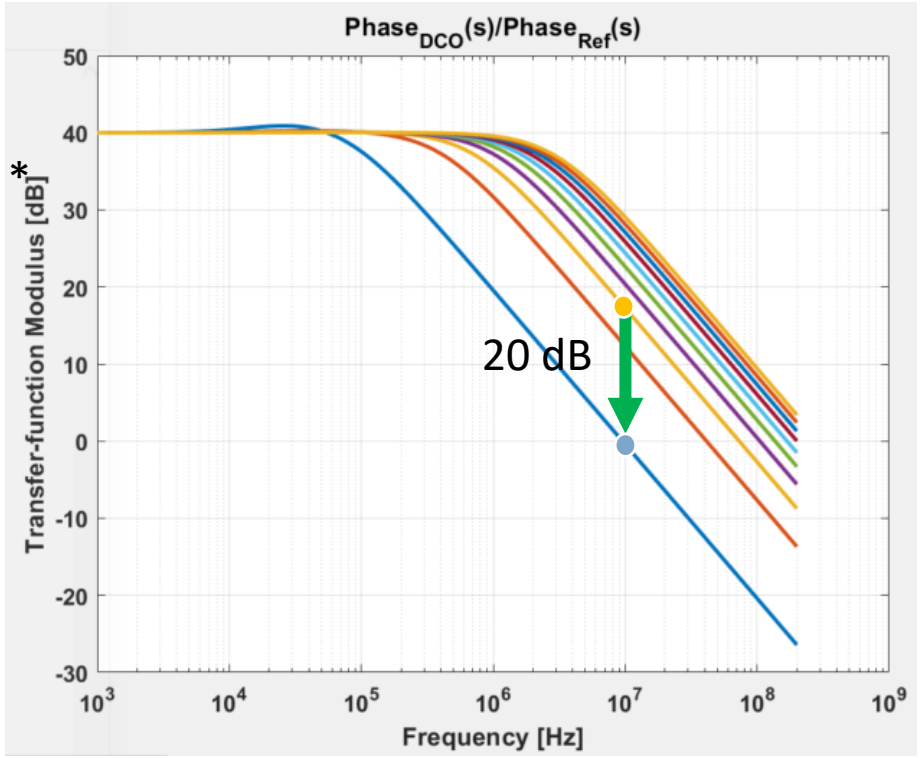
- Spur level reduced by 5 dB circa for each

Spur reduction in relation to PLL and Loop-filter Transfer Functions

Loop-filter used in the PLL model



Example PLL-noise transfer functions



- The spur reduction is consistent with the extra attenuation in the loop-filter in the PLL model
  - It also fits with the behavior of the example transfer functions previously shown.

**dB = dB20, *dB=dB10. The phase noise in the previous slides is expressed in dB10 because it's a Power-Spectral-Density.

Additional Design Constraints

- Differential and Integral Nonlinearity errors => larger frac-N spurs
- Smaller quantization step => lower frac-N spurs
- Design guideline: target TDC step needs to be small to reduce frac-N spurs

Wi-Fi Requirements: Spurs and DCO

Noise Requirements for Wif-Fi

	JSSC 2016 [7]	ISSCC 2016 [8]	JSSC 2017 [9]	ISSCC 2019 [10]	ISSCC 2020 [11]	ISSCC 2021 [12]	ISSCC 2021 [13]	JSSC 2020 [14]
Technology	28nm	28nm	14nm	28nm	14nm	28nm	16nm	22nm
Type	Subsampling analog	Subsampling digital	TDC-based	PFD-CP based	Sampling analog	Sampling analog	TDC Stochastic	Time-Amplifier plus TDC
Fref [MHz]	40	40	26	160	500	153	245	80
Fout [GHz]	11.72	5.825	2.69	5.82	12.47	3.1	15.7	6.5
RMS jitter [fs]	176	159	137	82	58	91	45	151
Fractional spur [dBc]	< -56	< -54	< -78	< -60	< -63	< -72	Integer-N only	< -49
Reference spur [dBc]	-69	-78	-86.6	-66.6	-73.5	-72	-75	-80
Power [mW]	5.6	8.2	13.4	14.7	18	8.2	56	23
FoM [dB]	-247.6	-246	-250	-250	-252.1	-251	-248	-242
Area [mm^2]	0.25	0.3	0.257	0.47	0.16	0.31	0.5	0.17

- State of the art integrated-jitter is getting pushed well below **100 fs**
- Fractional-N spurs < -60 dBc
- FoM = Integrated Jitter * Power

$$\mathrm{FOM_{PLL}} = 10\log\left[\left(\frac{\sigma_{t,\mathrm{PLL}}}{1s}\right)^2 \cdot \frac{P_{\mathrm{PLL}}}{1\,\mathrm{mW}}\right]$$

MaxLinear

VCO/DCO Oscillators in the State-of-the-Art [12]

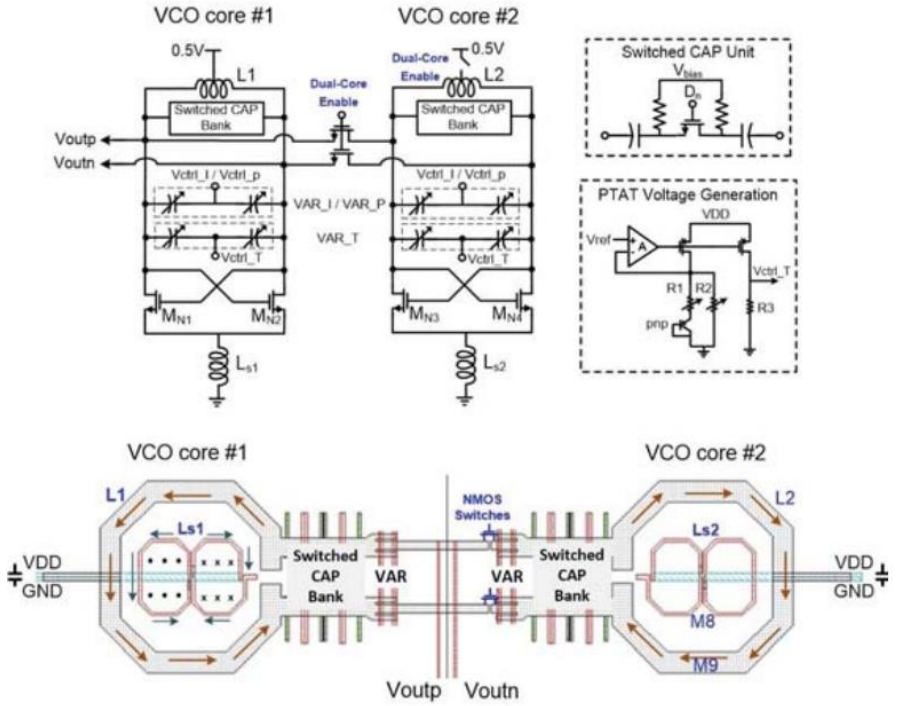


Figure 32.2.3: Circuit and layout implementation of the dual-core VCO.

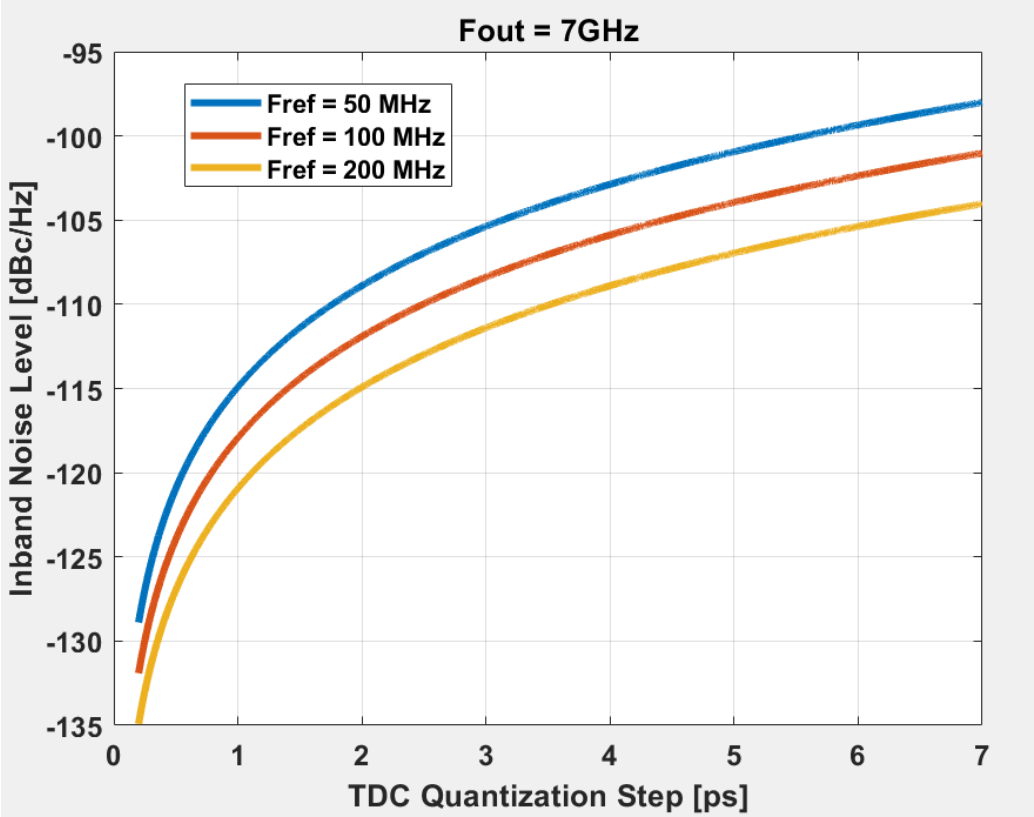
- We can assume that the VCO/DCOs reached almost the limit of the CMOS technology => in fact, in order to push further the performance, the state-of-the-art PLLs use multi-core VCO/DCOs.
  - Improving the VCO/DCOs noise performance becomes increasingly more challenging

- We will assume an example fixed DCO noise profile that is close to that in state-of-the art PLLs.
  - Is so much important to lower the VCO/DCO noise performance?

Wi-Fi Requirements:
In-band noise and TDC Quantization Error

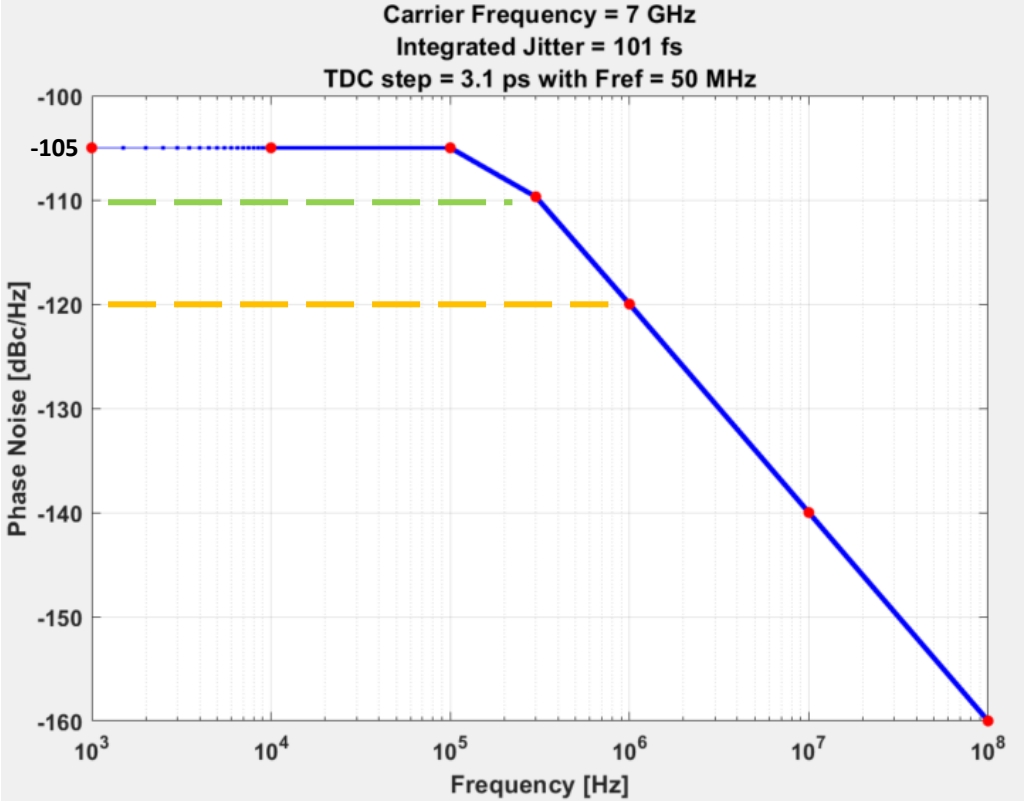
Theoretical In-band Noise as a function of the TDC quantization step

$$S_{\mathrm{TDC}}(f) = \frac{2}{f_{\mathrm{REF}}} \frac{(2\pi f_{\mathrm{OUT}} \tau_{\mathrm{TDC}})^2}{12} \left(\frac{\sin\left(\frac{\pi f}{f_{\mathrm{REF}}}\right)}{\frac{\pi f}{f_{\mathrm{REF}}}} \right)^2$$



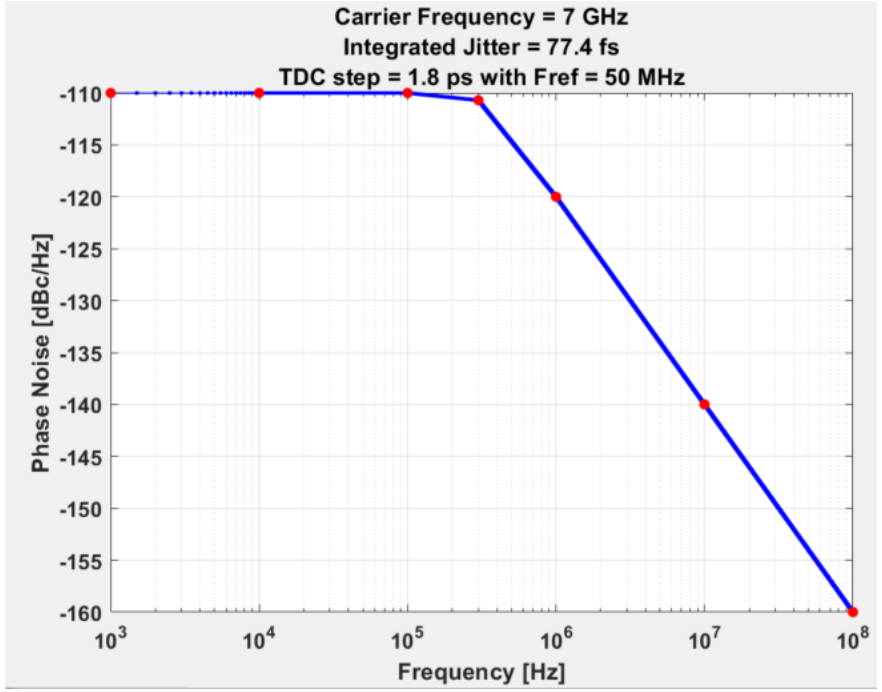
- In a TDC-based PLL, the TDC quantization contributes to the in-band noise floor directly
  - Smaller TDC step => lower in-band noise
  - When Fref increases the contribution to the noise floor decreases
- Equation from [19]

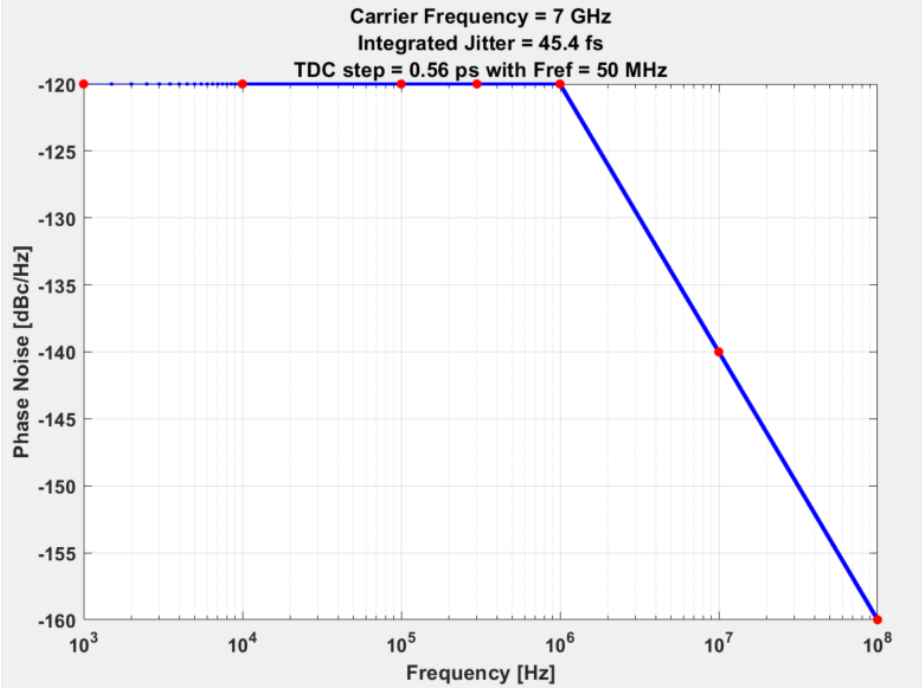
An Example Theoretical Phase Noise for 100fs integrated Jitter



- Simple DCO noise profile => -120dBc/Hz at 1MHz offset, pure thermal noise
- Integrated jitter towards = 100fs => required **3 ps TDC-step** with Fref = 50MHz
- What if we set the bandwidth larger, as shown by the green and yellow dashed lines?

Examples for PLLs with Extended Bandwidth





- **Design trade-off (bandwidth: integrated-jitter vs TDC-complexity)**: when the DCO noise profile is fixed, increasing the bandwidth reduces the integrated jitter but the required TDC quantization step reduces.
- Integrated jitter towards 50fs => required subpicosecond TDC-step (with Fref 50MHz)
  - TDC requirements are relaxed when Fref increases
- Improve in-band noise floor => improve integrated jitter greatly => this is what we can also see in the state-of-the-art

State-of-the-Art PLLs

A Way to Compare very different PLL Architectures

- In the following, we will review some state-of-the-art PLLs.
- For each PLL, we will ask the question:
    - What TDC quantization step is required to build an equivalent TDC-based PLL?

- The “equivalent TDC quantization step” is obtained with the following procedure:
    1) **Estimate the in-band** noise floor from the reported phase noise (**visual inspection**)
    2) Calculate the **equivalent TDC quantization** step associated by reworking the equation below:

$$S_{\mathrm{TDC}}(f) = \frac{2}{f_{\mathrm{REF}}} \frac{(2\pi f_{\mathrm{OUT}} \tau_{\mathrm{TDC}})^2}{12} \left(\frac{\sin\left(\frac{\pi f}{f_{\mathrm{REF}}}\right)}{\frac{\pi f}{f_{\mathrm{REF}}}} \right)^2$$

State of the Art: Equivalent TDC quantization step

	JSSC 2016 [7]	ISSCC 2016 [8]	JSSC 2017 [9]	ISSCC 2019 [10]	ISSCC 2020 [11]	ISSCC 2021 [12]	ISSCC 2021 [13]	JSSC 2020 [14]
Technology	28nm	28nm	14nm	28nm	14nm	28nm	16nm	22nm
Type	Subsampling analog	Subsampling digital	TDC-based	**PFD-CP based**	**Sampling analog**	**Sampling analog**	**TDC Stochastic**	Time-Amplifier plus TDC
Fref [MHz]	40	40	26	160	500	153	245	80
Fout [GHz]	11.72	5.825	2.69	5.82	12.47	3.1	15.7	6.5
RMS jitter [fs]	176	159	137	82	58	75	45	151
Estimated In-band floor referred to 7GHz [dBc/Hz]	-116	-113	-109	-108	-126	-114	-119	-106
Estimated TDC step [ps]	0.7	1.0	1.3	3.5	0.7	1.8	1.3	3.3
Estimated PN Roll-off frequency [MHz]	3	1	0.8	0.6	10	1	1	0.5

- Inband noise floor levels are equivalent to TDCs with quantization steps of 1 picosecond or smaller
- TDC-based PLLs can be competitive when compared to popular sampling and subsampling

Best integrated jitter

Best estimated in-band noise floor at 7GHz

It is challenging to implement such high frequency

State of the Art: Spurs

	JSSC 2016 [7]	ISSCC 2016 [8]	JSSC 2017 [9]	ISSCC 2019 [10]	ISSCC 2020 [11]	ISSCC 2021 [12]	ISSCC 2021 [13]	JSSC 2020 [14]
Technology	28nm	28nm	14nm	28nm	14nm	28nm	16nm	22nm
Type	Subsampling analog	Subsampling digital	TDC-based	PFD-CP based	Sampling analog	Sampling analog	TDC Stochastic	Time-Amplifier plus TDC
Fref [MHz]	40	40	26	160	500	153	245	80
Fout [GHz]	11.72	5.825	2.69	5.82	12.47	3.1	15.7	6.5
RMS jitter [fs]	176	159	137	82	58	75	45	151
Fractional spur [dBc]	< -56	< -54	< -78	< -60	< -63	< -72	Integer-N only	< -50
Reference spur [dBc]	-69	-78	-86.6	-66.6	-73.5	-72	-75	-80
Estimated PN Roll-off frequency [MHz]	3	1	0.8	0.6	10	1	1	0.5

Lowest fractional-N spurs

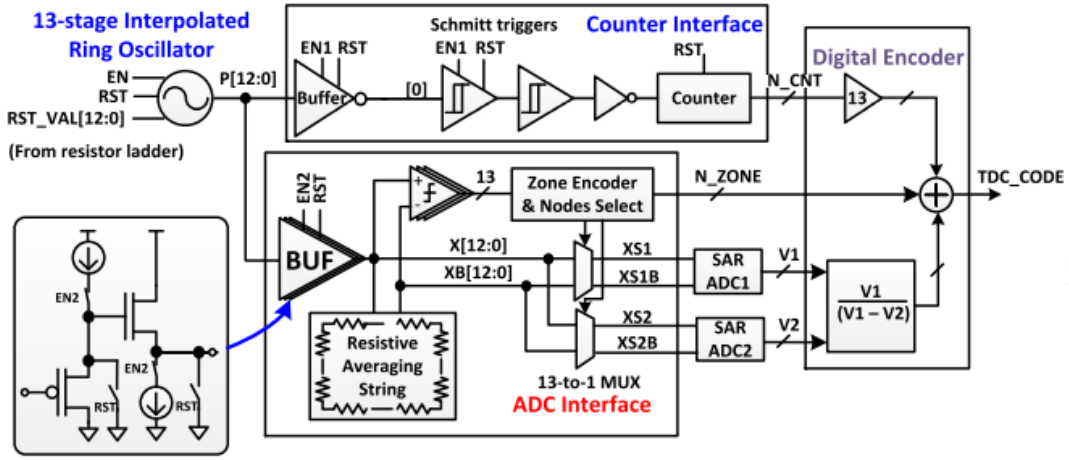
Lowest Reference spur

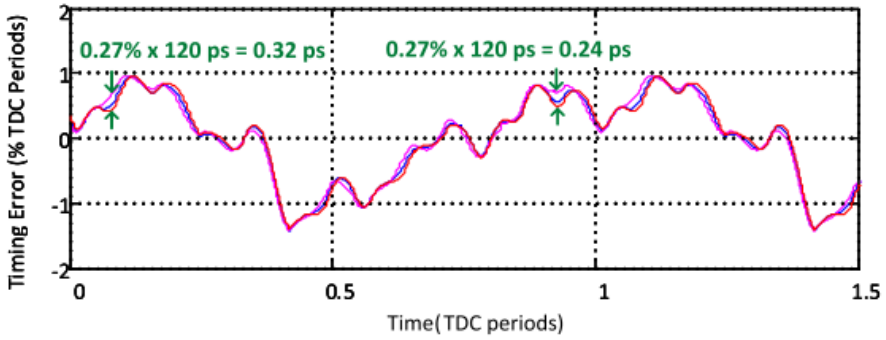
Large fractional-N spurs

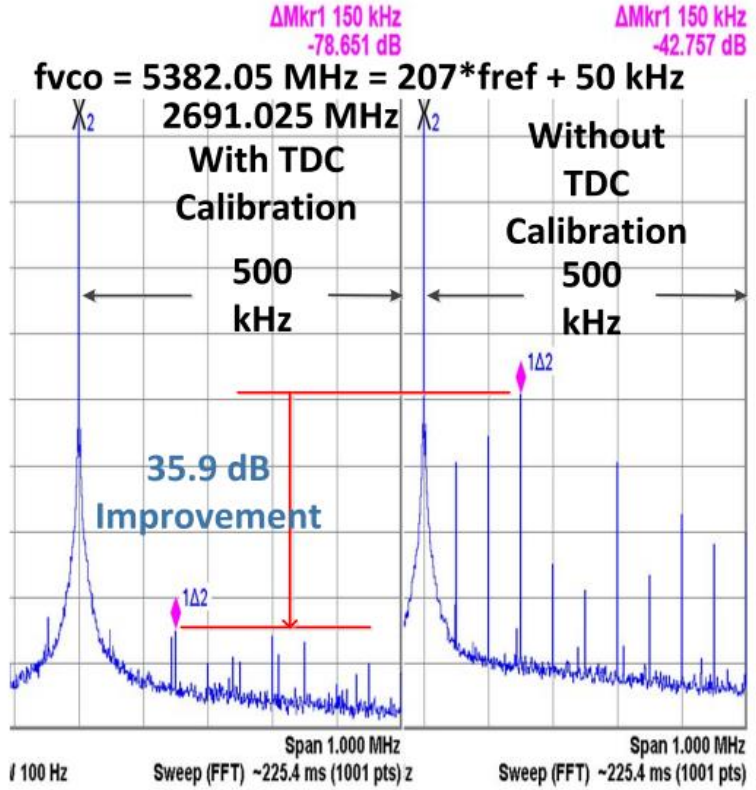
- Quite remarkable that TDC-based PLLs are competitive in terms of reference spur

Techniques to Advance the State-of-the-Art

TDC Linearization [9]







- Ring-oscillator with resistive interpolation => high linearity
- TDC calibration is a digital mapping of the TDC output codes

DTC Linearization [8] (ISSCC 2016)

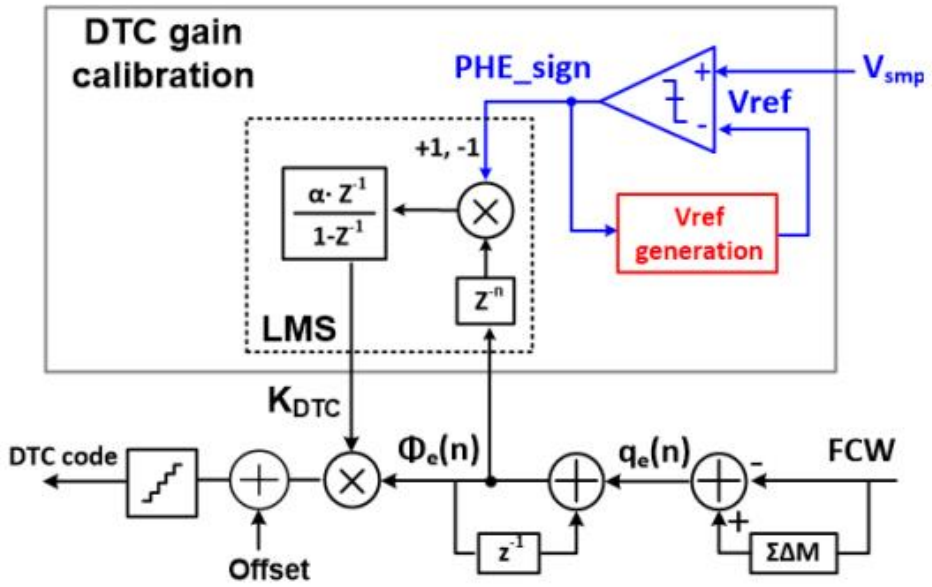
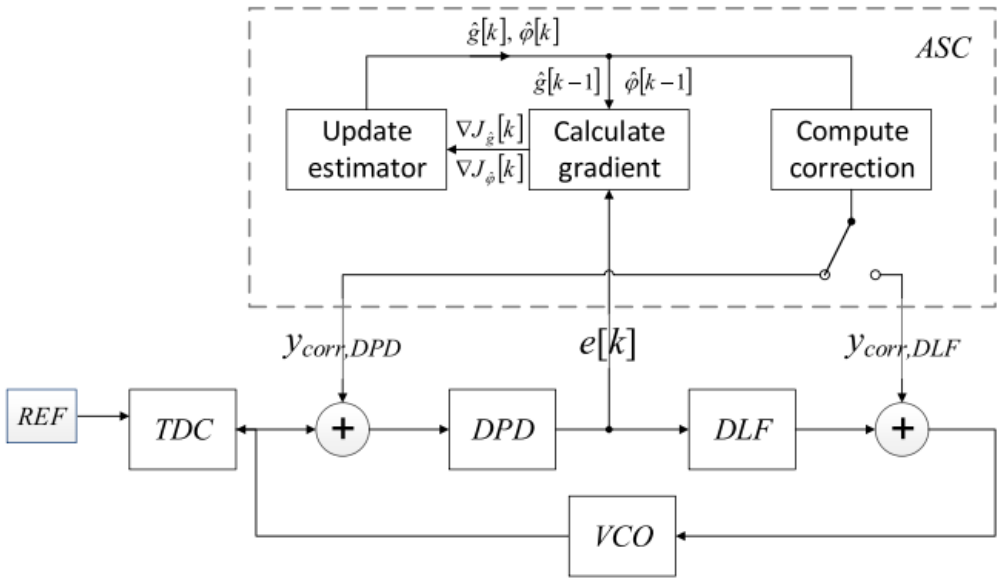
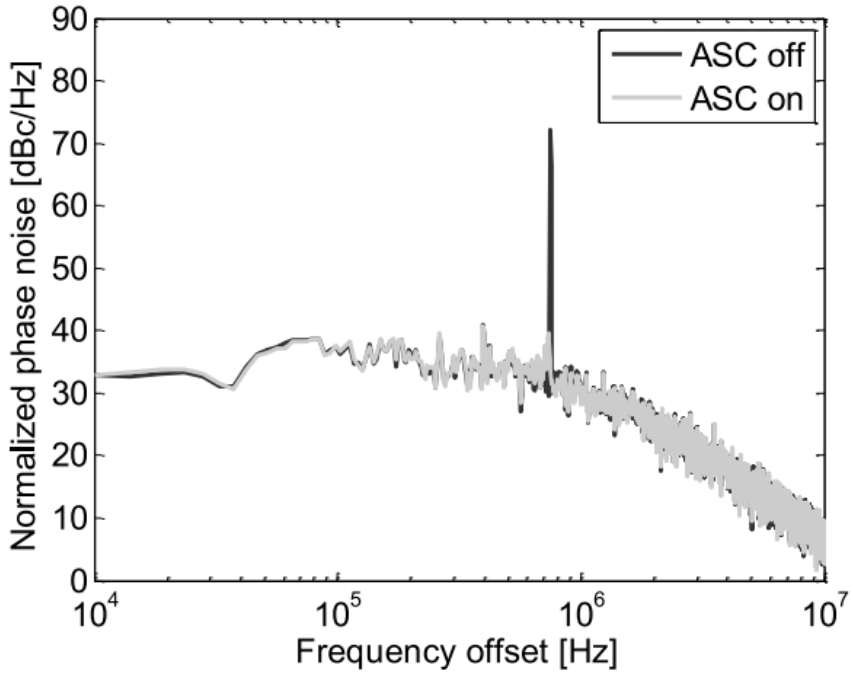


Fig. 4. Comparator with dynamically adjusted threshold for DTC gain calibration.

- Pure digital gain correction at the DTC control word.

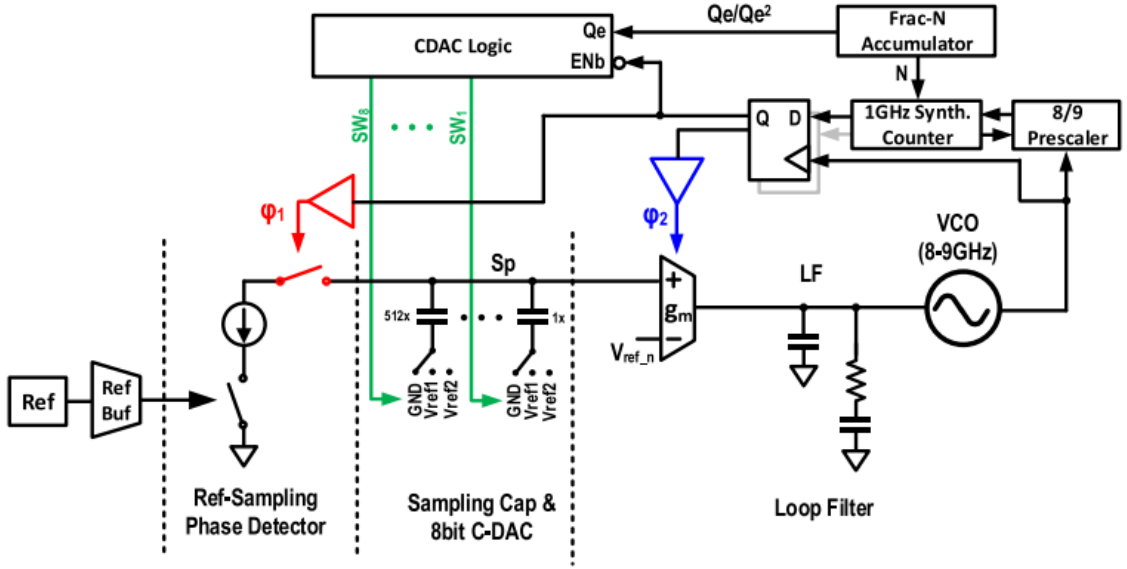
Fully-digital Spur Cancellation [15] (TCAS-II 2017)

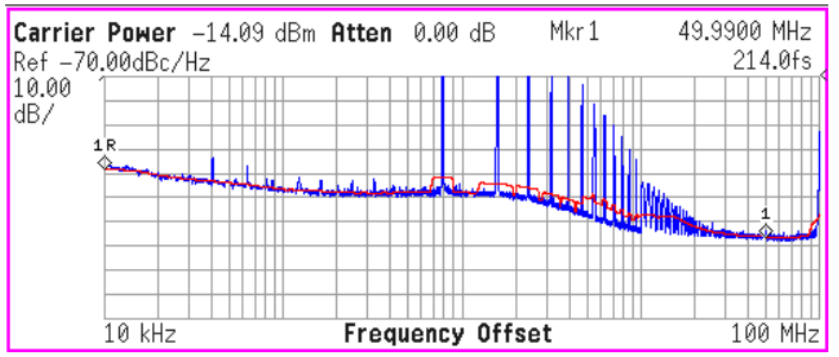




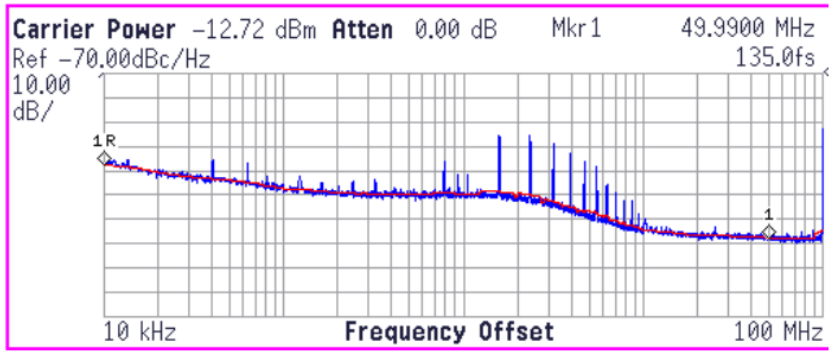
- Very promising topic
- Adding spur identification/canceller in a digital PLL is “cheap” when the identification/canceller is fully implemented in RTL code.

Analog Spur Cancellation [16] (JSSC 2021)





(a)

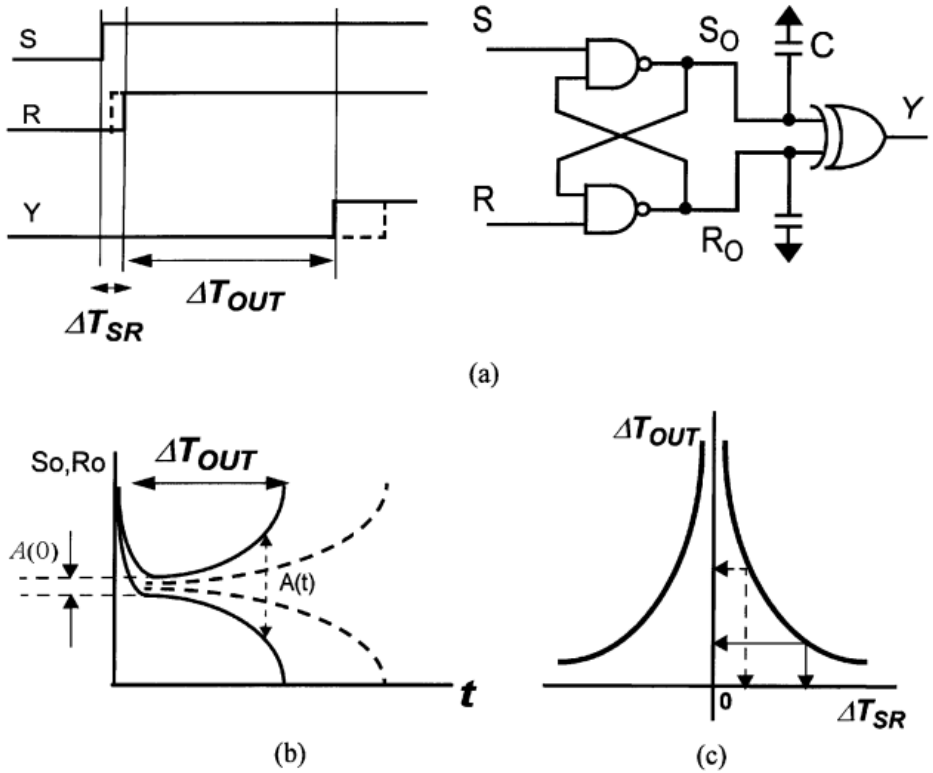


(b)

Fig. 18. Measured PLL output (divided by 2) phase noise in fractional mode (a) without quantization error cancellation and (b) with quantization error cancellation.

- Quite remarkable results
- Clearly spur cancellation is a topic for future generation of PLLs

Time Amplifiers [17] (JSSC 2008)



- A latch operates as a time amplifier when the transitions of the “set” and “reset” inputs are close enough
- This phenomenon is also referred to as “metastability” in the digital flow

PLL with Time-Amplifier-assisted-TDC [14] (JSSC 2021)

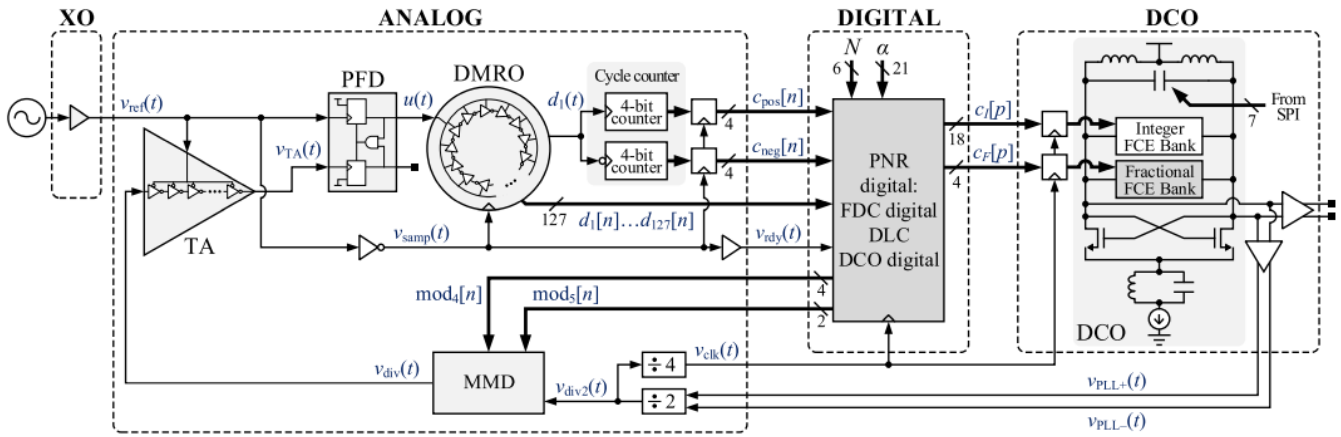
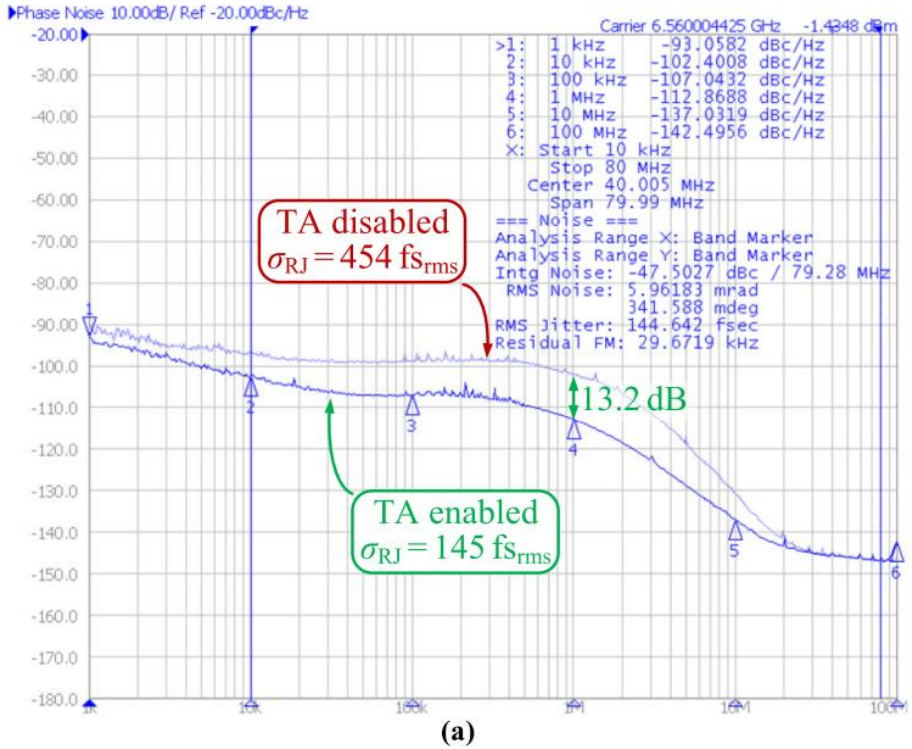


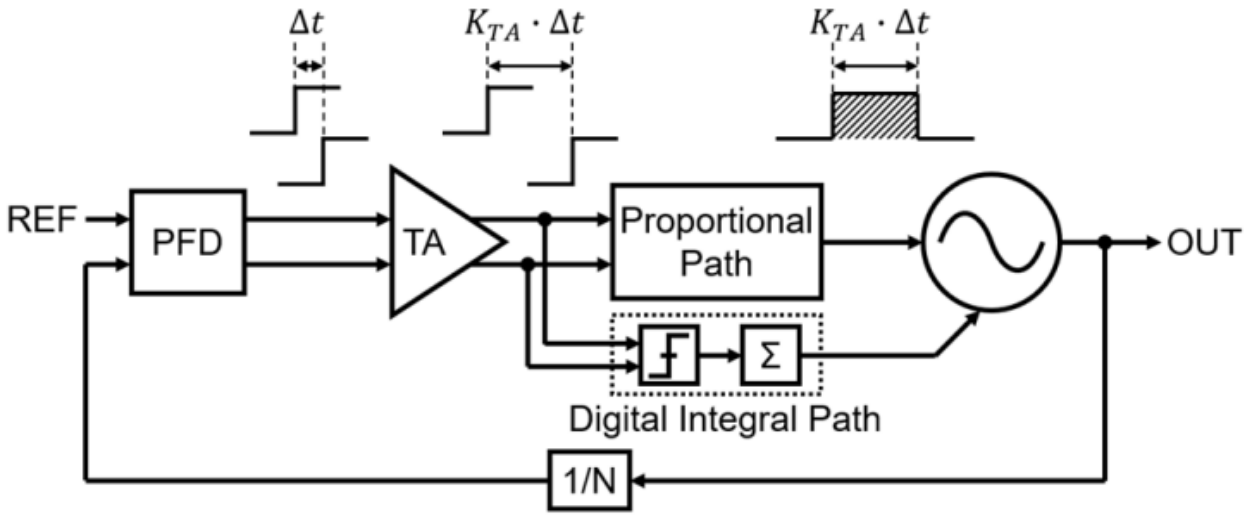
Fig. 3. Block diagram of the PLL showing implementation details and the four different power domains in dashed boxes.



(a)

- Significant improvement in the in-band noise level
- Improve equivalent TDC step size at the cost of amplification of TA input noise

PLL with PFD-plus-Time-Amplifier [18] (IEEEAccess 2022)



- A PFD-TA is used as a 1-bit TDC
- Better phase noise compared to a BB-PD
- Integrated jitter achieved = 5ps

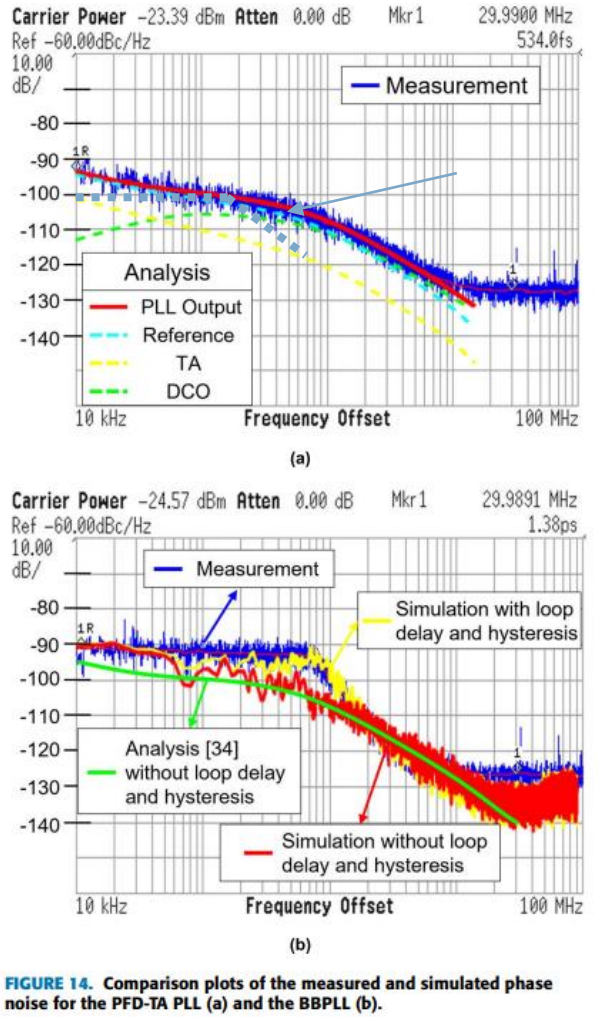


FIGURE 14. Comparison plots of the measured and simulated phase noise for the PFD-TA PLL (a) and the BBPLL (b).

Conclusion

- Summary of basic definitions and block diagrams for several PLL architectures have been shown
  - Simple comparison between very different PLL topologies

- Design trade-offs
  - More in-band noise filtering vs more DCO noise filtering
  - Reduced integrated jitter at the cost of higher frac-N spurs

- Very different state-of-the-art PLL architectures achieve similar performance in terms of integrated jitter and fractional-N spur
  - In-band noise in the reviewed state-of-the-art PLLs can be related to an equivalent TDC-based PLL with a sub-picosecond or picosecond TDC

- Promising techniques to improve the PLL performance
  - TDC linearization
  - Spur cancellers
  - Time-amplifiers

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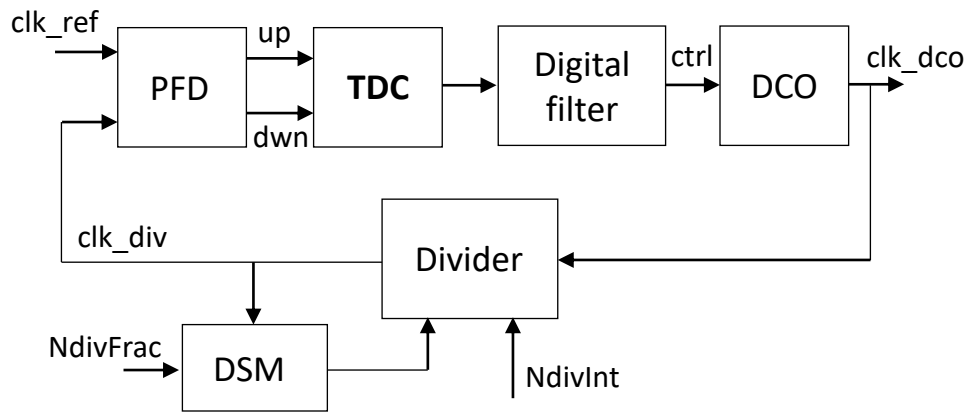
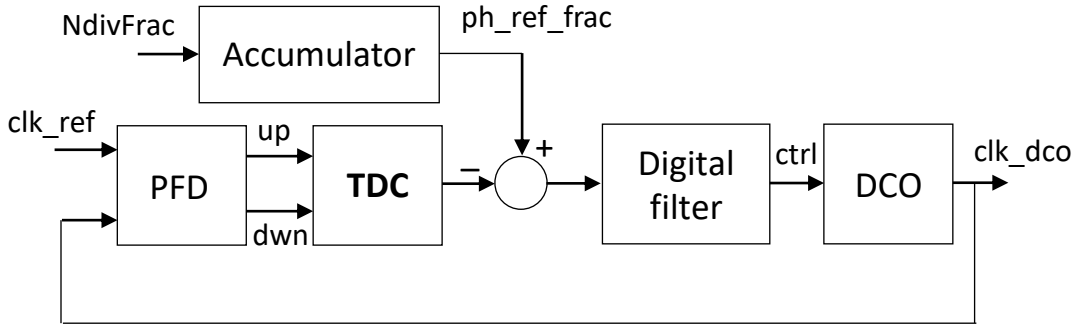
Extra Slides

Two simplified Topologies



Let's remove the feedback divider and add a target fractional phase



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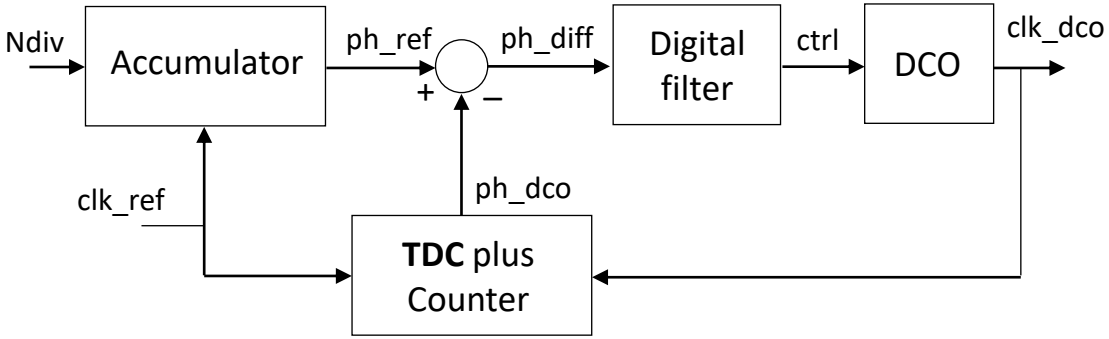
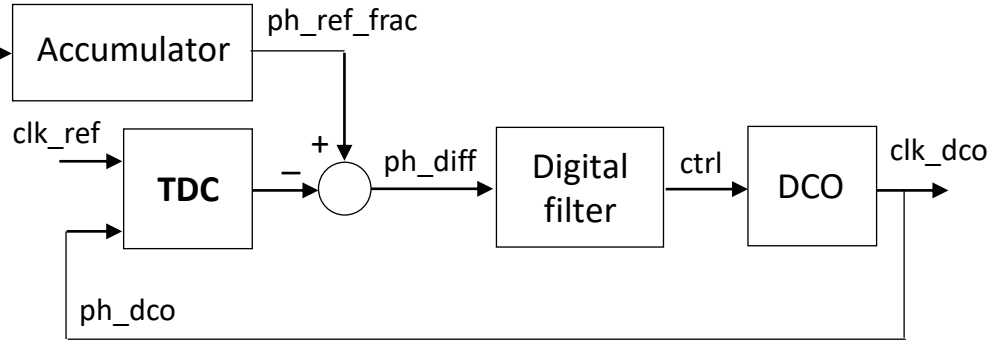


Ndiv = NdivInt + NdivFrac

Let's built a loop that operates only on the fractional phase



An analog Sub-sampling PLL with DTC [7]

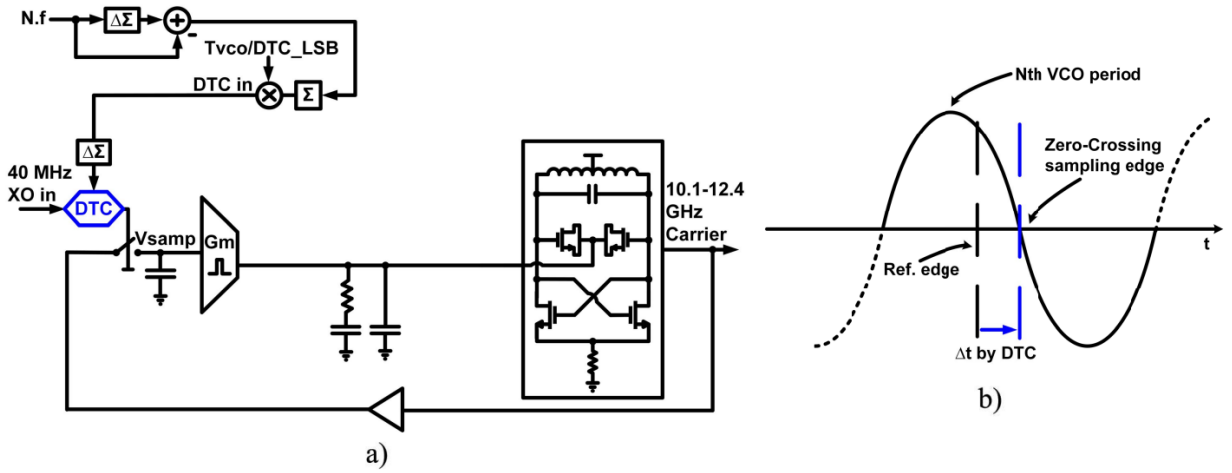
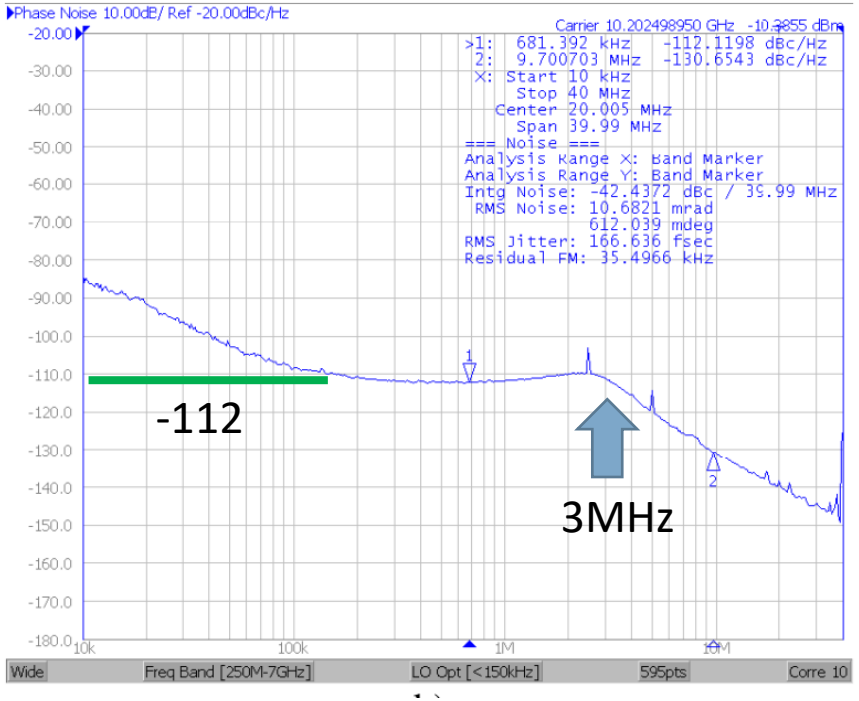


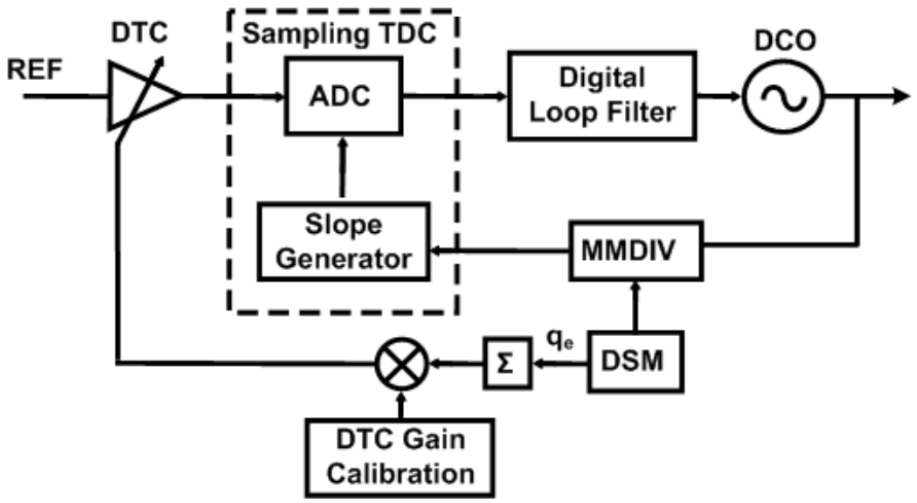
Fig. 3. (a) Simplified schematic of a DTC based fractional-N subsampling PLL (FNSSPLL). (b) Time domain operation of a DTC based FNSSPLL.



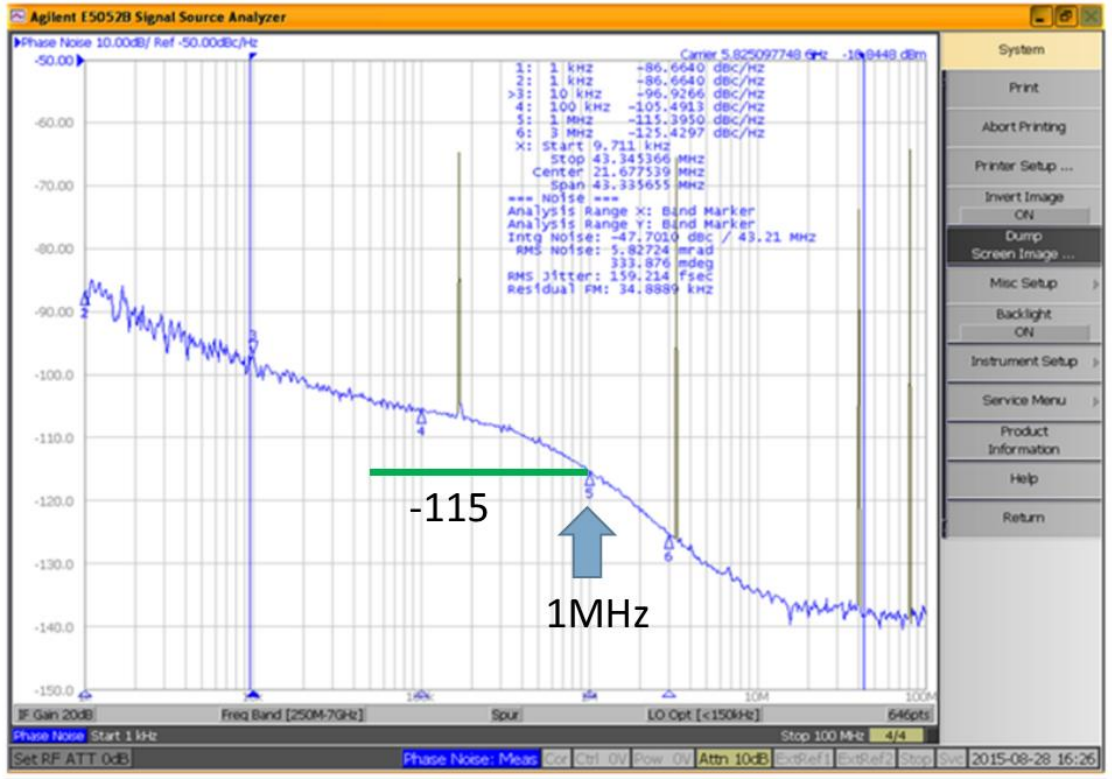

```
Fcarrier = 11.7 GHz
Fref = 40 MHz
In-band PSD Level = -112 dBc/Hz
TDC quantization step = 748.6087 fs
PSD referred to 7GHz = -116.4618 dBc/Hz
```

- Very compact PLL

A Slope-generator-plus-ADC-based PLL [8]




```
Fcarrier = 5.8 GHz
Fref = 40 MHz
In-band PSD Level = -115 dBc/Hz
TDC quantization step = 1069.0863 fs
PSD referred to 7GHz = -113.3666 dBc/Hz
```



- Notice the “DTC plus DSM error” used for enabling Fractional-N operations

A PFD-plus-TDC-based PLL [9]

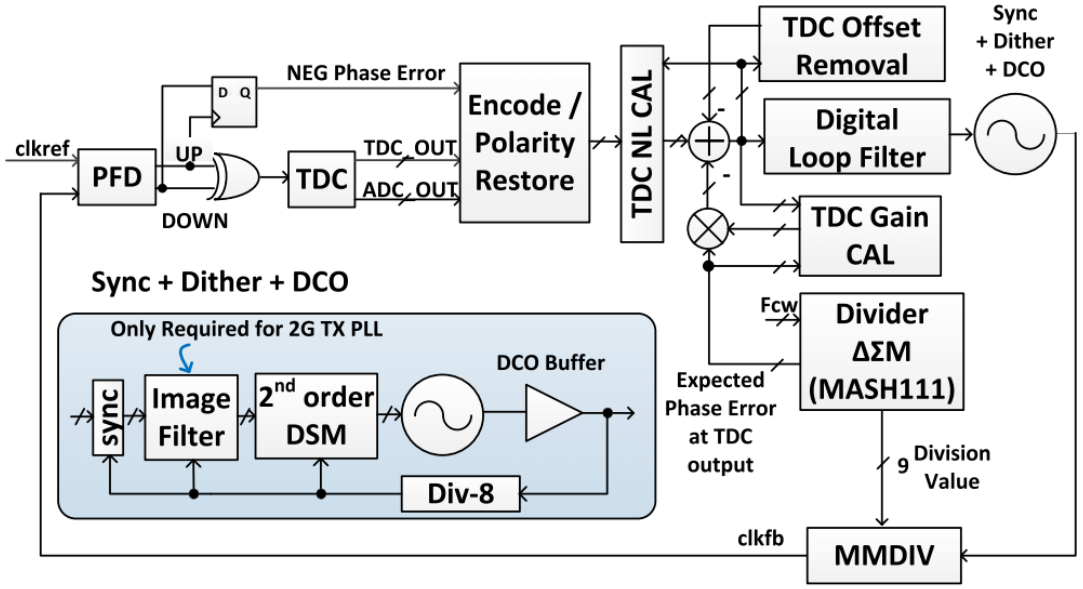
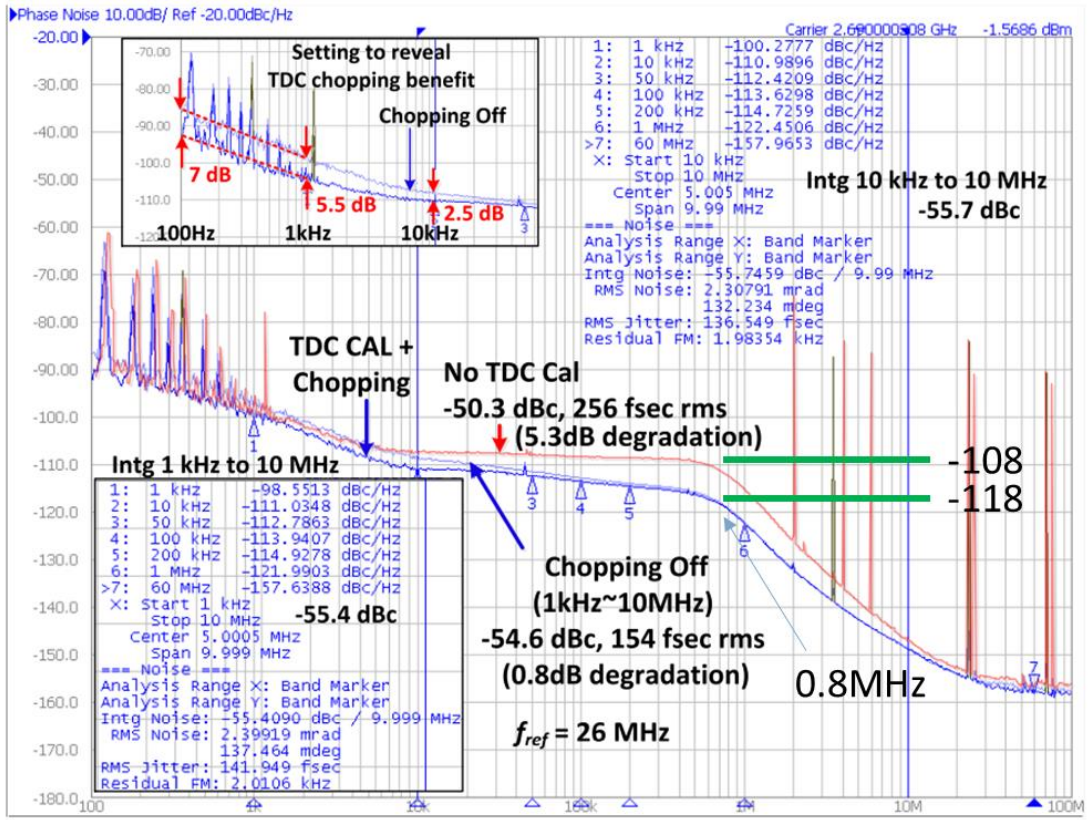


Fig. 1. Digital PLL architecture.

```
Fcarrier = 2.69 GHz
Fref = 26 MHz
In-band PSD Level = -118 dBc/Hz
TDC quantization step = 1315.6645 fs
PSD referred to 7GHz = -109.6931 dBc/Hz
```



- TDC input is chopped
- Strong focus on TDC calibration

A PFD-plus-Charge-Pump-based PLL [10]

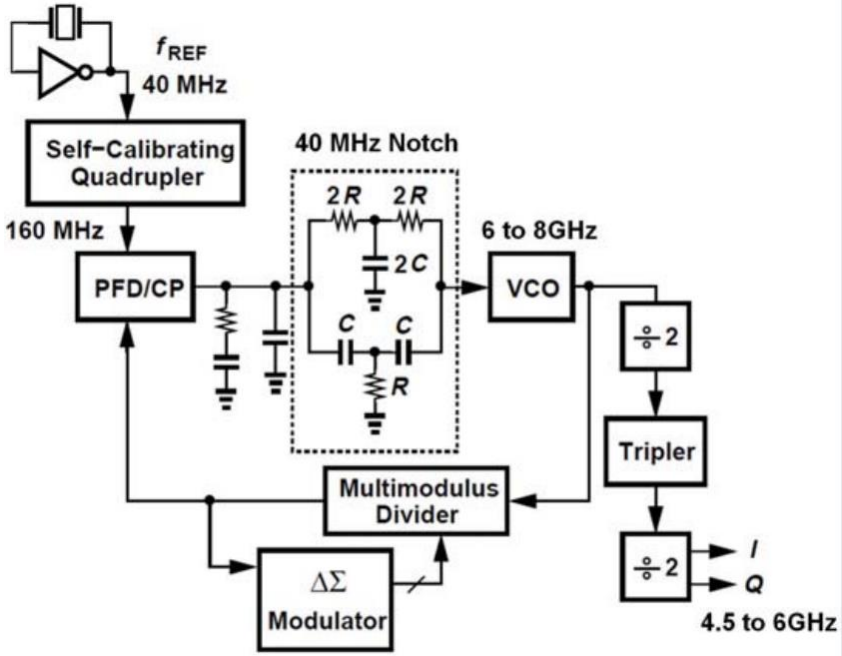
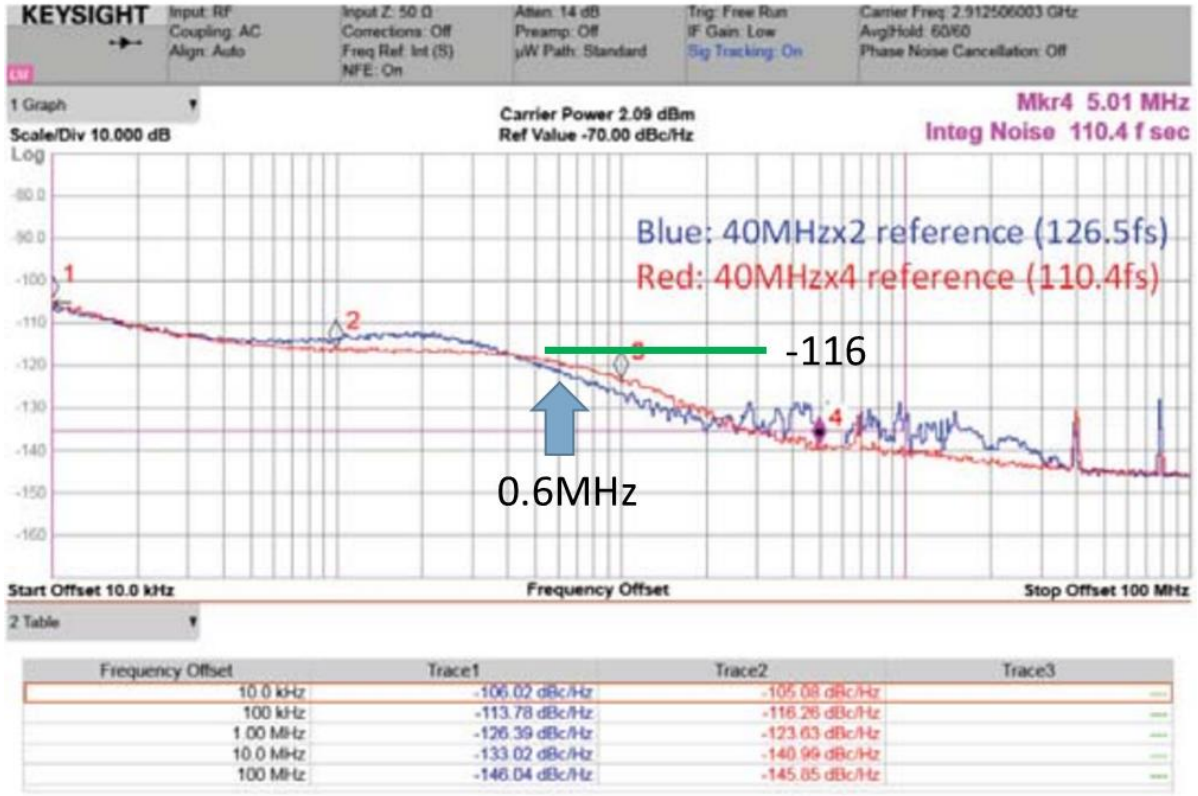


Figure 16.5.1: Proposed synthesizer architecture.




```
Fcarrier = 2.9 GHz
Fref = 140 MHz
In-band PSD Level = -116 dBc/Hz
TDC quantization step = 3565.1415 fs
PSD referred to 7GHz = -108.346 dBc/Hz
```

- The phase noise seems dominated by in-band noise (red-curve)
- Notch filter might complicate the design in the presence of PVT

A type-1 Sampling PLL [11]

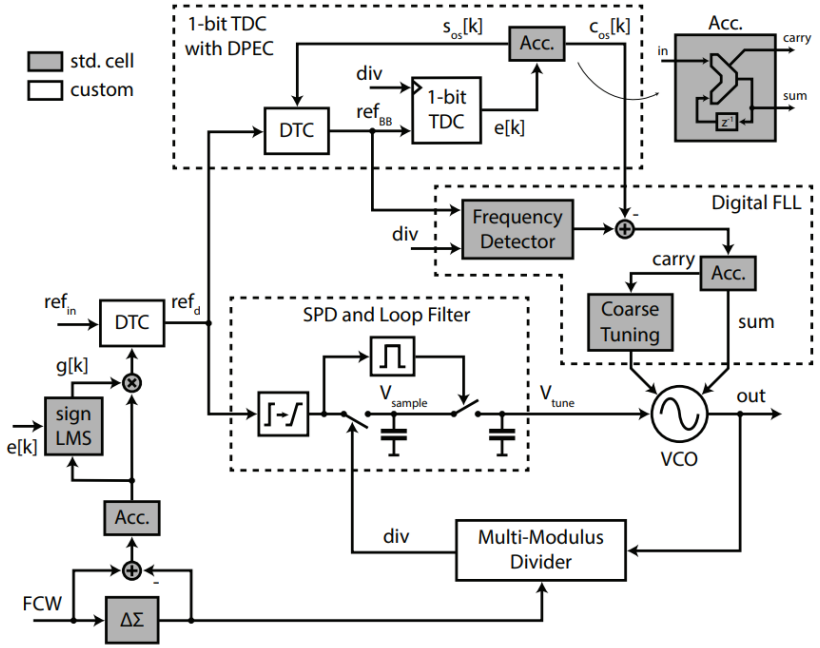
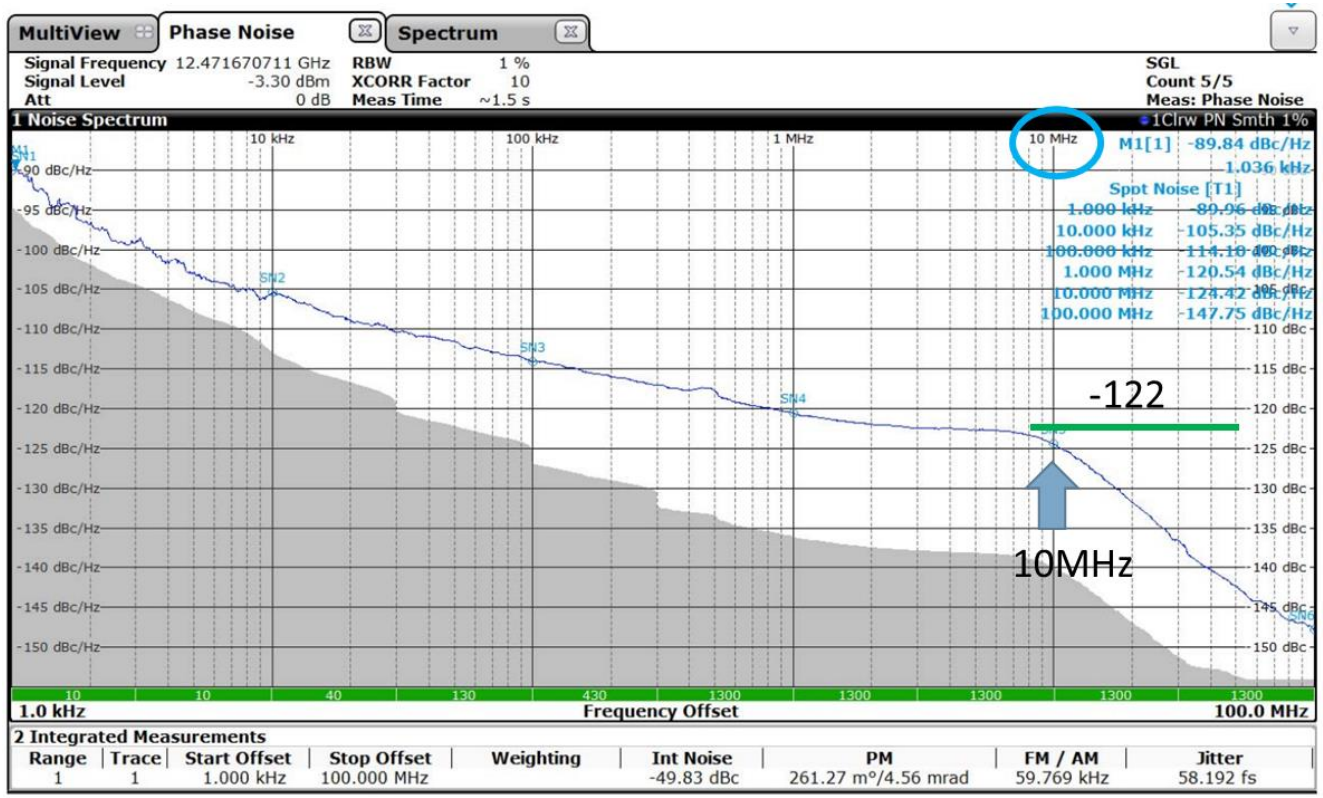


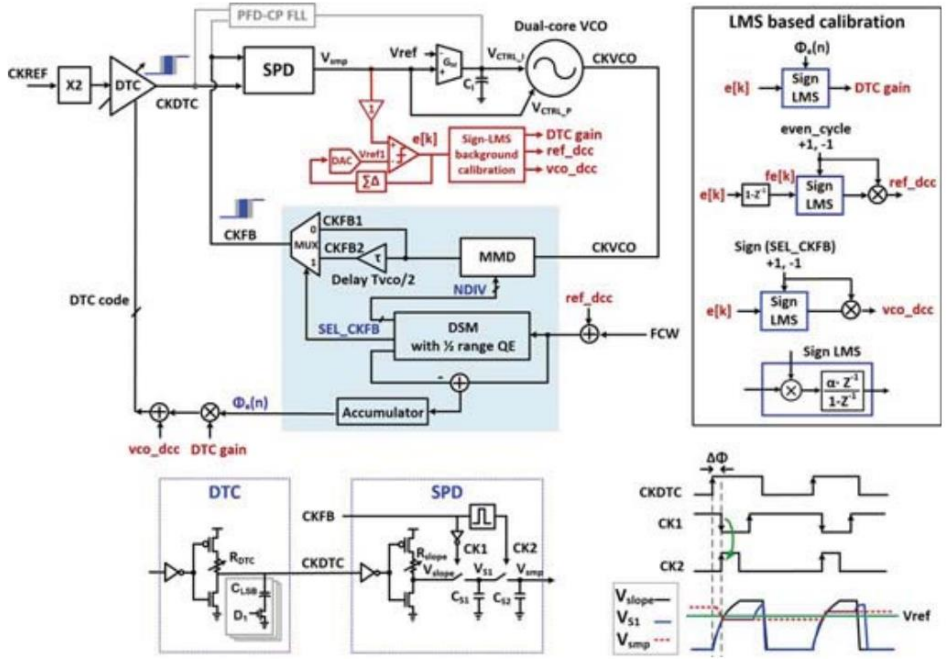
Figure 17.5.1: Block diagram of the presented fractional-N type-I sampling PLL.

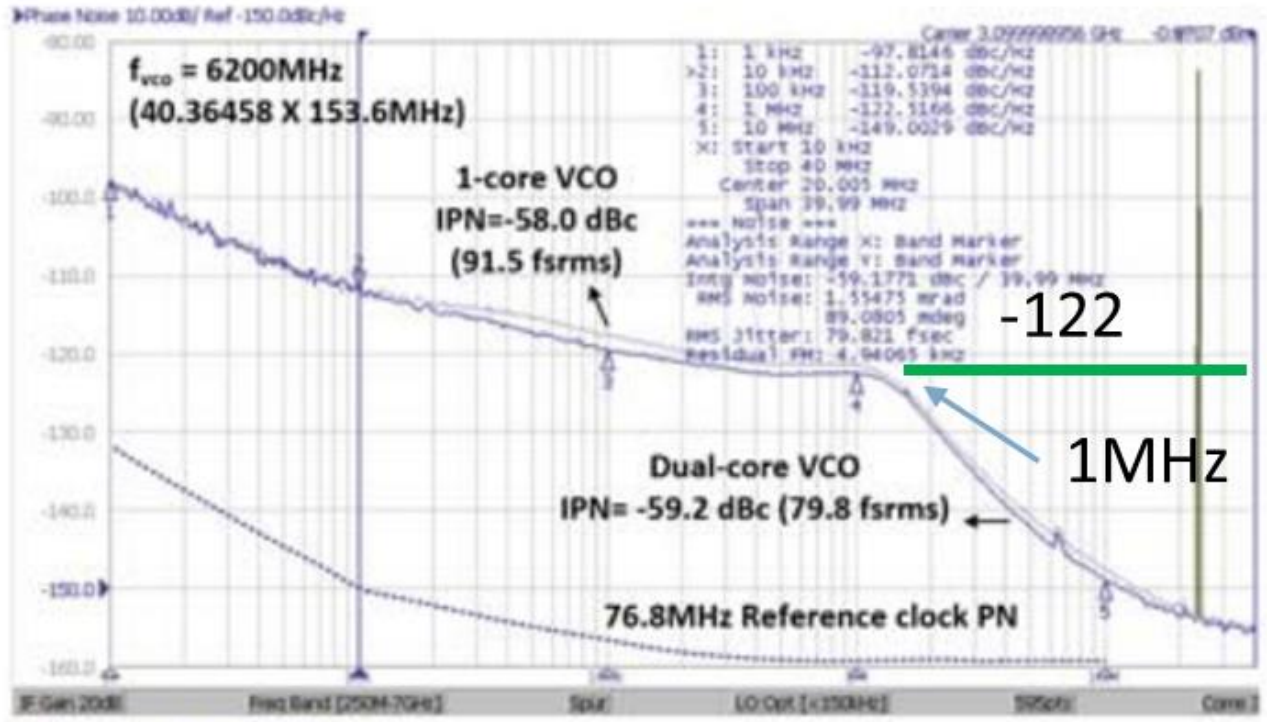
```
Fcarrier = 12.4 GHz
Fref = 500 MHz
In-band PSD Level = -122 dBc/Hz
TDC quantization step = 789.7217 fs
PSD referred to 7GHz = -126.9665 dBc/Hz
```



- Very large PLL bandwidth (compared to other works)
- Very compact architecture

A Sampling PLL [12]






```
Fcarrier = 3 GHz
Fref = 153 MHz
In-band PSD Level = -122 dBc/Hz
TDC quantization step = 1805.6568 fs
PSD referred to 7GHz = -114.6405 dBc/Hz
```

- Seems dominated by the reference clock phase noise

A Stochastic-TDC-based PLL [13]

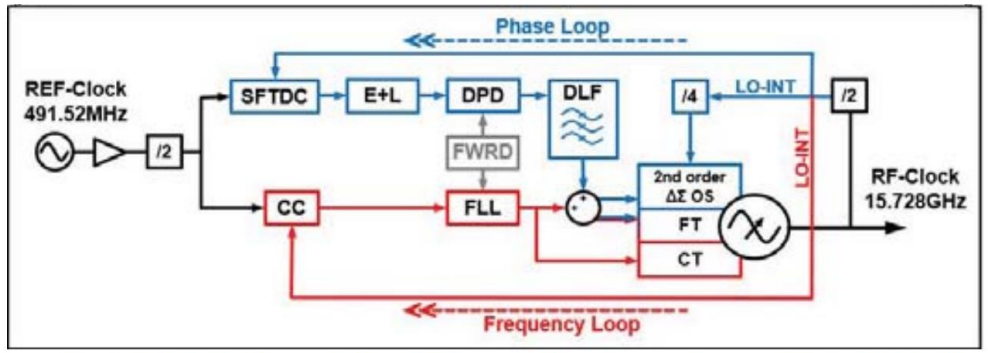
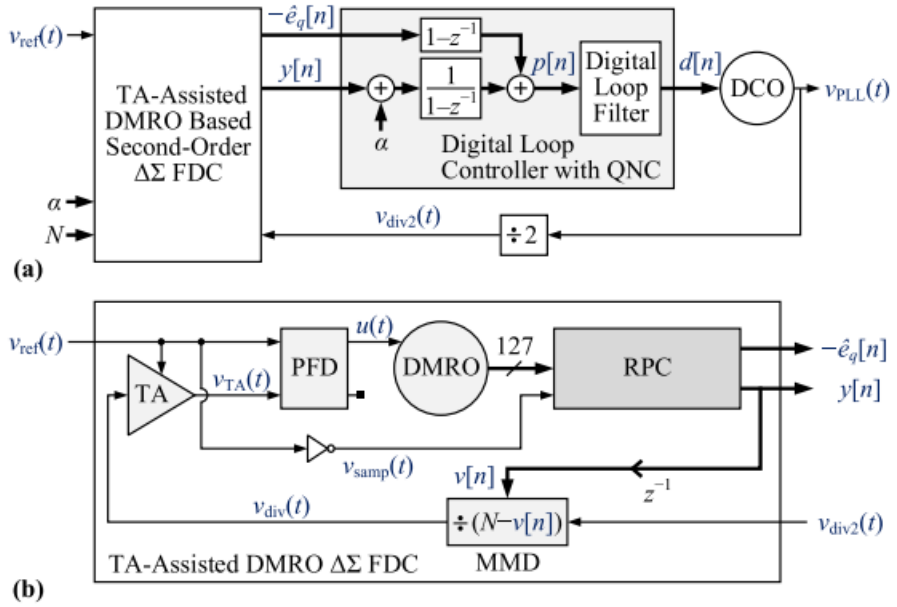


Figure 32.6.1: Multi-channel direct RF-sampling transceiver and SS-ADPLL block diagrams. Abbreviations are explained in the text.

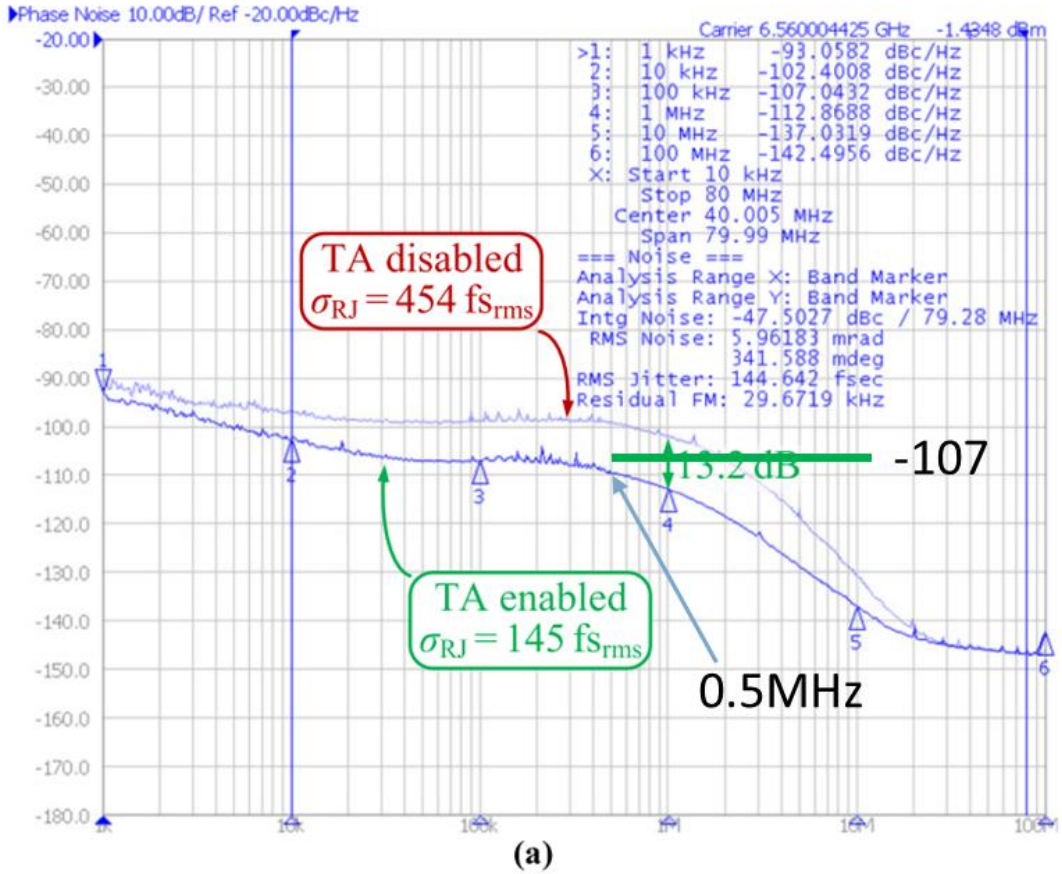
```
Fcarrier = 15.7 GHz
Fref = 245 MHz
In-band PSD Level = -112 dBc/Hz
TDC quantization step = 1380.6835 fs
PSD referred to 7GHz = -119.016 dBc/Hz
```

- Simple architecture with simple TDC
- Stochastic TDC is highly nonlinear

A Time-Amplifier-plus-TDC-based PLL [14]




```
Fcarrier = 6.5 GHz
Fref = 80 MHz
In-band PSD Level = -107 dBc/Hz
TDC quantization step = 3388.7723 fs
PSD referred to 7GHz = -106.3563 dBc/Hz
```



- Complex TDC
- Huge improvement in the phase noise when Time-Amplifier is enabled