BGA Reliability and Manufacturing Challenges

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Dr. Nathan Blattau

Ansys

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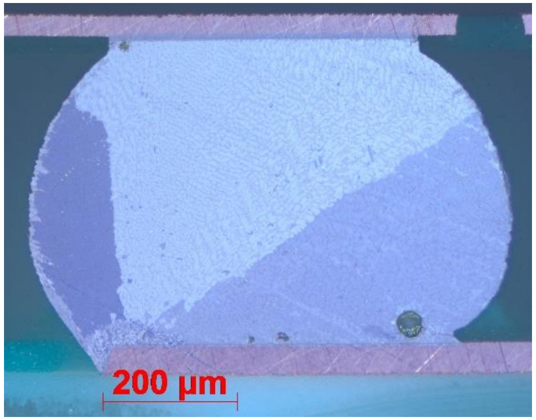
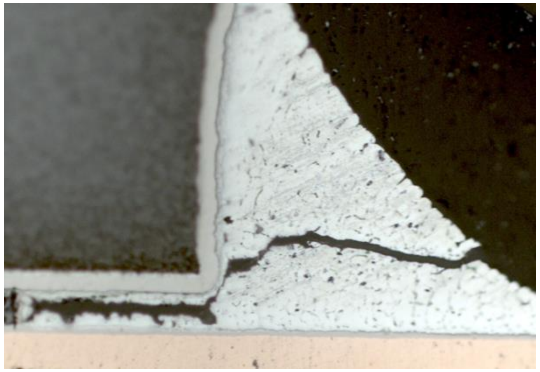
Solder Joint Reliability

- Solder provides the structural and electrical connections between the components and the printed circuit board
- Soldering is a “messy” process, flux outgassing, variations in solder volume, voids, wetting characteristics, grain structure, etc…
- Solder is one of the few structural materials that is required to undergo plastic deformation repeatedly during its lifetime
  - Low temperature process temperatures so as not thermally overstress the components
  - Low yield strength to prevent fracture of components
- Very few structural materials are expected to survive this and be reliable, inelastic deformation is low cycle fatigue

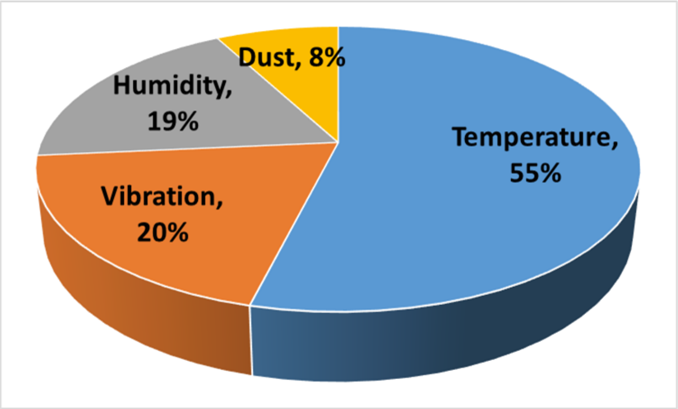


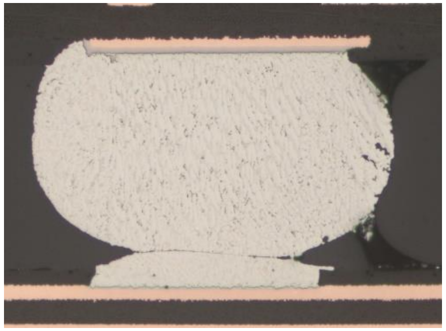


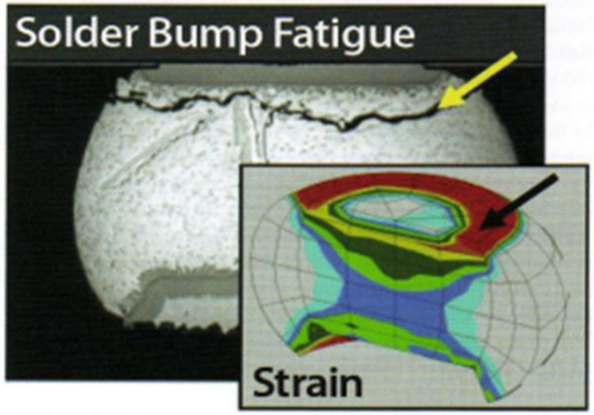
BGA Reliability

- Manufacturing defects and temperature issues are the leading causes of failures for electronics
- Solder fatigue in electronics components is the results of temperature fluctuations or mechanical loads transmitted to the components through the assembly.
- Manufacturing defects – Head in Pillow, de-wetting

Steinberg D.S. Vibration analysis for electronic equipment. John Wiley & Sons, 2000.



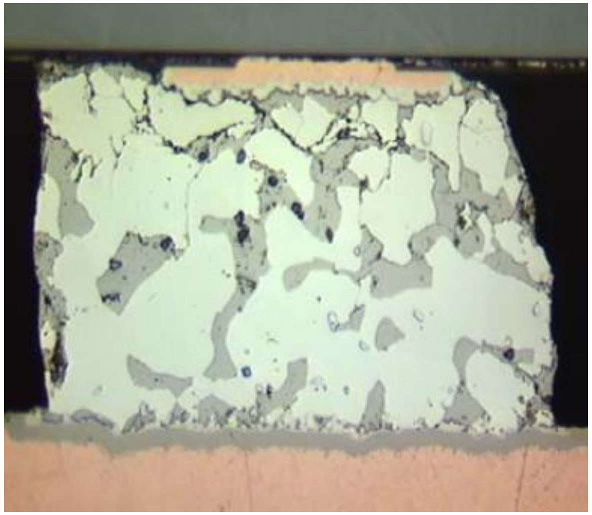


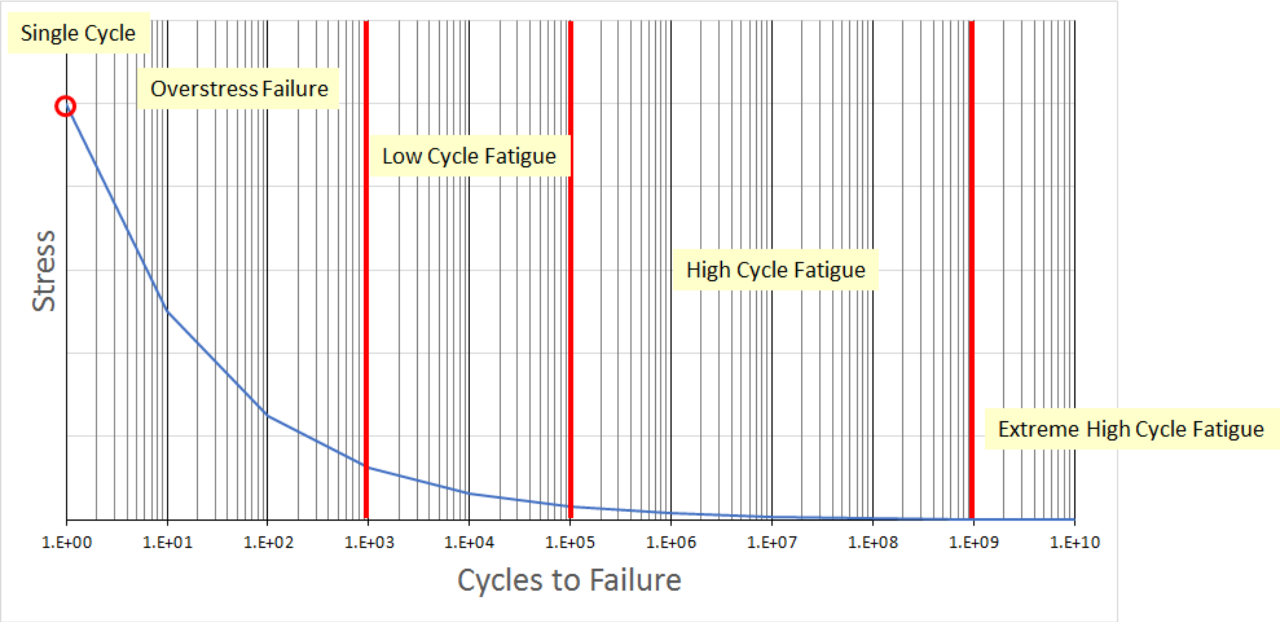


A. MacDiarmid, "Thermal Cycling Failures", RIAC Journal, Jan., 2011.

Solder Joint Reliability

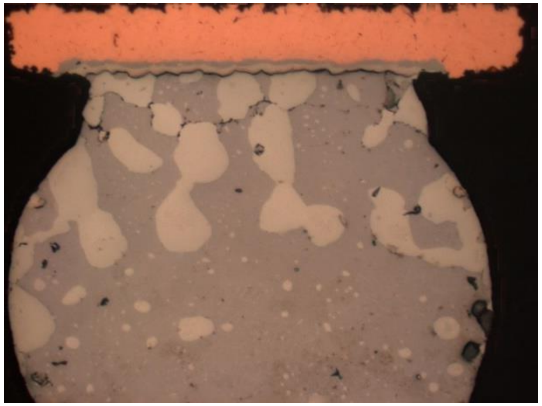
- How do solder joints fail?
- Wearout/Fatigue
  - Thermal cycling
    - Changes in ambient temperature
    - Power cycling
  - Vibration/Cyclic Bending
- Overstress
  - Mechanical shock

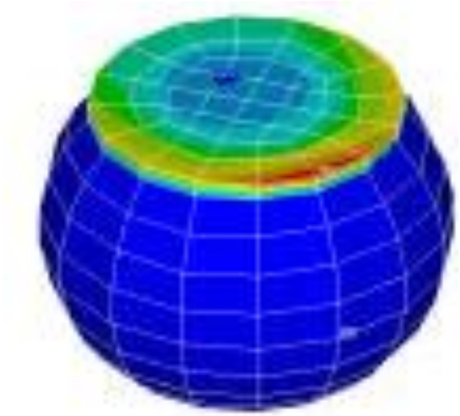




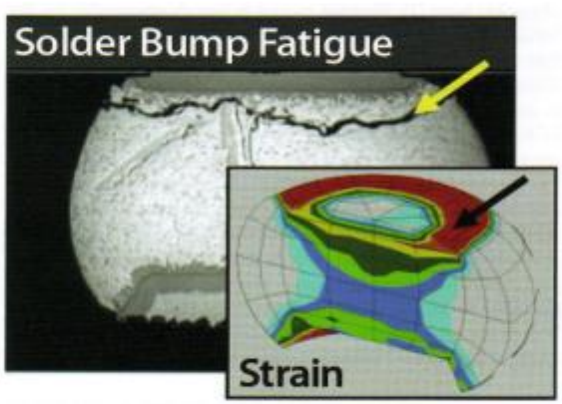
Solder Alloy Reliability – Low Cycle Fatigue

- Most electronic failures are thermo-mechanically related
  - By thermally induced stresses and strains
  - Root cause: excessive differences in coefficient of thermal expansion
  - Leads to low cycle fatigue of the solder joint (wearout)





Source: Syed, Ahmer. "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints." *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No. 04CH37546).* Vol. 1. IEEE, 2004.

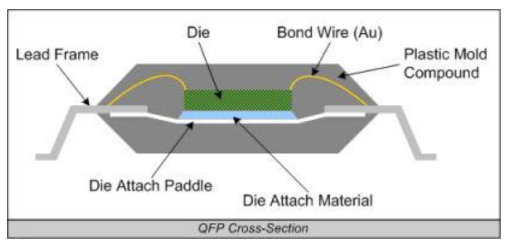


A. MacDiarmid, "Thermal Cycling Failures", RIAC Journal, Jan., 2011.

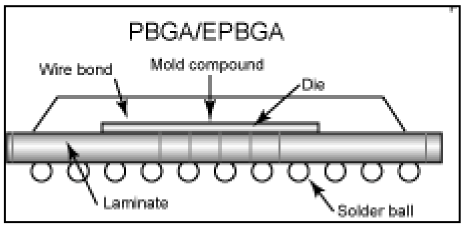
Solder Joint Fatigue

- Elimination of leaded devices to meet the demand for faster and denser electronics
  - Provides lower RC and higher package densities
  - Reduces compliance (stiffer)

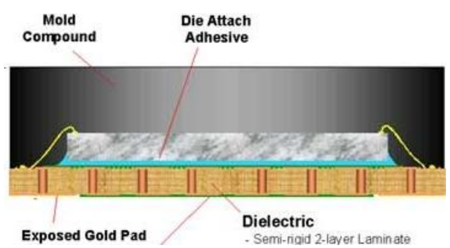
Cycles to failure
-40 to 125C



QFP: >10,000



BGA: 3,000 to 8,000

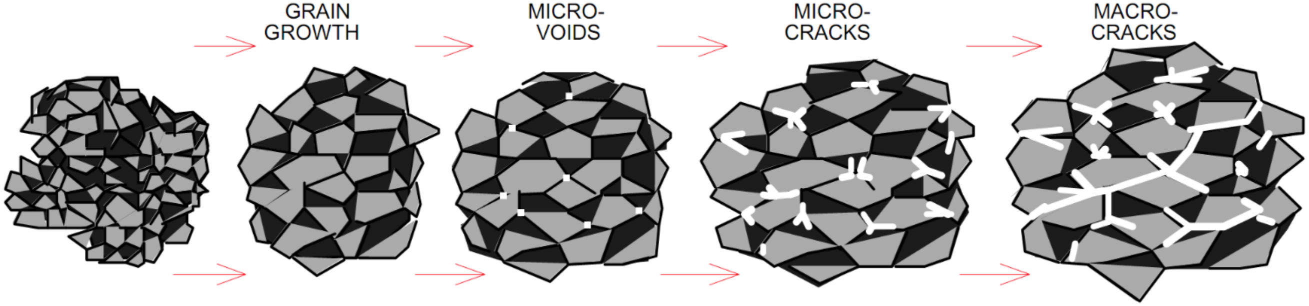


QFN: 1,000 to 3,000

CSP / Flip Chip: <1,000

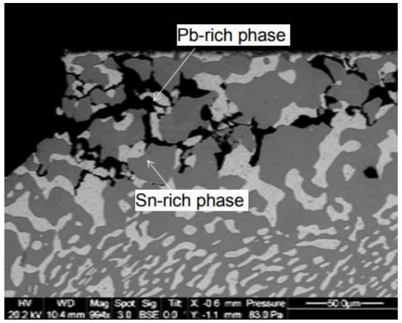
Temperature cycling: The solder fatigue mechanism

- Precursor to cracking, indicates areas of high stress/strain
- Grain growth in solder is an indicator of fatigue (SnPb)



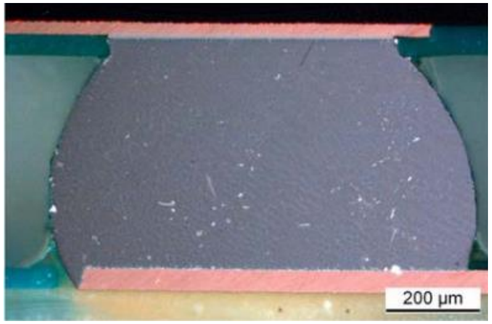
Source: Werner Engelmaier, Engelmaier Associates, L.C.

SnPb Solder

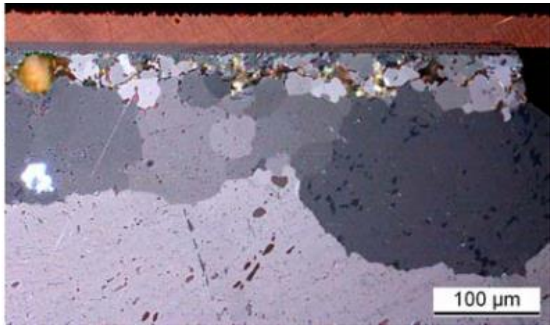


Actually, this is called phase coarsening

- Grain refinement for pb-free



Single grain solder joint (pb-free)



Grain refinement solder joint (pb-free) –thermal cycling

TEMPERATURE CYCLING RELIABILITY OF REBALLED AND REWORKED BALL GRID ARRAY PACKAGES IN SNPB AND SAC ASSEMBLY, Lei Nie, Doctor of Philosophy (Ph.D.), 2010

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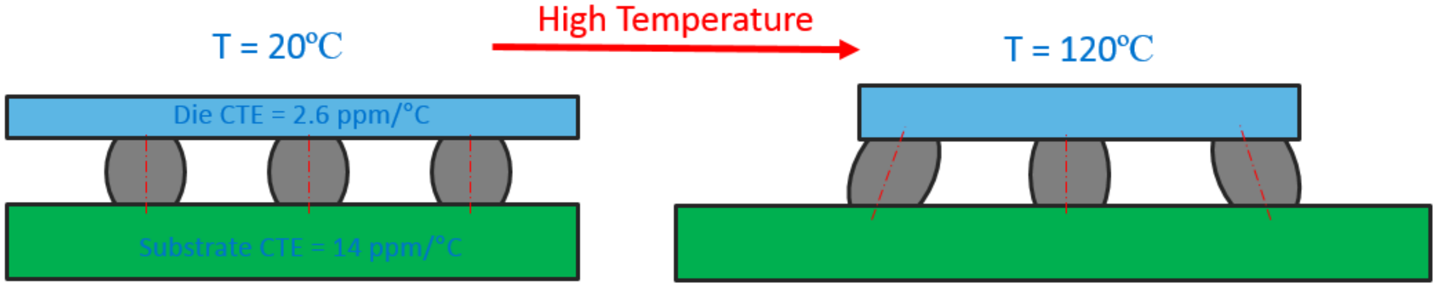
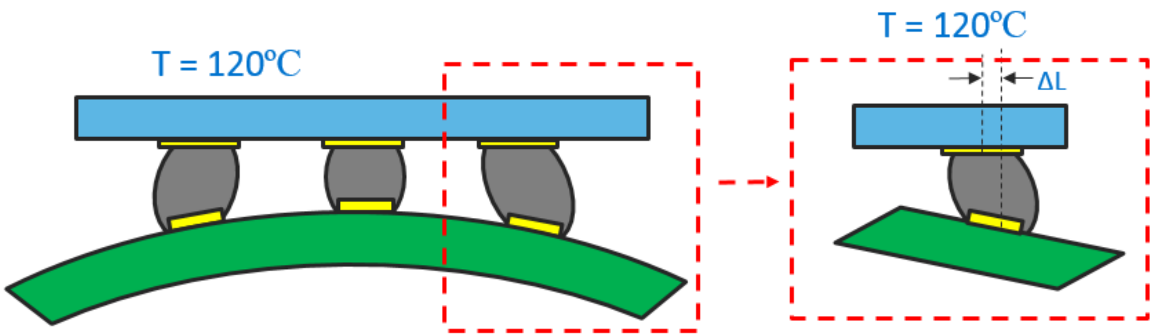
Temperature Cycling: Low Cycle Fatigue

- Idealized CTE mismatch

Shear strain $\gamma = \frac{CL_h \Delta T \Delta\alpha}{h}$



- Realistic CTE mismatch



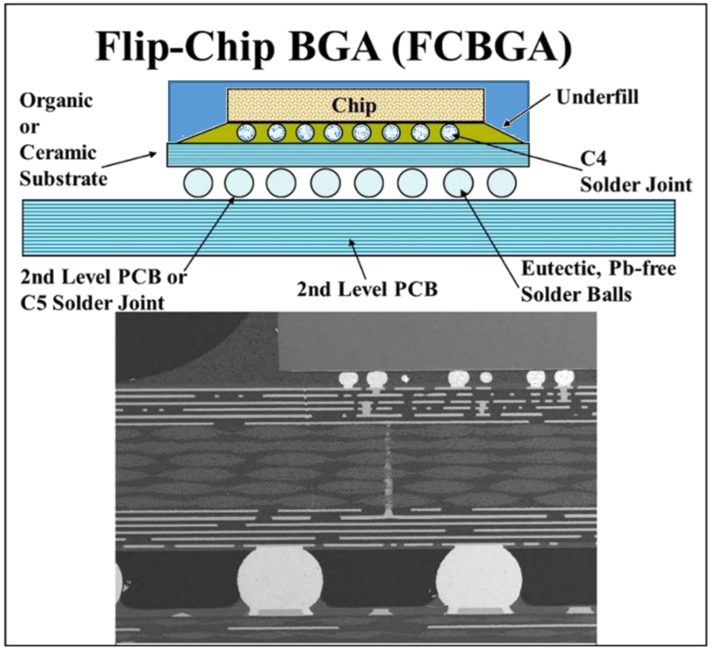
This natural bending actually decreases the stress on the solder

BGA Thermal Cycling

- Factors that impact the thermal cycling performance of a BGA device
  - Size
  - Material properties
  - Construction
  - Solder properties and geometry
  - Printed Circuit Board (PCB) properties/Layout
  - Thermal cycle parameters
- If simulation/prediction doesn't match the test results, it's usually due to a lack of information
  - Manufacturers may not share the information required to make a good model
  - There are internal package structures they use to mitigate solder fatigue of their devices

BGA Thermal Cycling

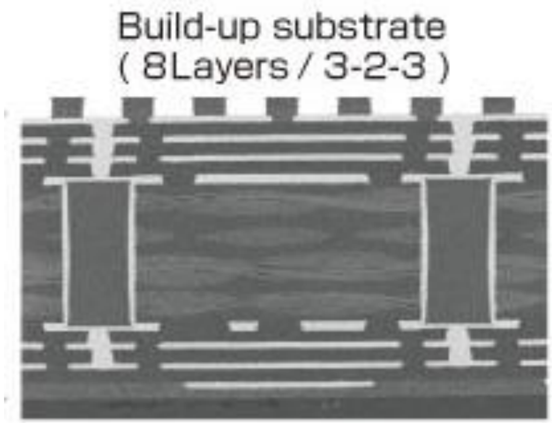
- The usage of flip-chip and buildup layers has improved the thermal cycling fatigue performance of BGA devices
- Die size and package size are no longer primary drivers for fatigue performance
- The ABF/RCC layers isolate the die and decouple the die from the 2nd level solder joints
  - This greatly increases the compliance of the package which increases the fatigue life
  - The core is usually a very low CTE laminate 3-8 ppm/C (Hitachi)

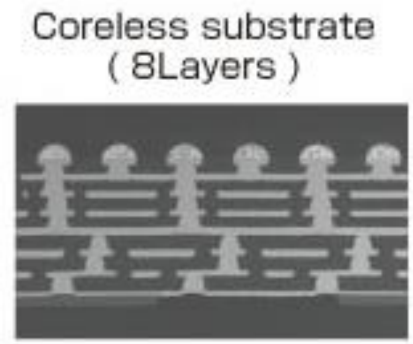


Ghaffarian, Reza. "NASA Guidelines for Ball Grid Array (BGA) and Die-Size BGA (DSBGA) Selection and Application," n.d.

BGA Substrates

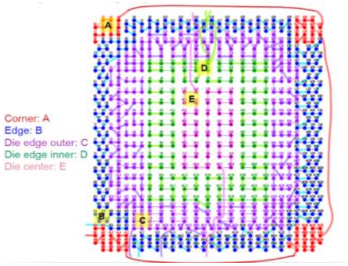
- Standard packages have a laminate core
  - Thickness 200-800µm
  - Various E-glass options
- Coreless packages
  - Only "build-up" layers exist
  - Can be more prone to warpage during assembly
  - Have a higher CTE than standard packages
- In this study:
  - Large BGA package with a large die
  - No failures after 8,000 temperature cycles

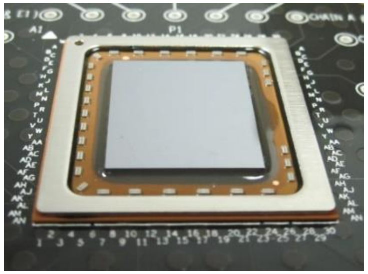


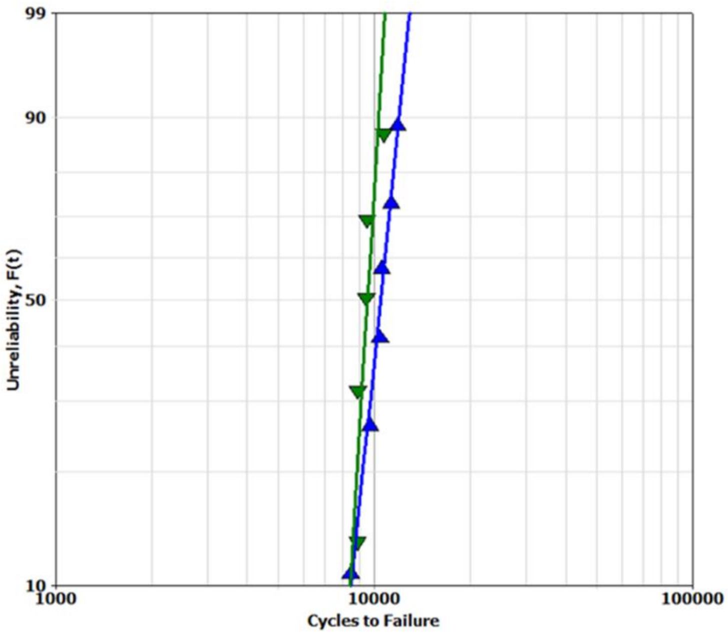


Large Mobile Processor

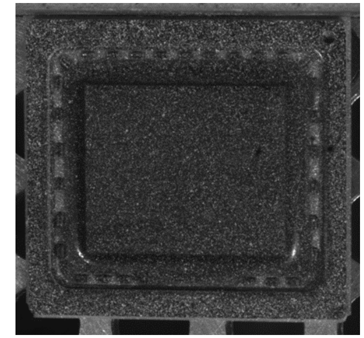
- BGA Package
  - Footprint: 25 by 27 mm, Total thickness: 1.54 mm
  - Silicon die details: 13.8 by 16.5 mm, Thickness: 750µm
  - Stiffener ring: Single piece, Perimeter
- Samples:
  - 6 samples with edge bonding
  - 5 samples with no bonding
- In-situ monitoring of 5 daisy chains
- 8027 Temp Cycles
  - (-40) to 85 °C with 23-minute dwells
  - 17°C/min ramp rates
- Why did it perform so well
- Green: with edge bonding
  - Shape parameter, β = 8.9575
  - Characteristic Life η = 10,924 cycles
- Blue: without edge bonding
  - Shape parameter, β = 15.369
  - Characteristic Life η = 9,777 cycles



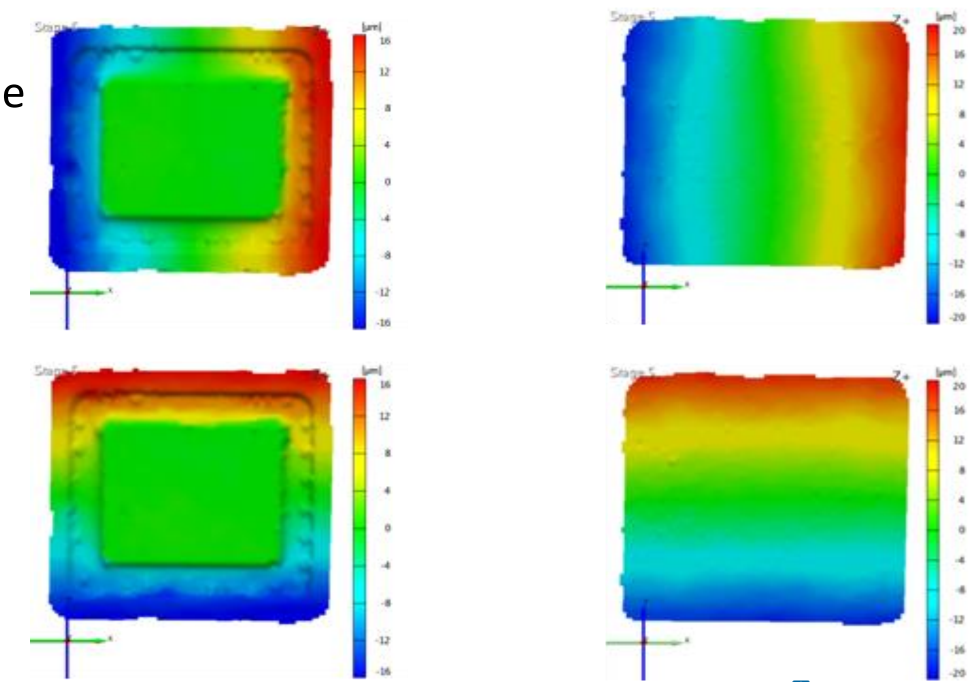




Coefficient of Thermal Expansion



- Top of package, die presence clearly seen
- Relatively uniform displacement on the bottom side
  - Die influence not apparent
  - No die shadow
  - Measured CTE value very close to copper/pcb
- Very low stresses on solder balls during thermal cycling



CTE Results		
Side	X ppm/°C	Y ppm/°C
Top	13.5	15
Bottom	16	17.2

CTE Board Properties

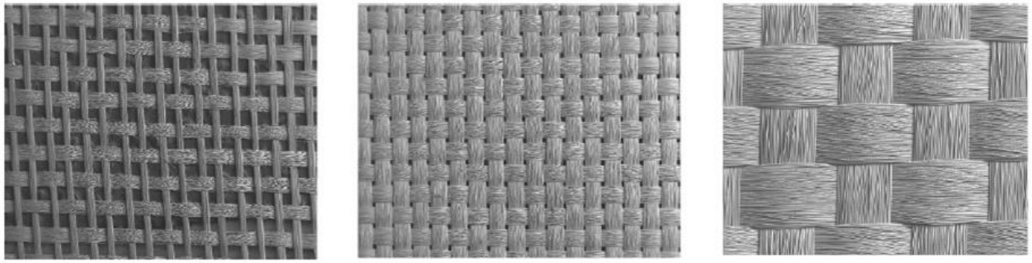
- In the past most electronic packages had CTE values closer to that of copper, 17.6 ppm/°C

- Larger die and smaller packages have driven a reduction in the component CTE, examples:
  - Leadless ceramic chip resistors – 5.6 ppm/°C
  - QFN (quad flat no-leads) – 8 to 12 ppm/°C

- The CTE of the laminates has decreased over the years
  - The PCB laminate manufactures do not make it easy to determine the CTE of their laminate

Effects of PCB glass fabric weave pattern styles

- The woven glass fabric in a PCB provides structural reinforcement and reduces the high in-plane CTE properties of the resin (typically 60-75 ppm/C) to an effective CTE typically between 14-18 ppm/C
  - The lower CTE mismatch between the PCB and it's components results in improved PCBA reliability
- When in-plane CTE is defined in a base laminate data sheet (which many laminate suppliers don't do) it is based on laminated only (no copper) samples fabricated with the high thread count 7628 pattern
  - Allows an advertised low CTE value (to infer that the material can provide a potentially long thermal cycling life)
  - Also indicates a higher elastic modulus (which infers improves vibration and shock endurance)



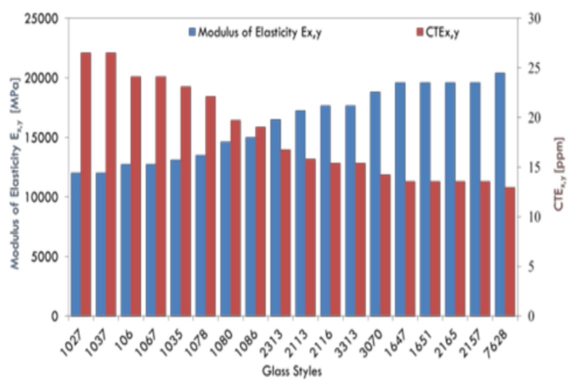
1080 2116 7628

- But production PCBs are not always fabricated with 7628 fabric
  - This is why it is important for high reliability electronics to specify PCB base laminates with both the formulations make(s) & brand name(s) and layer fabric weave styles
  - Even with specifications, bare boards should undergo material characterization testing to verify final CTE, modulus characteristics

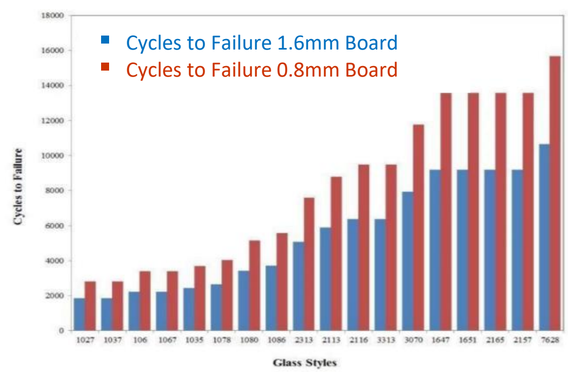
Impact of fabric weave on performance

- Table below shows the resin content for various PCB fabrics pattern styles
- The middle plot shows the tradeoff impact of CTE & Elastic Modulus of the cured insulating layer as the Resin content decreases as fiber content increases
  - Modulus increases improve vibration & shock endurance
- The right plot shows that temperature cycling performance improving as PCB CTE decreases

Glass Style	Resin Content [Weight %]	Resin Content [Vol %]
1027	75%	86%
1037	75%	86%
106	72%	84%
1067	71%	84%
1035	70%	83%
1078	68%	82%
1080	64%	79%
1086	63%	78%
2313	57%	74%
2113	55%	72%
2116	54%	71%
3313	54%	71%
3070	50%	68%
1647	48%	66%
1651	48%	66%
2165	48%	66%
2157	48%	66%
7628	48%	64%



Calculated Elastic Modulus and CTE for the same Laminate with Different Glass Fabric Styles



Fatigue life of a 2512 resistor mounted on a PCB with different glass styles and board thickness

Ref: Sharon, Gilad, & Cheryl Tulkoff.
"Temperature Cycling and Fatigue in Electronics *Acesso em* 10 (2015).

Effect of Glass Style

- Realistic target for board CTE is between 15 and 17 ppm/°C
- Most laminate suppliers provide CTExy values

Property		Typical Value
Glass Transition Temperature (Tg) by DSC, spec minimum		180
Decomposition Temperature (Td) @ 5% wt loss		340
T260 Deg C (TMA)		60
T288 Deg C (TMA)		30
CTE, Z-axis	A. Pre-Tg	45
	B. Post-Tg	230
CTE, X-, Y-axes	A. Pre-Tg	13/14
	B. Post-Tg	14/17

- Key concern, these values are typically for a low resin content laminate (43%-46% resin content by weight, 7628 glass style)
- However, the most popular laminates have much higher resin contents
  - Higher resin content = higher CTE
  - Lower modulus

Molding Compound Properties

- Typically treated as an elastic material for simulation
  - If the glass transition temperature is above the use temperature
  - Some molding compounds may have low Tg
- Molding compounds for packages with large die
  - Low cte materials 7 – 12 ppm/°C
  - Sometime low Tg (in use temperature range), this reduces the stress on the solder joints at high temperature but may make failures occur more rapidly at lower peak temperatures
  - Important to know the glass transition temperature

Material Properties	Unit	Sumitomo G770 series
Spiral Flow	Cm	150.000
Gel Time	sec	36.000
Koka's Viscosity	Pa-s	9.000
CTE-1	$x10^{-5}/C$	0.800
CTE-2	$x10^{-5}/C$	4.000
Tg	C	130.000

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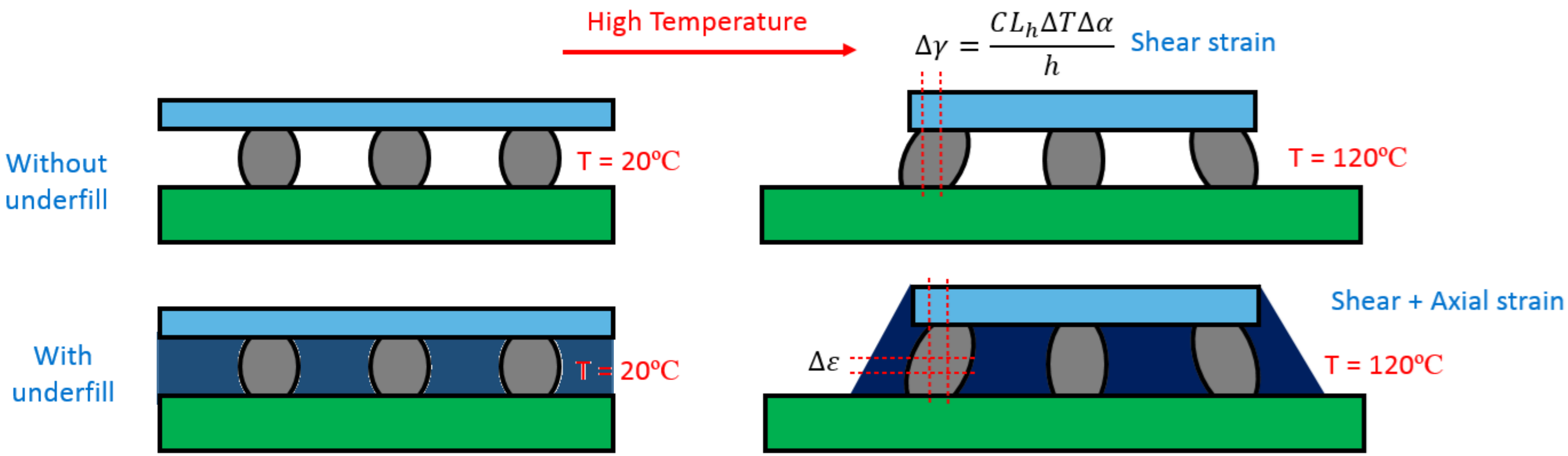
Reliability

- Underfill is increasingly used for PoP and BGAs
  - Improves 2nd level reliability
    - Underfill that is good for drop may greatly reduce reliability under temperature cycling
    - Underfill needs to be formulated for thermal cycling
- Example (-40 to 125C)
  - With underfill: 300 cycles
  - Without underfill: >1000 cycles

Thermomechanical Fatigue: Underfill

- Reduced/increased fatigue life in BGA packages with underfill
- Axial strain and shear strain contribution to thermo-mechanical fatigue life
- How does axial loading contribute to reduction in fatigue life of BGA components



Underfill and Thermal Cycling (cont.)

Underfill name	Dispensing pattern	Filler content (wt%)	Tg by TMA ('C)	CTE, α1 (ppm/'C)	CTE, α2 (ppm/'C)
A	Full	70	113.1	19.9	83
B	Full	0	67.0	61.5	129
C	Corner dot & L	0	123.9	64.7	180
D	Full	0	62.9	69.4	195
E	Full	65	50.3	51.9	181
F	Full	50	60.1	42.8	125
G	Full	0	89.0	58.0	193
H	Full	0	94.4	59.0	195

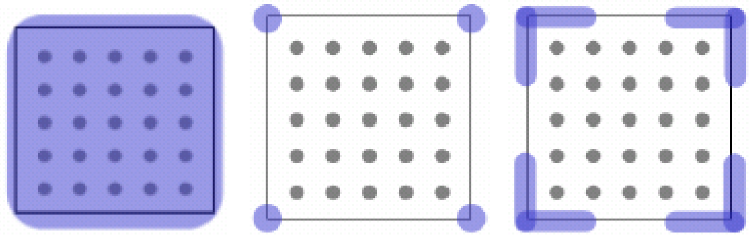
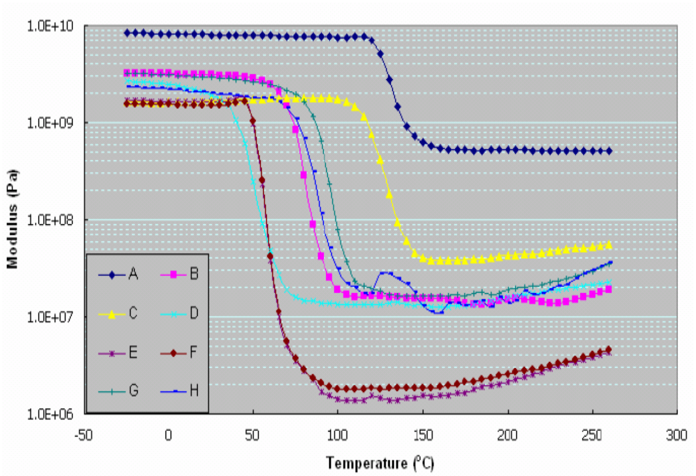
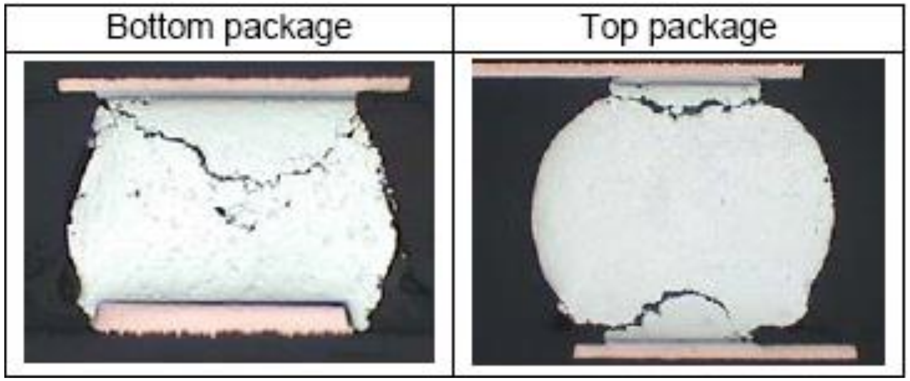


Figure 5. Dispensing pattern; (a) Full filled, (b) Corner Dot , (c) Corner L shape





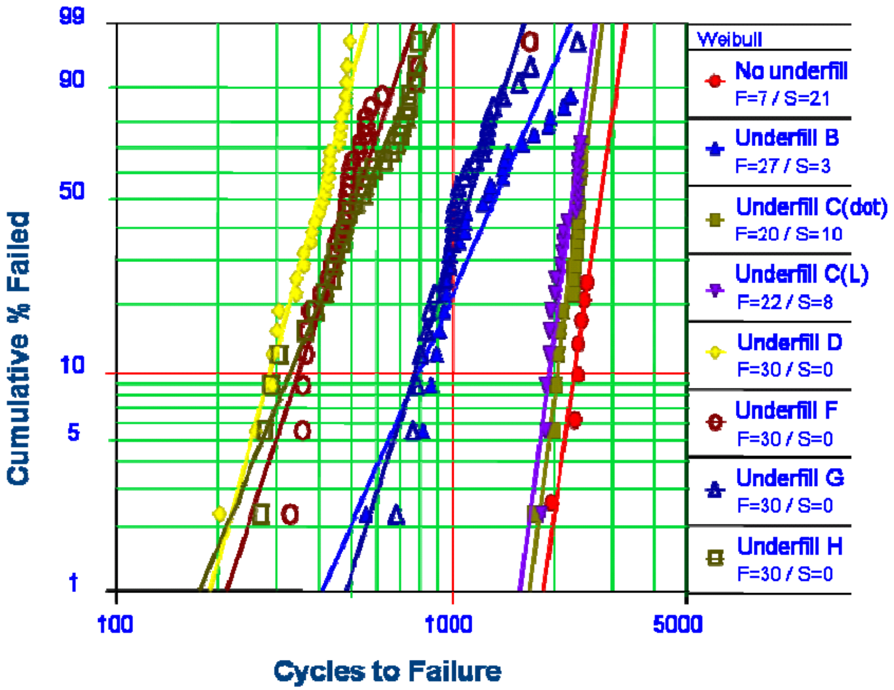
Lee, Joon-Yeob, Tae-Kyung Hwang, Jin-Young Kim, Min Yoo, Eun-Sook Sohn, Ji-Young Chung, and Moody Dreiza. “Study on the Board Level Reliability Test of Package on Package (PoP) with 2nd Level Underfill.” In 2007 Proceedings 57th Electronic Components and Technology Conference, 1905–10, 2007. https://doi.org/10.1109/ECTC.2007.374059.

Underfill and Temperature Cycling

Table 4. Temperature cycling test result summary after 2525 cycles

Underfill name	NBR of failure	1^{st} failure	MTTF	63.2%, η	Slope, β
No underfill	8/28	1968	2727	2858	10.74
A	0/30				
B	27/30	555	1334	1481	3.58
C (dot)	20/30	1738	2369	2470	12.22
C (L)	22/30	1832	2470	2348	11.75
D	30/30	202	394	426	5.67
F	30/30	329	512	560	4.75
G	29/30	681	1110	1209	5.02
H	30/30	270	539	597	3.77

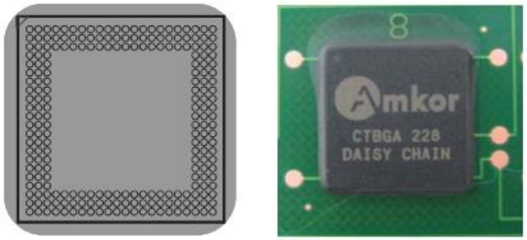
*data was extrapolated from the test results



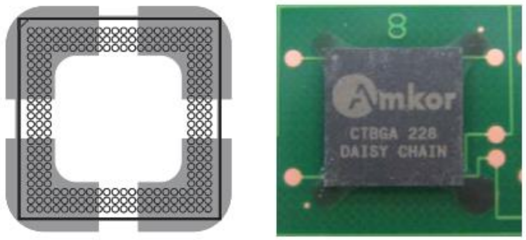
- Rapid time to failure for underfills D / F / G
- Best reliability
  - No underfill or underfill with Tg > 110C

Underfill and Temperature Cycling

- Lower cycles to failure observed for underfill with certain materials properties
- Partial flow underfill - slightly lower fatigue life.
- CSP package – 12x12, 228 I/O, 0.5mm pitch, SAC305 solder, 0.3mm ball diameter, 1 mm thick FR4 PCB.
- -40ºC to 125ºC, 10 min dwell, 15ºC/min ramp thermal cycles



(a) Full underfill



(b) Partial underfill

Underfill	Viscosity at 25°C (mPa.s)	Tg (°C)	CTE (ppm/°C)		Modulus (GPa)	Typical curing performance
			α1	α2		
A	375	69	52	188	3.080	8 minutes at 130°C
B	2000~4500	85	60	200	3.500	5 minutes at 120 °C

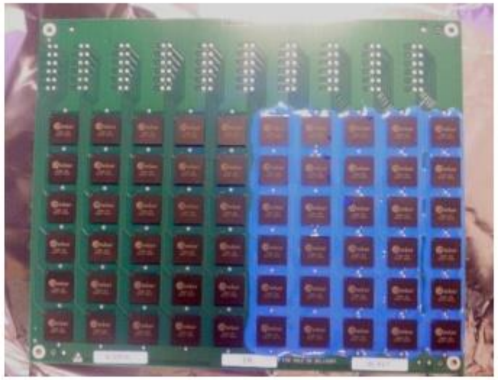
Sample	FCFU-A	FCFU-B	PCFU-A	PCFU-B	Control
α or $N_{63.2\%}$	3206	3640	3406	3932	4268
$N_{50\%}$	2844	3281	3100	3694	4059
$N_{1\%}$	712	988	1046	1796	2272
$N_{First\ failure}$	960	1046	1519	2251	2650
β	3.056	3.527	3.895	5.871	7.296
# Failures /# Samples	41/45	43/45	39/45	37/45	19/45

Shi, Hong-Bin, and Toshitsugu Ueda. "Mitigation of thermal fatigue failure in fully underfilled lead-free array-based package assemblies using partial underfills." *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*. IEEE, 2011.

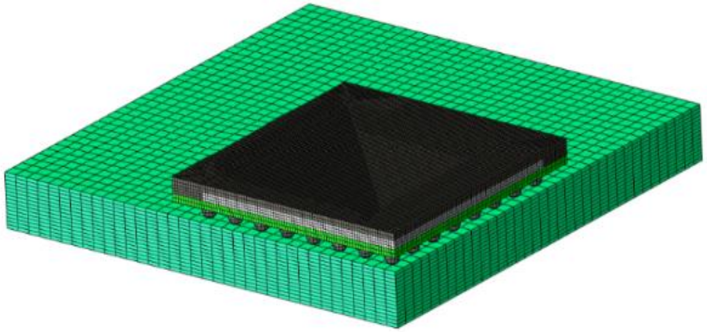
EFFECT OF CONFORMAL COATING ON BGA FATIGUE

- Study effect of improper conformal coating on fatigue life of Pb-free and SnPb BGA packages.
- Applied standard and thick conformal coating using spray and dip application.
- Followed study performed by Rockwell Collins on SnPb.
- Failure resulting in axial dominated damage on solder interconnects due to conformal coating expansion and shrinking during thermal cycling

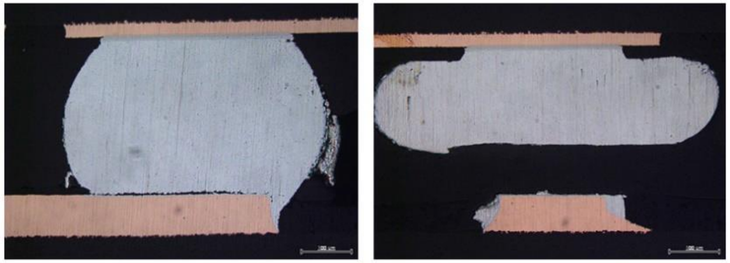
This is why we don't like conformal coating under BGA devices



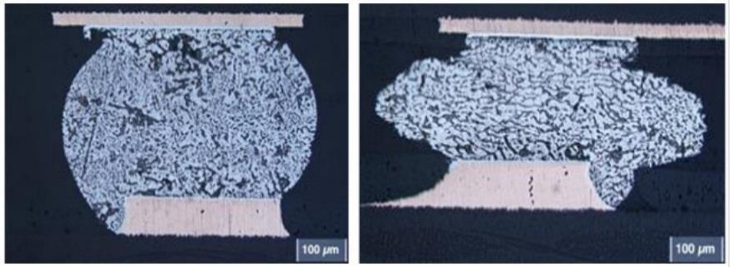
Conformal coated BGA with standard and thick coating



Quarter symmetric FEA model



Pb-free BGA



SnPb BGA

Effect of Improper Conformal Coating

- BGA with SAC305 (Pb-Free) solder joints under temperature profile 2 with thick coating found to have lowest fatigue life
- High β value for the thick coating indicates influence of failure mechanism on transition from wear-out dependent failure
- BGA with SnPb solder joints with standard and thick application of acrylic conformal coating shows greater fatigue resistance compared to the Pb-free components under equivalent test conditions

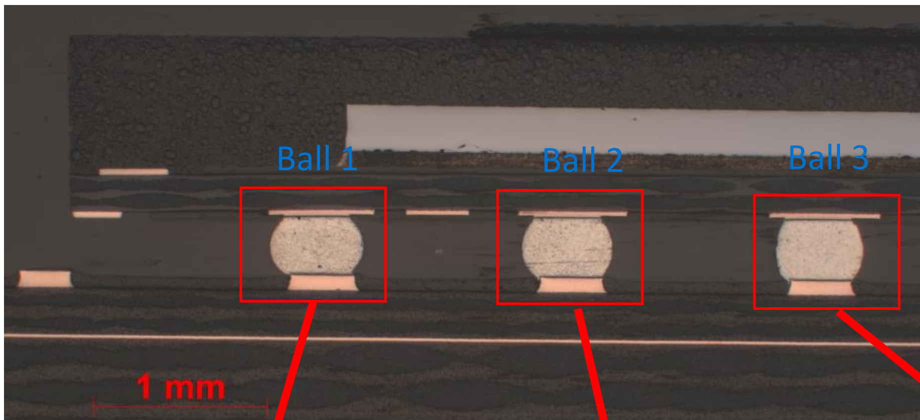
$$F(n) = 1 - \exp\left(-\left(\frac{n}{\theta}\right)^{\beta}\right)$$

2 parameter Weibull fit

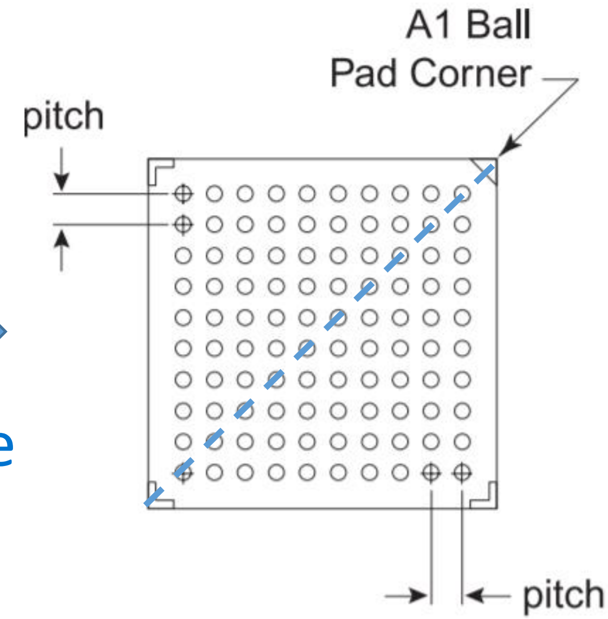
Alloy	Application method	Temp Profile	β	θ	First failure
SAC305	Control	1	7.9	256	173
	Standard	1	5.7	448	245
	Thick	1	16.7	197	171
	Control	2	8.4	2600	1532
	Standard	2	4.2	2054	935
	Thick	2	3.8	191	88
SnPb	Control	1	16.9	631	514
	Standard	1	14.6	567	472
	Thick	1	6.1	573	364
	Control	2	N/A	N/A	N/A
	Standard	2	13.5	1453	1060
	Thick	2	4.8	1554	756

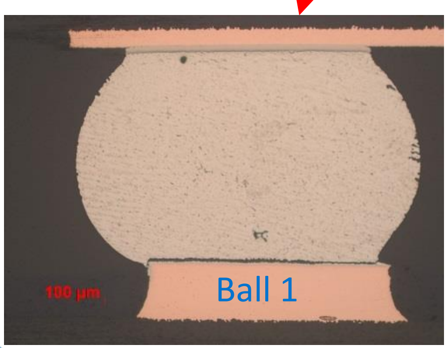
BGA with Silicone Conformal Coating

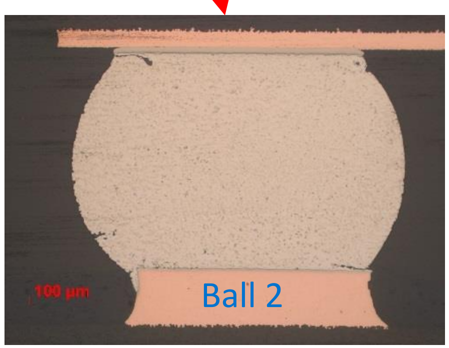
- Even Silicone can cause issues
- -55°C to 125°C for 620 cycles

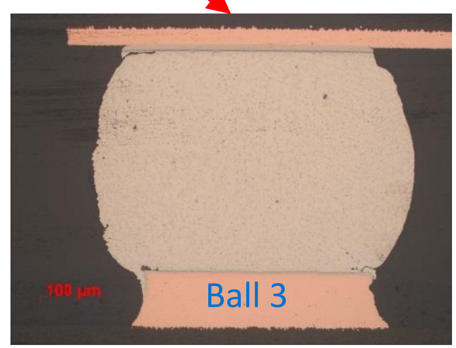


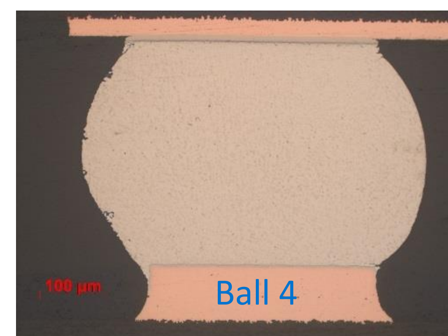
Package Center







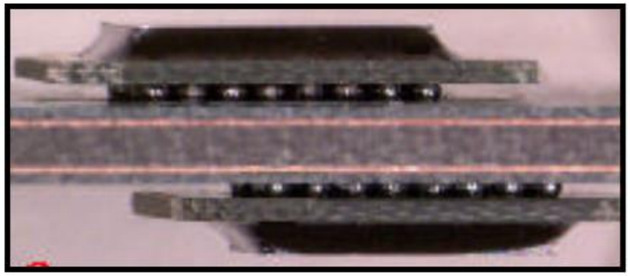




Effect of Mirroring

- Previous researchers have shown the negative effect of double-sided configuration on the thermo-mechanical fatigue life of area array components.
- A 2x to 3x decrease in reliability can occur in mirror image assemblies compared to single sides configurations.

Assembly	Reliability (cycles)	
	Measured	**Predicted**
Single-Sided BGA (20 mil pad)	8,284	8,153
Single-Sided BGA (22 mil pad)	7,897	7,991
Single-Sided BGA (24 mil pad)	7,736	7,814
Mirror Image BGA	1,576	2,890
Single-Sided CSP	7,611	6,140
Mirror Image CSP	3,174	2,300
50% Offset CSP	3,026	3,000



Meifunas, M., et al. "Measurement and prediction of reliability for double-sided area array assemblies." *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*. IEEE, 2003.

Mirroring effects in BGA

Over-constraining of the PCB resulting in reduced package compliance and larger strain transfer to solder joints along with the DNP effect.

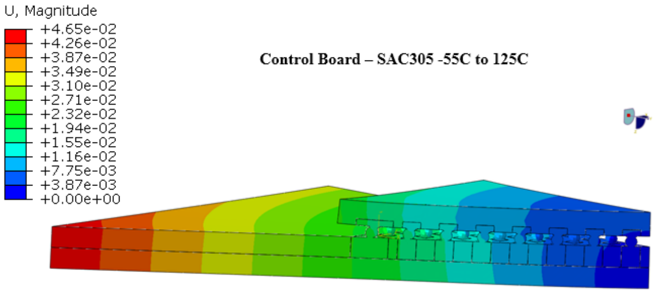


Figure 1. Displacement magnitude of control board at 125C (20x mag).

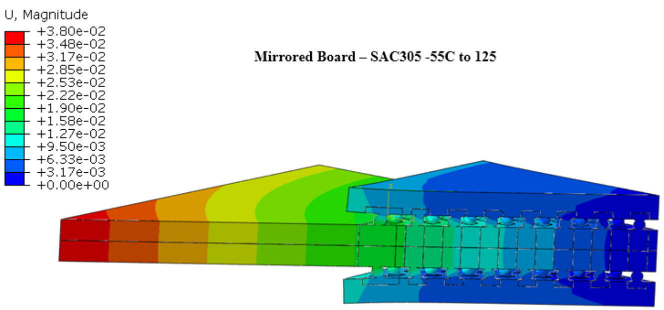


Figure 3. Displacement magnitude of mirrored board at 125C (20x mag).

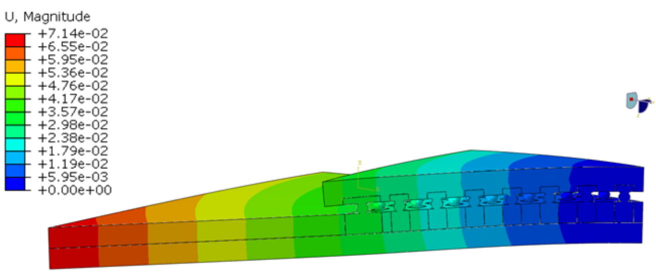


Figure 2. Displacement magnitude of control board at -55 C (20x mag).

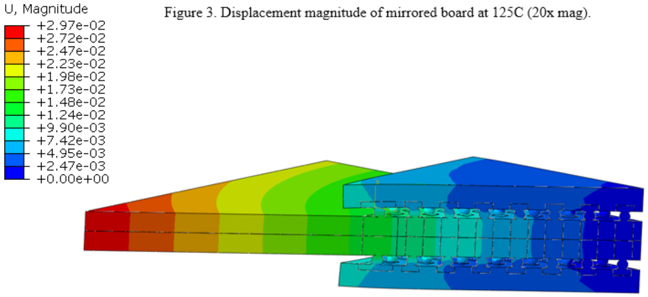
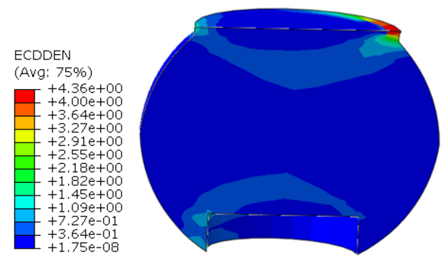


Figure 4. Displacement magnitude of control board at -55C (20x mag).

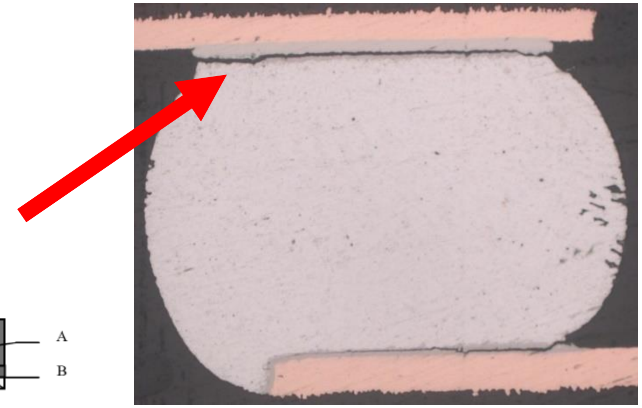
Corners joints in mirrored BGA package show a 25% increase in strain magnitude compared to single sided configuration at the peak of the first high temperature dwell of 125°C.

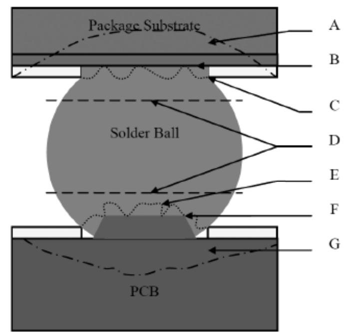
After 3 thermal cycles, peak difference between mirrored and control boards indicate 2x increase in strain energy density. This indicates about a 50% decrease in the life



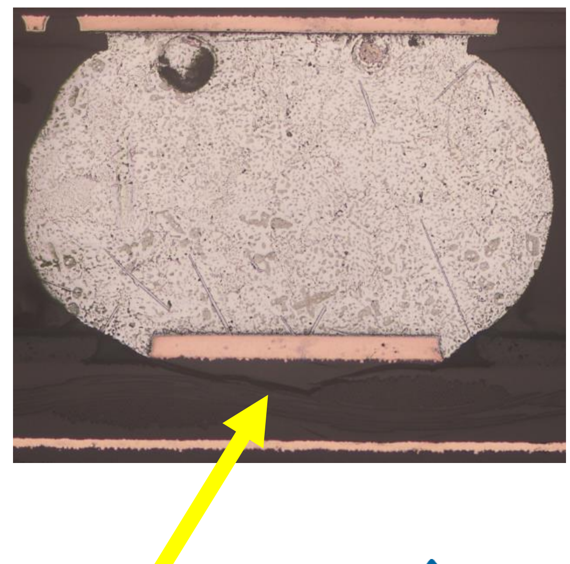
BGA Reliability - Mechanical

- With low profile surface mount components, shock failures are primarily driven by board flexure
  - BGAs don't care about in-plane shock/vibration
- Specific failure modes for shock are
  - Pad cratering (A,G)
  - Intermetallic fracture (B, F)
  - Component cracking
- Vibration tends to be in the bulk of the solder (D)
- Shock tends to be an overstress event (though, not for car doors)
  - Failure distribution is 'random'
- Vibration and Drop/Shock for BGA devices is due to board bending



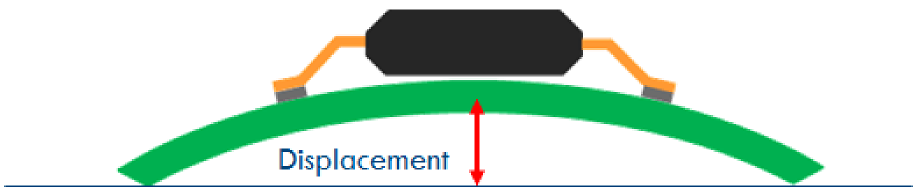


Legend
A Package Pad Lift/Crater
B Pkg Base Metal/IMC Interface Fracture
C Pkg IMC/Solder Interface Fracture
D Bulk Solder Fracture
E PCB IMC/Solder Interface Fracture
F PCB Solder pad/IMC Interface Fracture
G PCB Pad Lift/Crater



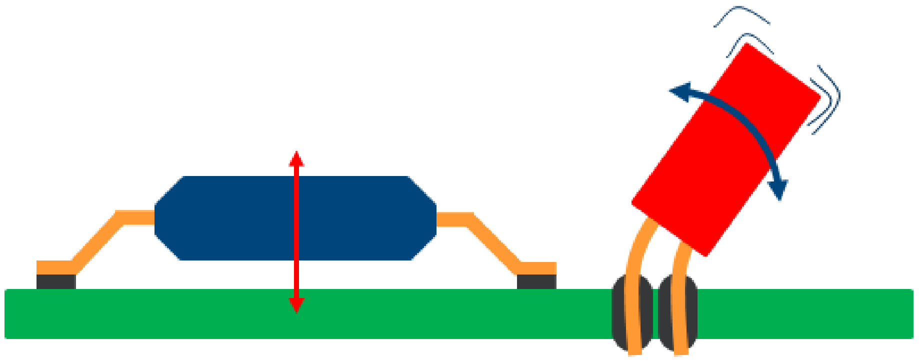
High Cycle Fatigue

- Solder fatigue due to the board bending



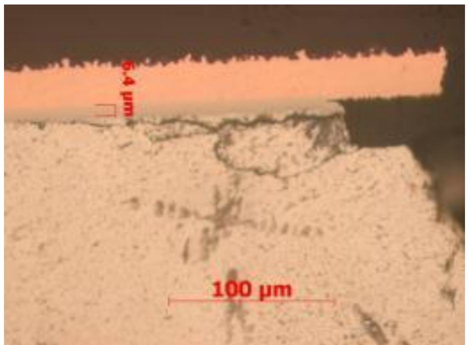
- The displacement causes a strain on the board
  - Fully reversed
  - Damage indicator is surface strain on the board under the component
- Compare the applied strain to maximum allowable strain

- Lead fatigue due to component motion

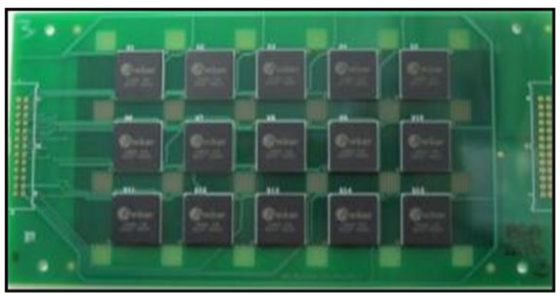


- The motion causes a strain in the lead
  - Damage indicator is VM strain in the lead
- Enter the strain to an S-N curve for the material

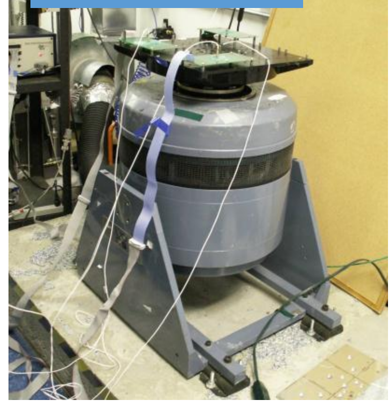
High Cycle Fatigue



Failure site verification



Vibration Table



Event Detector

Temperature & Vibration

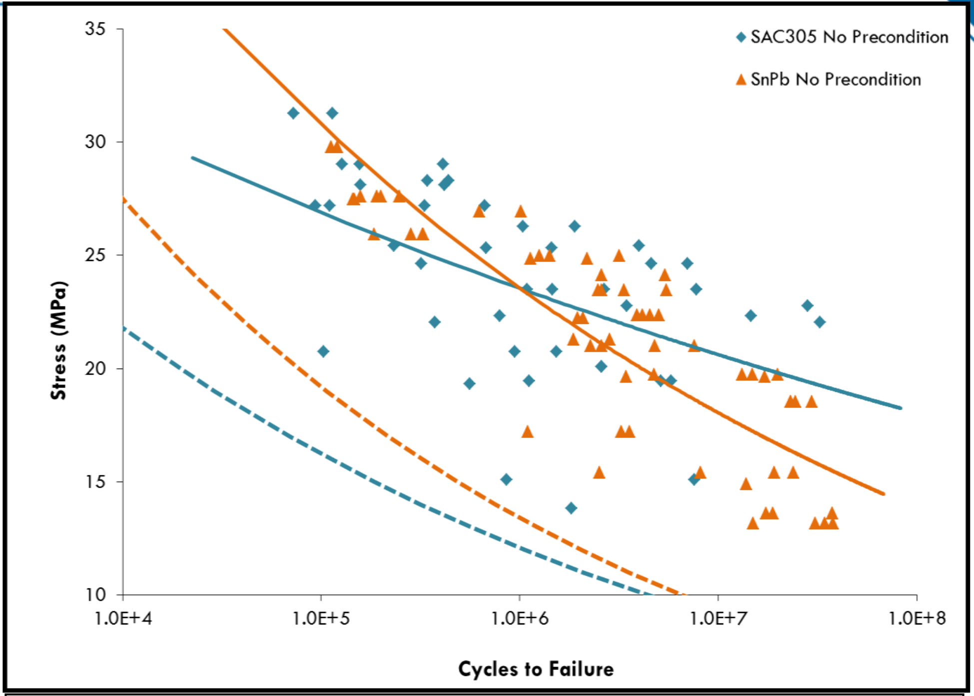
Basquin Equation

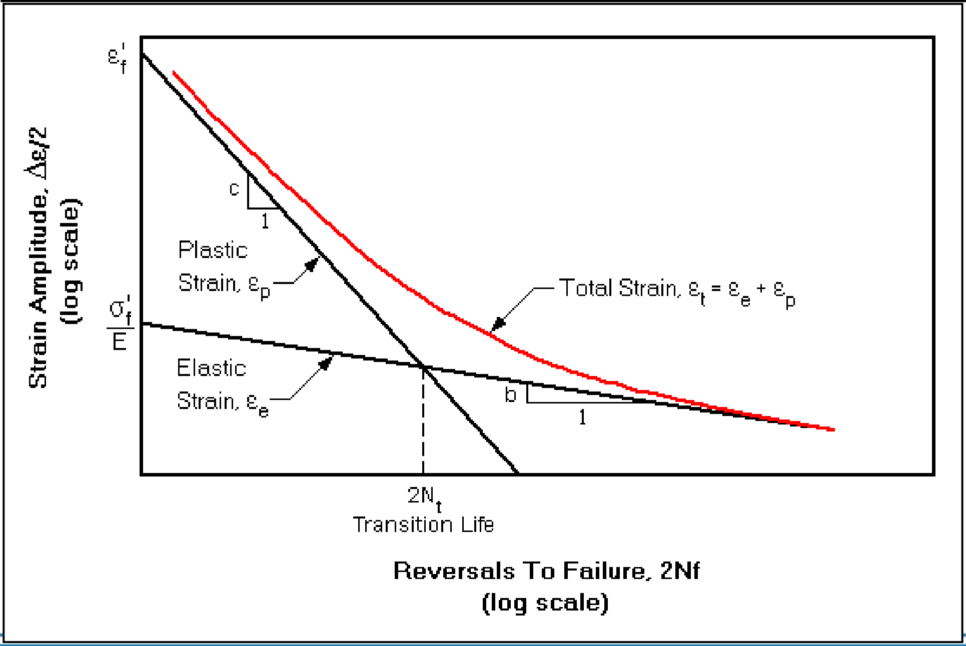
- Elastic fatigue
- Elastic strain or stress
- Very sensitive to geometric and material variations due to high exponent on power law

$$\varepsilon_e = \frac{\sigma_f}{E}\left(2N_f\right)^b$$

-0.05 < b < -0.12; 8 > -1/b > 20

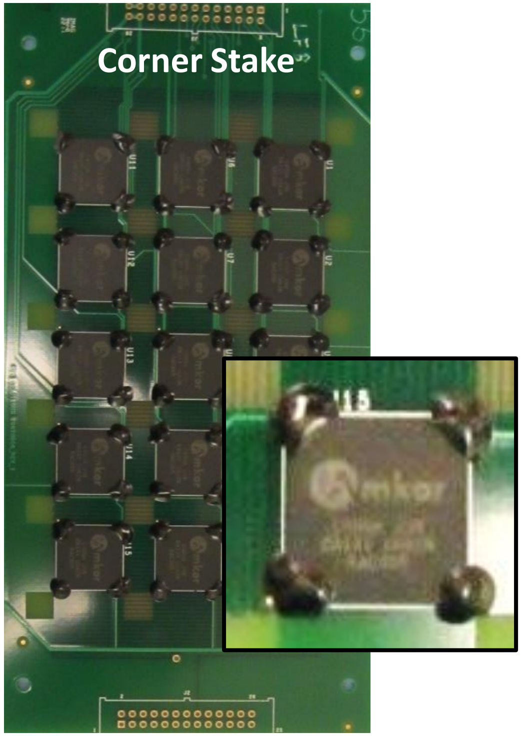
Solder Alloy	SnPb	SAC305
Cycles to Failure	$N_f = \left(\frac{\sigma}{116}\right)^{-6.4}$	$N_f = \left(\frac{\sigma}{71}\right)^{-7.8}$

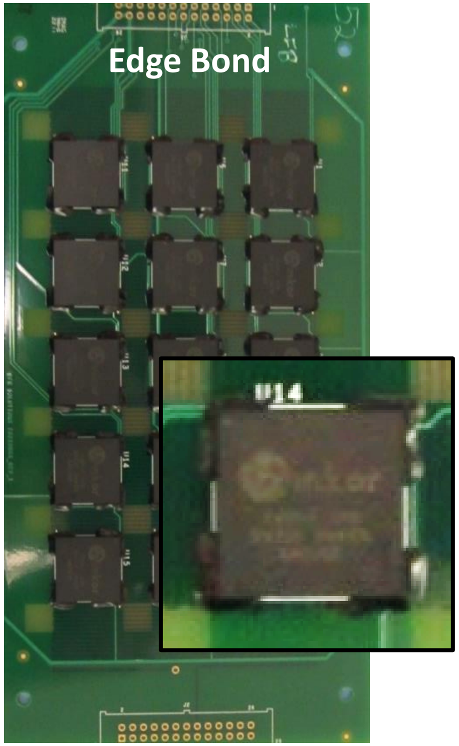


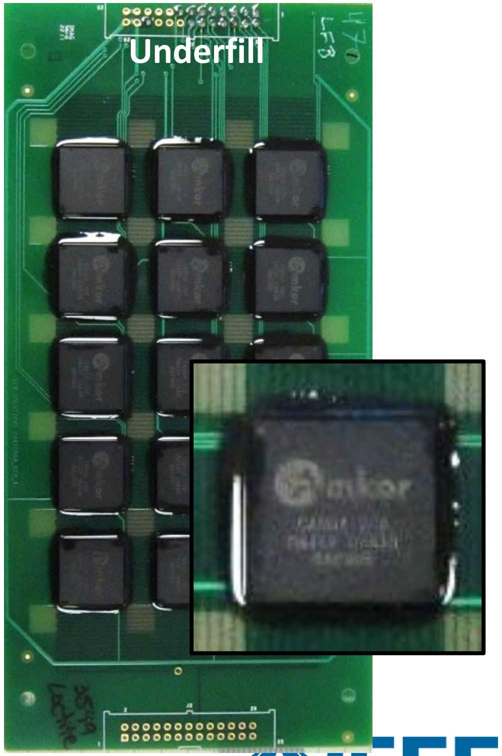


Experimental Design – Mitigation (BGA208)

- Edge bond/Corner Stake: Zymet & Namics
- Underfill: Loctite & Namics

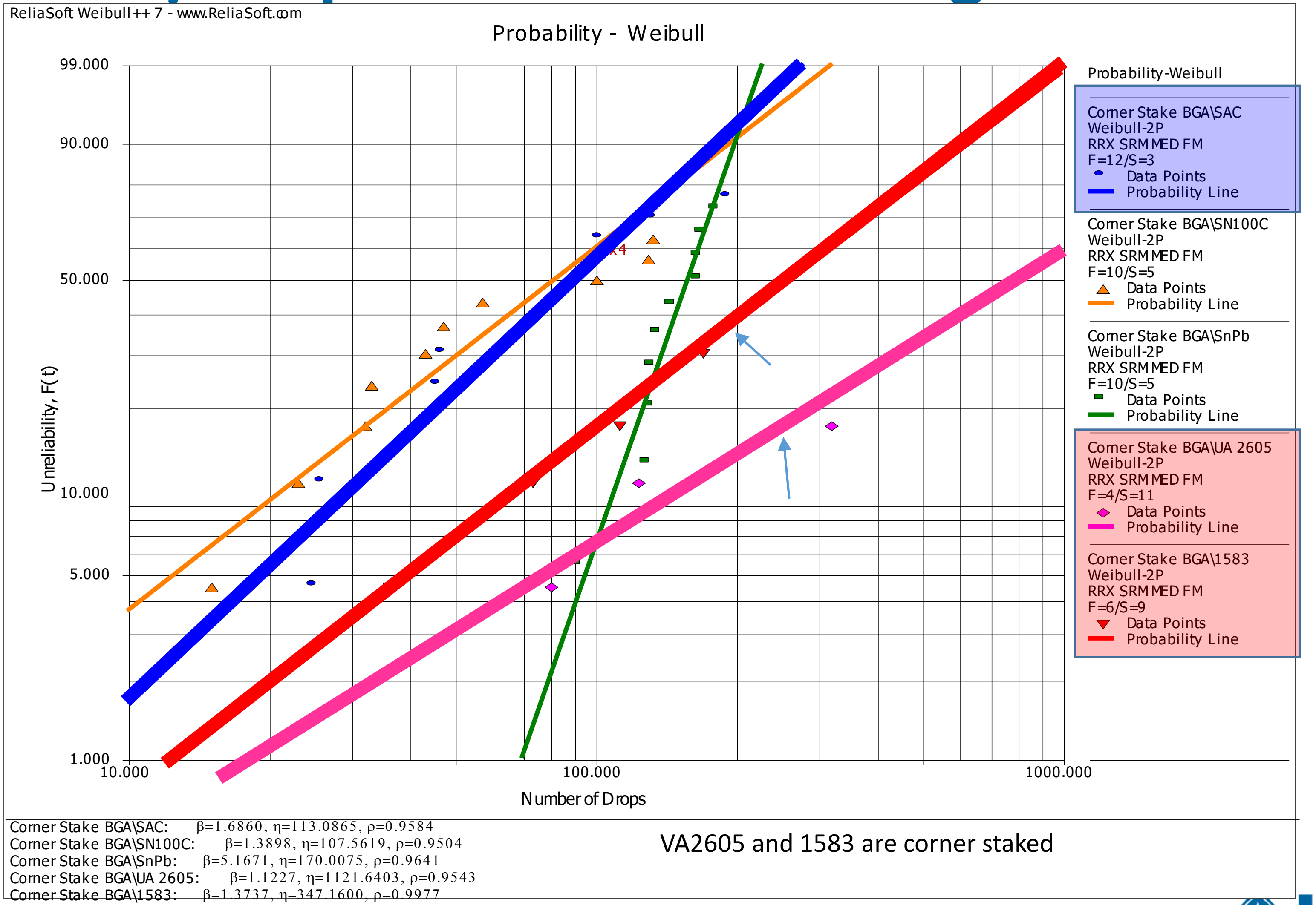






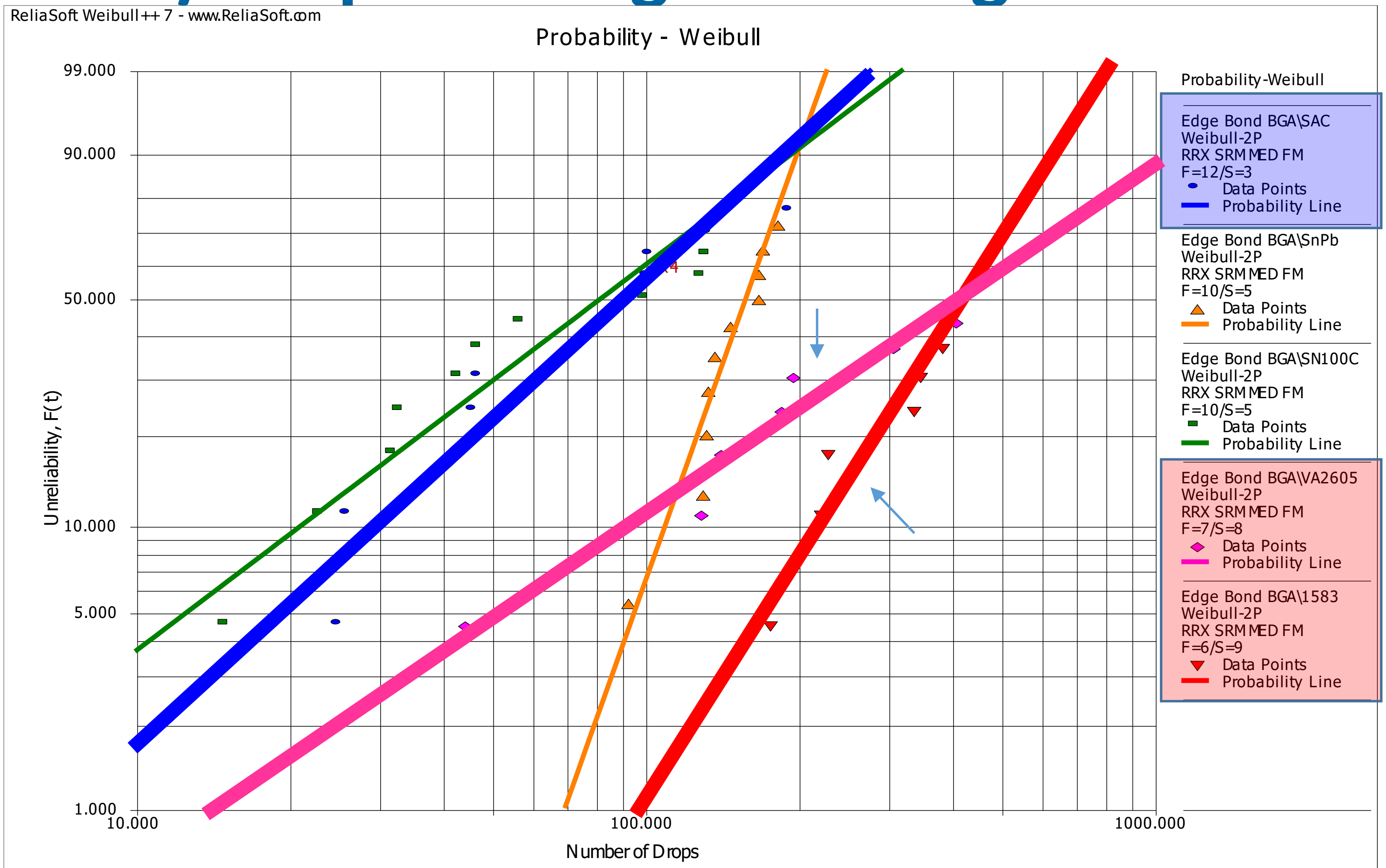
IEEE

Shock/Drop and Corner Staking



VA2605 and 1583 are corner staked

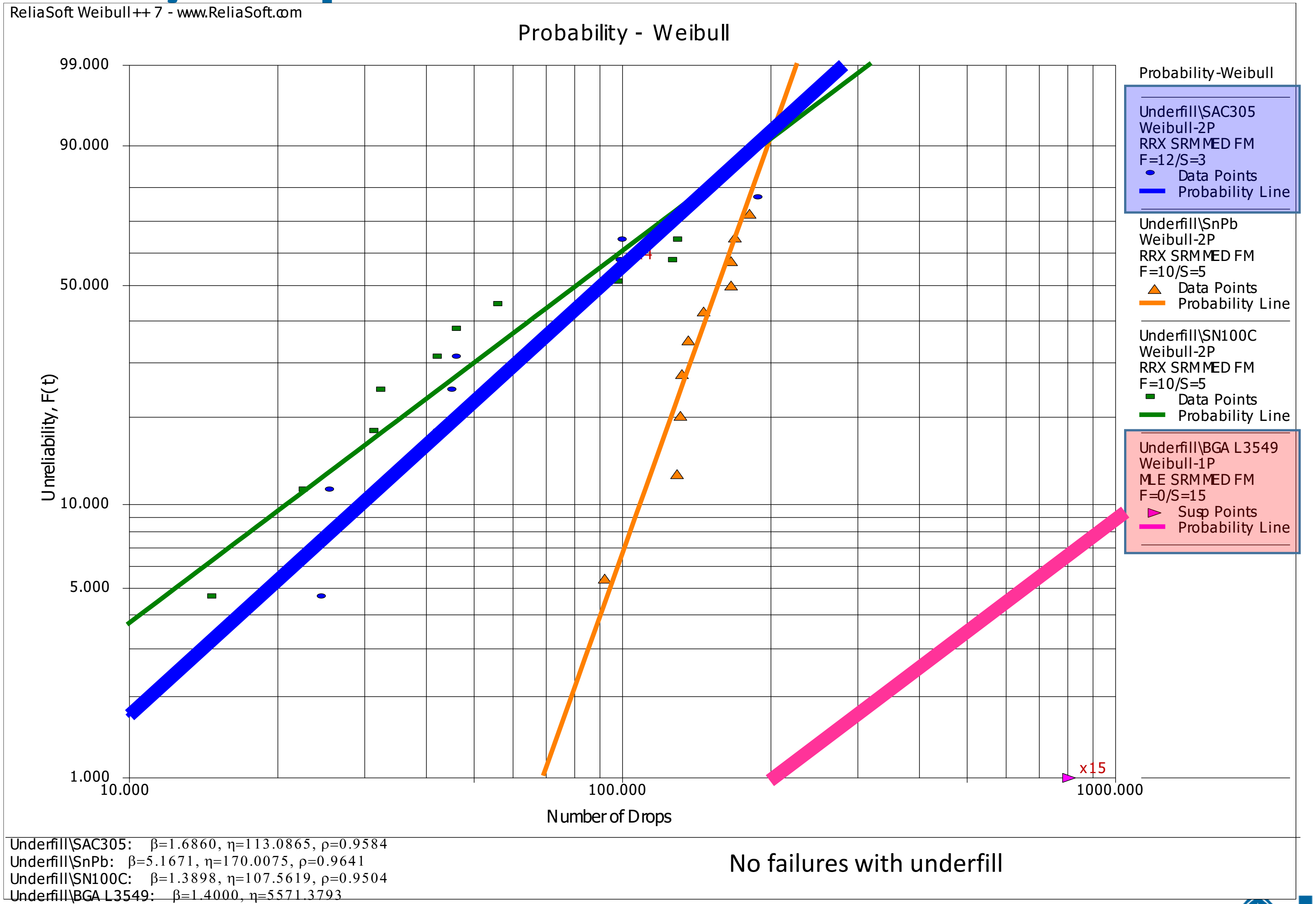
Shock/Drop and Edge Bonding



Edge Bond BGA\SAC: β=1.6860, η=113.0865, ρ=0.9584
Edge Bond BGA\SnPb: β=5.1671, η=170.0075, ρ=0.9641
Edge Bond BGA\SN100C: β=1.3898, η=107.5619, ρ=0.9504
Edge Bond BGA\VA2605: β=1.2613, η=546.9283, ρ=0.9743
Edge Bond BGA\1583: β=2.8533, η=482.6829, ρ=0.9524

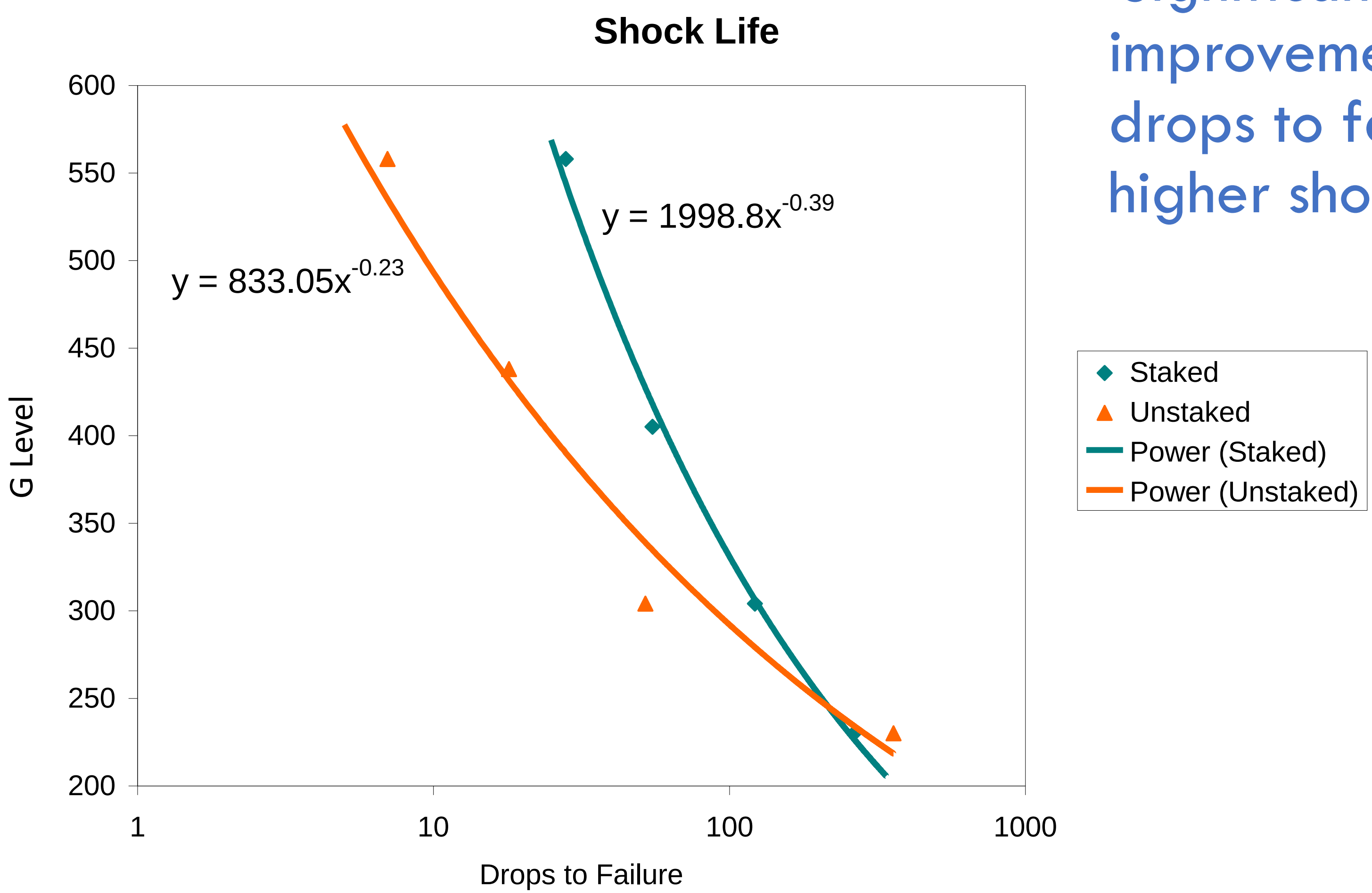
VA2605 and 1583 are the edge bonds the others are not

Shock/Drop and Underfill



No failures with underfill

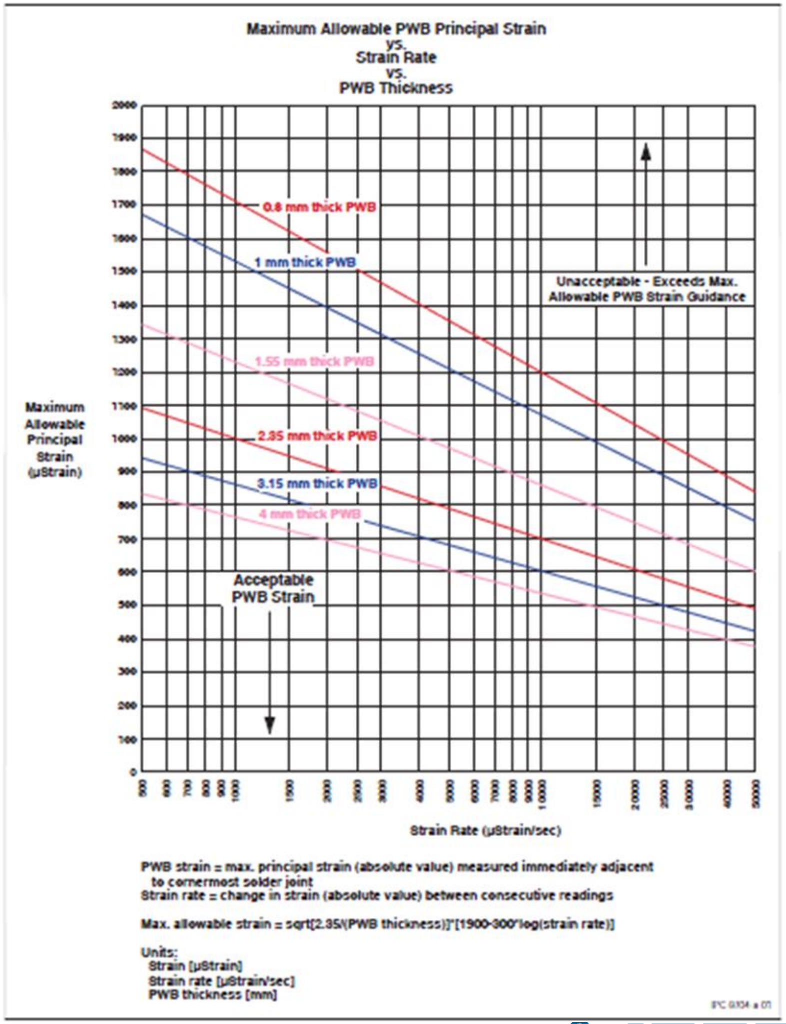
Effect of Staking



- Significant improvement in drops to failure at higher shock loads

Mechanical Stress Vibration/Shock

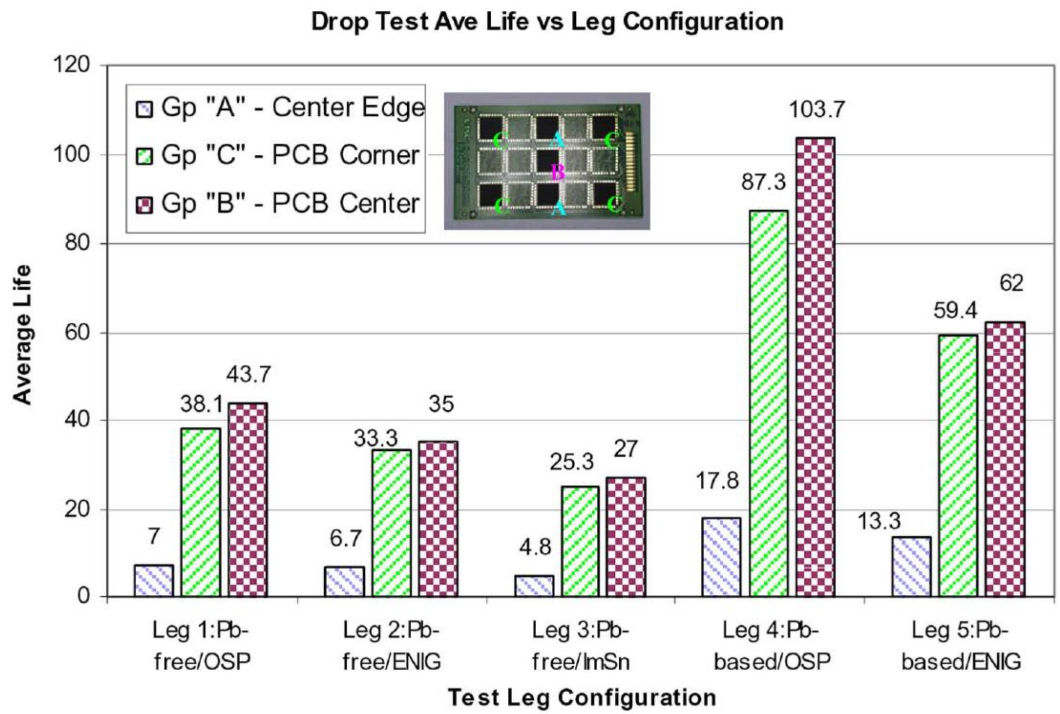
- The goal is to limit board deflection during shock and vibration
  - Make sure the PCB is well supported
  - Simulation can be used to determine the optimal support locations and potential problem areas
  - Pad design can also play a role
    - However, this will mainly be for pad cratering prevention
    - Intermetallic fracture could still occur
  - PCB board finish
    - Surface finishes that form Tin-Copper intermetallics are more robust than the ENIG which has a Tin-Nickel intermetallic
  - Even a little staking can add some robustness to a BGA device but underfill is the most robust



IPC 9704

Board Finish – Mechanical Shock

- OSP which forms a Tin-Copper intermetallic outperforms ENIG which forms a Tin-Nickel intermetallic
- As expected, the more ductile solder SnPb outperforms pb-free
- Immersion silver forms a Tin-Copper intermetallic but isn't performing as expected



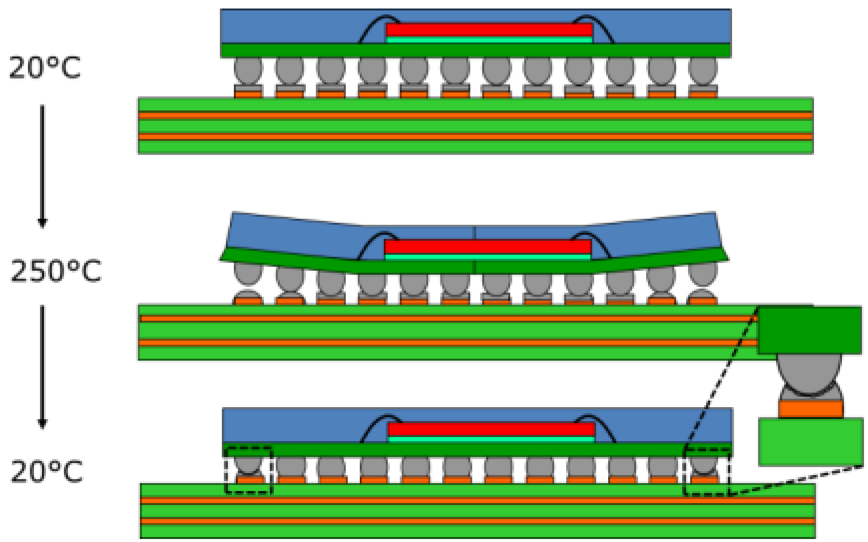
Std Dev (Min / Max)	Leg 1	Leg 2	Leg 3	Leg 4	Leg 5
Gp "A"	3.5 (1 / 12)	4.9 (2 / 15)	1.3 (3 / 7)	3.9 (14 / 24)	3.9 (9 / 17)
Gp "C"	9.1 (20 / 49)	19.7 (5 / 72)	11.4 (15 / 54)	24.9 (42 / 119)	19.5 (36 / 85)
Gp "B"	13.7 (28 / 53)	5.7 (31 / 39)	10.4 (21 / 39)	24.4 (84 / 131)	25.1 (33 / 77)

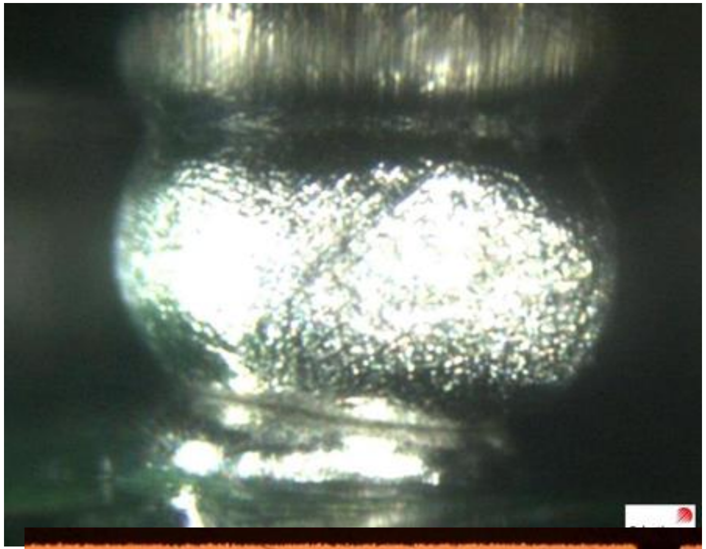
Chong, Desmond, F.X. Che, John Pang, Luhua Xu, B.S. Xiong, H.J. Toh, and B.K. Lim. "Evaluation on Influencing Factors of Board-Level Drop Reliability for Chip Scale Packages (Fine-Pitch Ball Grid Array)." Advanced Packaging, IEEE Transactions On 31 (March 1, 2008): 66–75. https://doi.org/10.1109/TADVP.2007.908024.

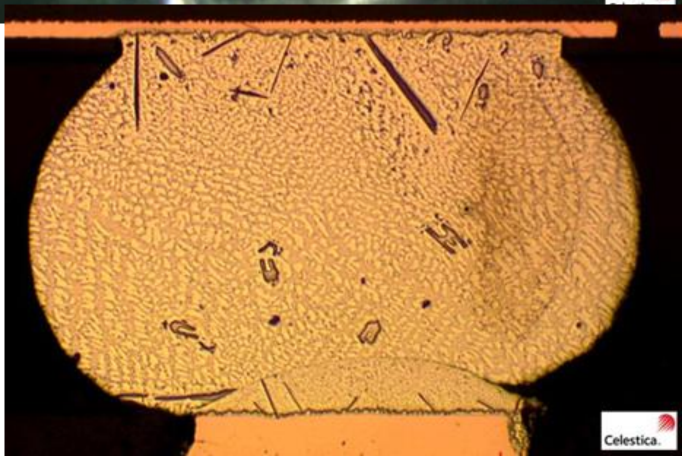
Some Manufacturing Challenges

Head in Pillow

- Two main causes
  - Component warpage
  - Incorrect reflow profile or flux problems
- Solder paste reflows but doesn't mix with the solder ball
- Can be hard to distinguish between the two when trying to solve the problem





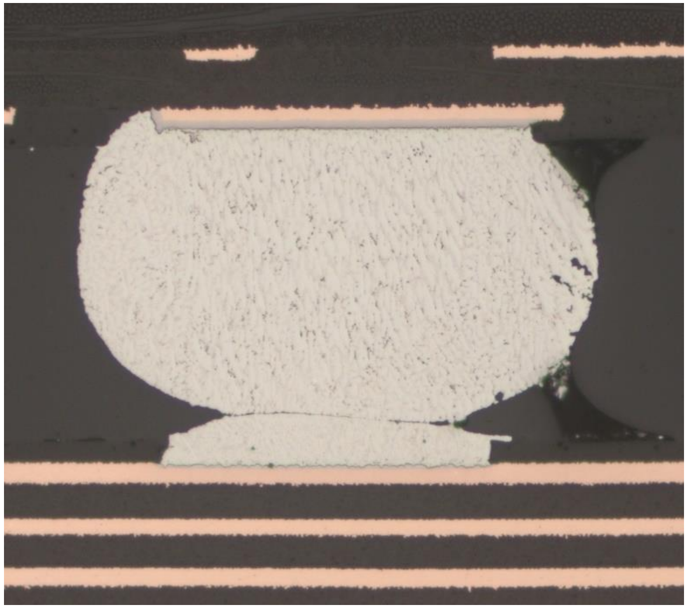


Parts Standardization & Management Committee (PSMC) Spring Conference
McLean, VA
April 20-22, 2010

Vandevelde, Bart, Geert Willems, and Bart Allaert. "Hidden Head-In-Pillow Soldering Failures." In 2014 15th International Conference on Thermal, Mechanical and Mulit-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 1–6. Belgium: IEEE, 2014

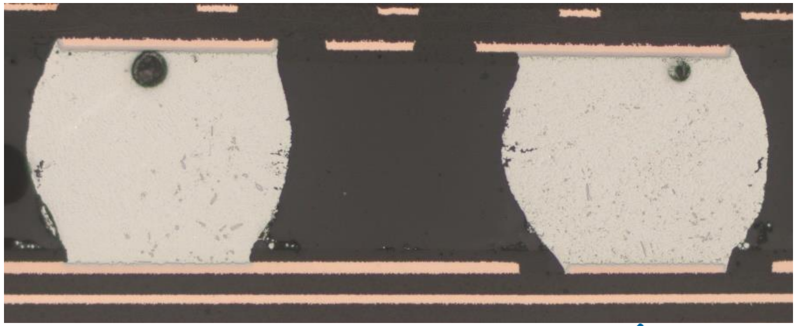
IEEE

Component Warpage



- During reflow the substrate of the BGA will expand more than the die and overmold portion causing the corners to bend upward
- This can lift the solder ball high enough that it isn't in contact with the solder paste during reflow
- One good indicator is the presence of solder joints that appear stretched and other that appear compressed
- Possible causes
  - Reflow profile
  - Moisture in the package

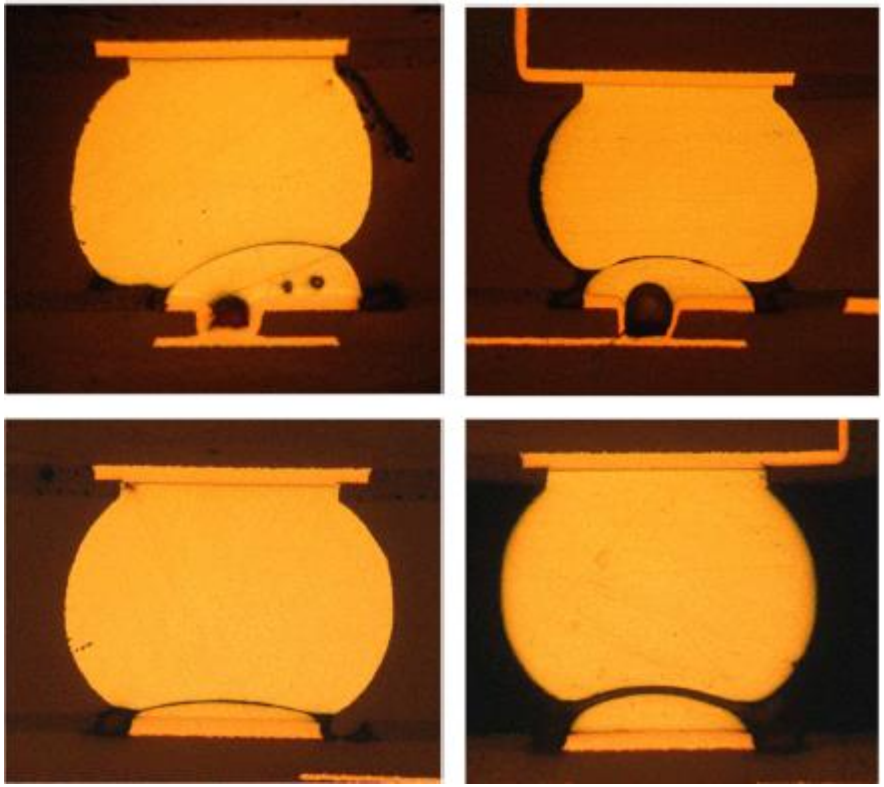
Package Center



Package Corner

Solder Wetting

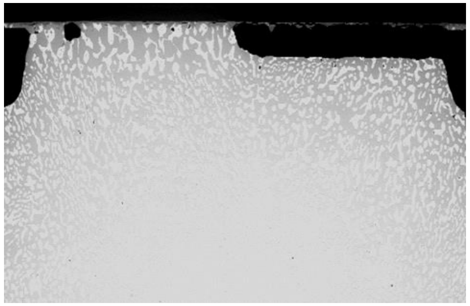
- Usually due to oxidation of the solder ball
- Component wasn't stored properly, and oxide layer formed that was too thick for the flux to remove
- Flux activation issue due to reflow profile or flux age
  - Flux contains acids which are used to breakdown the oxide layer on the solder ball
  - During reflow the flux removes the oxides
  - If the reflow profile is incorrect the flux can be consumed to quickly before breaking down the oxides
  - If the flux is activated for too long, it can actually oxidize the surface of the solder ball causing a wetting issue

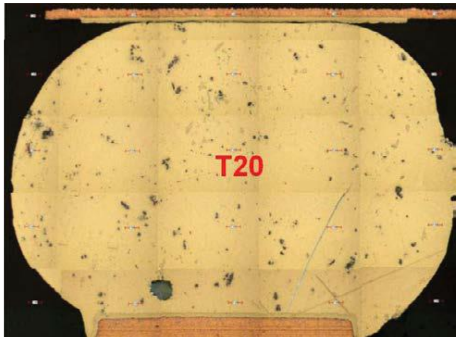


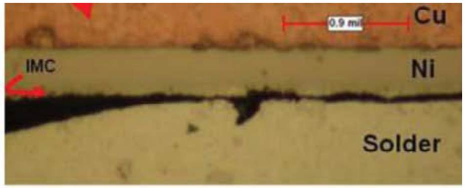
Arazna, Aneta, Grazyna Koziol, Wojciech Steplewski, and Krzysztof Lipiec. "Head on Pillow Defects in BGAs Solder Joints." In 3rd Electronics System Integration Technology Conference ESTC, 1–4, 2010. https://doi.org/10.1109/ESTC.2010.5642849.

Dewetting

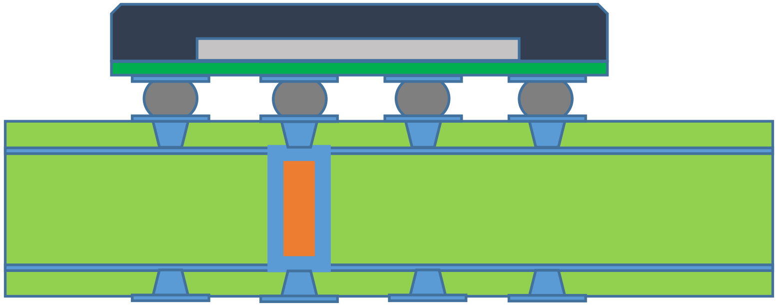
- Can be caused by component warpage or PCB expansion due to buried vias
- This can lead to Head in Pillow or actual solder separation (usually during secondary side reflow operations)
- The buried via also conducts more heat to the solder joint which may cause it to partially melt and separate

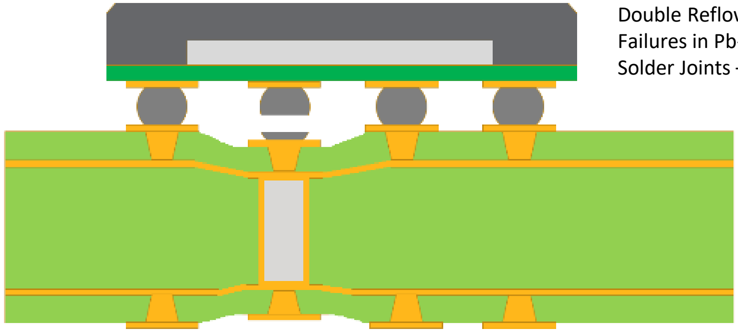






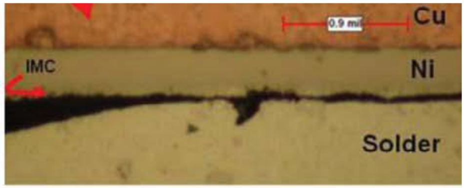
Double Reflow-Induced Brittle Interfacial Failures in Pb-free Ball Grid Array Solder Joints –Julie Silk et. al , IPC Apex

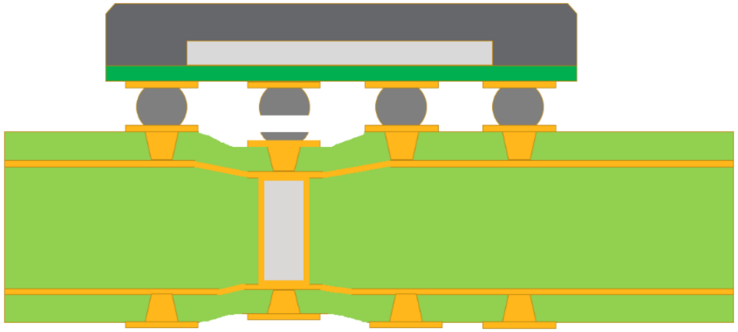


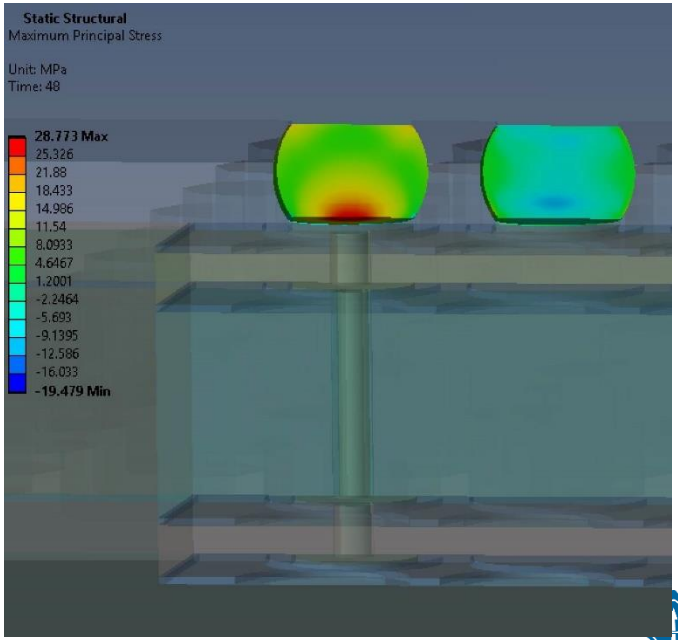


Reinforcement: Case Study

- Supplier experienced solder separation
  - PCB expanded non-uniformly due to buried via, which acts like a rivet
- This mechanism could only simulated using a trace reinforcement technique

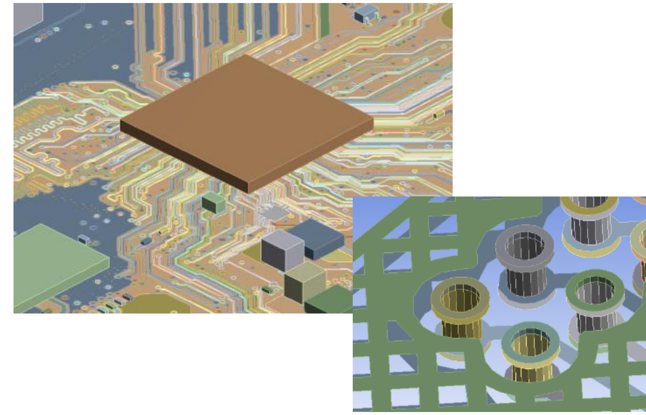




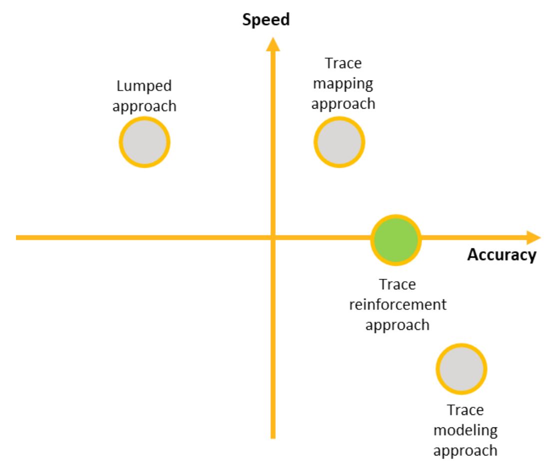


Simulations - Reinforcements

- Helps model electronics <u>more accurately</u>
  - Captures all geometry (metal, trace, plane, pad, via, microvia)
  - Can be used to model chip, substrate, and PCB layout
  - Easily repeatable for any design change, reduces model build time



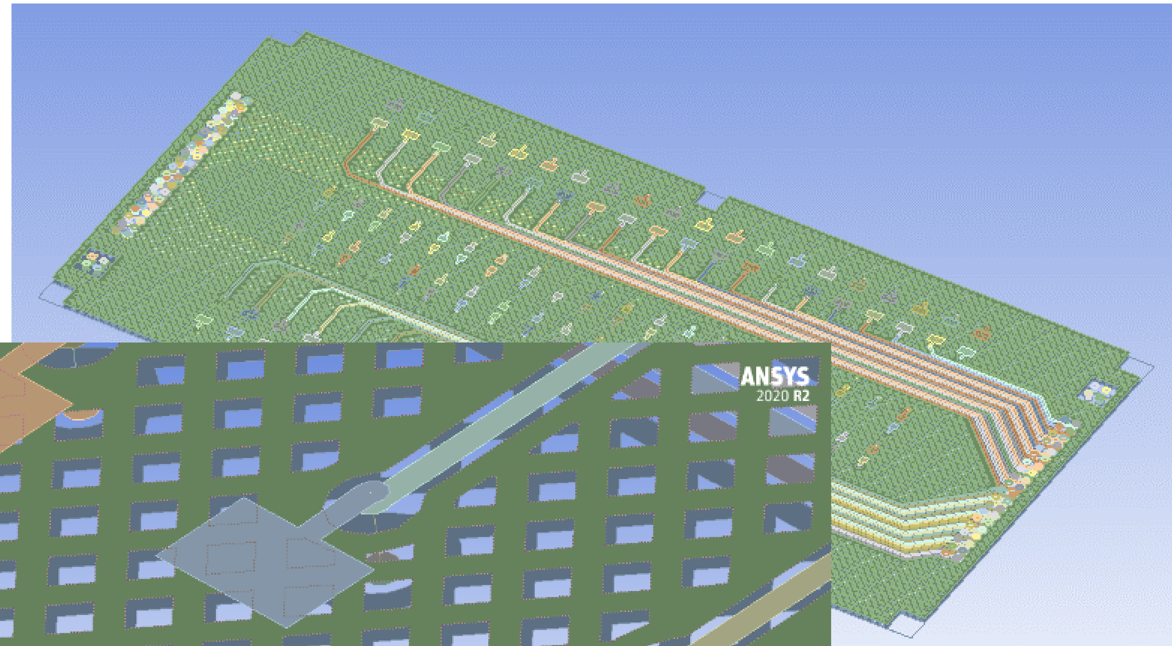
- Important because increasing number of test and field
  failures are driven by the <u>exact</u> layout
  - Extreme Low-K (ELK) fracture
  - Joule Heating, Warpage
  - Microvia separation, Solder dewetting
  - Thermo-mechanical fatigue (solder joints)

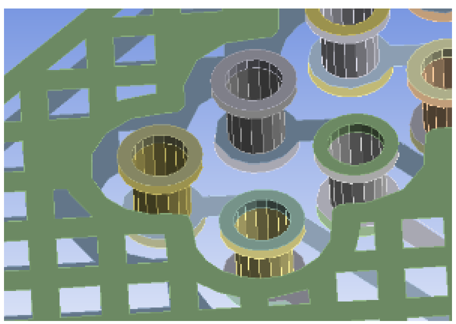


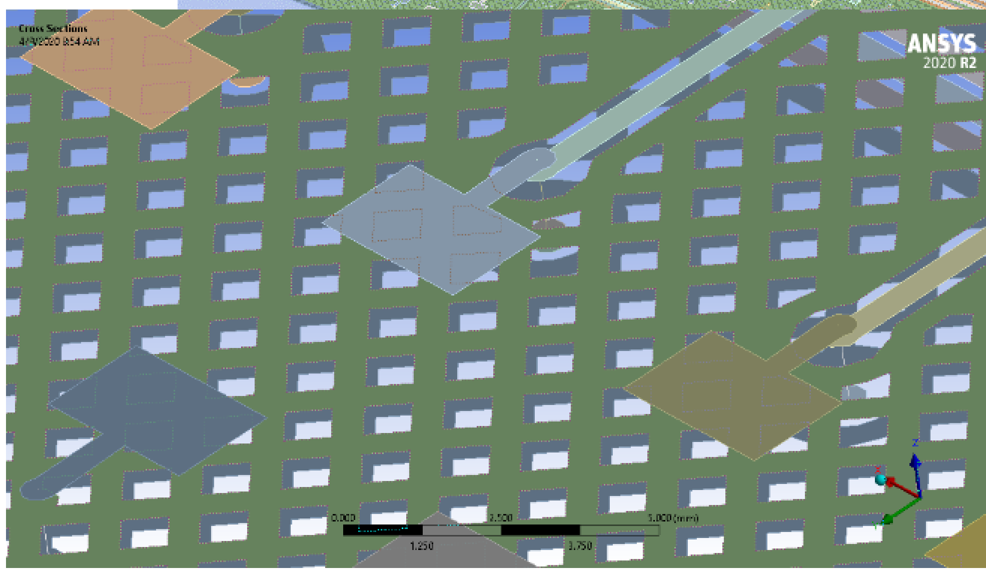
- Unique technique for modeling electronics

Reinforcement Model

- Surfaces for traces and large through holes
- Curves for small through holes and microvias

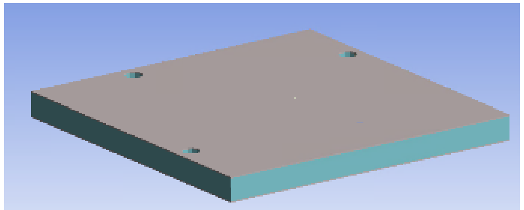


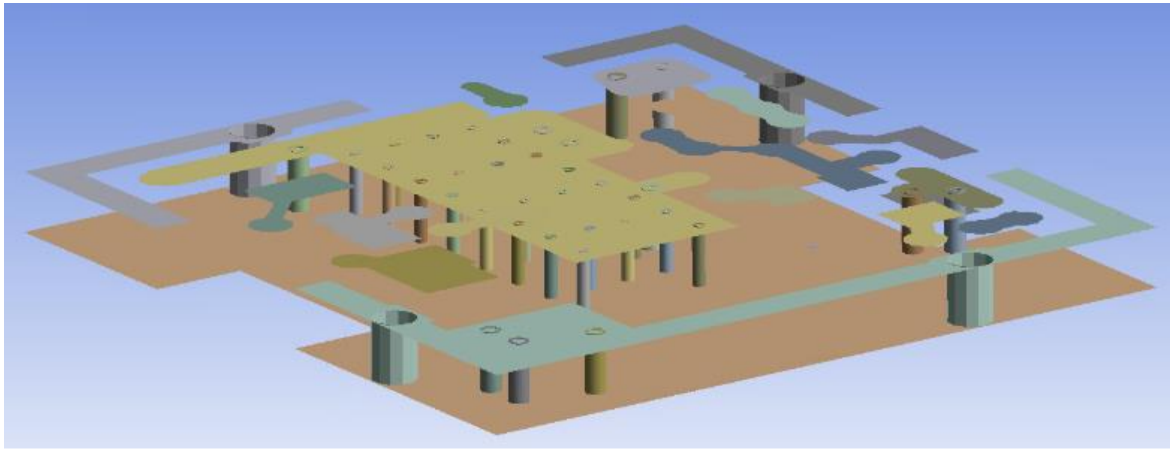




Model Example

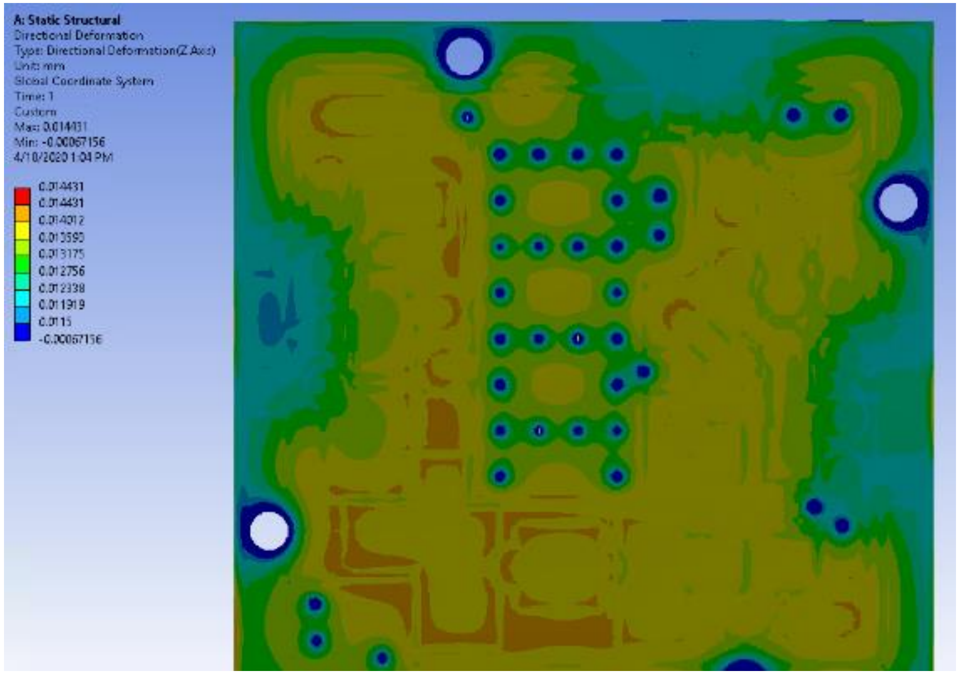
- Small RF circuit board experiencing overstress failures during reflow
- Copper features modeled using shell and beam reinforcements

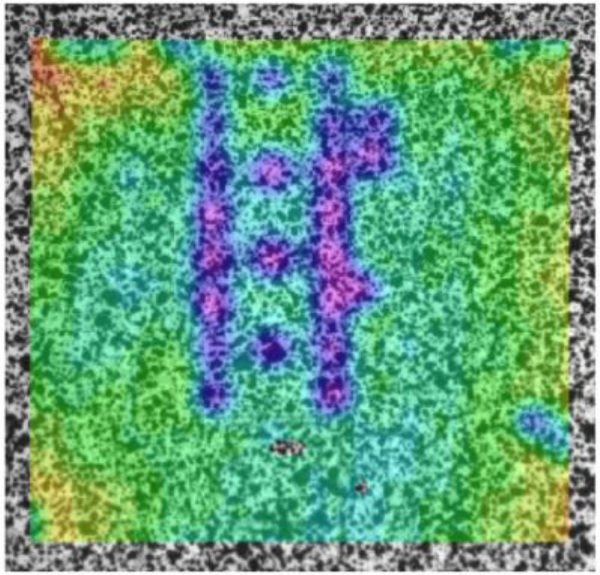




Substrate Deformations

- Substrate with buried vias, excessive deformations causing solder separation
- 22 to 220°C Thermal mechanical simulation



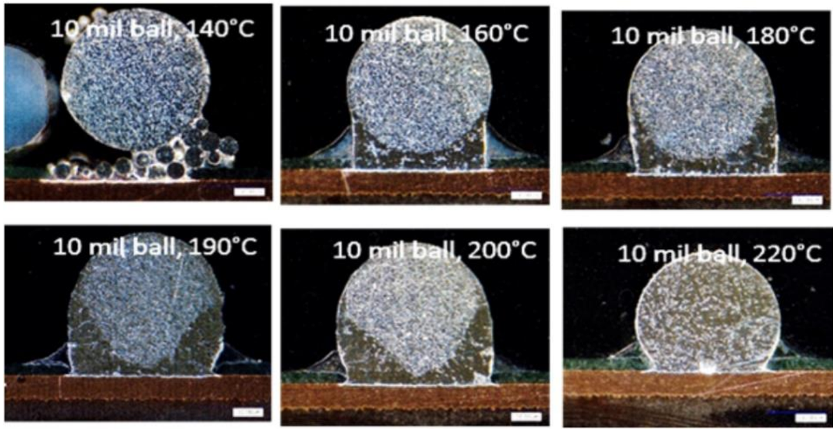


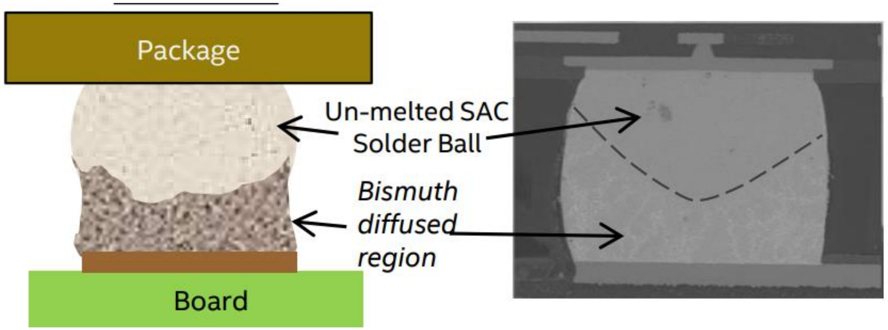
Digital Image Correlation, Z Measurements

20µm variation and defects aligned with the low spots

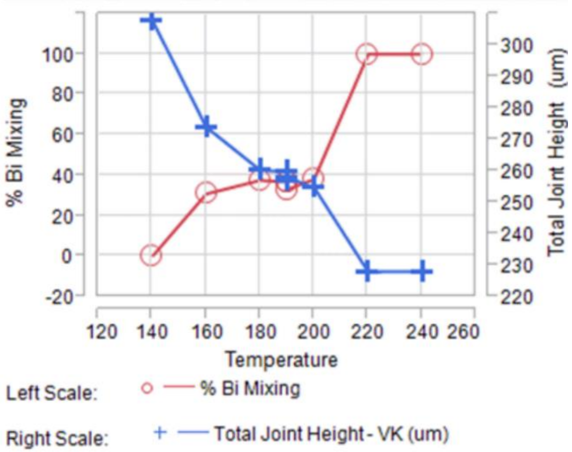
Another Issue - Bismuth Solders

- Low melting point alloy of Bismuth and Tin
- Eutectic 58% Bi 42% Sn
  - 139°C
- Non-Eutectic 63% Sn 37% Bi
  - 174°C Liquidus
  - 139°C Solidus
- A lot of interest in mixed solder joints
  - SAC solder sphere with Bismuth solder paste
  - Critical components would have BiSn spheres





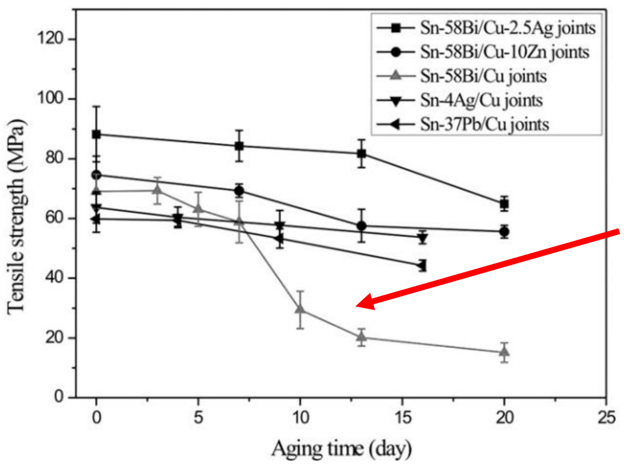
THE APPLICATION OF BI-BASED SOLDERS FOR LOW TEMPERATURE REFLOW TO REDUCE COST WHILE IMPROVING SMT YIELDS IN CLIENT COMPUTING SYSTEMS
Scott Mokler, Ph.D., P.E., Raiyo Aspandiar, Ph.D., Kevin Byrd, Olivia Chen, Satyajit Walwadkar, Kok Kwan Tang, Mukul Renavikar and Sandeep Sane
Intel Corporation
Hillsboro, OR, USA
scott.mokler@intel.com



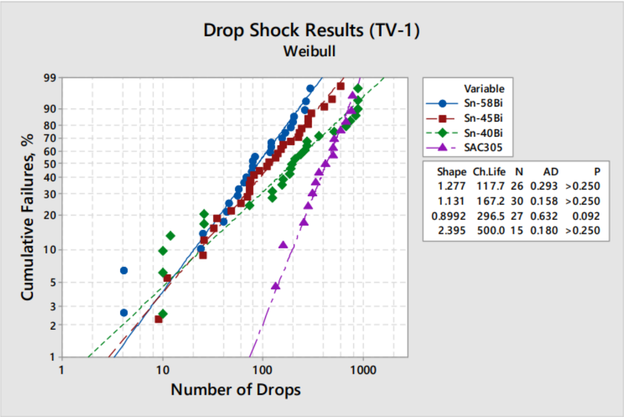
Introduction to Low Temperature Soldering - Intel

Main Concerns - Bismuth

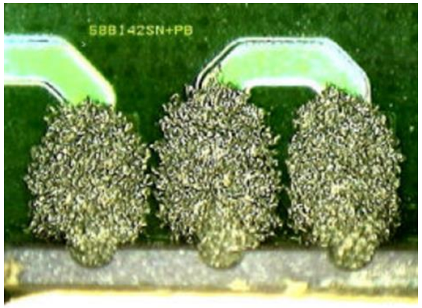
- Drop shock performance
  - If you thought SAC was bad
  - Worse than SAC305
- Pb contamination
- Bismuth segregation/aging (120°C)



Improving tensile and fatigue properties of Sn–58Bi/Cu solder joints through alloying substrate
QingKe Zhang, HeFei Zou, and Zhe-Feng Zhanga)
Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences



LOW TEMPERATURE SOLDERING USING SN-BI ALLOYS
Morgana Ribas, Ph.D., Anil Kumar, Divya Kosuri, Raghu R. Rangaraju, Pritha Choudhury, Ph.D.,
Suresh Telu, Ph.D., Siuli Sarkar, Ph.D.
Alpha Assembly Solutions, Alpha Assembly Solutions
India R&D Centre
Bangalore, KA, India
siuli.sarkar@alphaassembly.com



58Bi42Sn Joints contaminated with Pb
(after 835 Thermal Cycles -55 to +125 °C)
Suspect issue with SnPbBi ternary eutectic (Tmelt = 96 °C)

Woodrow, “The Effects of Trace Amounts of Lead on the Reliability of Six Lead-Free Solders,” IPC Proceedings of the 3rd International Conference on Lead-Free Components and Assemblies, San Jose, CA April 23-24 (2003)

IEEE

Bismuth – Thermal Cycling Reliability

- Significant reduction in thermal cycling performance (mixed)

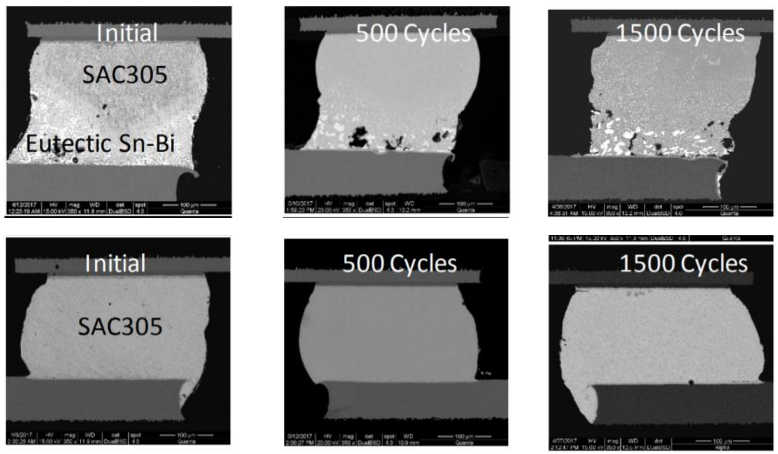
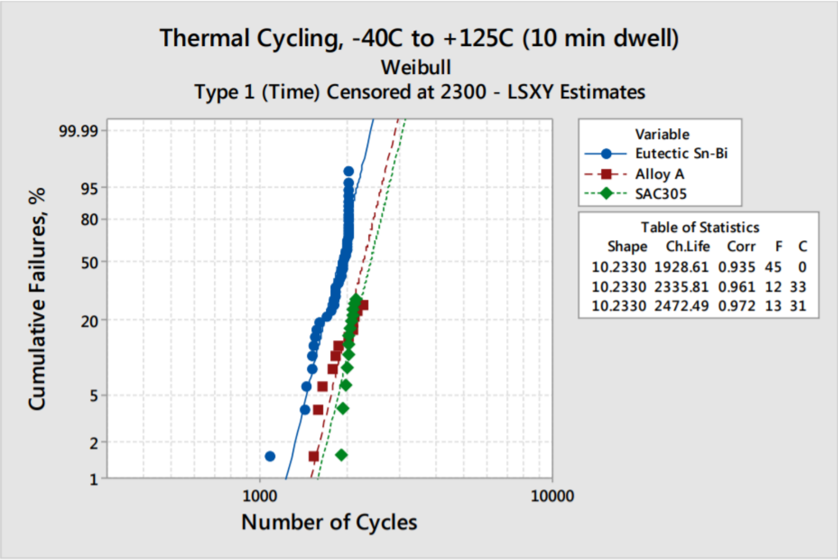


Table1 - In situ cumulative thermal cycling failures on CTBGA84

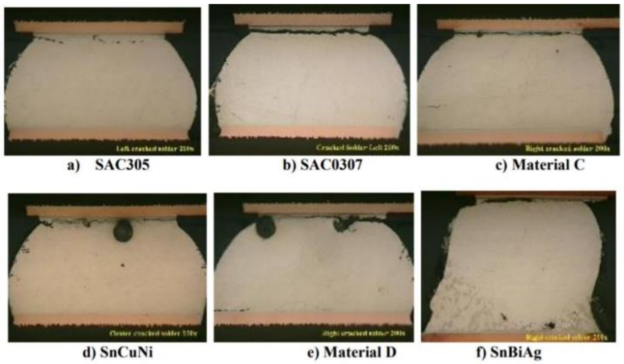
Alloy	% Failures		
	0-1000 TC	0-1500 TC	0-2000 TC
Eutectic Sn-Bi	0	7	67
Alloy A	0	0	13
SAC305	0	0	11



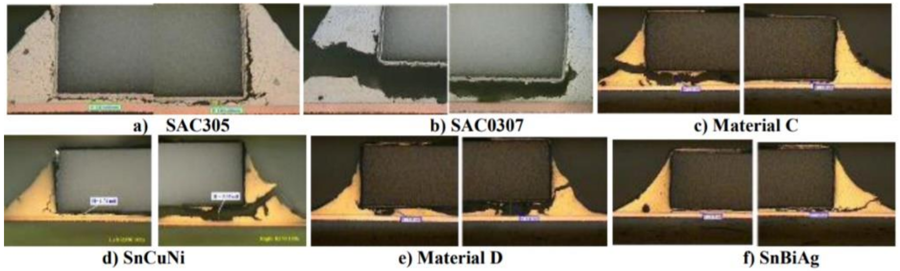
Low Temperature Soldering: Thermal Cycling Reliability Performance
Morgana Ribas, Ph.D., Prathap Augustine, Pritha Choudhury, Ph.D., Raghu Raj Rangaraju, Anil Kumar, Siuli Sarkar, Ph.D.
MacDermid Alpha Electronics Solutions
Bangalore, KA, India

Bismuth – Thermal Cycling Reliability

- Large differentiation in performance for homogenous joints
  - Low silver alloys perform the worst
  - SAC305 and SnBiAg performed the best
- SAC solder balls with Bismuth solder paste is the worst



Thermal Cycling Test Summary	Number of Failed Components After 3000 Cycles							
	U309 (BGA1156)	U1 (BGA196)	U307 (BGA228)	U303 (BGA97)	U300 (BGA64)	U3 (QFP204)	U20 (QFP144)	R2512
SAC305	0/12	0/12	3/12	0/12	0/12	0/12	0/12	2/12
SAC0307	0/12	3/12	5/12	0/12	0/12	0/12	0/12	12/12
Alloy C	0/12	4/12	6/12	0/12	0/12	0/12	0/12	11/12
Alloy D	0/12	4/12	6/12	1/12	0/12	0/12	0/12	12/12
SnCuNi	0/12	2/12	5/12	1/12	0/12	0/12	0/12	12/12
SnBiAg	12*/12	5/12	7/12	1/12	1/12	0/12	0/12	2/12



Reliability Study of Low Silver Alloy Solder Pastes
Jennifer Nguyen, David Geiger and Murad Kurwa
Flextronics International
847 Gibraltar Drive
Milpitas, CA, USA

Questions?