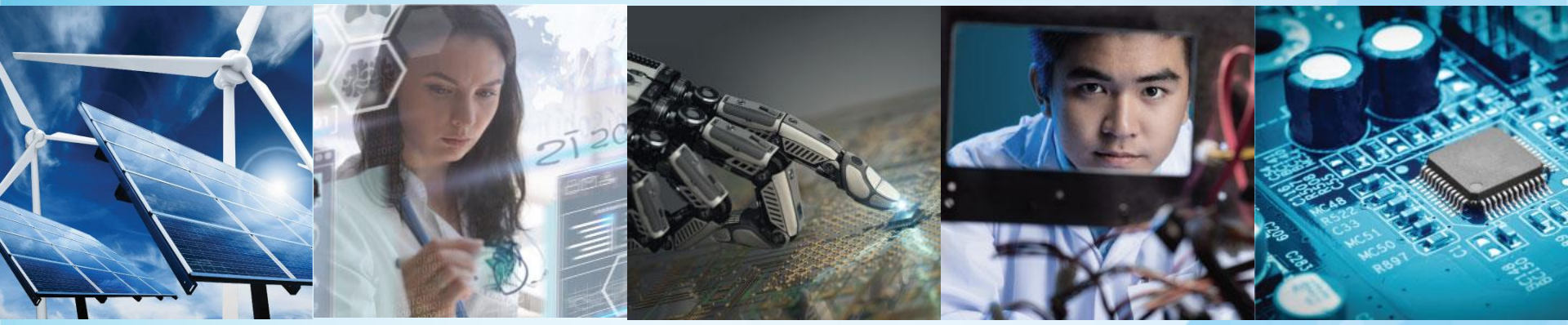

# IEEE AP-S/MTT-S Egypt Section Chapter

## On-Chip Antennas: The Last Barrier to True RF System-on-Chip


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*IEEE APS Distinguished Lecturer*


Date: 9 Feb 2023 | Time: 11:30 AM to 01:30 AM



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# Agenda

- Antenna and circuits: A Brief History
- IC and Antenna Integration Techniques
- Why Antenna-on-Chip?
- Technology stack-ups and features
- Antenna-on-Chip Issues
- Co-Design Examples
- Antenna-on-Chip Radiation Performance Enhancement
- Conclusions
- Discussion and questions.




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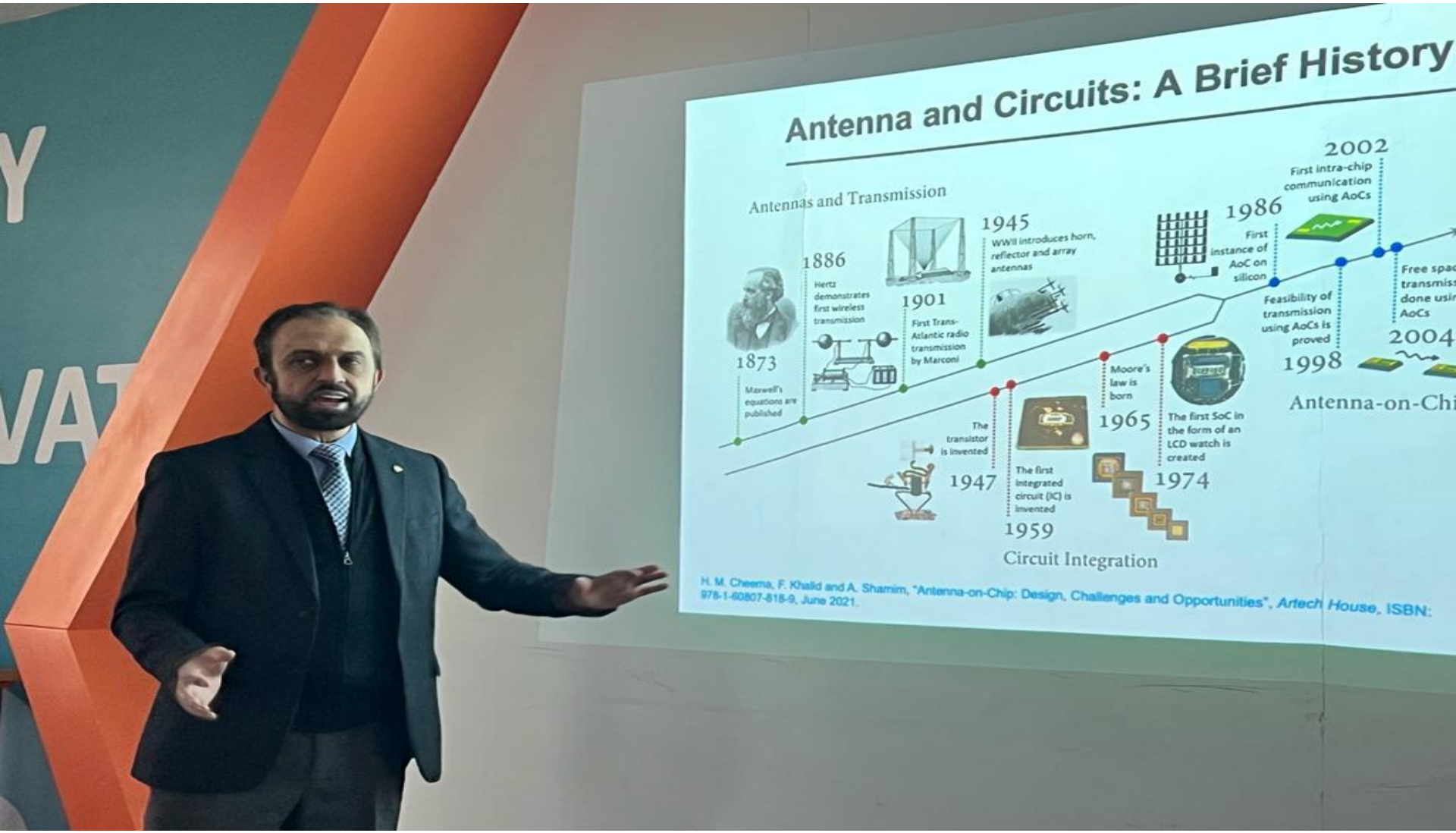
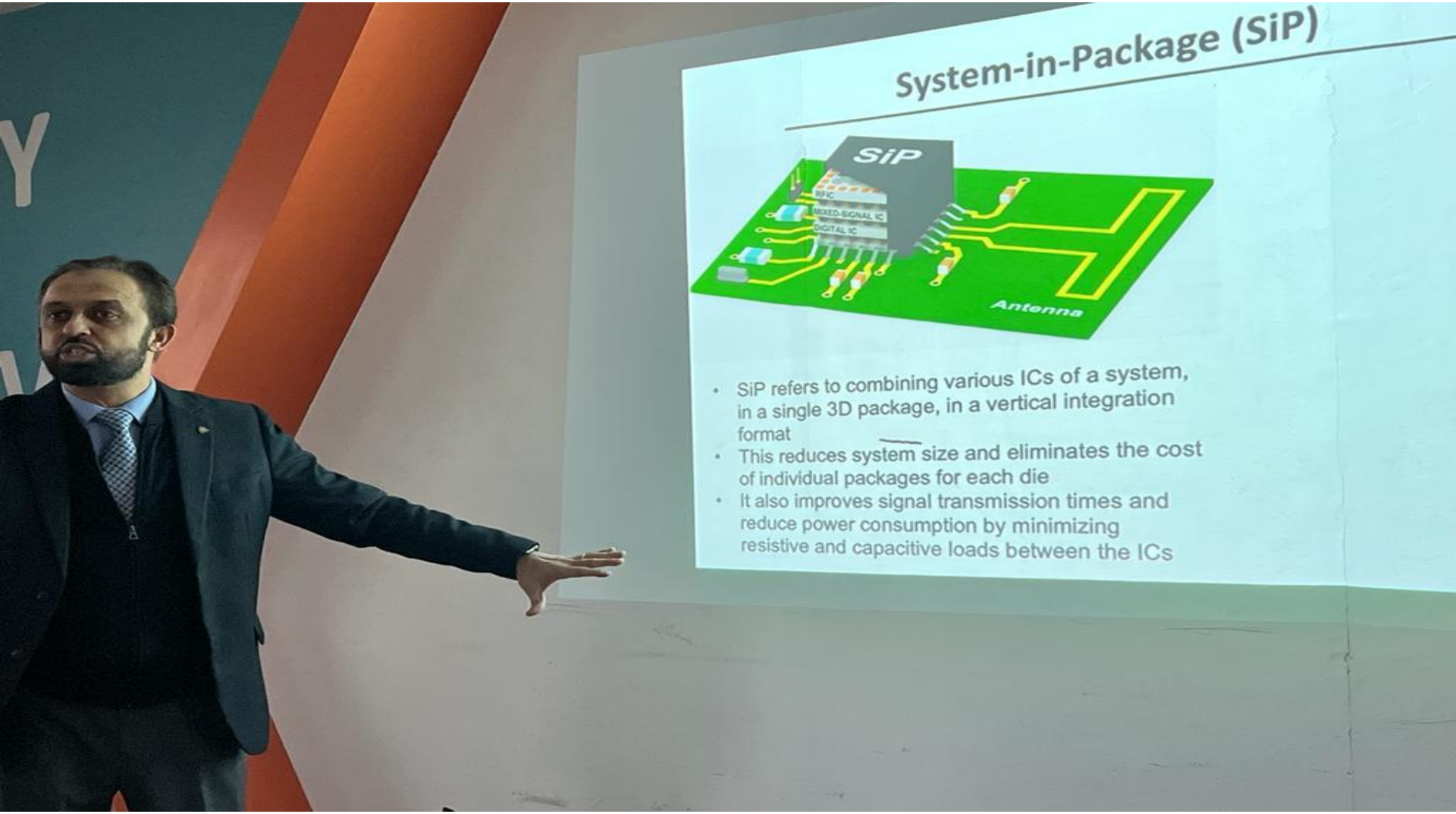
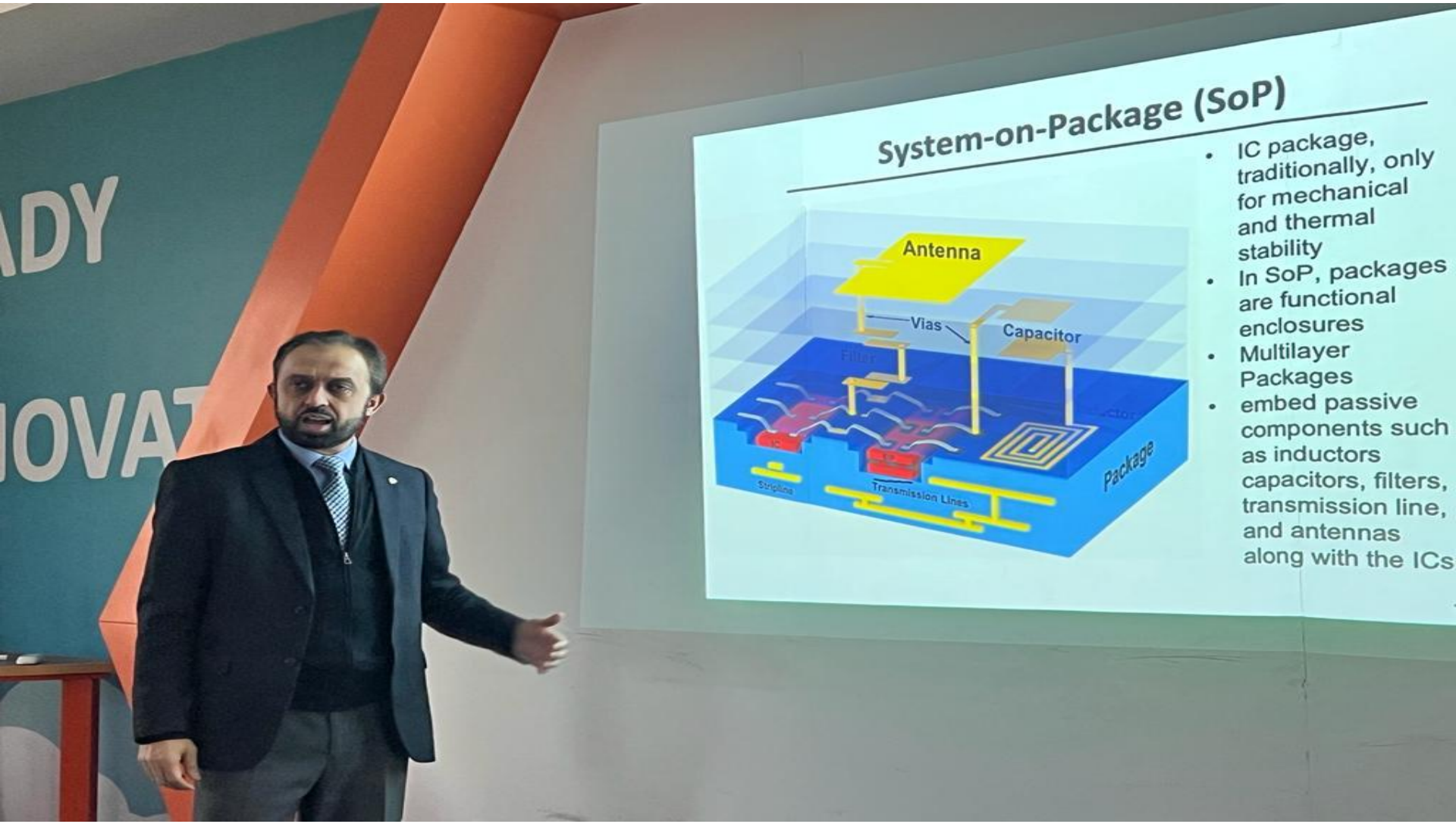
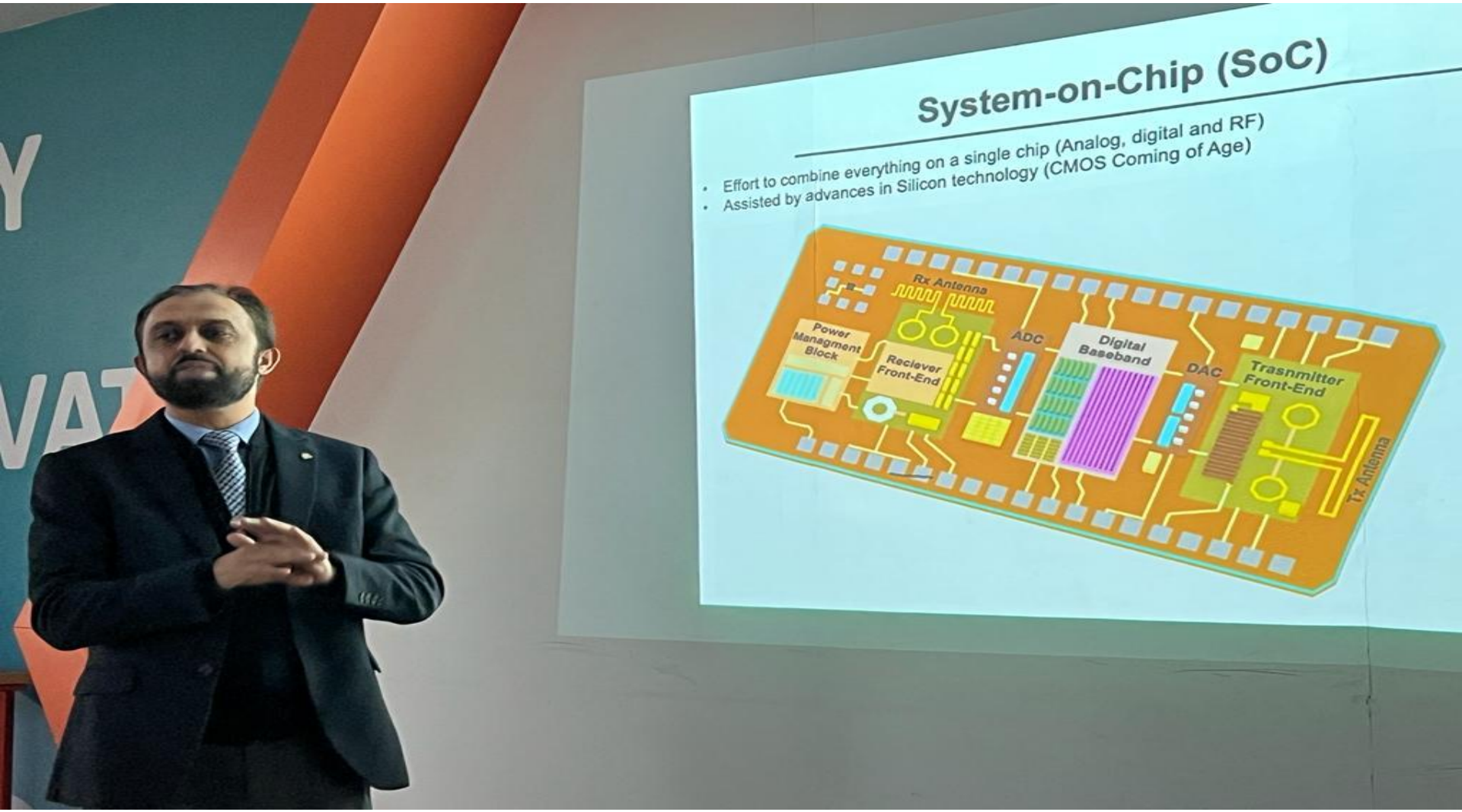
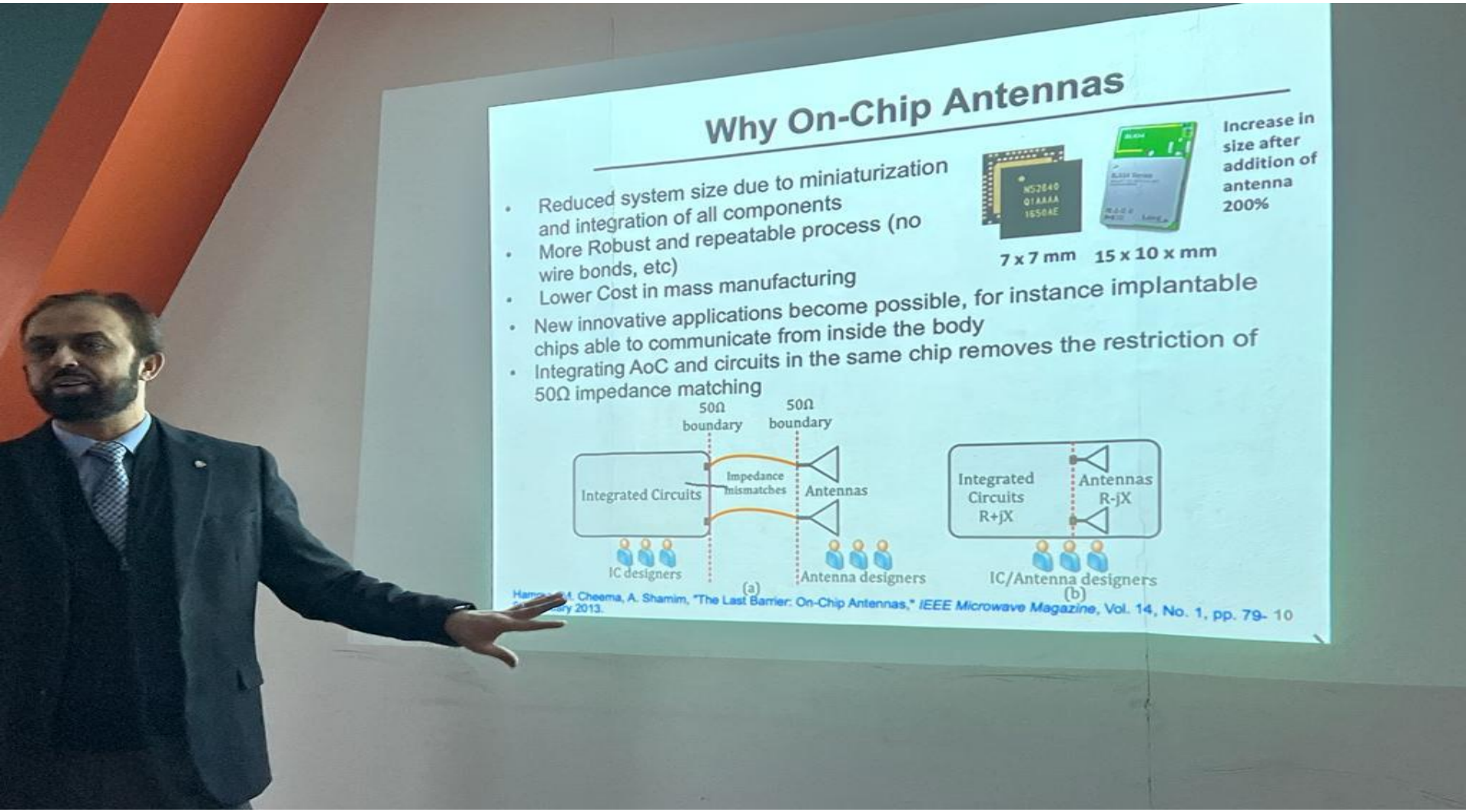
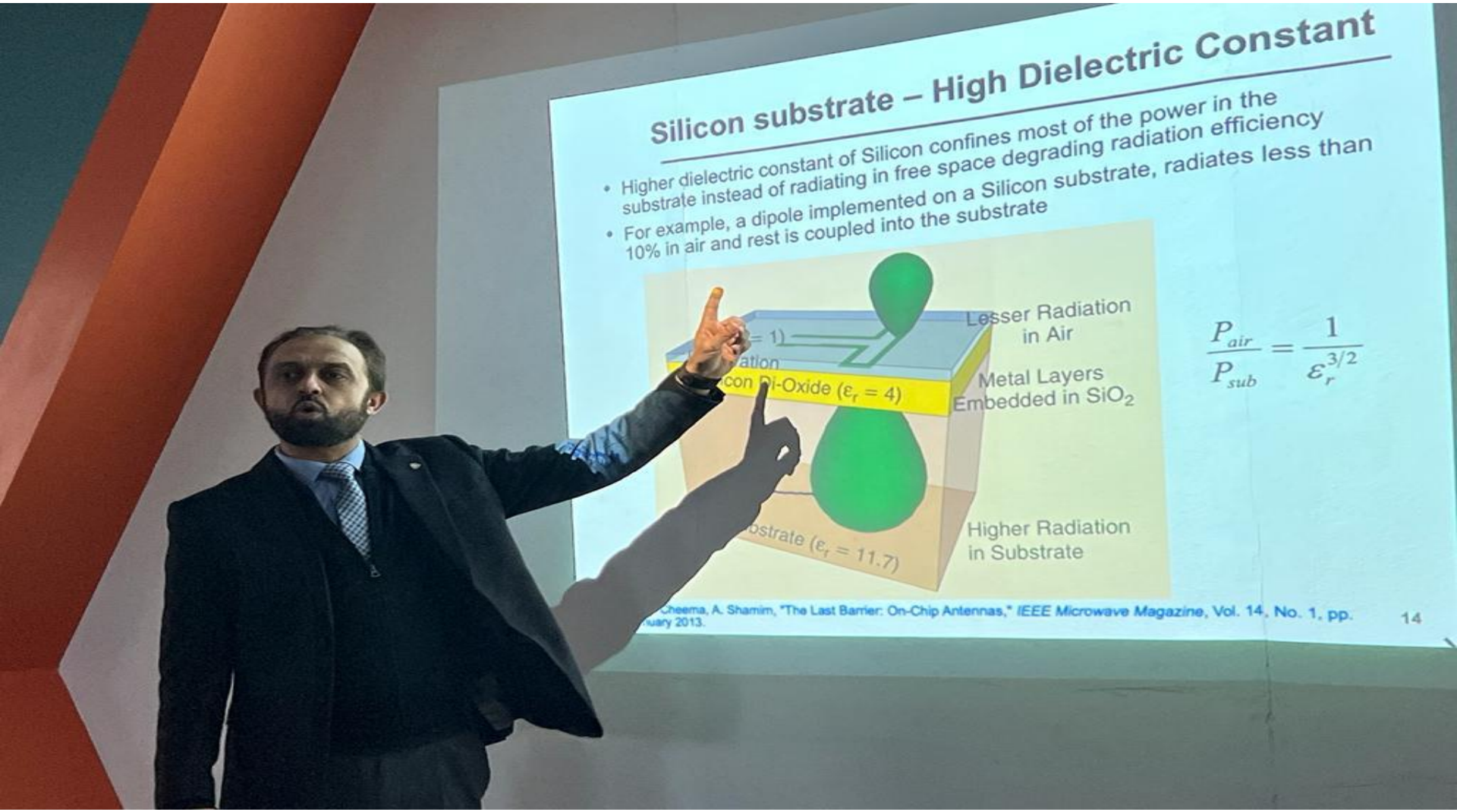

Antenna and Circuits: A Brief History
Antennas and Transmission
1873
Maxwell's equations are published
1886
Hertz demonstrates first wireless transmission
1901
First Trans-Atlantic radio transmission by Marconi
1945
WWII introduces horn, reflector and array antennas
1947
The transistor is invented
1959
The first integrated circuit (IC) is invented
1965
Moore's law is born
1974
The first SoC in the form of an LCD watch is created
1986
First instance of AoC on silicon
1998
Feasibility of transmission using AoCs is proved
2002
First intra-chip communication using AoCs
2004
Antenna-on-Chi
Circuit Integration
H. M. Cheema, F. Khalid and A. Shamim, "Antenna-on-Chip: Design, Challenges and Opportunities", Artech House, ISBN: 978-1-60807-818-9, June 2021.

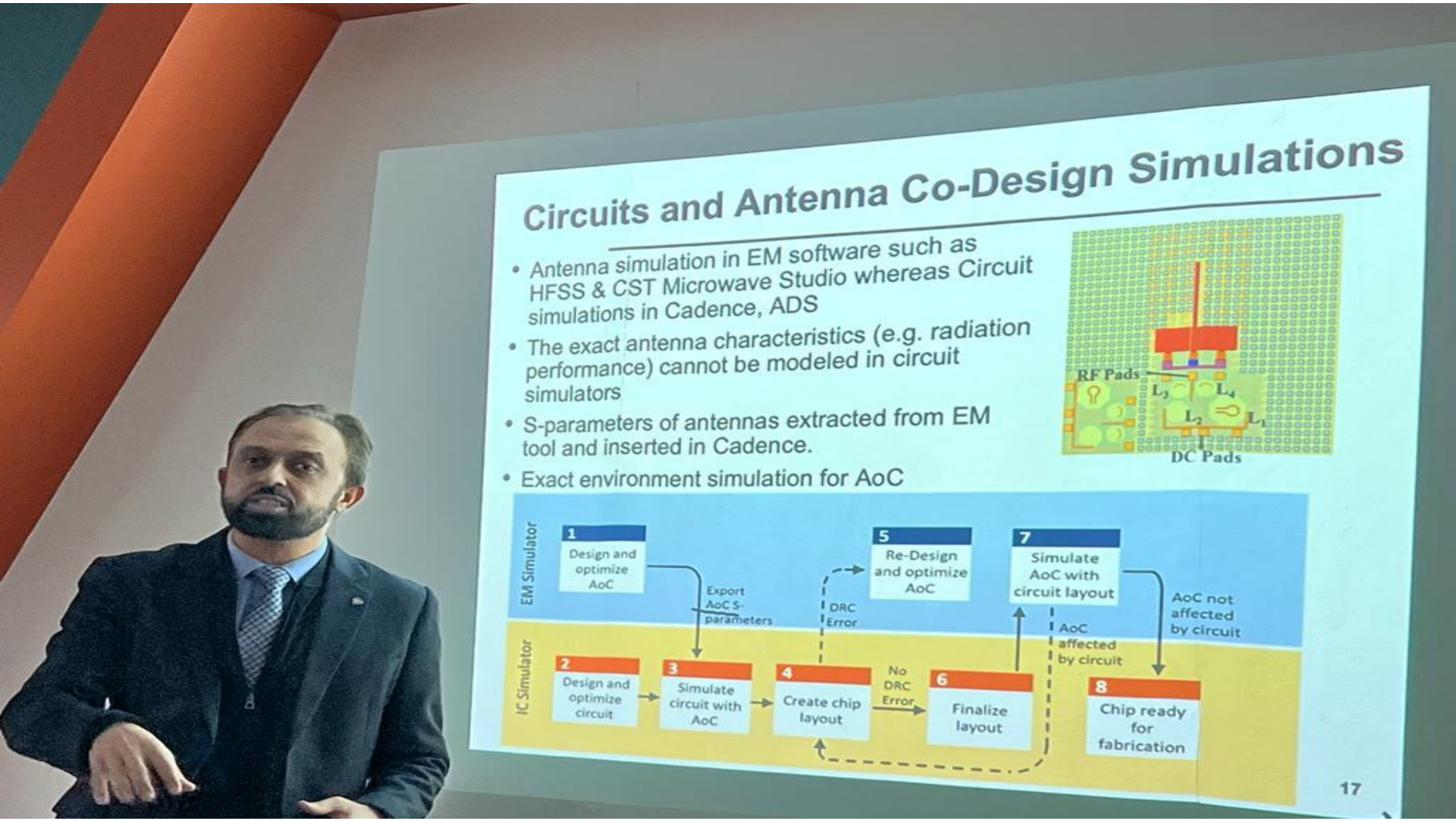

System-in-Package (SiP)
SiP
RFIC
MIXED-SIGNAL IC
DIGITAL IC
Antenna
• SiP refers to combining various ICs of a system, in a single 3D package, in a vertical integration format
• This reduces system size and eliminates the cost of individual packages for each die
• It also improves signal transmission times and reduce power consumption by minimizing resistive and capacitive loads between the ICs

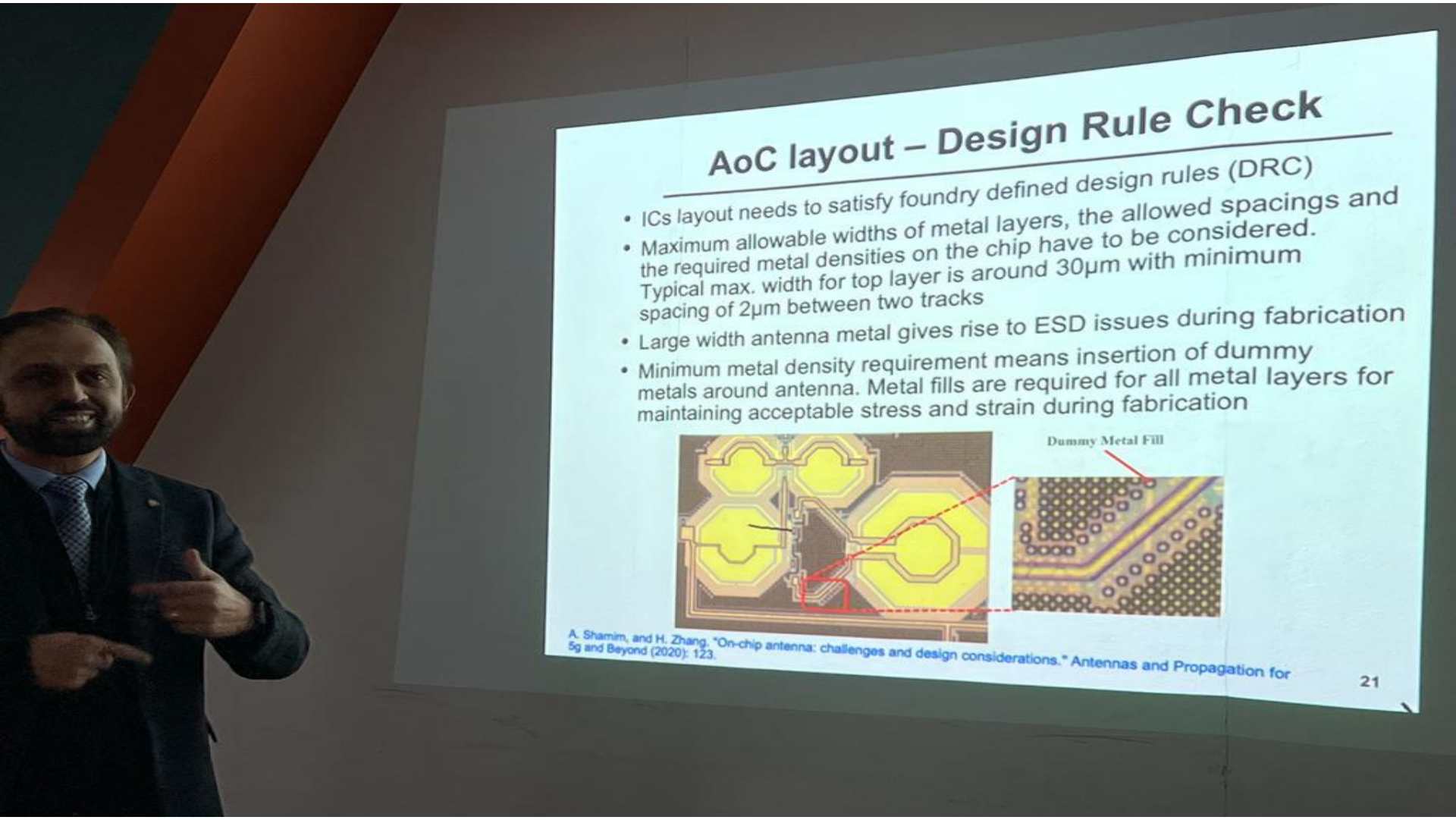

System-on-Package (SoP)
Antenna
Vias
Capacitor
Package
Transmission Lines
IC package, traditionally, only for mechanical and thermal stability
In SoP, packages are functional enclosures
Multilayer Packages
embed passive components such as inductors capacitors, filters, transmission line, and antennas along with the ICs

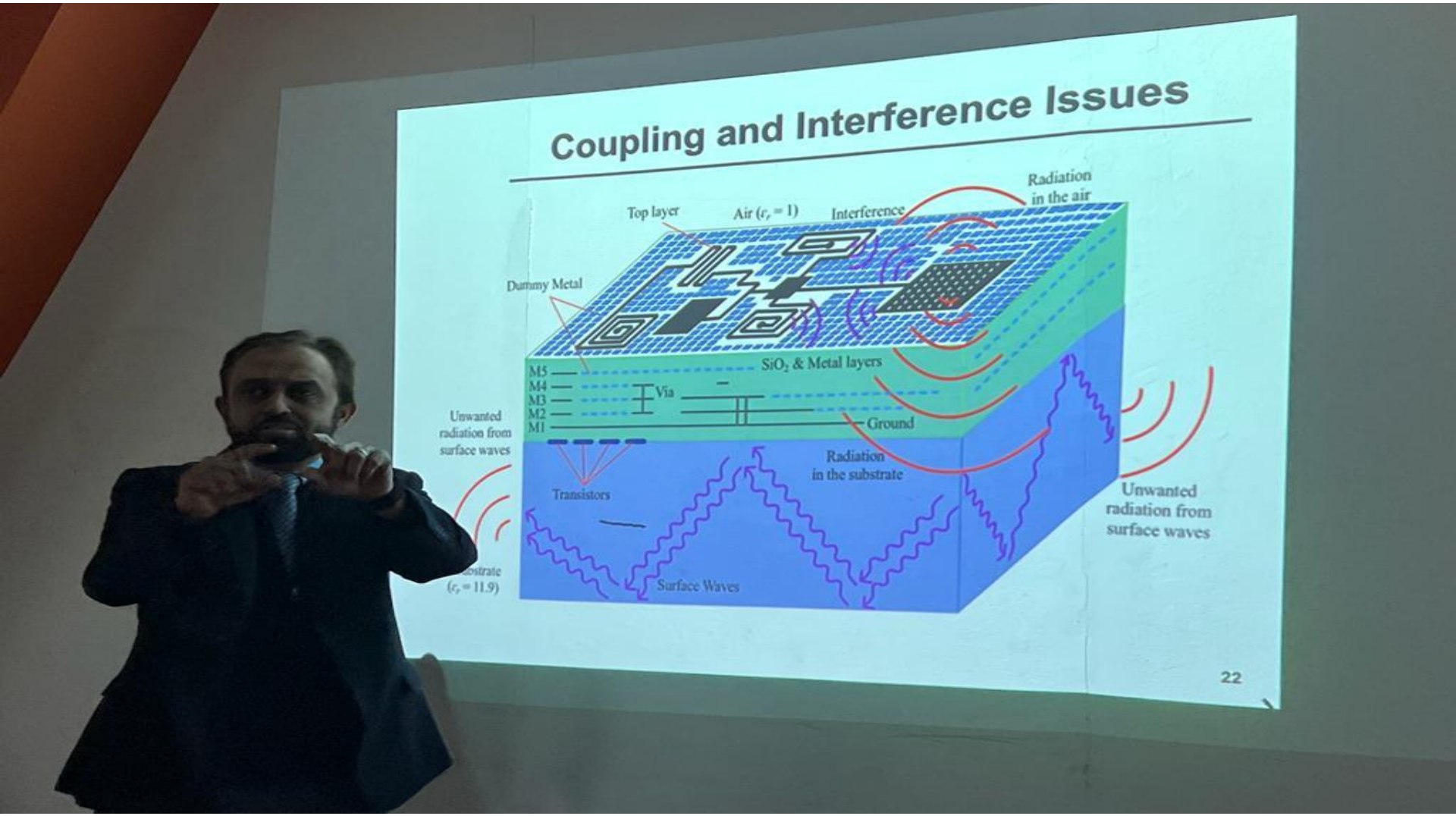

System-on-Chip (SoC)
Effort to combine everything on a single chip (Analog, digital and RF)
Assisted by advances in Silicon technology (CMOS Coming of Age)
Rx Antenna
Power Managment Block
Reciever Front-End
ADC
Digital Baseband
DAC
Trasnmitter Front-End
Tx Antenna

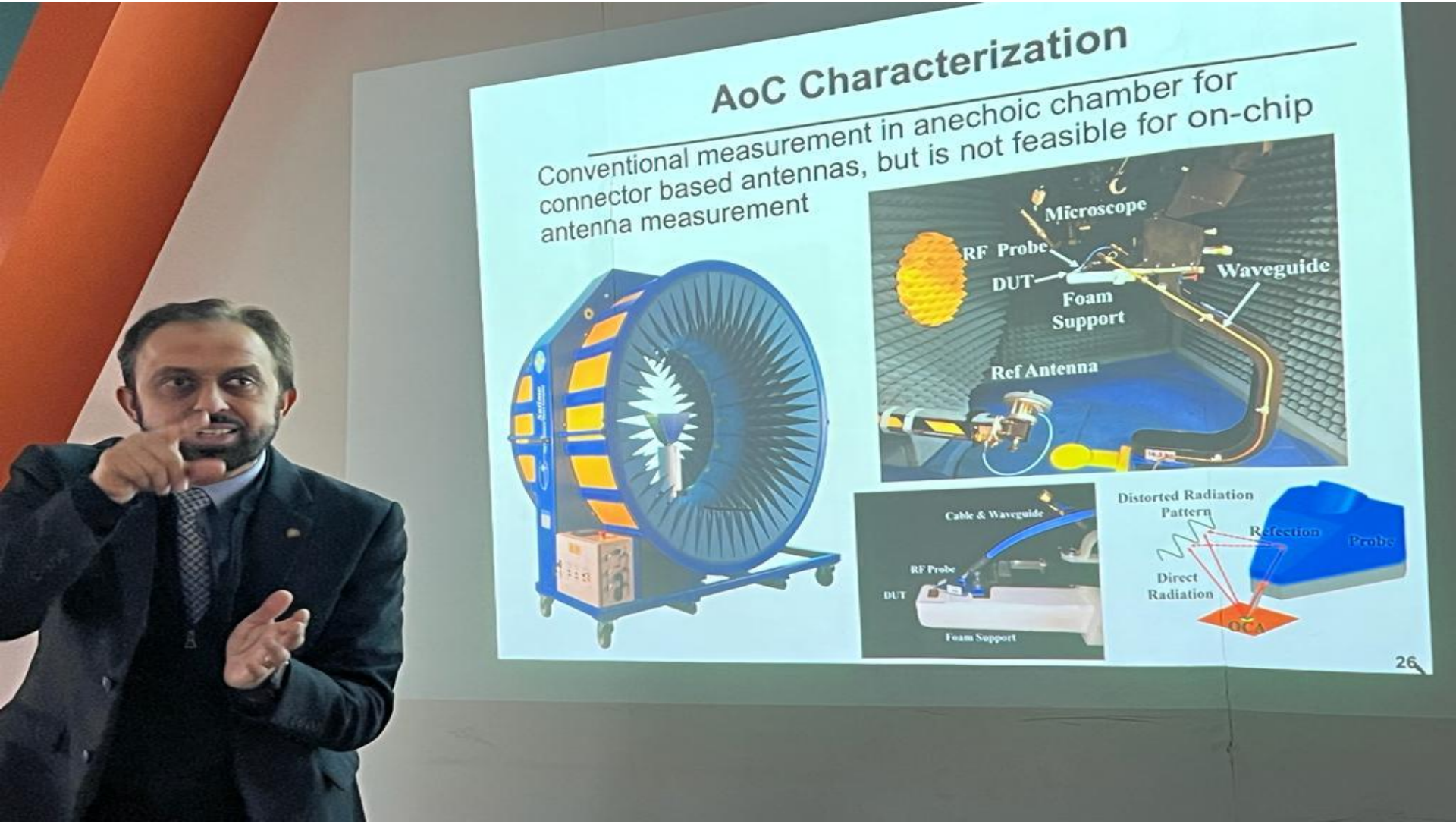

Why On-Chip Antennas
Reduced system size due to miniaturization and integration of all components
More Robust and repeatable process (no wire bonds, etc)
Lower Cost in mass manufacturing
New innovative applications become possible, for instance implantable chips able to communicate from inside the body
Integrating AoC and circuits in the same chip removes the restriction of 50Ω impedance matching
Increase in size after addition of antenna 200%
7 x 7 mm
15 x 10 x mm
50Ω boundary
50Ω boundary
Integrated Circuits
Impedance Mismatches
Antennas
IC designers
Antenna designers
(a)
Integrated Circuits R+jX
Antennas R-jX
IC/Antenna designers
(b)
A. Cheema, A. Shamim, "The Last Barrier: On-Chip Antennas," IEEE Microwave Magazine, Vol. 14, No. 1, pp. 79- 10
2013.

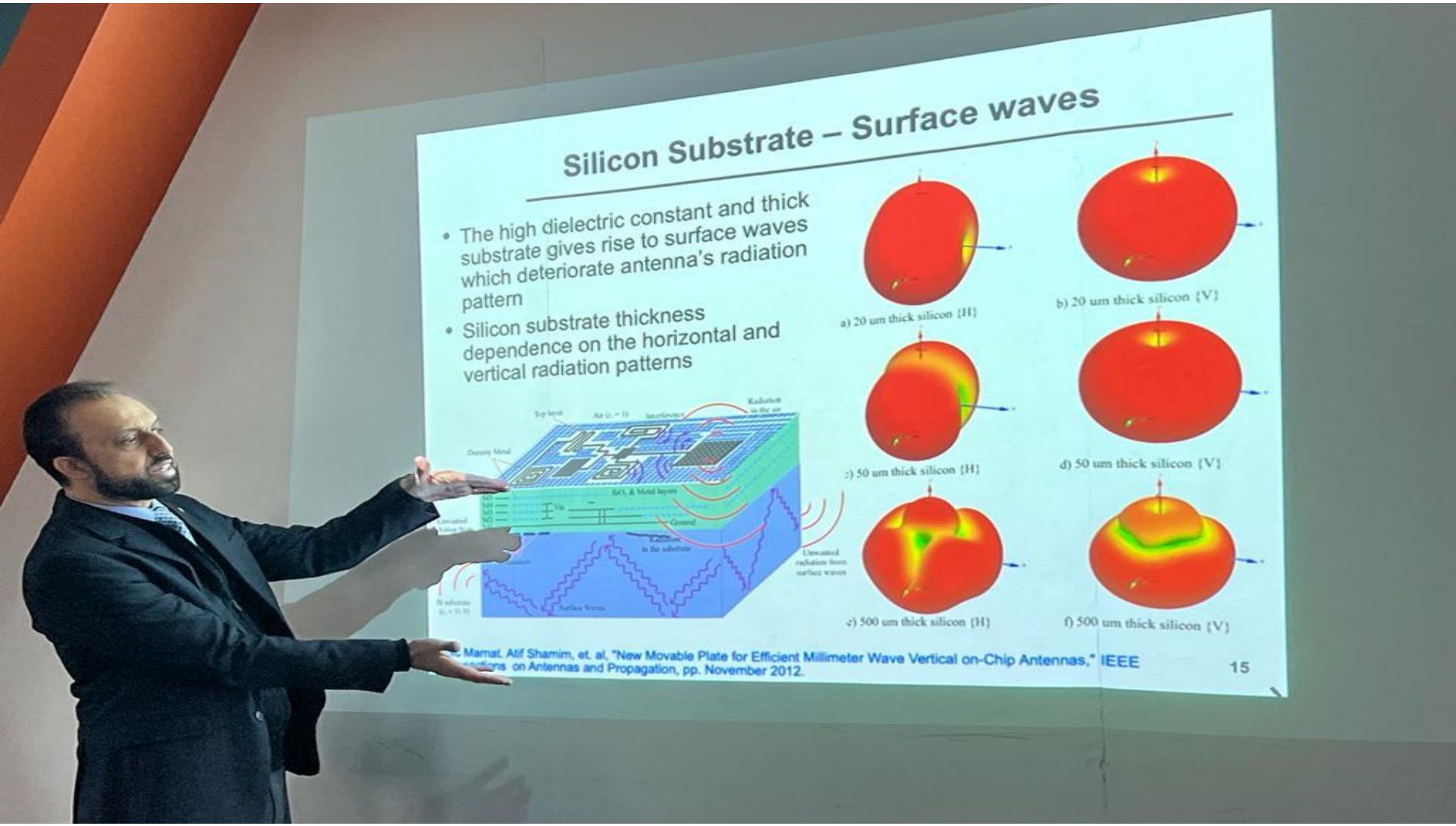

Silicon substrate – High Dielectric Constant
• Higher dielectric constant of Silicon confines most of the power in the substrate instead of radiating in free space degrading radiation efficiency
• For example, a dipole implemented on a Silicon substrate, radiates less than 10% in air and rest is coupled into the substrate
Lesser Radiation in Air
Metal Layers Embedded in $SiO_2$
Higher Radiation in Substrate
$\frac{P_{air}}{P_{sub}} = \frac{1}{\varepsilon_r^{3/2}}$
Cheema, A. Shamim, "The Last Barrier: On-Chip Antennas," IEEE Microwave Magazine, Vol. 14, No. 1, pp.
uary 2013.
14

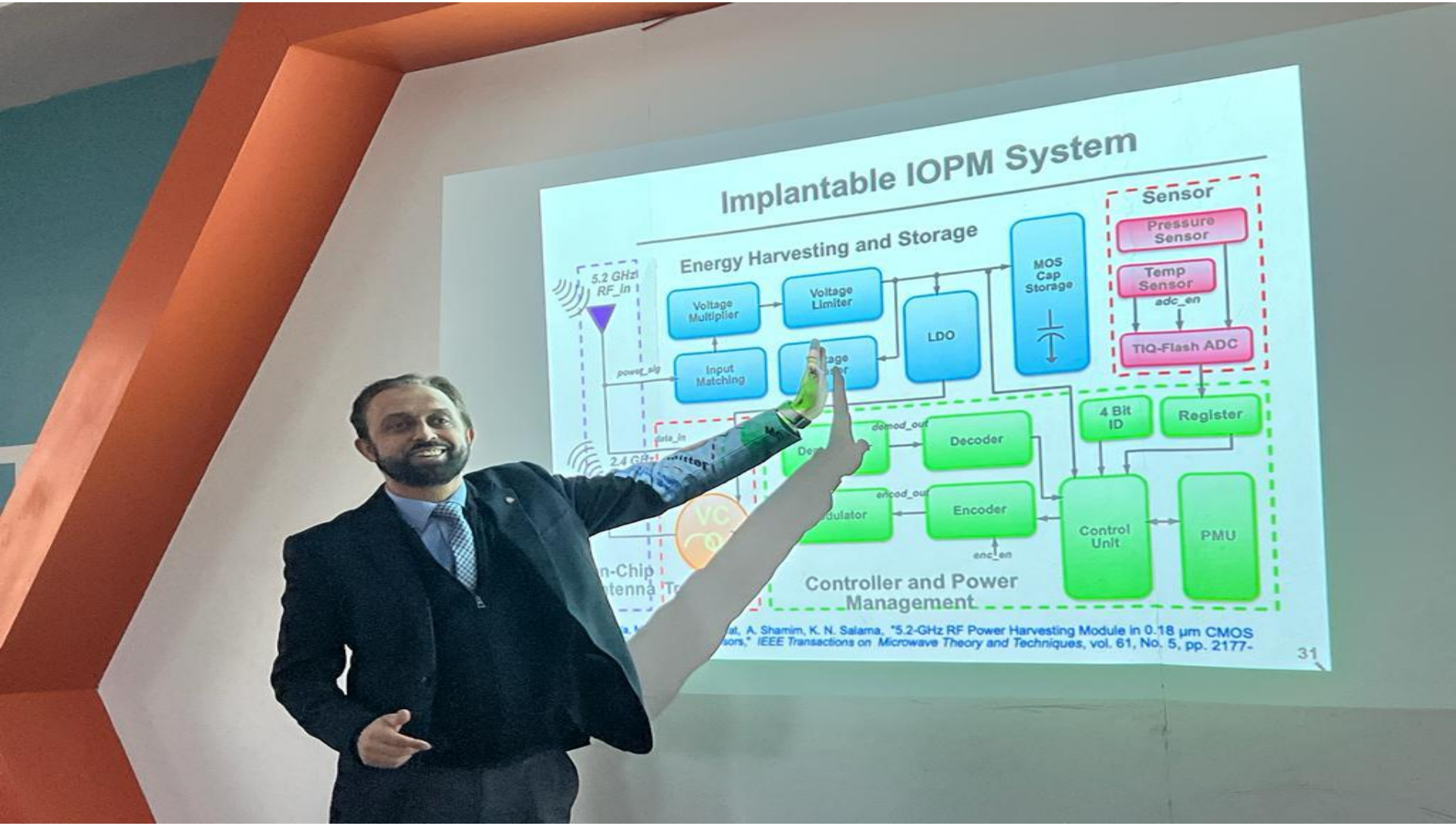

Circuits and Antenna Co-Design Simulations
• Antenna simulation in EM software such as HFSS & CST Microwave Studio whereas Circuit simulations in Cadence, ADS
• The exact antenna characteristics (e.g. radiation performance) cannot be modeled in circuit simulators
• S-parameters of antennas extracted from EM tool and inserted in Cadence.
• Exact environment simulation for AoC
RF Pads
DC Pads
EM Simulator
IC Simulator
1 Design and optimize AoC
2 Design and optimize circuit
3 Simulate circuit with AoC
4 Create chip layout
5 Re-Design and optimize AoC
6 Finalize layout
7 Simulate AoC with circuit layout
8 Chip ready for fabrication
Export AoC S-parameters
DRC Error
No DRC Error
AoC affected by circuit
AoC not affected by circuit
17

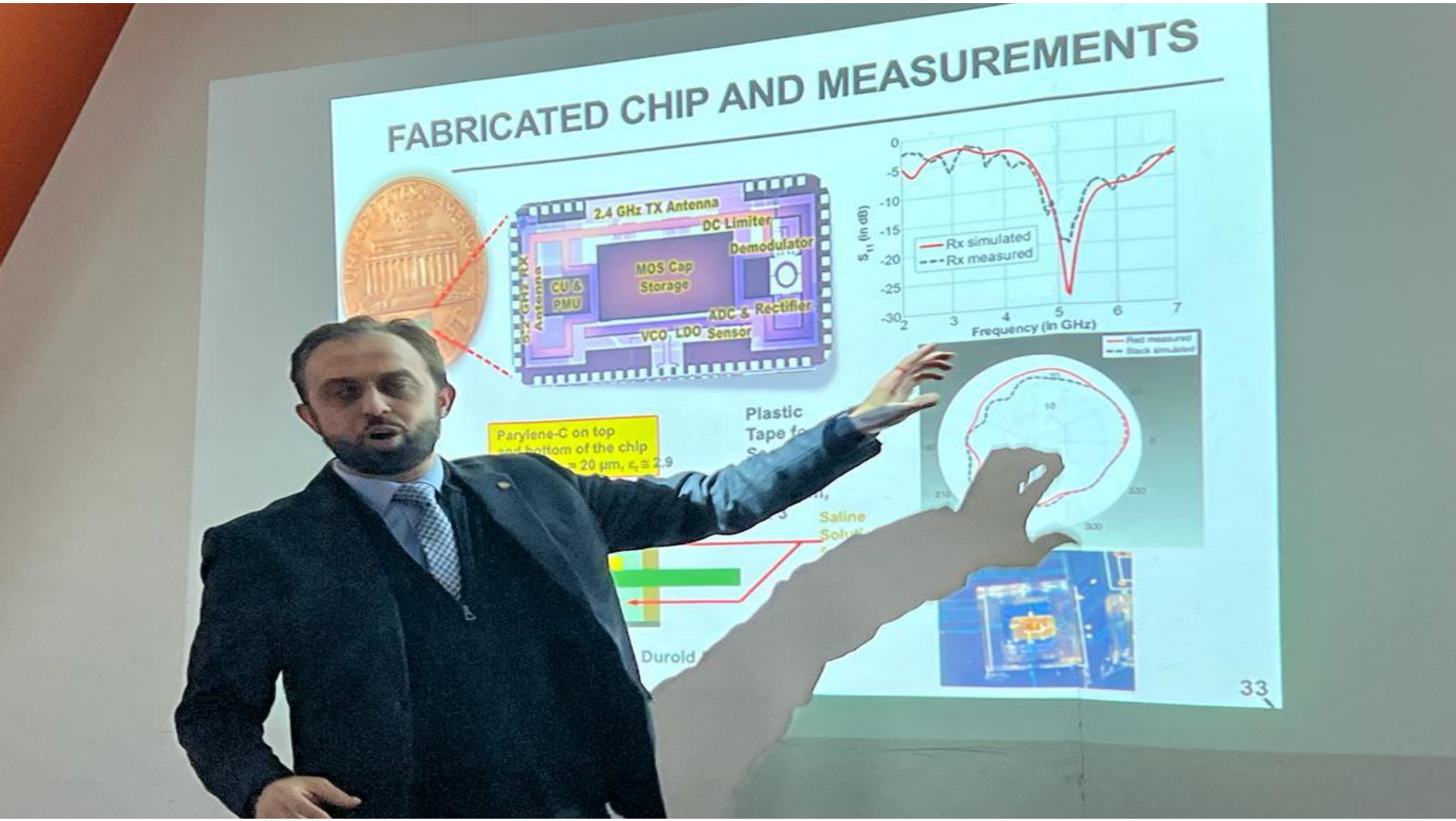

AoC layout – Design Rule Check
• ICs layout needs to satisfy foundry defined design rules (DRC)
• Maximum allowable widths of metal layers, the allowed spacings and the required metal densities on the chip have to be considered. Typical max. width for top layer is around 30μm with minimum spacing of 2μm between two tracks
• Large width antenna metal gives rise to ESD issues during fabrication
• Minimum metal density requirement means insertion of dummy metals around antenna. Metal fills are required for all metal layers for maintaining acceptable stress and strain during fabrication
Dummy Metal Fill
A. Shamim, and H. Zhang. "On-chip antenna: challenges and design considerations." Antennas and Propagation for 5g and Beyond (2020): 123.
21

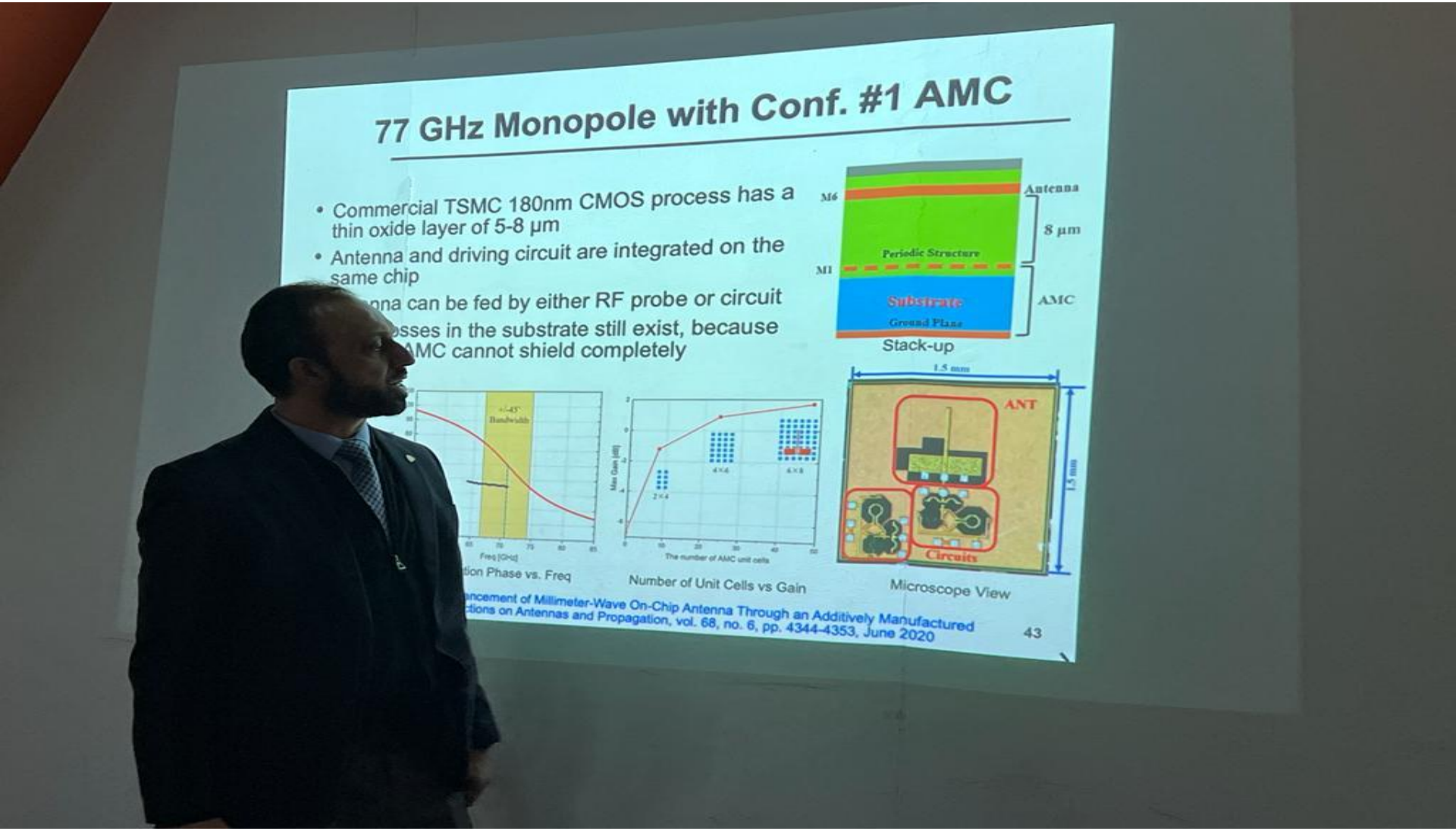

Coupling and Interference Issues
Radiation in the air
Top layer
Air ($\varepsilon_r = 1$)
Interference
Dummy Metal
$SiO_2$ & Metal layers
M5
M4
M3
M2
M1
Via
Ground
Unwanted radiation from surface waves
Radiation in the substrate
Transistors
Surface Waves
Unwanted radiation from surface waves
22


AoC Characterization
Conventional measurement in anechoic chamber for connector based antennas, but is not feasible for on-chip antenna measurement
Microscope
RF Probe
DUT
Waveguide
Foam Support
Ref Antenna
Cable & Waveguide
RF Probe
DUT
Foam Support
Distorted Radiation Pattern
Reflection
Probe
Direct Radiation
26


Silicon Substrate – Surface waves
• The high dielectric constant and thick substrate gives rise to surface waves which deteriorate antenna's radiation pattern
• Silicon substrate thickness dependence on the horizontal and vertical radiation patterns
a) 20 um thick silicon {H}
b) 20 um thick silicon {V}
:) 50 um thick silicon {H}
d) 50 um thick silicon {V}
e) 500 um thick silicon {H}
f) 500 um thick silicon {V}
Marmat, Atif Shamim, et. al, "New Movable Plate for Efficient Millimeter Wave Vertical on-Chip Antennas," IEEE
on Antennas and Propagation, pp. November 2012.
15

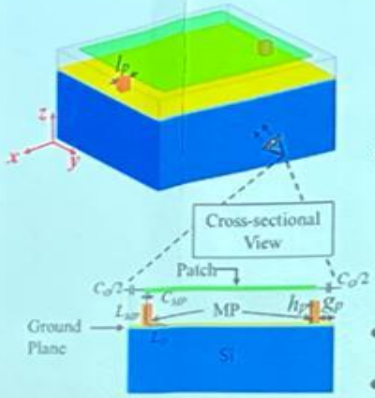

Implantable IOPM System
Energy Harvesting and Storage
5.2 GHz RF_in
Voltage Multiplier
Voltage Limiter
Input Matching
LDO
MOS Cap Storage
Sensor
Pressure Sensor
Temp Sensor
adc_en
TIQ-Flash ADC
4 Bit ID
Register
Decoder
Encoder
Control Unit
PMU
Controller and Power Management
31

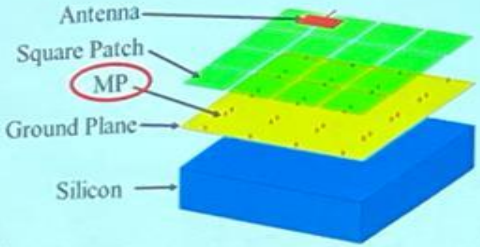

FABRICATED CHIP AND MEASUREMENTS
2.4 GHz TX Antenna
DC Limiter
Demodulator
MOS Cap Storage
CU & PMU
5.2 GHz RX Antenna
ADC & Rectifier
VCO LDO Sensor
Rx simulated
Rx measured
$S_{11}$ (in dB)
Frequency (in GHz)
Parylene-C on top
Plastic
Saline
33

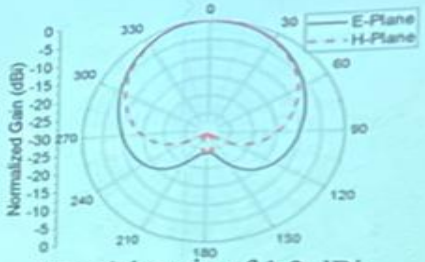

77 GHz Monopole with Conf. #1 AMC
• Commercial TSMC 180nm CMOS process has a thin oxide layer of 5-8 µm
• Antenna and driving circuit are integrated on the same chip
nna can be fed by either RF probe or circuit
sses in the substrate still exist, because AMC cannot shield completely
M6
Antenna
8 µm
Periodic Structure
M1
Substrate
Ground Plane
AMC
Stack-up
1.5 mm
ANT
1.5 mm
Circuits
Microscope View
ion Phase vs. Freq
Number of Unit Cells vs Gain
ncement of Millimeter-Wave On-Chip Antenna Through an Additively Manufactured
ctions on Antennas and Propagation, vol. 68, no. 6, pp. 4344-4353, June 2020
43

# 94 GHz Monopole with Ultra-thin Conf.#2 AMC

## Technique 1: Metallic Posts (MP)




Boresight gain of 1.2 dBi

- Vias are utilized to form MP
- Introduces additional $L_{MP}$ and $C_{MP}$ to reduce $v_p$
- The electrical thickness of the AMC increases equivalently
- The thickness of patch-based unit cell can be reduced by 33%

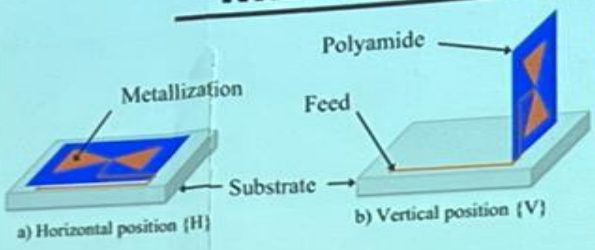
$$v_p \propto \frac{1}{\sqrt{2L_{MP} \times 2C_{MP}}}$$

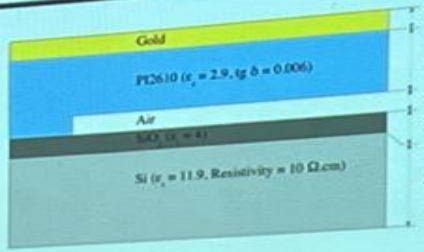
IEEE Transactions on Antennas ... ductor for Gain-Enhancement of Antenna-on-Chip," ... 09/TAP.2022.3140528.

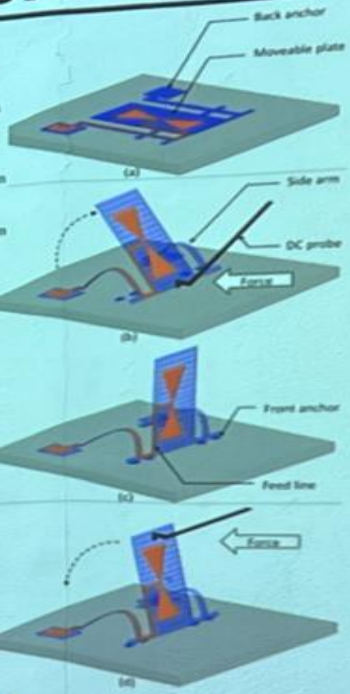
45


Radiation Performance Enhancement
1. Substrate post-processing techniques: Modification of the properties and dimensions of the substrate below the antenna.
2. On-chip reflecting surfaces: Insertion of specialized structures in the metal layers below the antenna to isolate the lossy substrate as well as enhance the gain through in phase reflections.
3. Three-Dimensional (3D) and MEMS based AoCs: Microelectromechanical Systems (MEMS) and radiators such as bond-wires antennas implemented as high efficiency AoCs due to physical separation from the substrate.
4. Off- Chip Techniques and Smart Packaging: Addition of superstrate layers, dielectric resonators and focusing lenses on top of the antenna.
Superstrate layers added above antenna
Antenna is made planar or 3D using MEMS
Substrate is thinned to reduce loss
Ground plane at the bottom of the substrate
Micromachining of substrate in selective areas beneath antenna
High resistivity substrate to reduce conductivity losses
AMC added in interlayers to boost gain
DRA added on top of chip to enhance radiation
Dielectric lens placed on top or bottom of AoC
39

# MEMS based Moveable Antenna



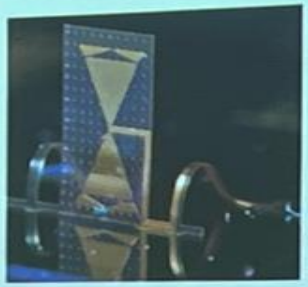
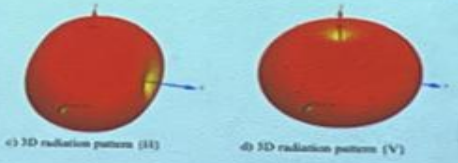



TABLE I: MEASURED GAIN (IN DBI) AT 60 AND 77 GHZ IN HORIZONTAL AND VERTICAL POSITION

| 60 GHz | | 77 GHz | |
|---|---|---|---|
| {H} | {V} | {H} | {V} |
| -3.0 | 3.5 | -2.1 | 4.8 |



c) 3D radiation pattern {H}  d) 3D radiation pattern {V}

Loïc Marnat, Atif Shamim, "New Movable Plate for Efficient Millimeter Wave Vertical on-Chip Antennas," IEEE Transactions on Antennas and Propagation, vol. 61, Issue 4, pp. 1608-1615, April 2013.

48

# Thank You



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