IEEE ELECTRONICS PACKAGING SOCIETY

Signal Integrity Issues and High-Speed Interconnects

Prof. Ram Achar, Fellow IEEE, Fellow EIC

Carleton University

5170ME, Dept. of Electronics
Ottawa, Ontario, Canada – K1S 5B6
Email: achar@doe.carleton.ca;
Ph: 613-520-2600, Ext: 5651; Fax: 613-520-5708

IEEE Electronics Packaging Society
Distinguished Lecture

This Presentation is supported by the IEEE Electronics Packaging Society's Distinguished Lecturer Program

eps.ieee.org

IEEE

IEEE at a Glance

Our Global Reach

400,000+
Members

46
Technical Societies and Councils

160+
Countries

Our Technical Breadth

1,800+
Annual Conferences

5,000,000+
Technical Documents

200+
Top-cited Periodicals

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

Electronics Packaging Society

A Global Society with…

…Chapters, members, constituents spanning the world

38 Chapters located in US, Asia/Pacific, Europe

12 Technical Committees

2200+ members worldwide

650k Trans/Conf Downloads/yr

4500 attendees at 25 Conferences/Workshops

Packaging Field + 6 EPS Awards + PhD Fellowship

Peer Reviewed Transactions

IEEE

EPS Local Chapters

Bangalore
Beijing
Benelux
Bulgaria
Canada (4)
France
Germany
Hong Kong
Hungary/Romania
Israel
Korea
Japan
Malaysia
Nordic
(Sweden, Denmark, Finland, Norway, Estonia, Iceland)
Poland
Russia
Shanghai
Singapore
Switzerland
Taipei
Ukraine (2)
United Kingdom & Republic of Ireland
United States (12)

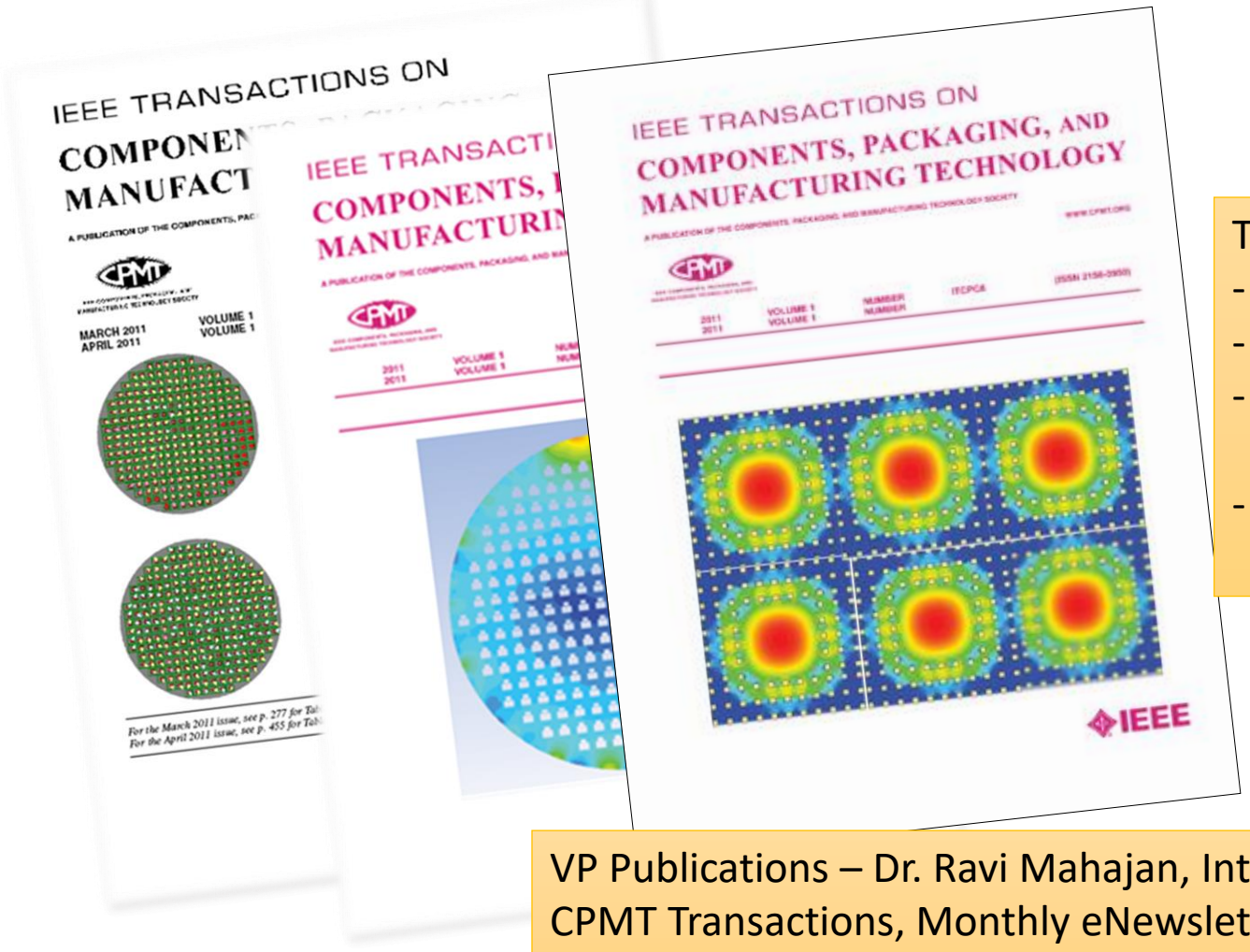
IEEE

EPS Technical Committees

- **Materials & Processes**
  - Chair: Bing Dang
- **High Density Substrates & Boards**
  - Chair: Yasumitsu Orii
- **Electrical Design, Modeling & Simulation**
  - Chair: Stefano Grivet-Talocia
- **Thermal & Mechanical**
  - Chair: Ankur Jain
- **Emerging Technology**
  - Chair: Benson Chan
- **Nanotechnology**
  - Chairs: Americas: Raj M. Pulugurtha, Europe: Attila Bonyar, Asia: Jian Cai
- **Power & Energy**
  - Chair: Patrick McCluskey
- **RF & Thz Technologies**
  - Chair: Manos Tentzeris,
- **Photonics - Communication, Sensing, Lighting**
  - Chair: Gnyaneshwar Ramakrishna
- **3D/TSV**
  - Chair: Peter Ramm
- **Reliability**
  - Chair: Przemek Gromala
- **Test**
  - Chair: Pooya Tadayon

IEEE

Peer-Reviewed Technical Publication



Transactions on CPMT
- 595 submissions (2020)
- 240 papers published
- Impact Factor: ~ 1.7 (2020)
- Xplore Usage: 40,000+

VP Publications – Dr. Ravi Mahajan, Intel
CPMT Transactions, Monthly eNewsletter, and Bi-Annual printed Newsletter

IEEE

Technical Program (data as of last year)		
	Average	**Electronics Packaging**
# of PDFs Published	8,469	6,822
# of Events	76	74
# of Articles Viewed (Downloads)	1,666,555	1,395,158
PDFs/Conference	112	92
Downloads/PDF	197	204
Avg OU Package Net	1.5%	1.3%

Financial Sponsor

- ECTC
- EDAPS
- HOLM
- ICSJ
- ITherm
- SPI
- 3DIC

Co Sponsor

- EPEPS
- EPTC
- ESTC
- IEMT
- EMAP
- IWASI
- IWIPP

Technical Sponsor

- ASMC
- DTIP
- EDPS
- EMPC
- EOS/ESD
- EuroSimE
- ICEPT
- 3D-PEIM

- IMPACT
- ISSE
- MID
- NordPac
- Pan Pacific
- SEMI THERM
- THERMINIC

IEEE

EPS Awards & Recognition

IEEE Electronics Packaging Award

(IEEE Technical Field Award)

Outstanding Sustained Technical Contribution Award

Electronics Manufacturing Technology

David Feldman Outstanding Contribution

Exceptional Technical Achievement

Outstanding Young Engineer

Transactions Best Papers

Regional Contributions

PhD Fellowship

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

Carleton University – Canada's Capital University

Research @ CAD Group in Carleton

- High-Speed Interconnects,
- Signal & Power Integrity
- Circuit Simulation
- Timing Analysis
- Model-Order Reduction Algorithms
- Variational Analysis
- Optimization
- Mixed Digital, Analog, EM, RF Analysis
- Parallel Algorithms
- Neural Networks
- ……

Design Trends

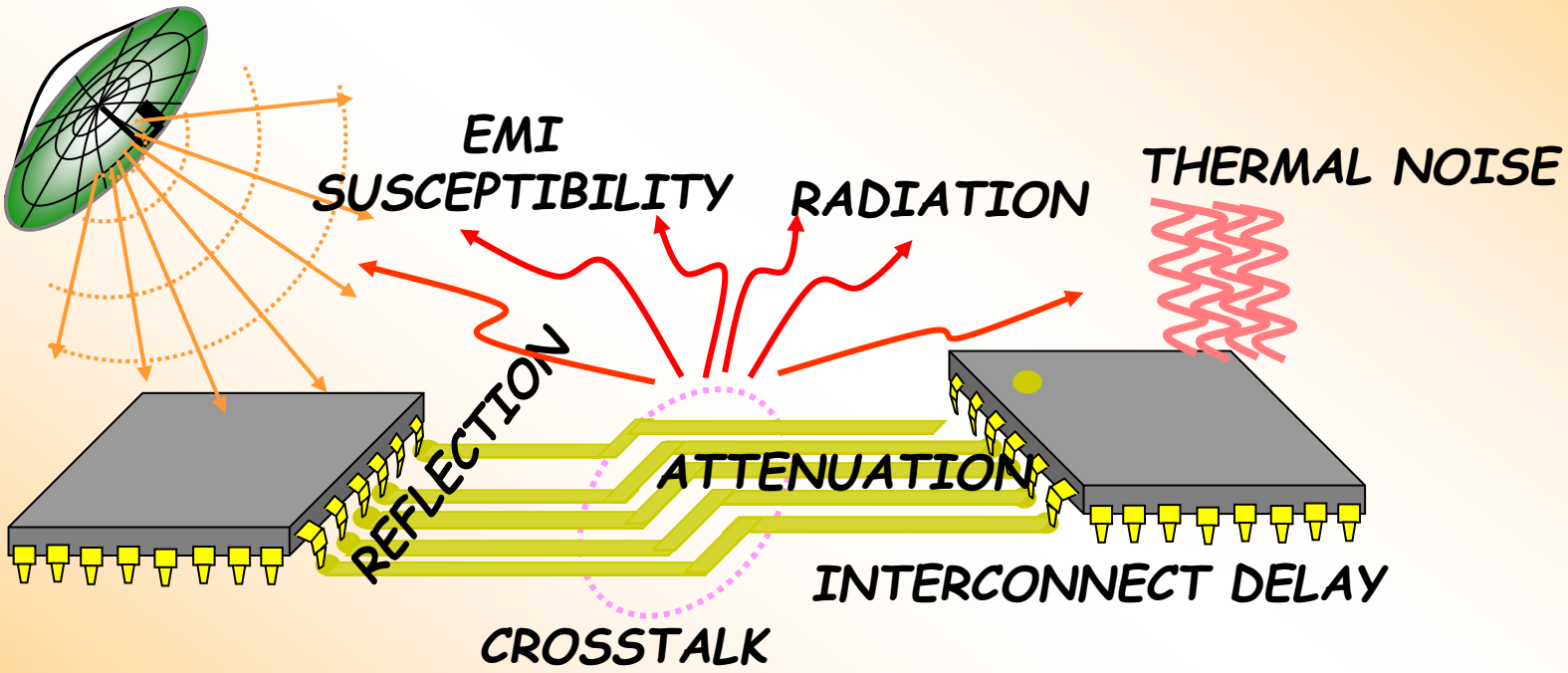
- Faster Devices
- Compact Products
- Multi-Function
- Less Clutter
- Use Less Power

- High-Frequency
- High-Density
- Wireless
- Low-Power

Agenda

- Emerging Product Trends
- Interconnect Scaling
- Signal Integrity Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

High-Speed Design Issues



Impact of Signal Integrity Issues

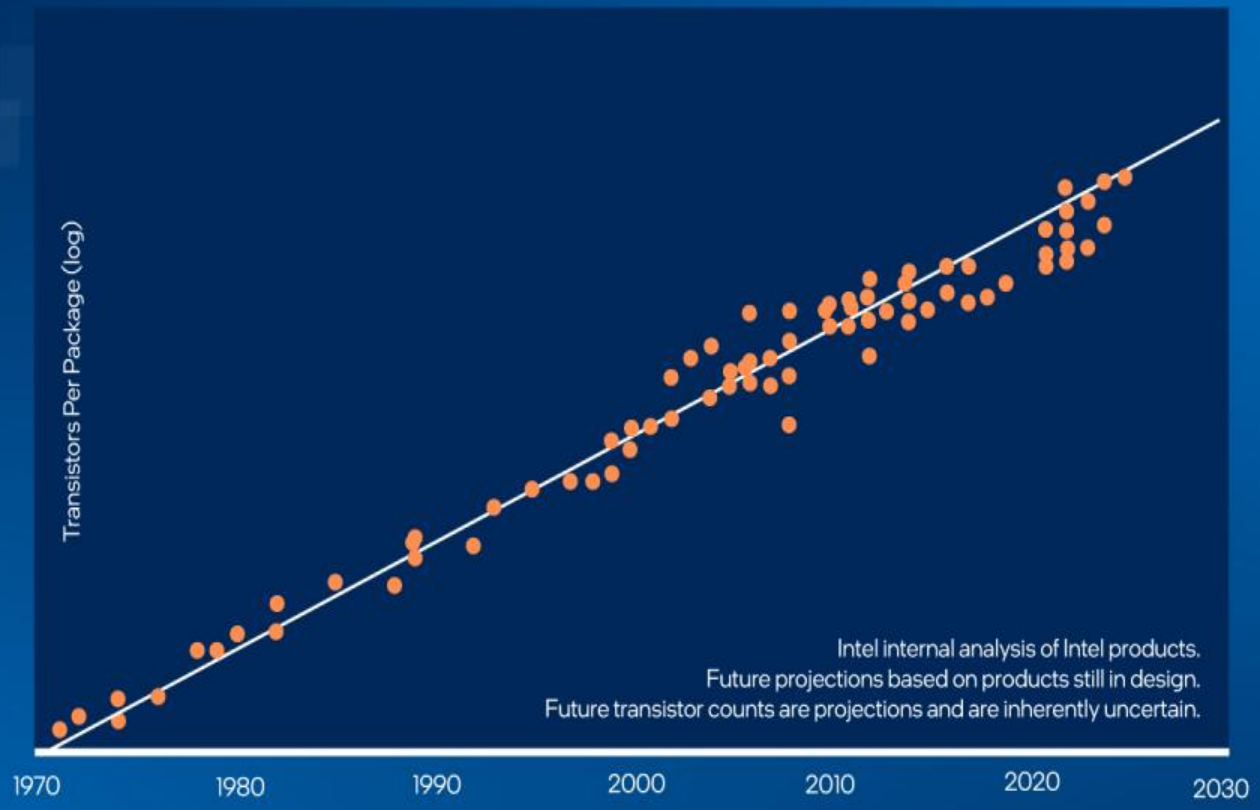
Current Design Trends + **High-Speed Effects**

Design **Modeling** **Simulation** **Optimization**

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

Moore's Law on Density/Speed



Aspiring to

1 Trillion

transistors in 2030

- ✓ RibbonFET
- ✓ PowerVia
- ✓ High NA
- ✓ 2.5D/3D packaging

Source: Intel, www.intel.com

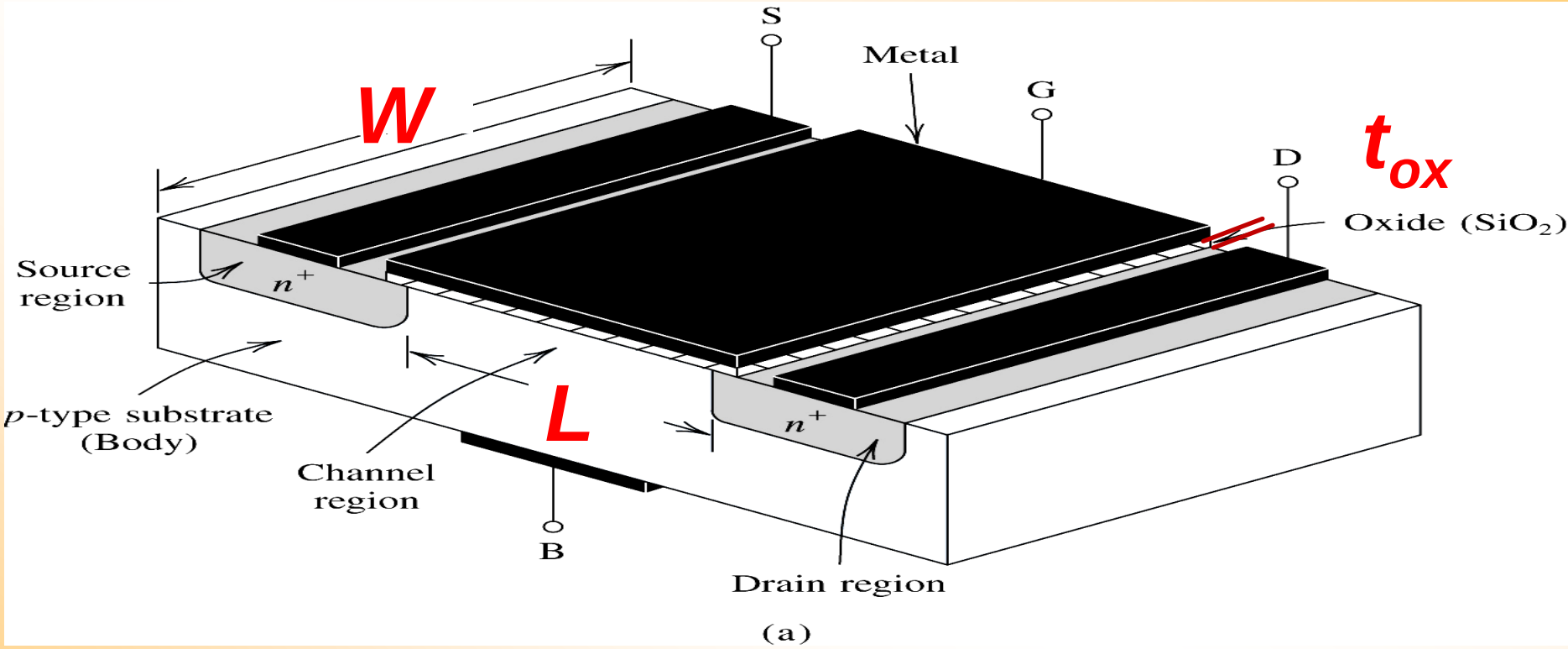
intel.

Evolution of Density and Frequency

In a Billion Transistor Design, there could be multiple billions of interconnects, many of which do not scale in performance

➔ High-Speed Signal Propagation Issues

Transistor, Interconnect – Scaling & SI Issues



Technology Scaling:

➔ Scale W, L & t_{ox} by a factor of 'S'

Transistor, Interconnect – Scaling & SI Issues

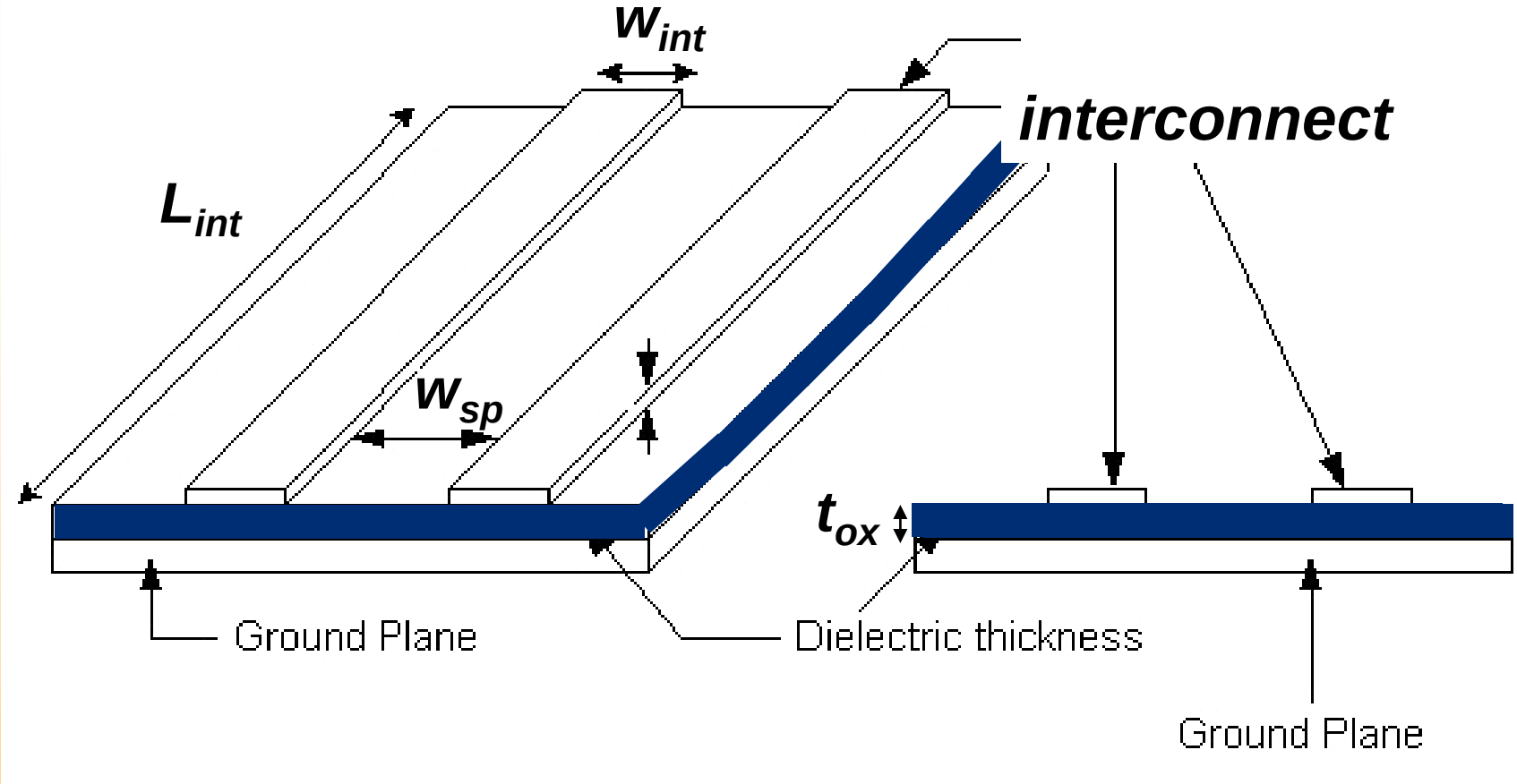
Parameter	*Relation*	*Scaling Factor*
Dimensions	W, L, t_{ox}	1/S
Voltages	V_{DD}, V_T	1/S
Currents	I_{DS}	1/S
Power Dissipation/Gate	P = IV	$1/S^2$
Area Per Device	A = WxL	$1/S^2$
Power Dissipation Density	P/A	1

Transistor - Ideal Scaling

Impact on Transistor Related Delays

Parameter	Relation	Scaling Factor
Gate Capacitance	$C_g = (\varepsilon_{ox}/t_{ox})(W \times L)$	1/S
Transistor On Resistance	$R_{tr} = V_{DD} / I_{DS}$	1
Intrinsic Gate Delay	$T_g = R_{tr} C_g$	1/S

A look at Interconnects…..



Scaling: Local Interconnections

Parameter	*Relation*	*Scaling Factor*
Cross-sectional Dimensions	W_{int}, H_{int}, W_{sp}, T_{int}	1/S
Capacitance Per Unit Length	C_{int} α $(\varepsilon_{ox})(W_{int}/t_{ox})$	1
Resistance Per Unit Length	$R_{int} = \zeta_{int} / (W_{int} \times H_{int})$	S^2
RC Time Constant per unit Length	$R_{int} \times C_{int}$	S^2
Local Interconnection Length	L_{int}	1/S
Total Local Interconnection RC Delay	$T= (R_{int} C_{int}) L^2_{int}$	1

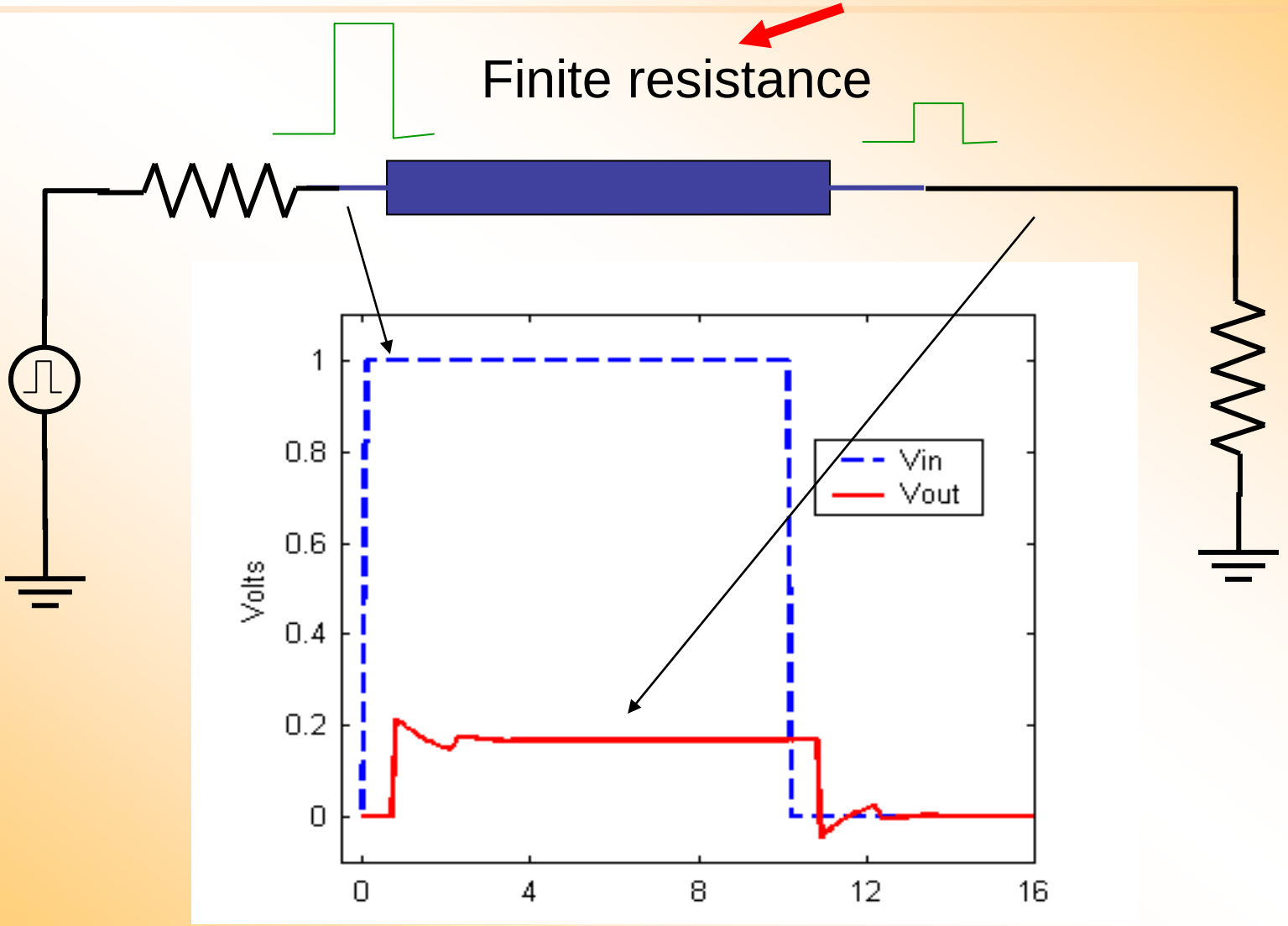
Scaling: Global Interconnections

Parameter	*Relation*	*Scaling Factor*
Die Size		S_c
Global Interconnection Length	L_{glob}	S_c
Global Interconnections RC Delay	$T = (R_{int} C_{int}) L^2_{glob}$	$S^2 S^2_c$

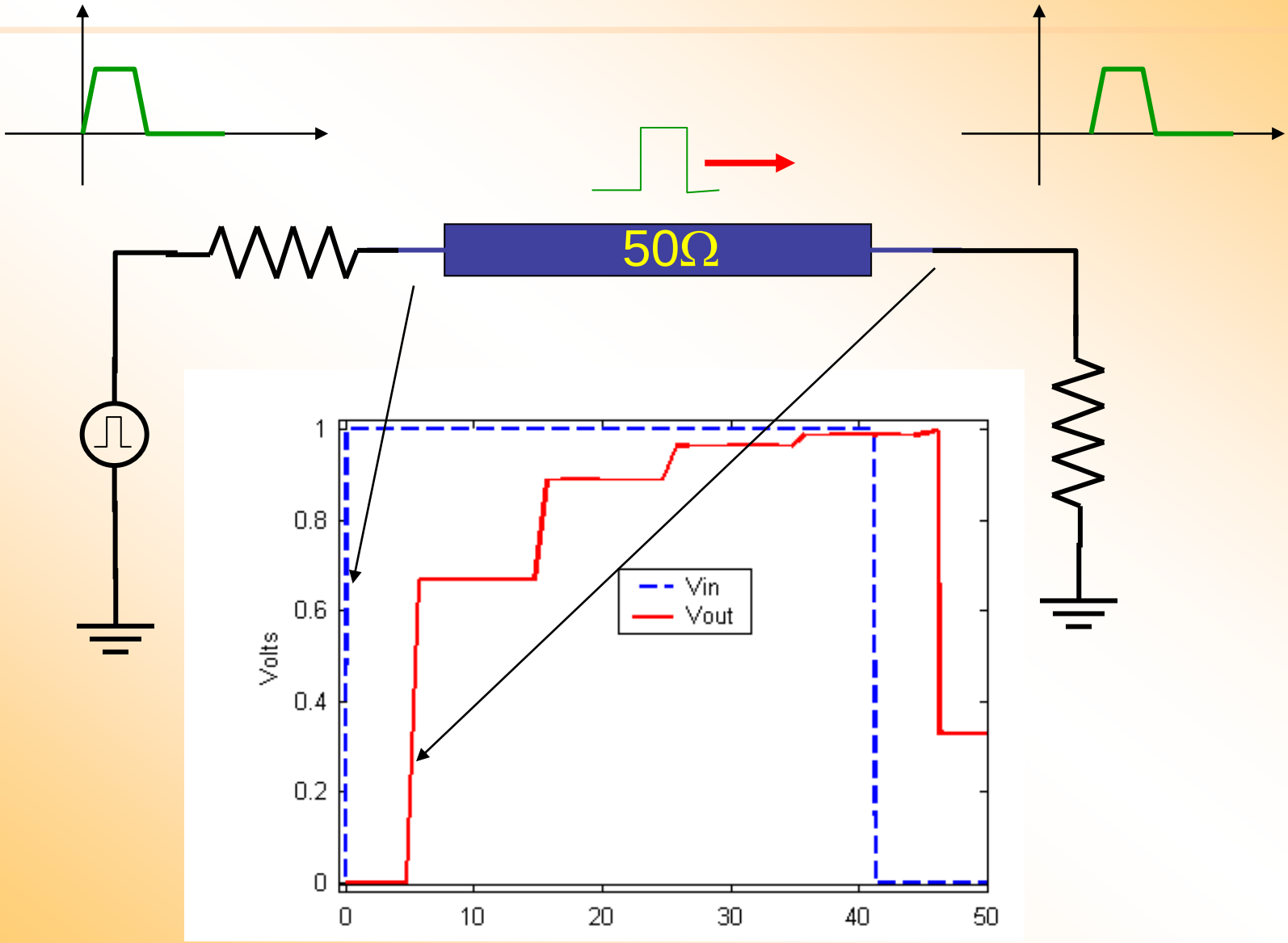
Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

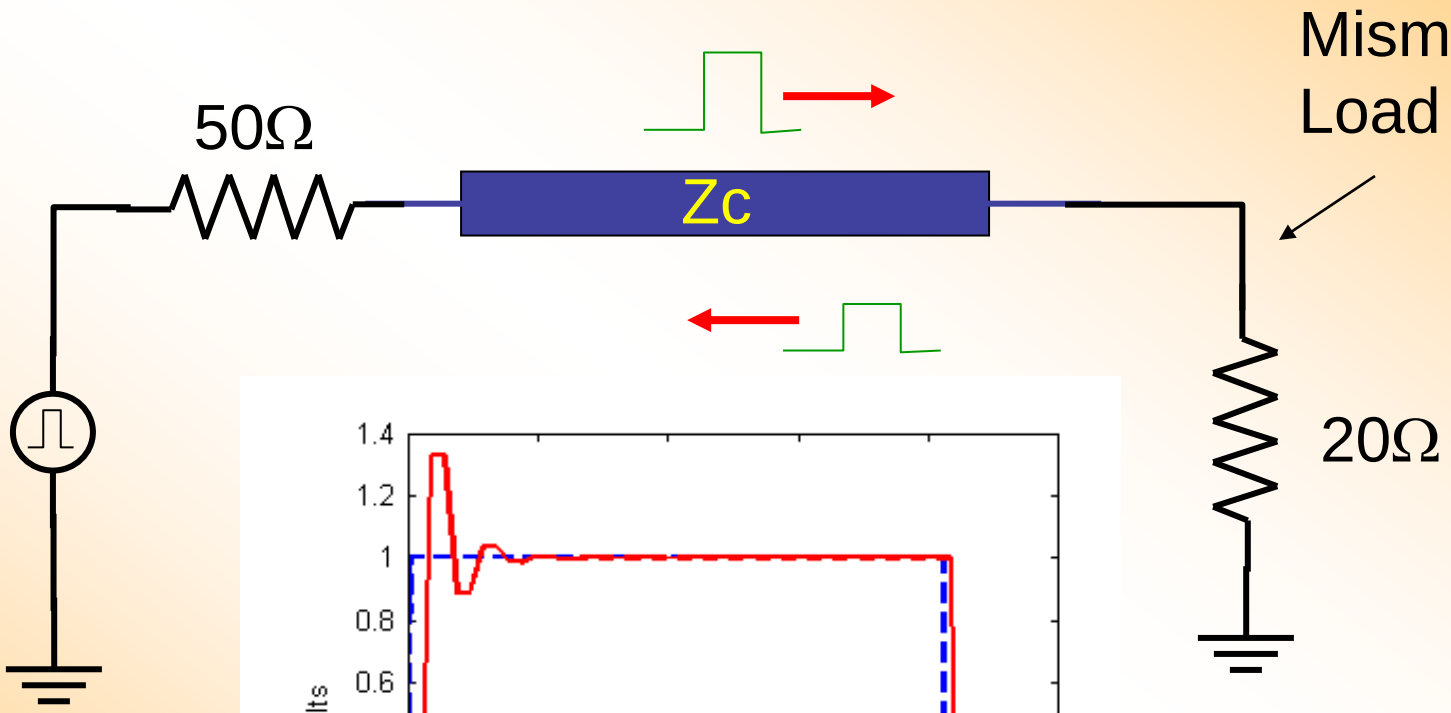
Attenuation

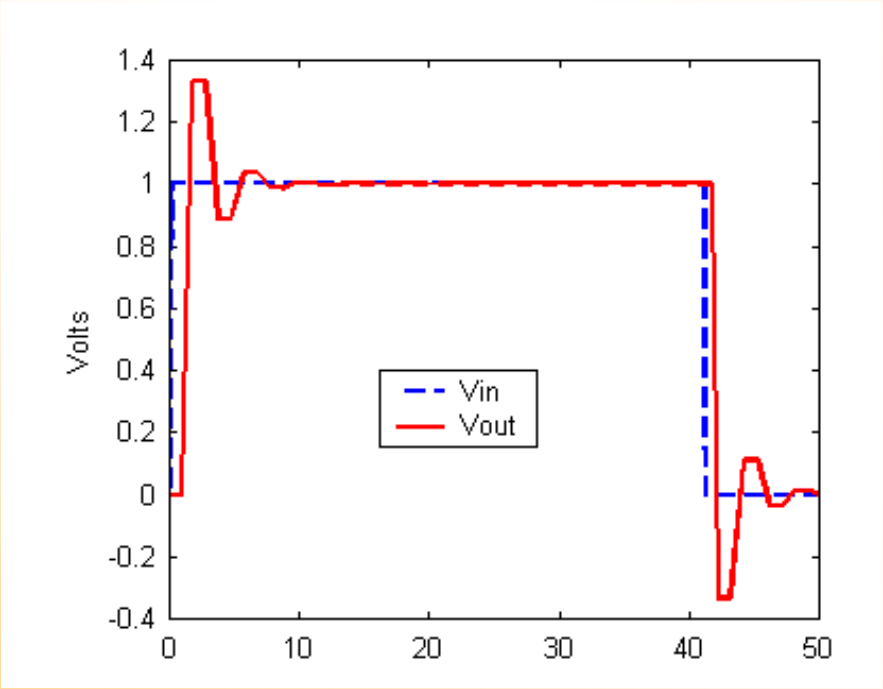


Interconnect Effects: Delay

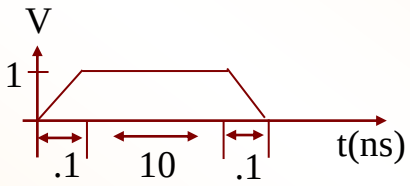


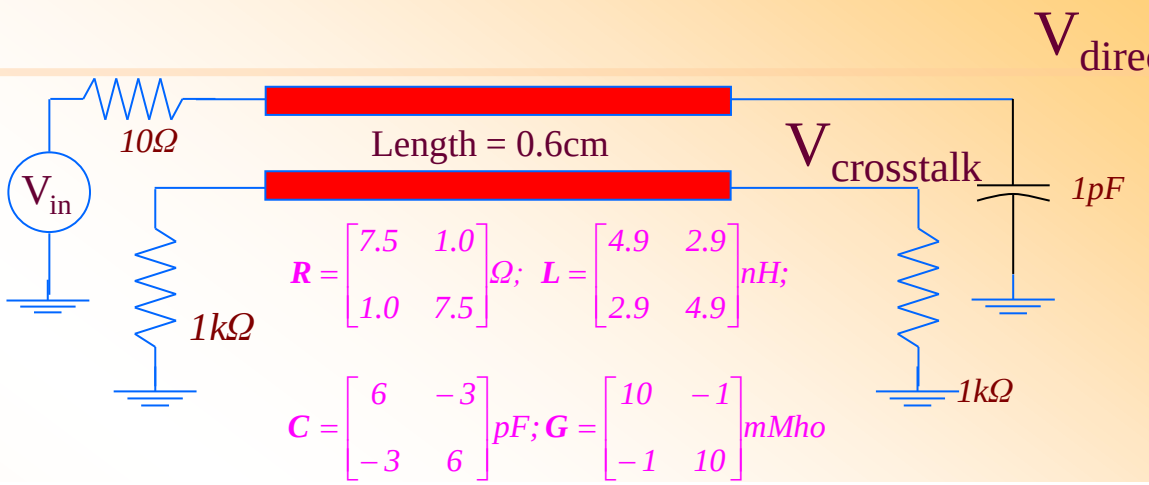
Reflection/Ringing

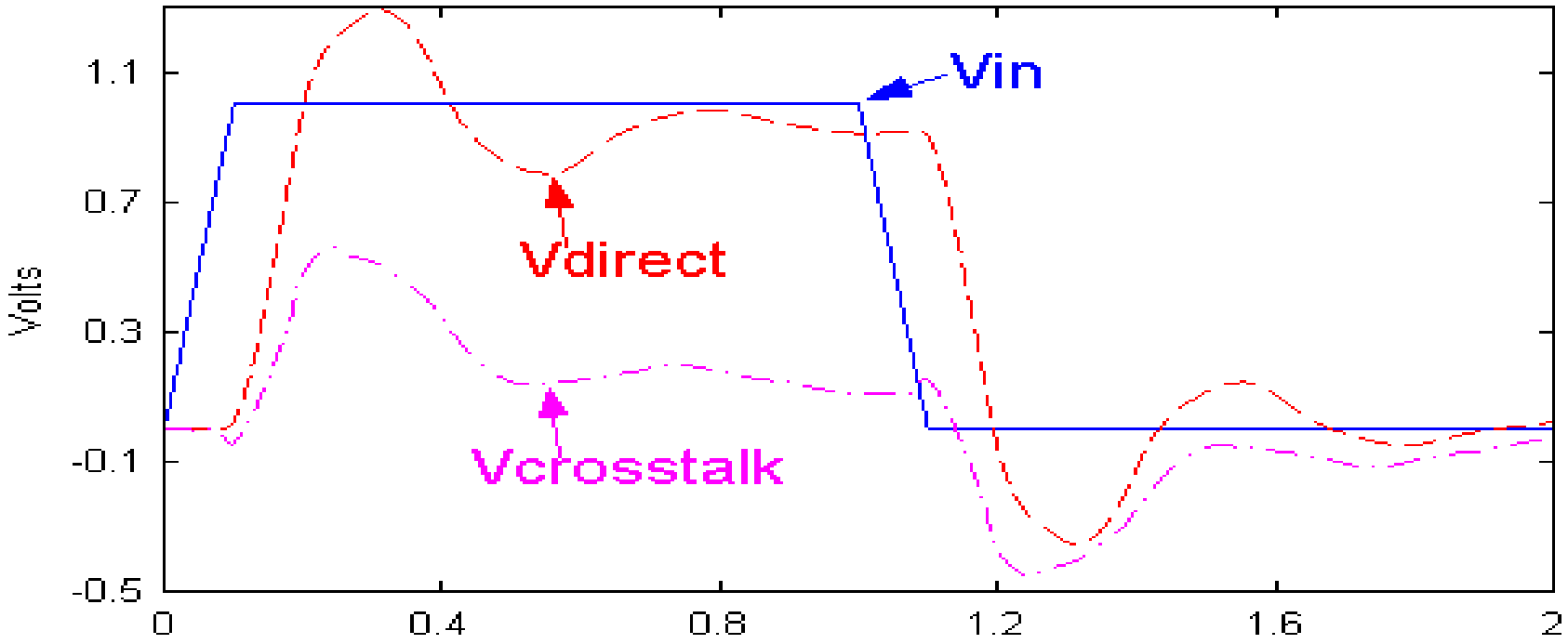




Crosstalk


V
1
.1
10
.1
t(ns)

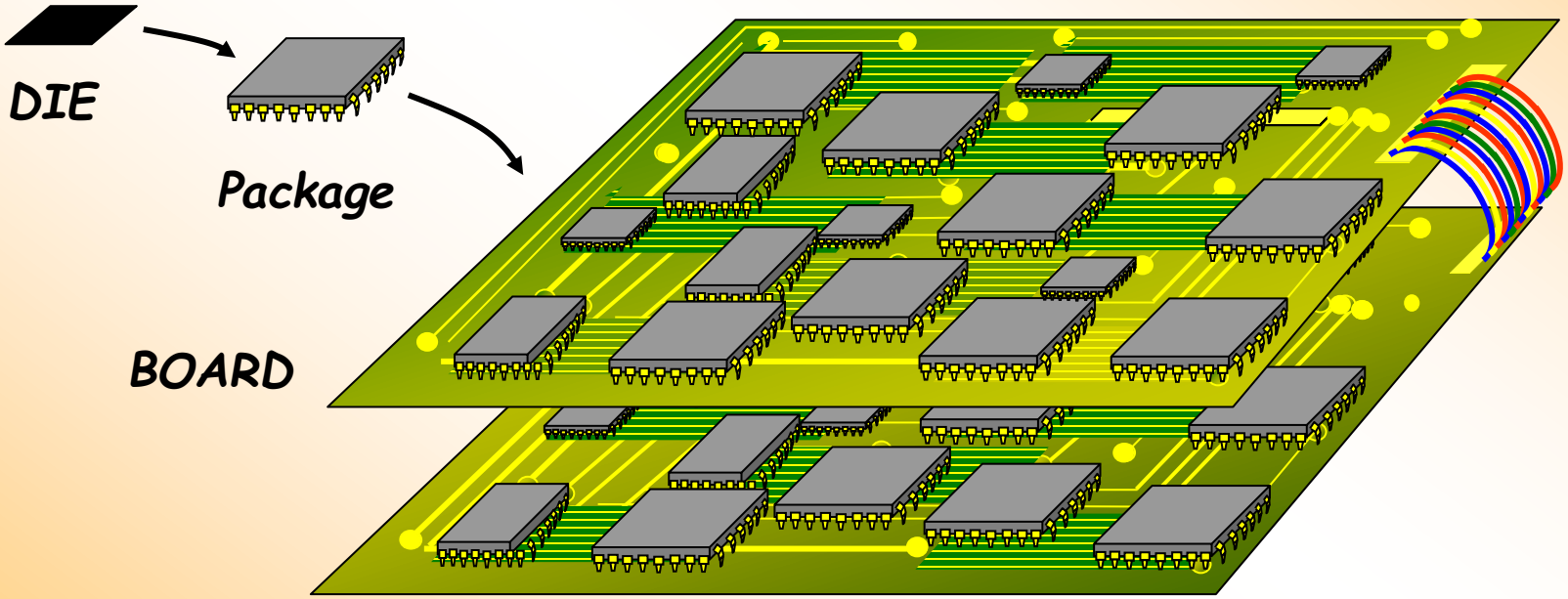

V direct
10Ω
Length = 0.6cm
V crosstalk
1pF
V in
1kΩ
1kΩ
R = [7.5 1.0; 1.0 7.5] Ω; L = [4.9 2.9; 2.9 4.9] nH;
C = [6 −3; −3 6] pF; G = [10 −1; −1 10] mMho


Vin
Vdirect
Vcrosstalk
Volts
1.1
0.7
0.3
-0.1
-0.5
0
0.4
0.8
1.2
1.6
2

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

Ubiquitous Interconnects



Role of the Package

- ***Distribute power and signals,***
- ***Dissipate the heat generated by the IC.***
- ***Mechanical support for the chip,***

Issues to tackle, parasitic elements such as:

- ***capacitive coupling between connections or leads,***
- ***inductance of the connections or leads,***
- ***resistance of the connections***

➔ ***The values of the parasitic elements depend on the package layout and structure,***

➔ ***Have Significant Impact on the Package Performance.***

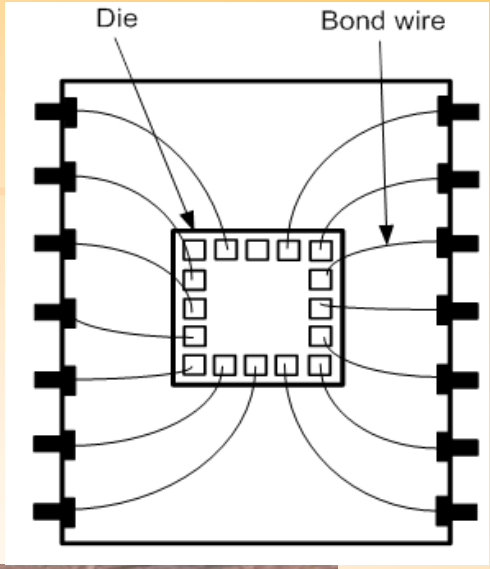
Role of the Package

- ***The design and construction of packages vary significantly, but most of them are fabricated either from plastic or ceramic materials.***

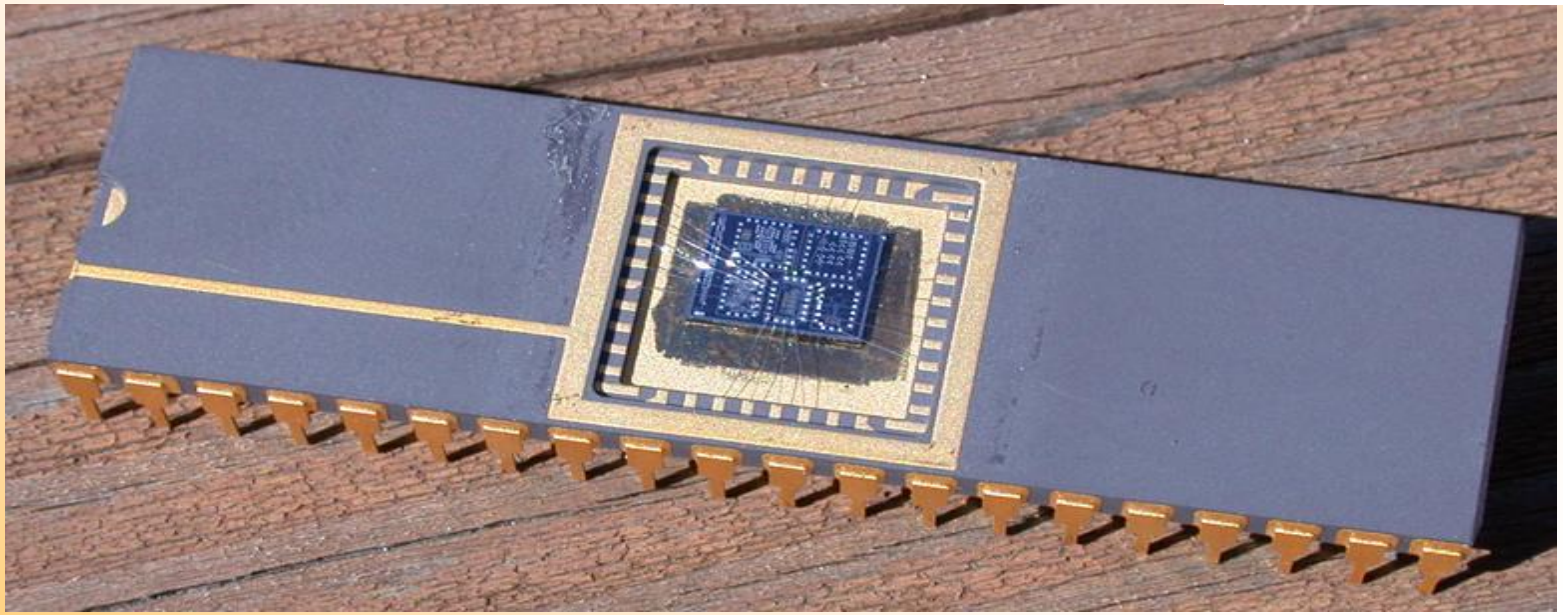
- ***The chip to package interconnects can be divided into three main categories:***

  Wire-bond (WB)
  Tape-automated-bond (TAB)
  Flip-chip

Package – Wire Bond

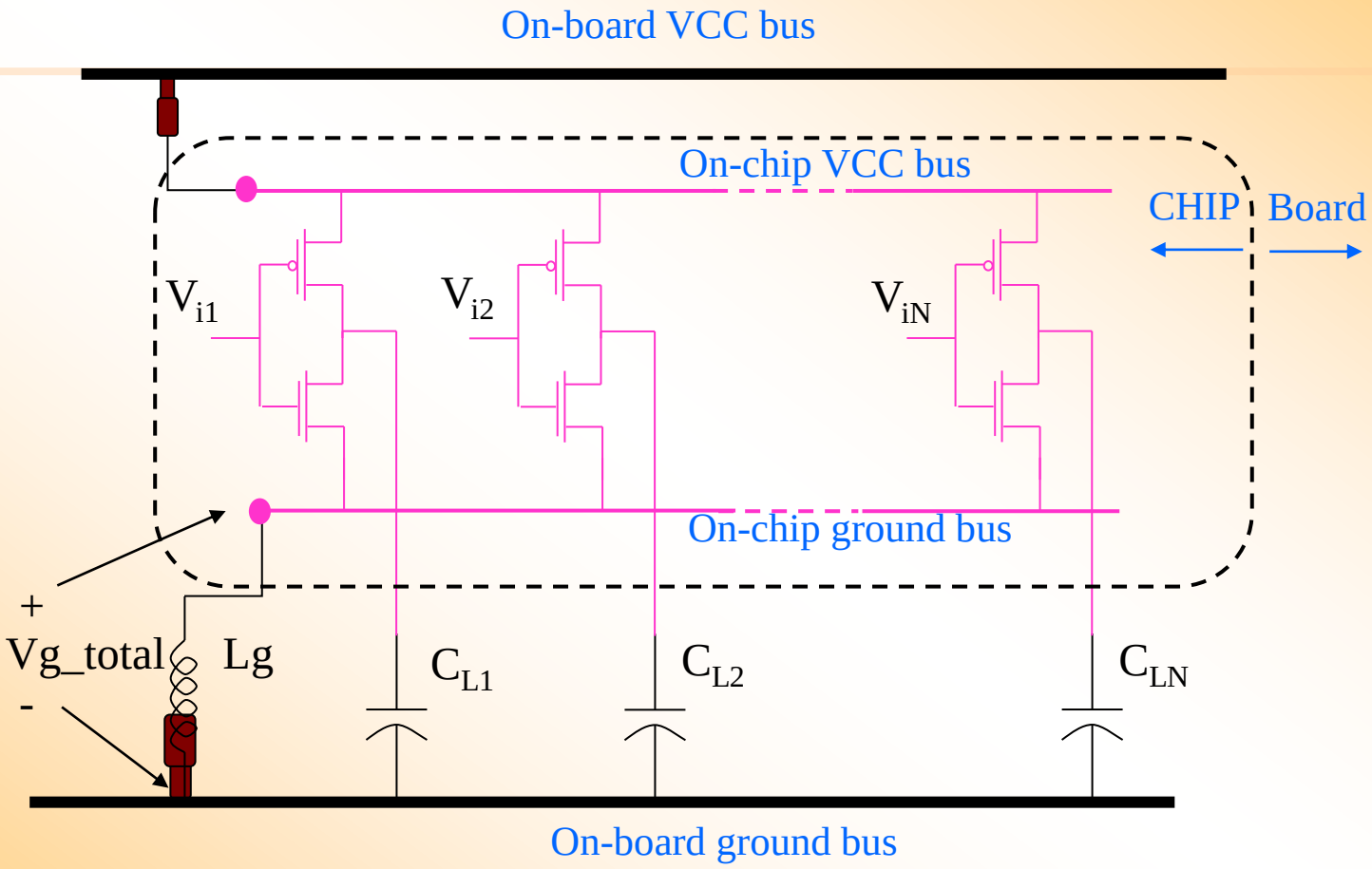


Wire-bond (WB): Although the oldest method, wire-bonding is still the dominant packaging method used today.



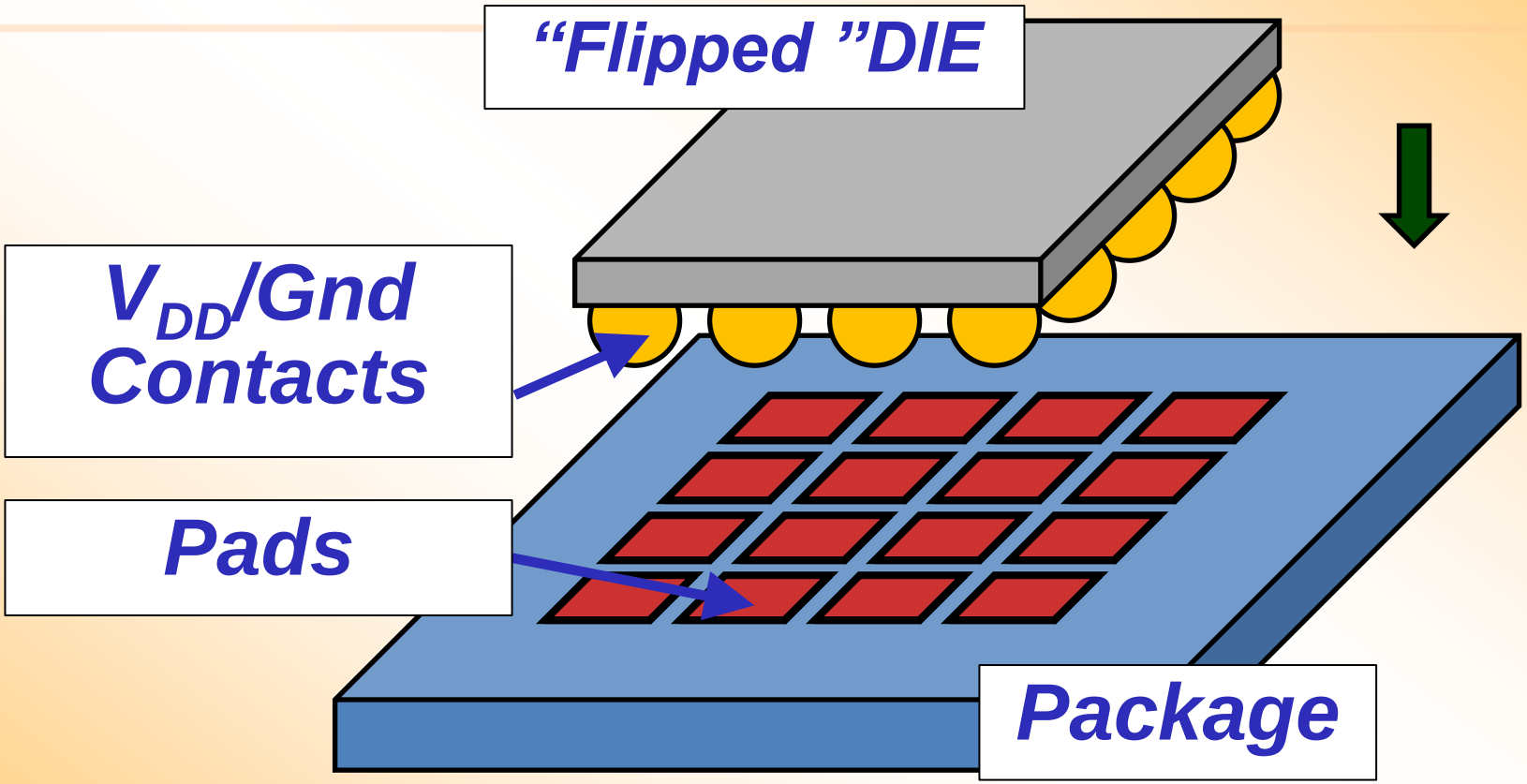
➔ ***Due to the self-inductance and mutual inductance of the wires, noise on the PDN and crosstalk between adjacent signals might occur.***

Ground Bounce



$$V_g = L_g \times \frac{d\,[i_{discharge}(t)\_total]}{dt}$$

Flip Chip Technology



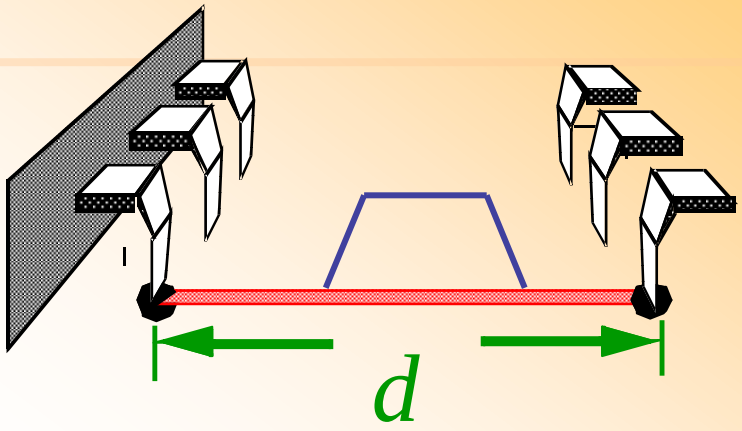
-*Uniform Distribution of Power*
-*Shorter contacts: reduced Parasitics*
-*More Widely used*

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

High-Speed!!

What is it??

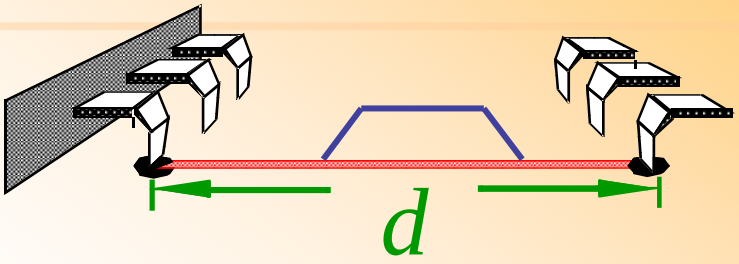


- **Time taken to travel through the interconnect can no longer be neglected!!**
- **Interconnects can no more be treated as electrically short (→ $d \leq \lambda/10$)**
- **Need to start worrying about high-frequency effects when:**

  $d \geq \lambda/10$ → Electrically Long Interconnects

What is a High-Speed Interconnect?

When??
for digital systems….



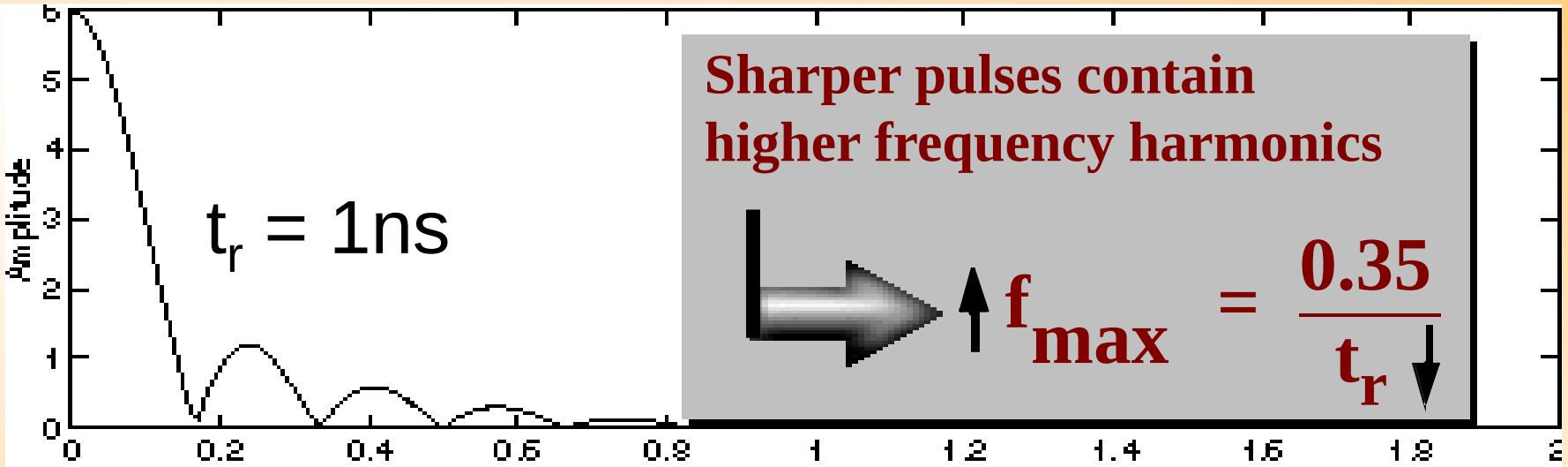
At higher frequencies,
Interconnect length becomes
comparable to the Wavelength

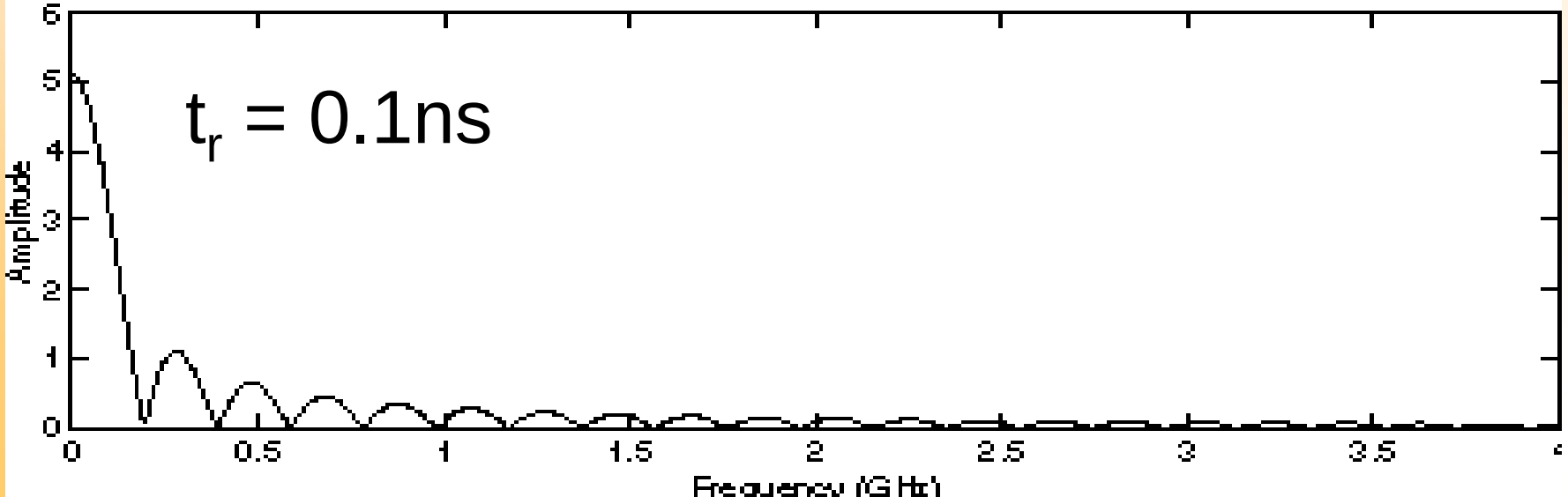
$$\downarrow \lambda = \frac{v}{f \uparrow}$$

Frequency = 1GHz ➔ $\lambda \approx \frac{v}{f} = \frac{1.5\times10^{10}}{1\times10^{9}} = 15\text{cm}$

➔ d > 1.5cm

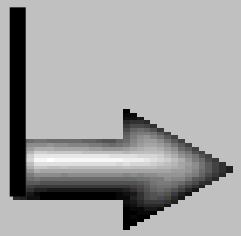
Time-Freq Relations





What is an High-Speed Interconnect?

Sharper pulses contain higher frequency harmonics



$$f_{max} = \frac{0.35}{t_r}$$

$t_r = 0.1ns$ → $f_{max} = 3.5GHz$ →

$$\lambda \approx \frac{v}{f} = \frac{1.5\times10^{10}}{3.5\times10^{9}} \approx 4cm$$

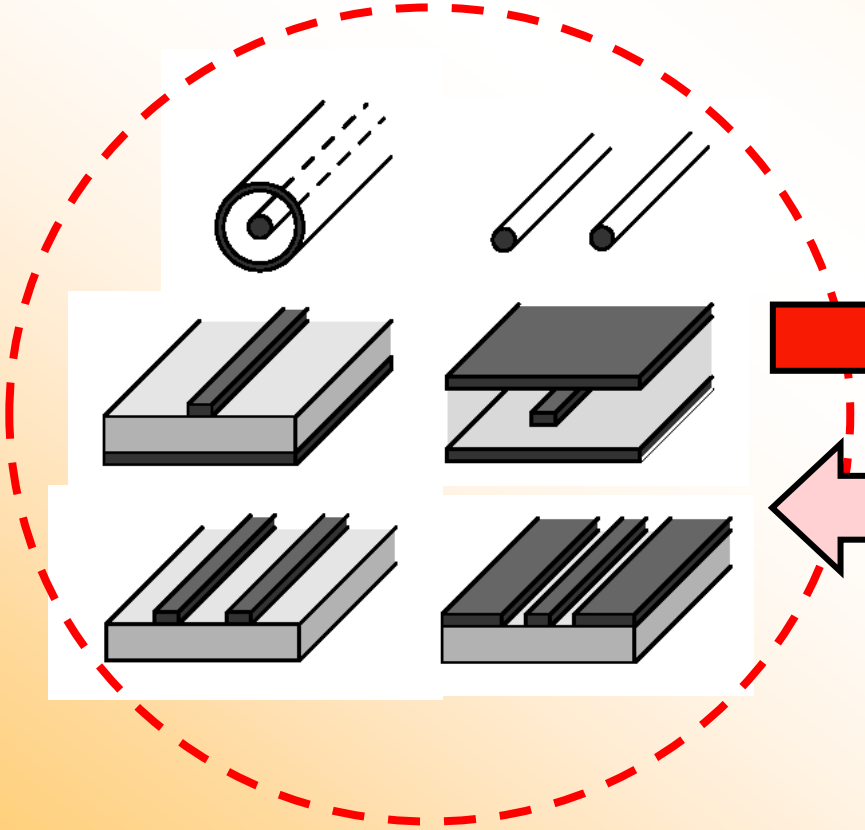
→ d < 4mm

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

Modeling of Interconnects

Physical Description



Electrical Description

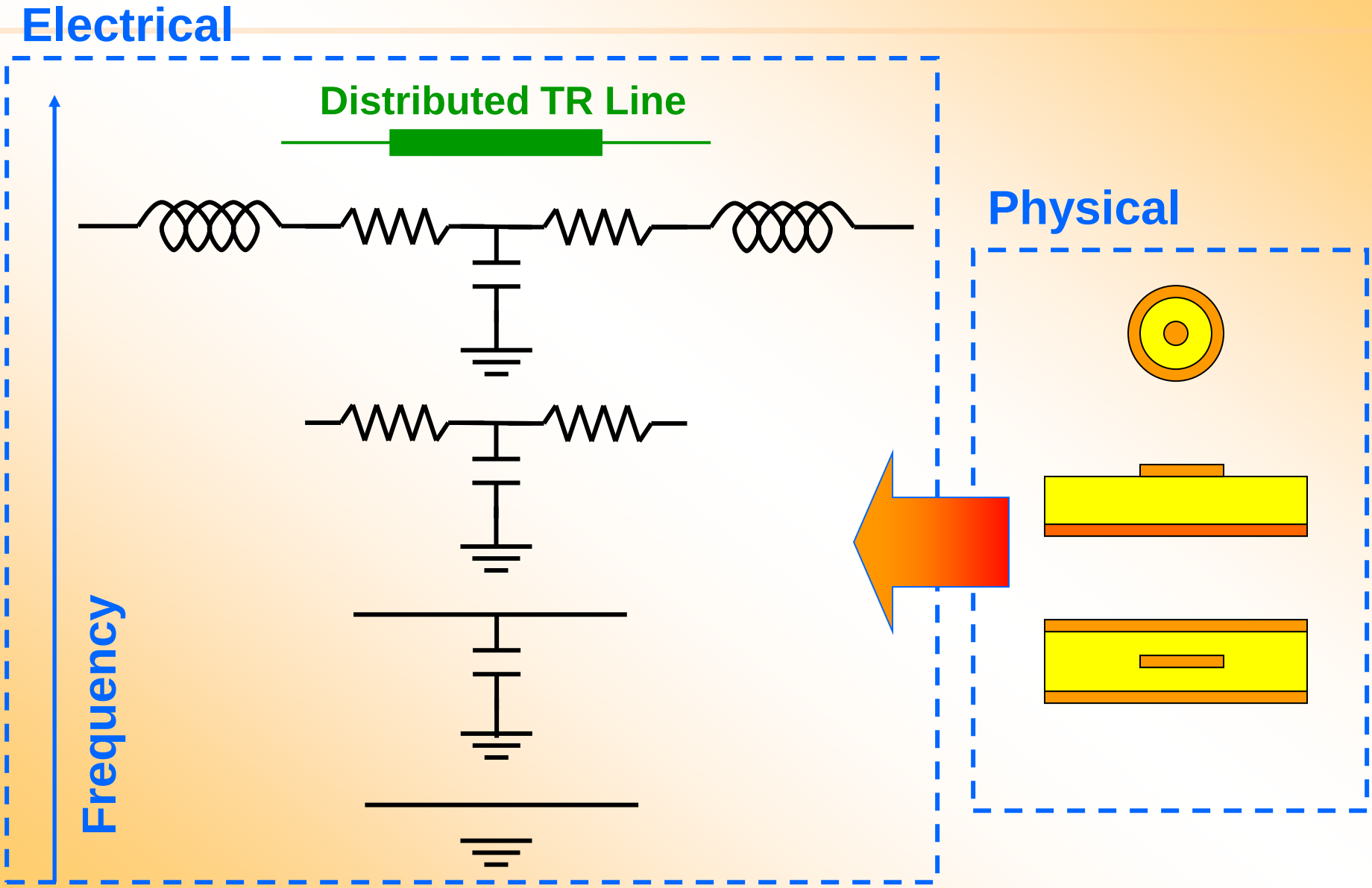
L C
R G

Distributed effects?

Freq-depend. effects?

Models ?

Interconnect Models



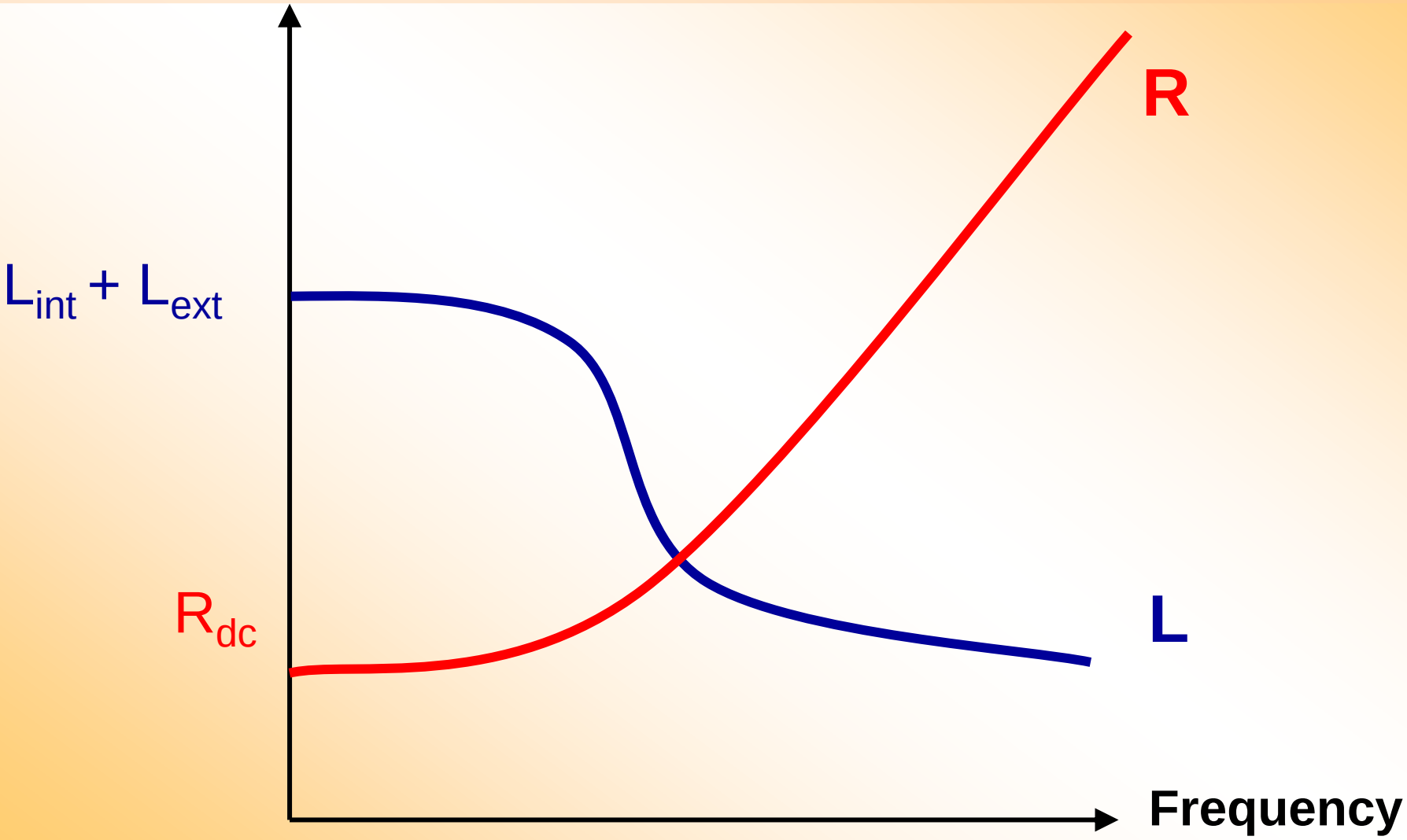
Distributed Transmission Lines

- **Distributed Transmission Lines**
  - ➔ **Lossless, Lossy**
  - ➔ **Single, Multiconductor**
  - ➔ **Frequency Independent/ dependent**
    p.u.l. parameters
    (skin/proximity/edge effects)
  - ➔ **Uniform/Non-uniform**

- **Current Distribution Related Effects:**
  - ➔ **Skin Effect**
  - ➔ **Edge Effect**
  - ➔**Proximity Effect**

- **Surface Roughness Effects**

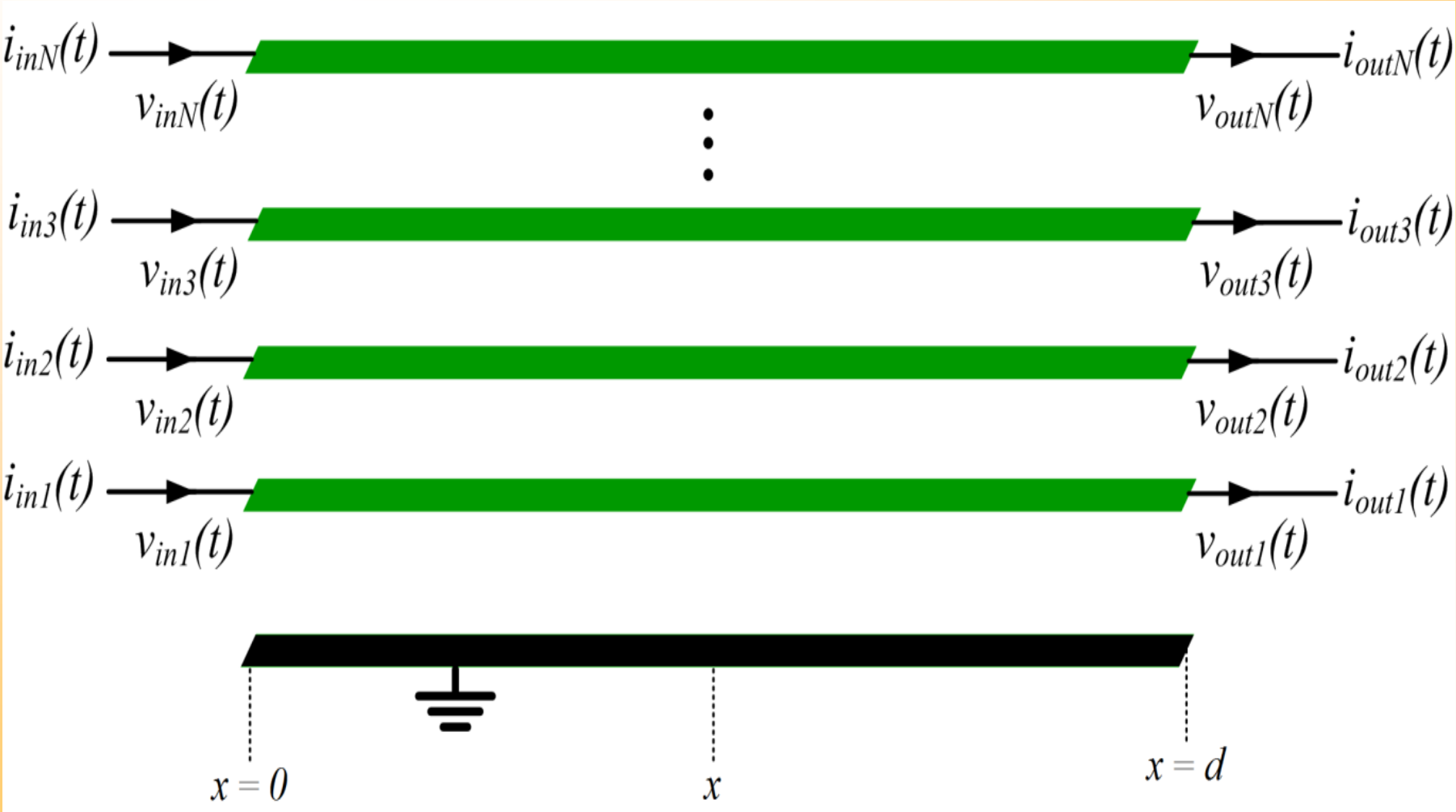
Frequency Dependence of *R & L* Parameters



Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
- Conclusions

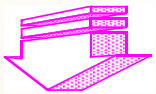
Multi-Conductor Transmission Lines



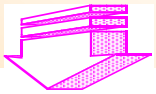
Transient Analysis

Mixed Frequency/Time Simulation

SPICE



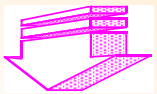
Nonlinear Simulator



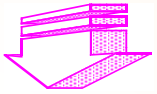
$$W\frac{\partial x}{\partial t}+Hx+F(x)=b(t)$$

Time Domain Equations

H-S Interconnect



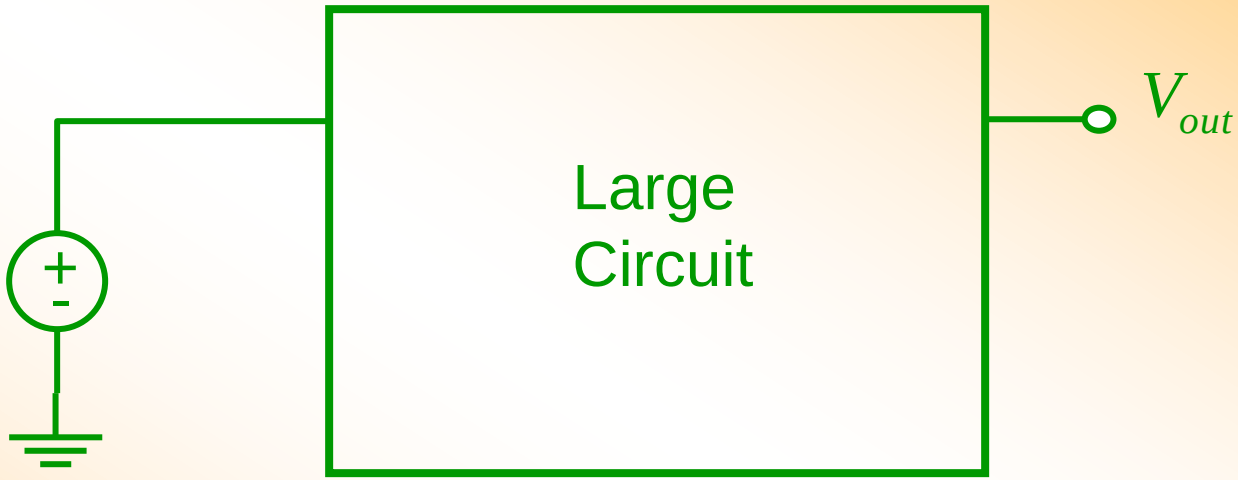
Telegrapher's Equation



$$A(s)\,V+B(s)\,I=0$$

Freq-Domain Equations

Lumped Segmentation - Large Circuit



Large CPU Cost

Transient Simulation Issues

- Mixed Frequency/Time
- Complexity
- CPU time
- Memory
- Simulator Interface

MACROMODELING

$$\frac{\partial}{\partial z}V(z,t) = -R\,I(z,t) - L\frac{\partial}{\partial t}I(z,t)$$

$$\frac{\partial}{\partial z}I(z,t) = -G\,V(z,t) - C\frac{\partial}{\partial t}V(z,t)$$

Macromodeling

$$\frac{d}{dt}x = Ax + Bu$$

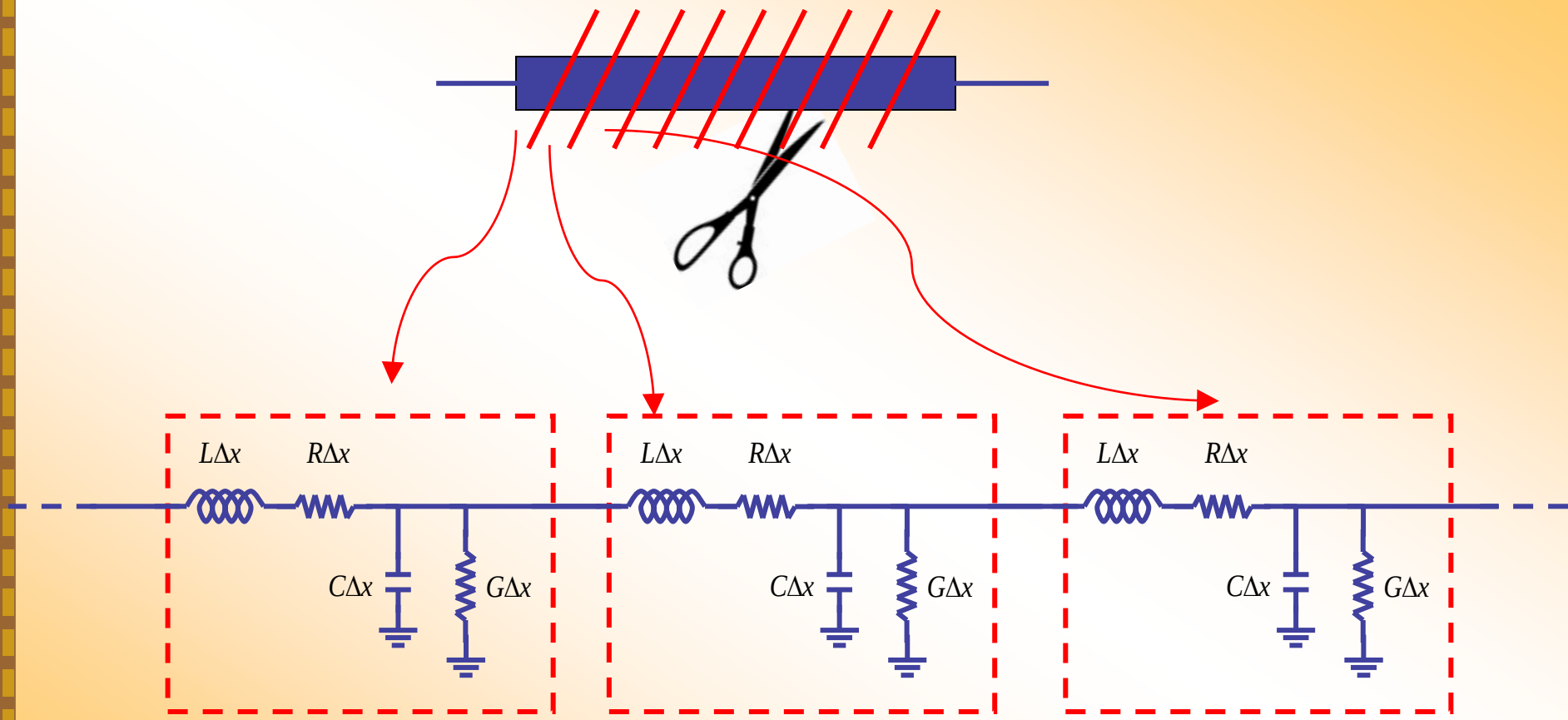
$$y = Cx$$

Circuit Simulators

Macromodeling

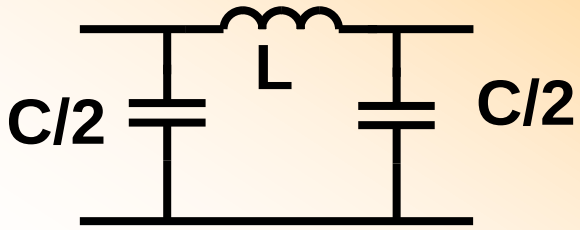
- Lumped Segmentation
- Method of Characteristics
- Least-Square Optimization
- Chebeshev, Wavelet Polynomials
- Compact Finite Differences
- Integrated Congruent Transformation
- Matrix Rational Approximation
- Model-Order Reduction Methods….

Discretization

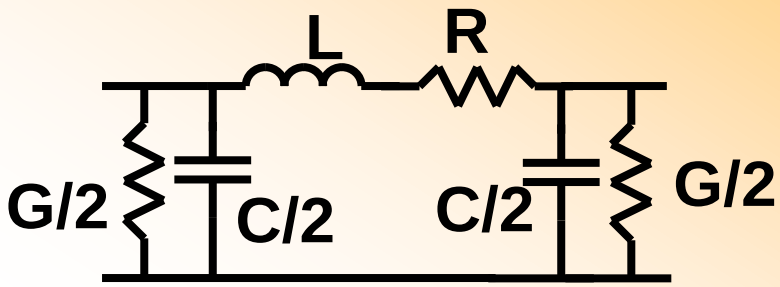


Lumped Models - Pi

Lumped LC Lossless Line

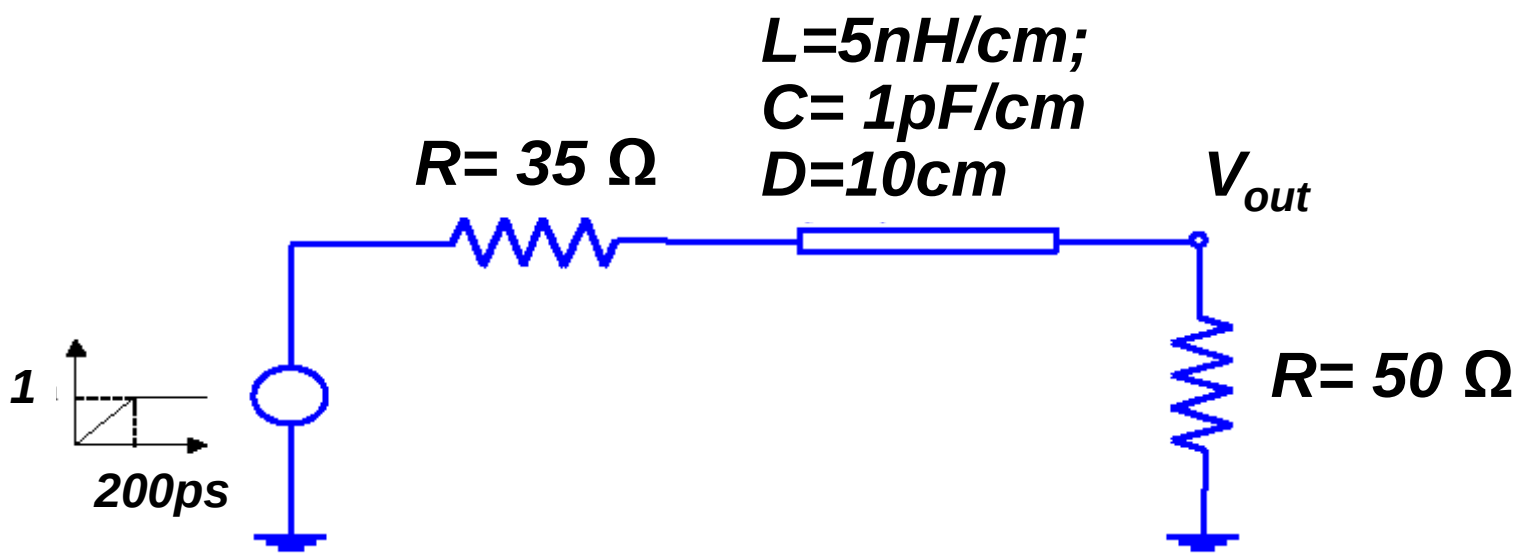


Lumped RLGC Lossy Line



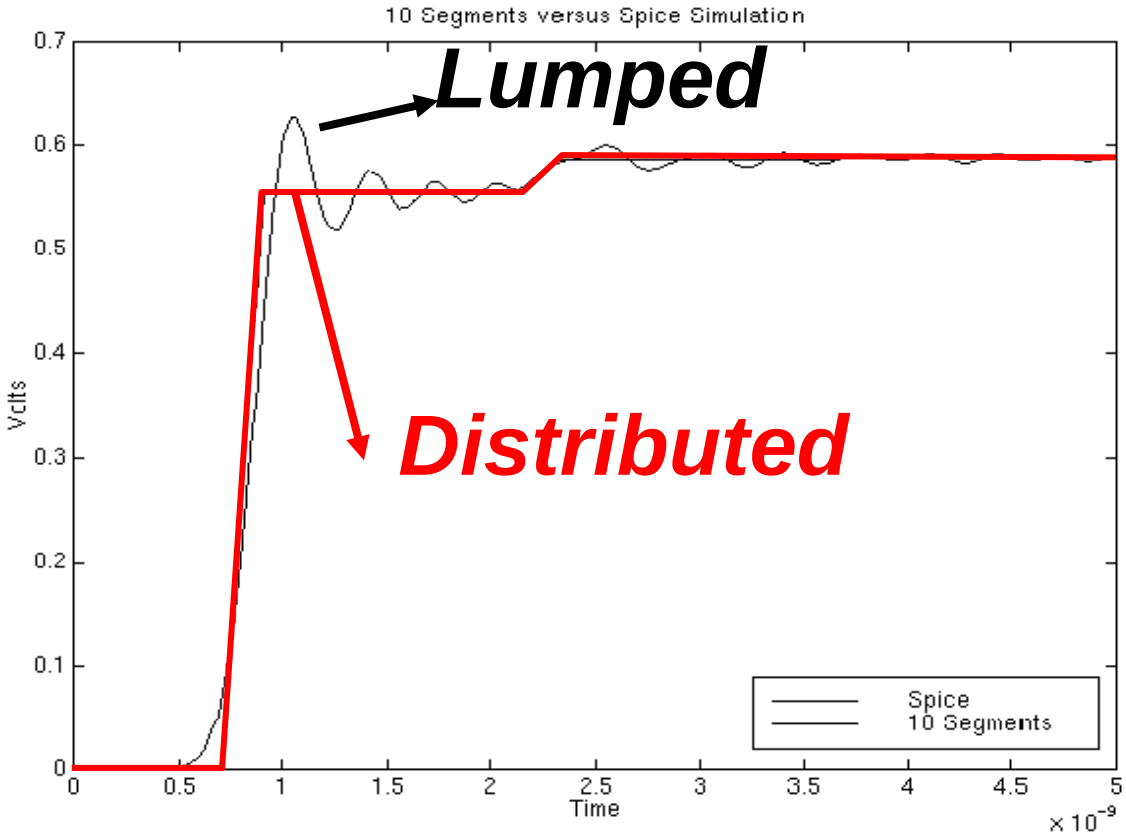
Lumped Cascaded Lossless Distributed Line

Lumped Segmentation: Example



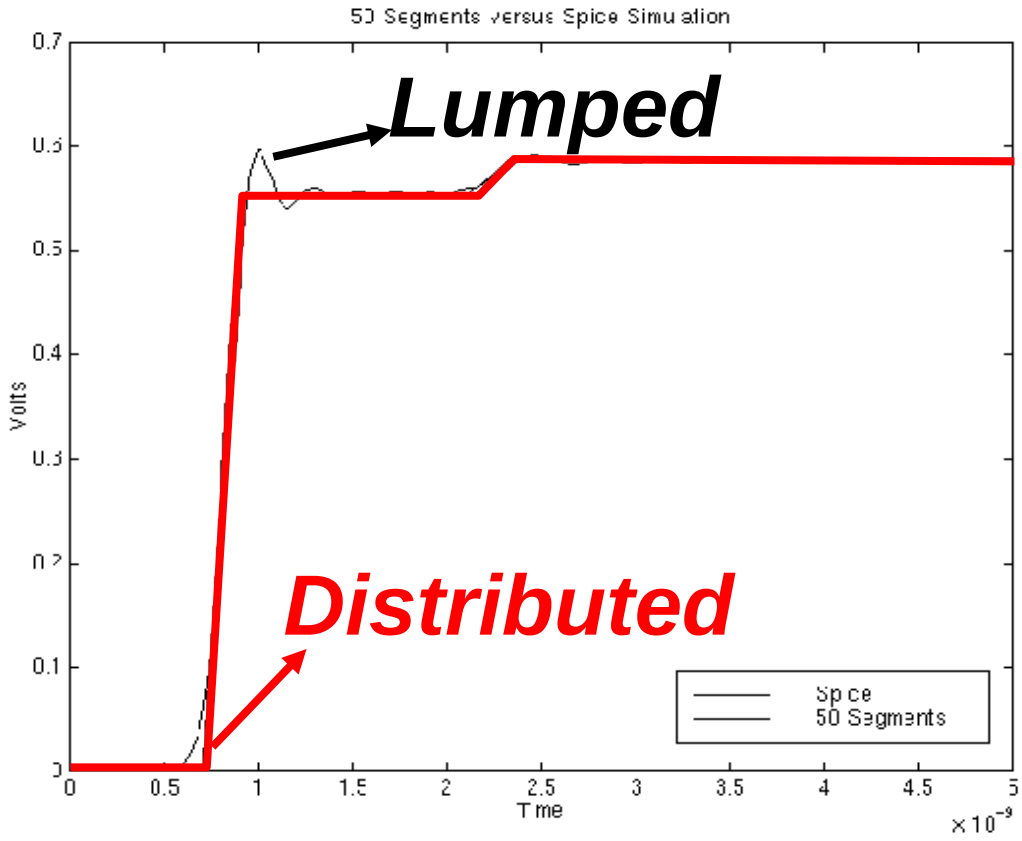
Lumped Segmentation: Example

10 segments v/s Distributed Model

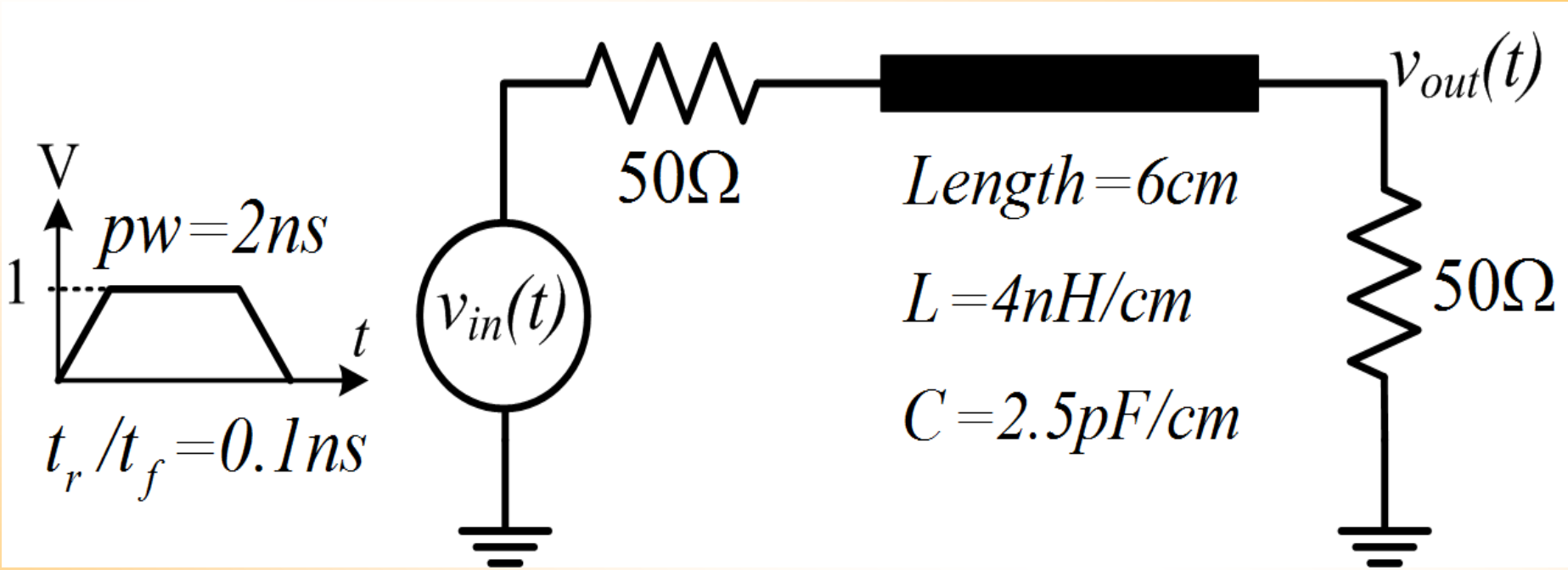


Lumped Segmentation: Example

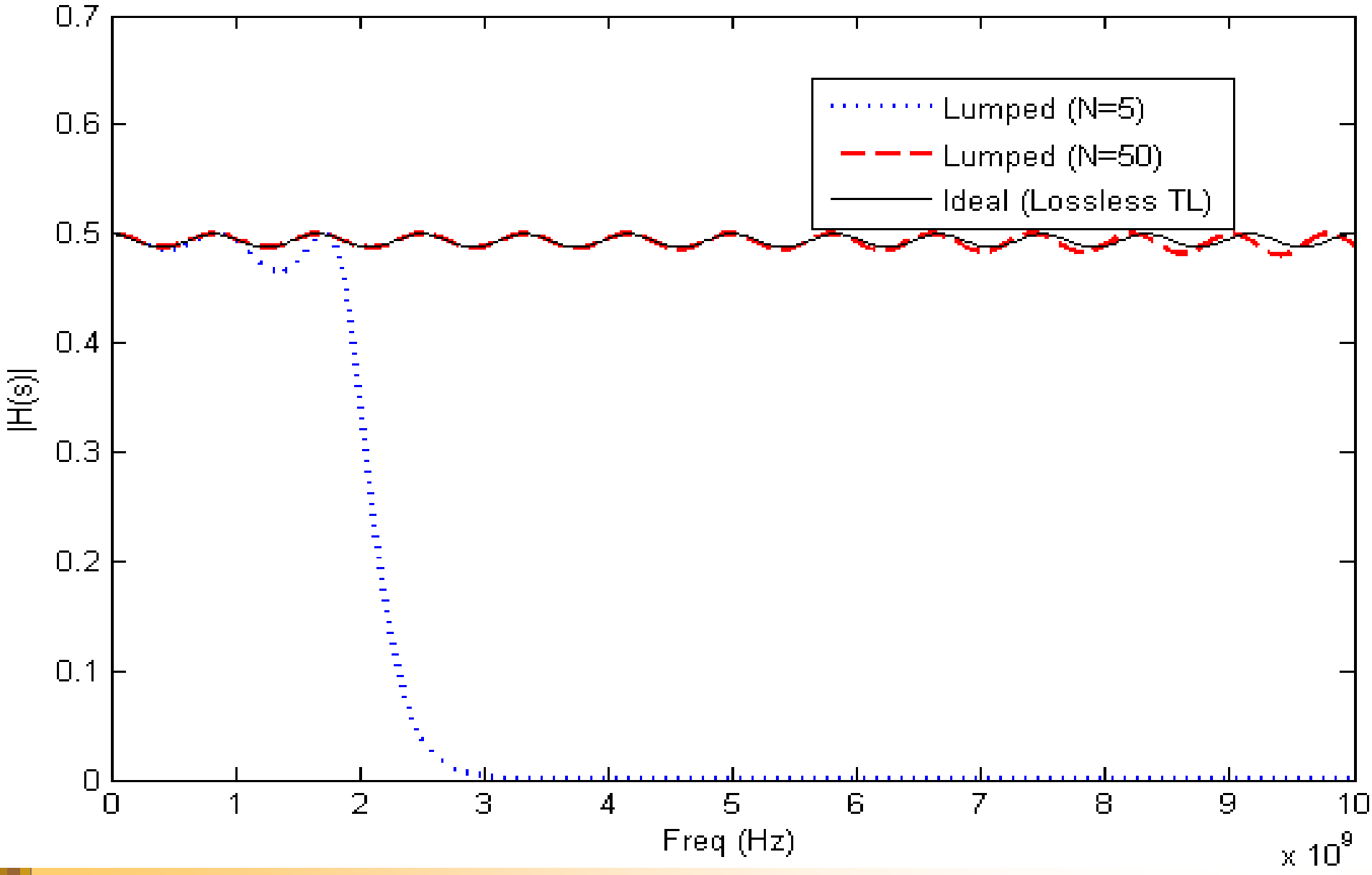
50 segments v/s Distributed Model



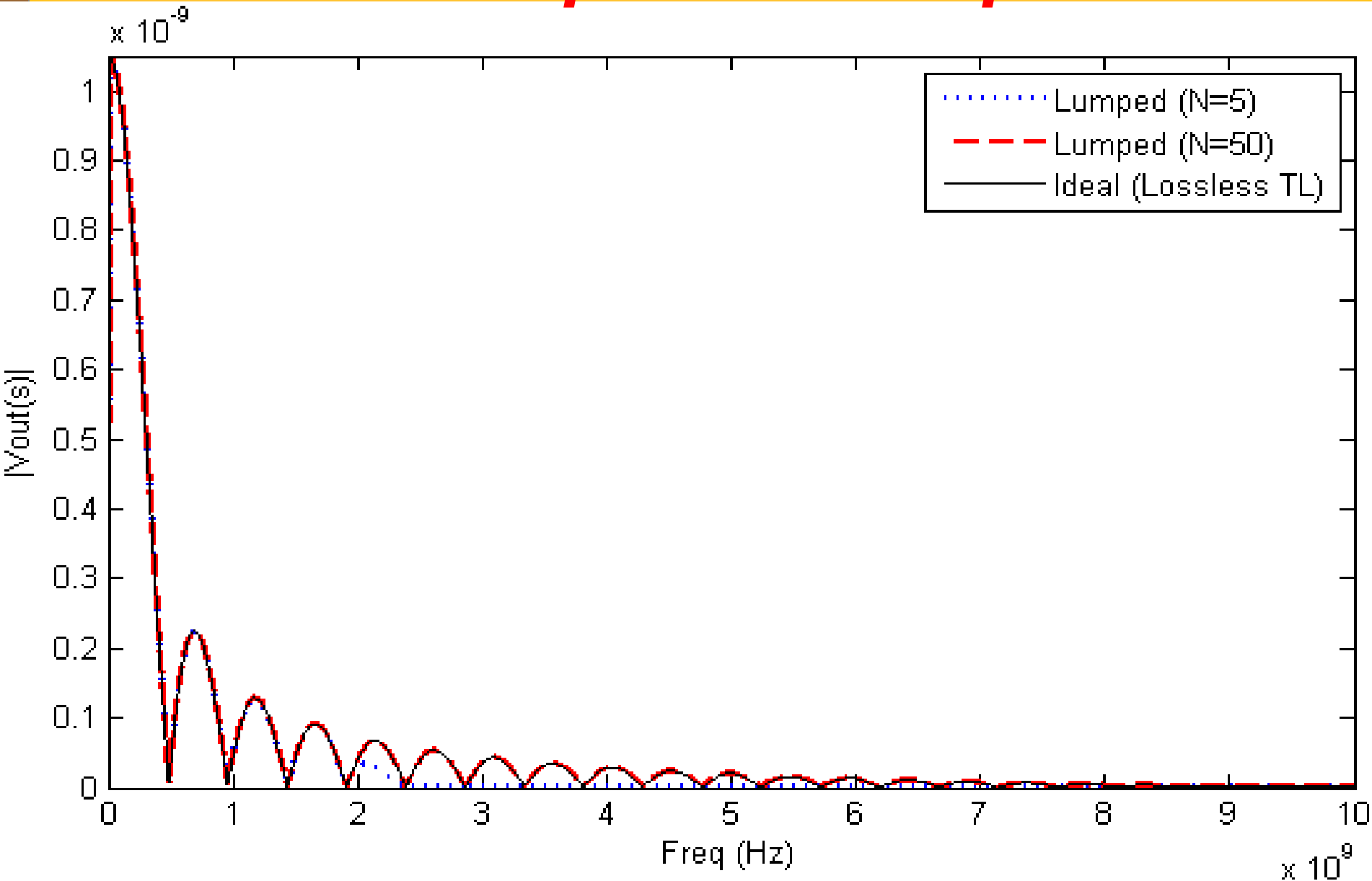
Transient Analysis with Distributed Interconnect



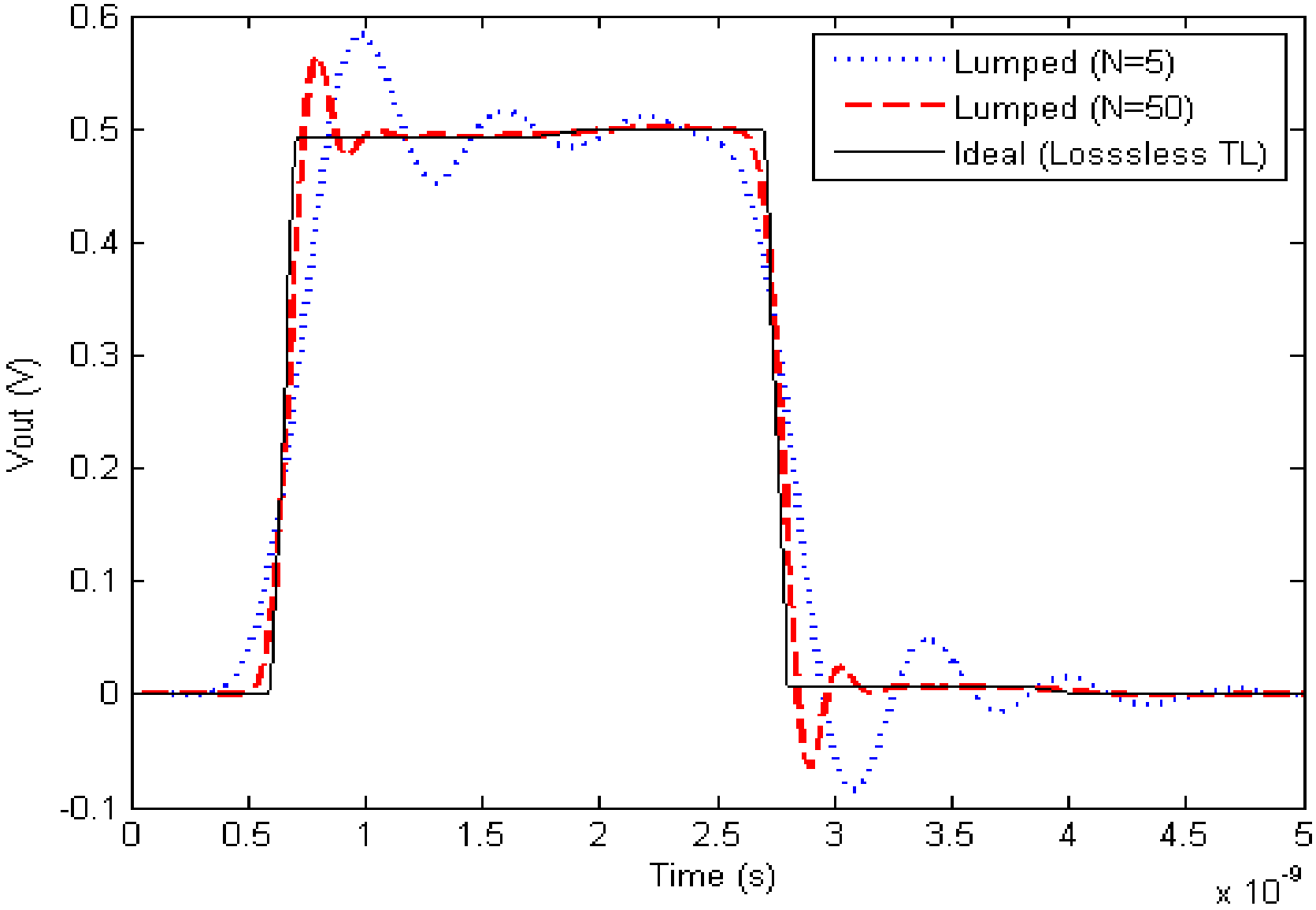
Frequency Response of Lumped Models



Frequency Response: Lumped Model with Input Pulse Spectrum



Transient Response



Lumped Segmentation: Example

A practically used expression to determine the number of sections (N) needed is given by:

$$N = (10\tau d)/t_r$$

t_r = *risetime*

τ = *line delay*

d = *line length*

Example: **Rise time = 0.2ns; Lossless line: 10cm, per-unit delay =of 70.7ps.**

$$N = (10 \times 70.7e^{-12} \times 10)/(0.2e^{-9}) = 35$$

Direct Lumped Segmentation

Disadvantages

* Large number of Sections (worsens in the case large line delays or steep rise times): CPU ineffcient.

Large CPU Cost

* Difficult to handle frequency-dependent Lines

* Leads to ringing in the waveform - Gibb's Phenomenon

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
  - MRA, DEPACT
  - WR+TP, WR+TP+EMI
  - Tabulated Data, Parallelization
- Conclusions

Possible Efficient Macromodeling Approaches

1) MoC based Algorithms

2) Matrix Rational Approximations

MoC based Algorithms

→ *Delay Extraction + Rational Approximation*

→ *Efficient for Long Low Loss Lines*

Difficulties

1) Coupled Lines: Curve Fitting

n Lines → $(2n^2 + n)$ Tr. functions

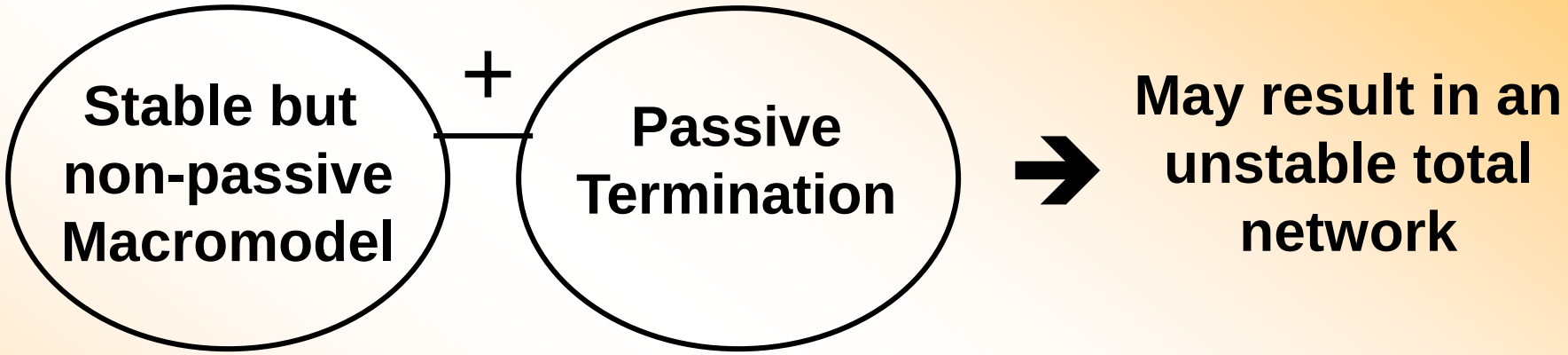
Eg. 10 Lines → 210 Tr. functions

2) Does not Guarantee Passivity

Problem faced…….

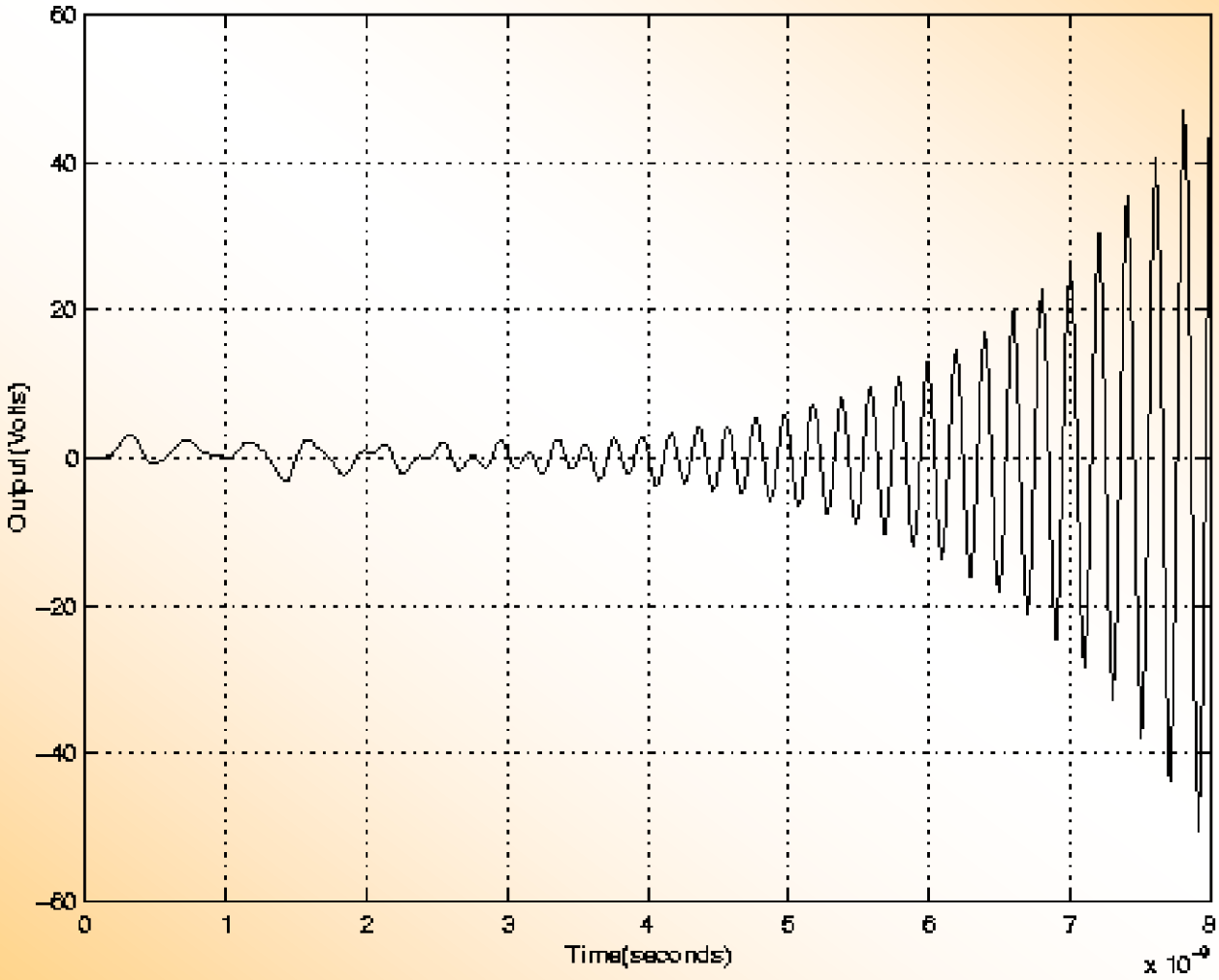
- Limited Bandwidth of Approximation
- Individual numerical fitting of parameters of a matrix function
- Loss of physical properties – such as passivity

Importance of Passivity



- Error: Failure to Converge
- Error: Time Step Too Small – Abort
- Error: ……

Unstable response



Time response of stable but nonpassive reduced model

Passivity

Y(s) is passive iff

1) $Y(s^*) = Y^*(s)$

2) $z^{*t}[Y^t(s^*) + Y(s)]z \geq 0,$ **Re(s)>0**

Y(s) is a positive real matrix

Ensuring passivity of the reduced Macromodel is a challenging task!!

Defining the objectives…….

- Can we improve the bandwidth of approximation without facing ill-conditioning?

- Can we come up with a matrix based approximation without resorting to individual entity approximations?

- Can we do the approximation analytically without resorting to numerical curve fitting?

- Can we ensure the physical properties for the model?

Agenda

- Emerging Product Trends
- Interconnect Scaling: Trend & Issues
- High-Speed Design Issues
- Interconnect Hierarchy
- What is a “High-Speed Interconnect”?
- Interconnect Models and Simulation Challenges
- Advanced/Recent Models
  - MRA, DEPACT
  - WR+TP, WR+TP+EMC
  - Tabulated Data, Parallelization
- Conclusions

Matrix Exponential Stamp

$$\frac{\partial}{\partial z}\mathbf{V}(z,t) = -\mathbf{R}\,\mathbf{I}(z,t) - \mathbf{L}\frac{\partial}{\partial t}\mathbf{I}(z,t)$$

$$\frac{\partial}{\partial z}\mathbf{I}(z,t) = -\mathbf{G}\,\mathbf{V}(z,t) - \mathbf{C}\frac{\partial}{\partial t}\mathbf{V}(z,t)$$

$$\begin{bmatrix}\mathbf{I}(d,s)\\ \mathbf{V}(d,s)\end{bmatrix} = e^{\mathbf{Z}}\begin{bmatrix}\mathbf{I}(0,s)\\ \mathbf{V}(0,s)\end{bmatrix}$$

$$\mathbf{Z} = (\mathbf{D} + s\mathbf{E})d \qquad \mathbf{D}=\begin{bmatrix}0 & -\mathbf{R}\\ -\mathbf{G} & 0\end{bmatrix} \qquad \mathbf{E}=\begin{bmatrix}0 & -\mathbf{L}\\ -\mathbf{C} & 0\end{bmatrix}$$

This is what we are approximating……

Matrix Rational Approximation

$$\begin{bmatrix} V(d,s) \\ I(d,s) \end{bmatrix} = e^{Z} \begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix}$$

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$$

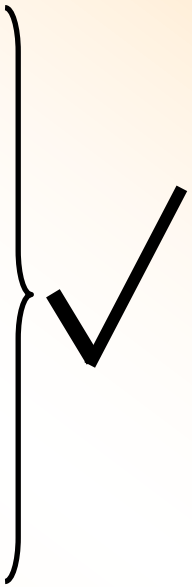
Rational Functions

1) Scalar Approximation

2) Independent of PUL parameters

3) Passivity is guaranteed
   → Closed-Form Relations

4) Can achieve higher bandwidth



CONCEPT - MRA

Pade' Approximation of Exponential Function

$$e^x = \frac{\sum_{i=0}^{M} P_i x^i}{\sum_{j=0}^{N} Q_j x^j} = \frac{\sum_{i=0}^{M} \frac{(M+N-i)!}{(M+N)!} \times \frac{M!}{(M-i)!} x^i}{\sum_{j=0}^{N} \frac{(M+N-j)!}{(M+N)!} \times \frac{N!}{(N-j)!} (-x)^i}$$

➔Closed-form relation for coefficients

➔High-order approximation possible

➔No ill-conditioning

Time-Domain Macromodel

$$\mathbf{Q}_N(Z)\begin{bmatrix} V(d,s) \\ I(d,s) \end{bmatrix} \approx \mathbf{P}_M(Z)\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix}$$

Z=(D+sE)d

Analytically

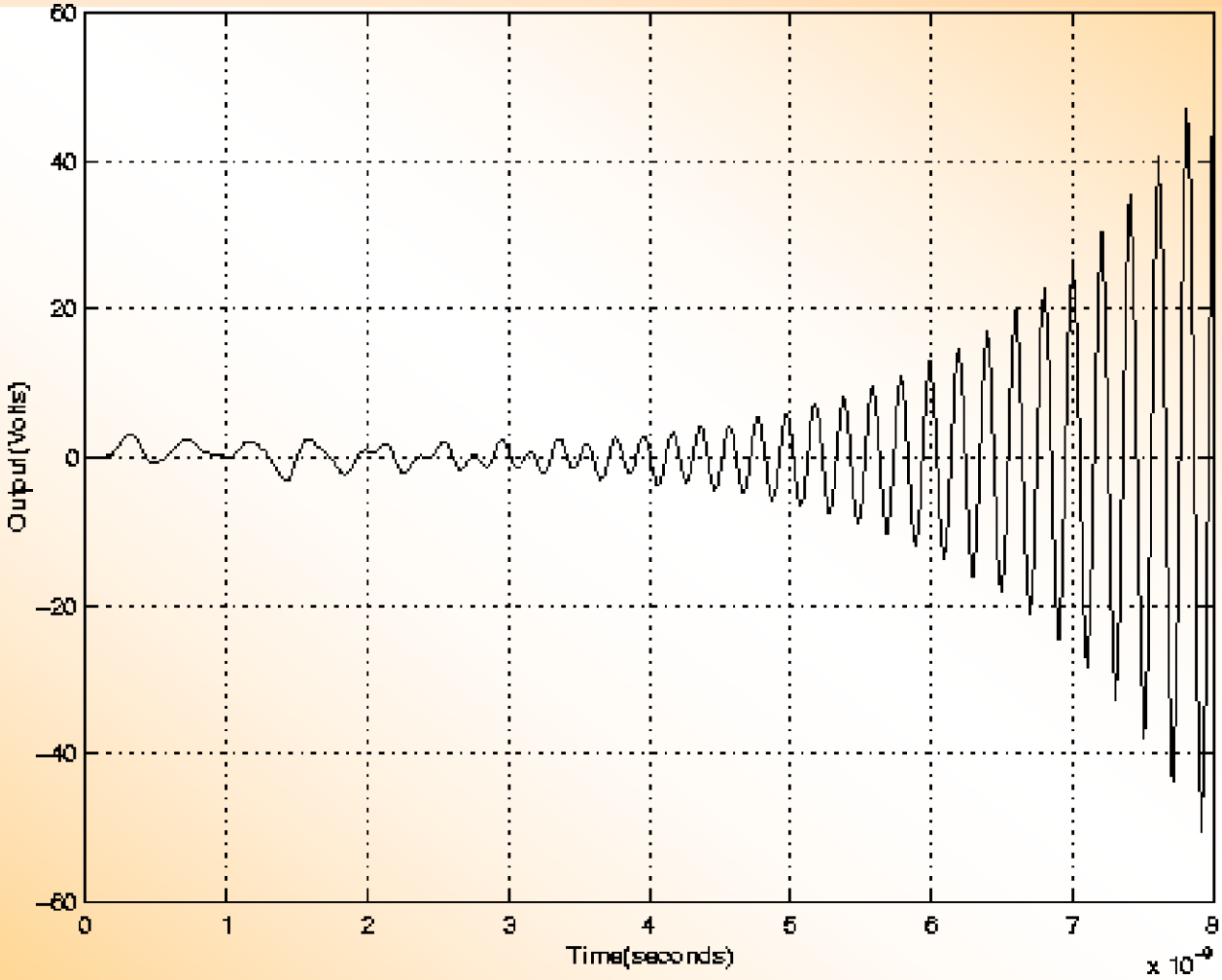
$$\begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix}\begin{bmatrix} V(0,s) \\ V(d,s) \end{bmatrix} = \begin{bmatrix} I(0,s) \\ I(d,s) \end{bmatrix}$$

Analytically

$$\dot{X}(t) = AX(t) + BI(t)$$

$$y(t) = CX(t) + DI(t)$$

Passivity??



Time response of stable but nonpassive reduced model

Passivity Conditions

***Theorem**:* Let the rational function of e^x be:

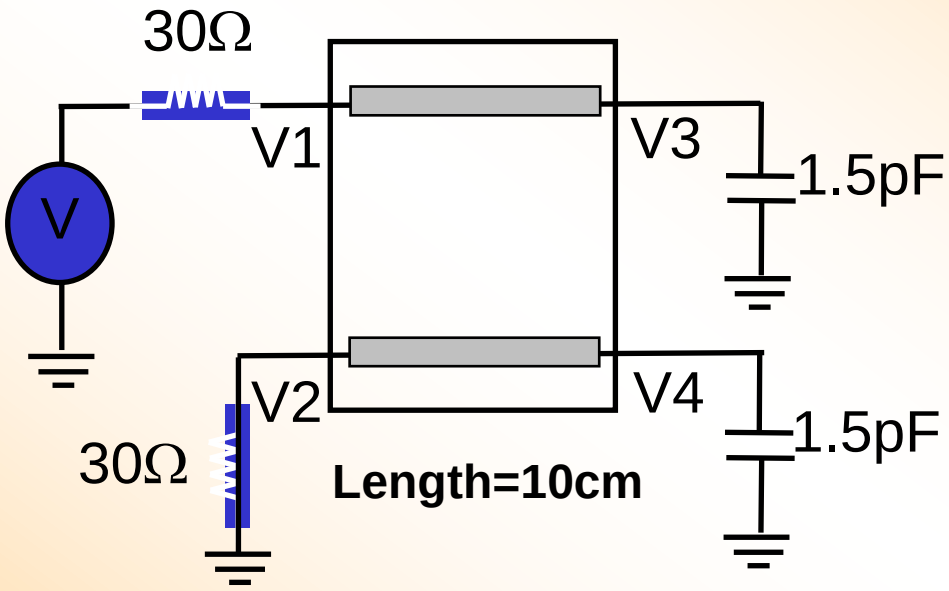
$$e^x \approx \frac{Q_N(x)}{Q_N(-x)} = \frac{\sum_{i=0}^{N} q_i x^i}{\sum_{i=0}^{N} q_i (-x)^i}$$

IF the polynomial $Q_N(x)$ is strictly Hurwitz* THEN

the rational matrix obtained by replacing the scalar x with the matrix Z=(D+sE)d results in a passive transmission line macromodel

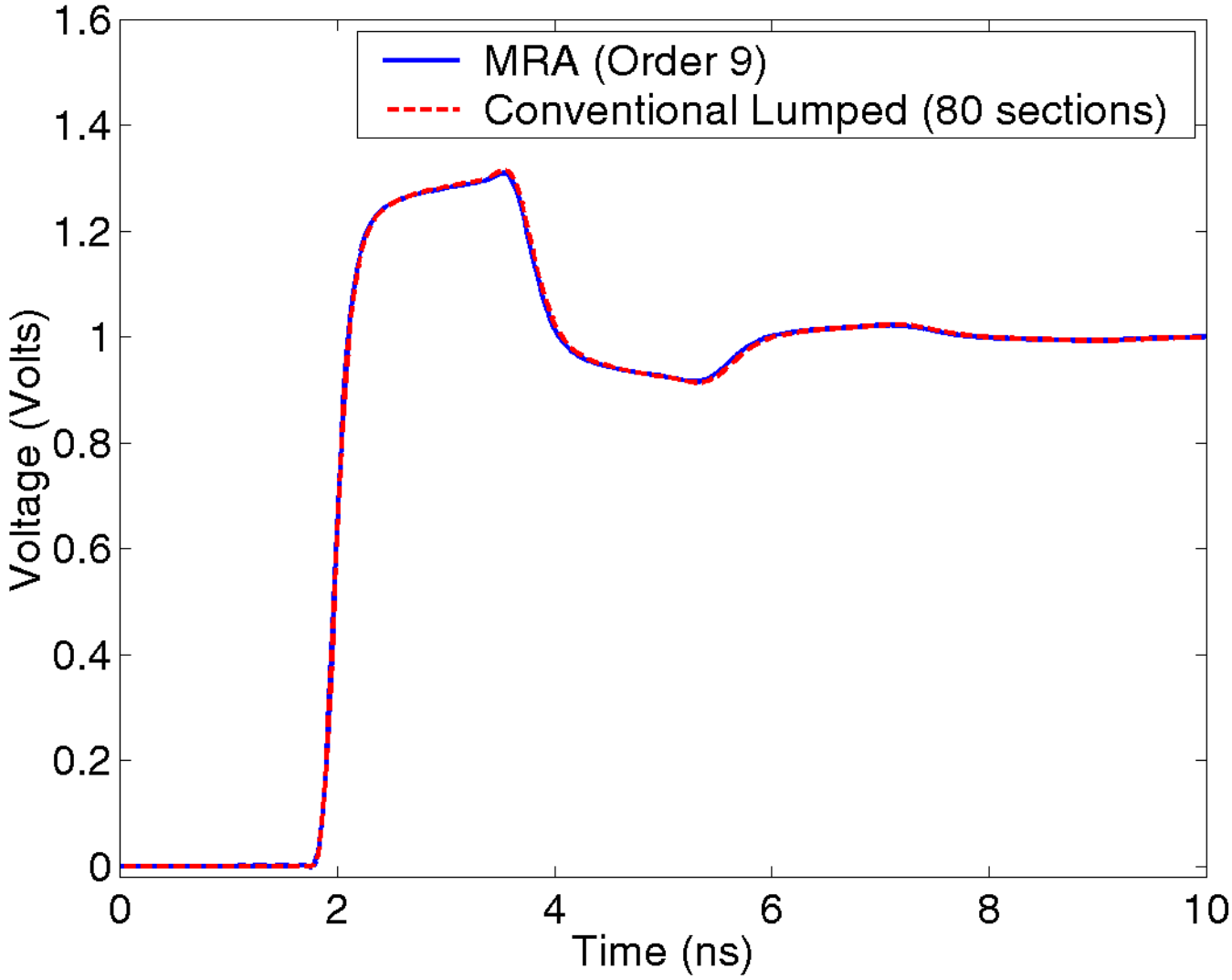
**A polynomial with real positive coefficients and roots which are either negative or pairwise conjugate with negative real parts.*

Example 1: Coupled Lossy TL



Input: step response, rise time = 0.2 ns

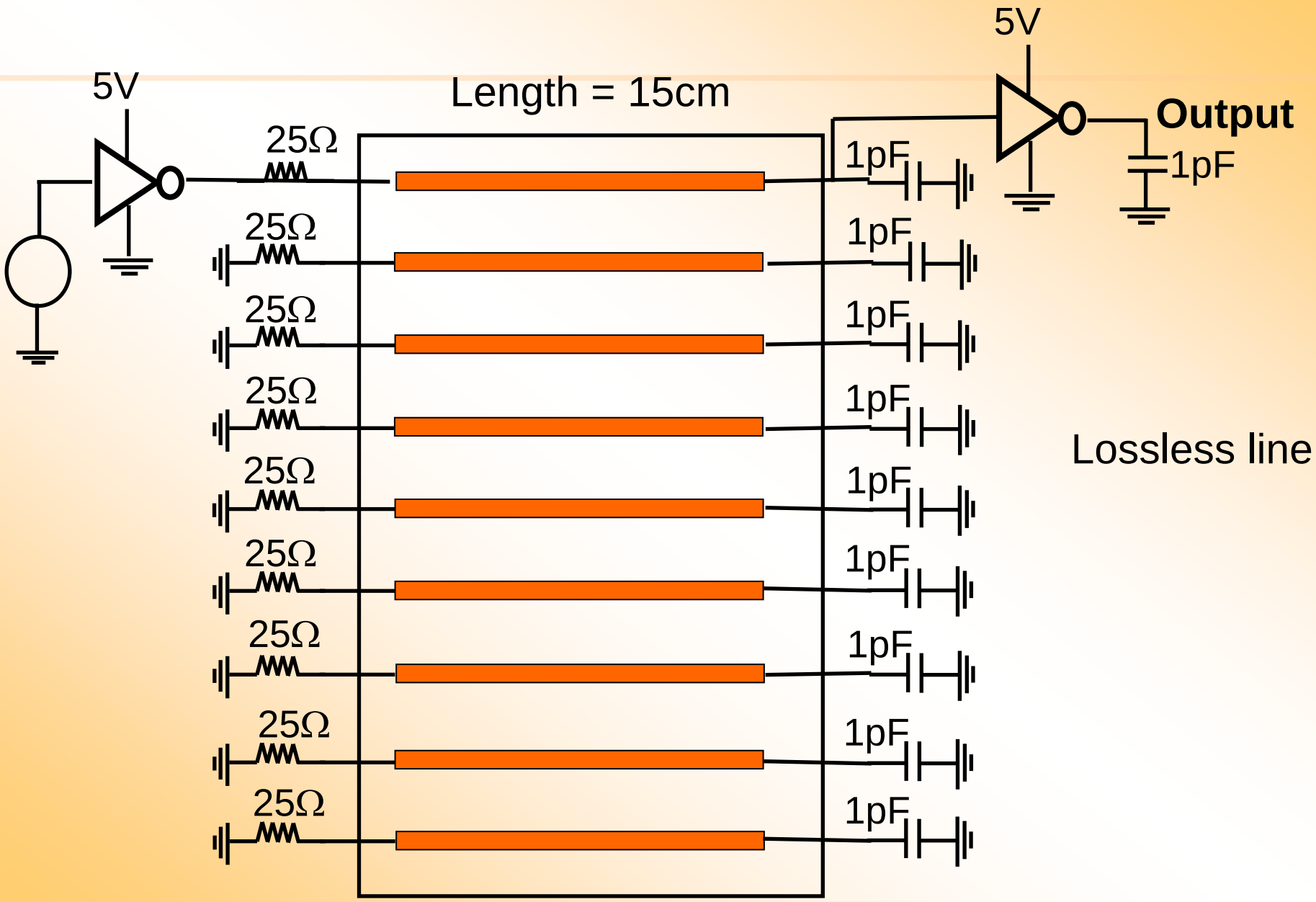
Example 1: Far End Active Line



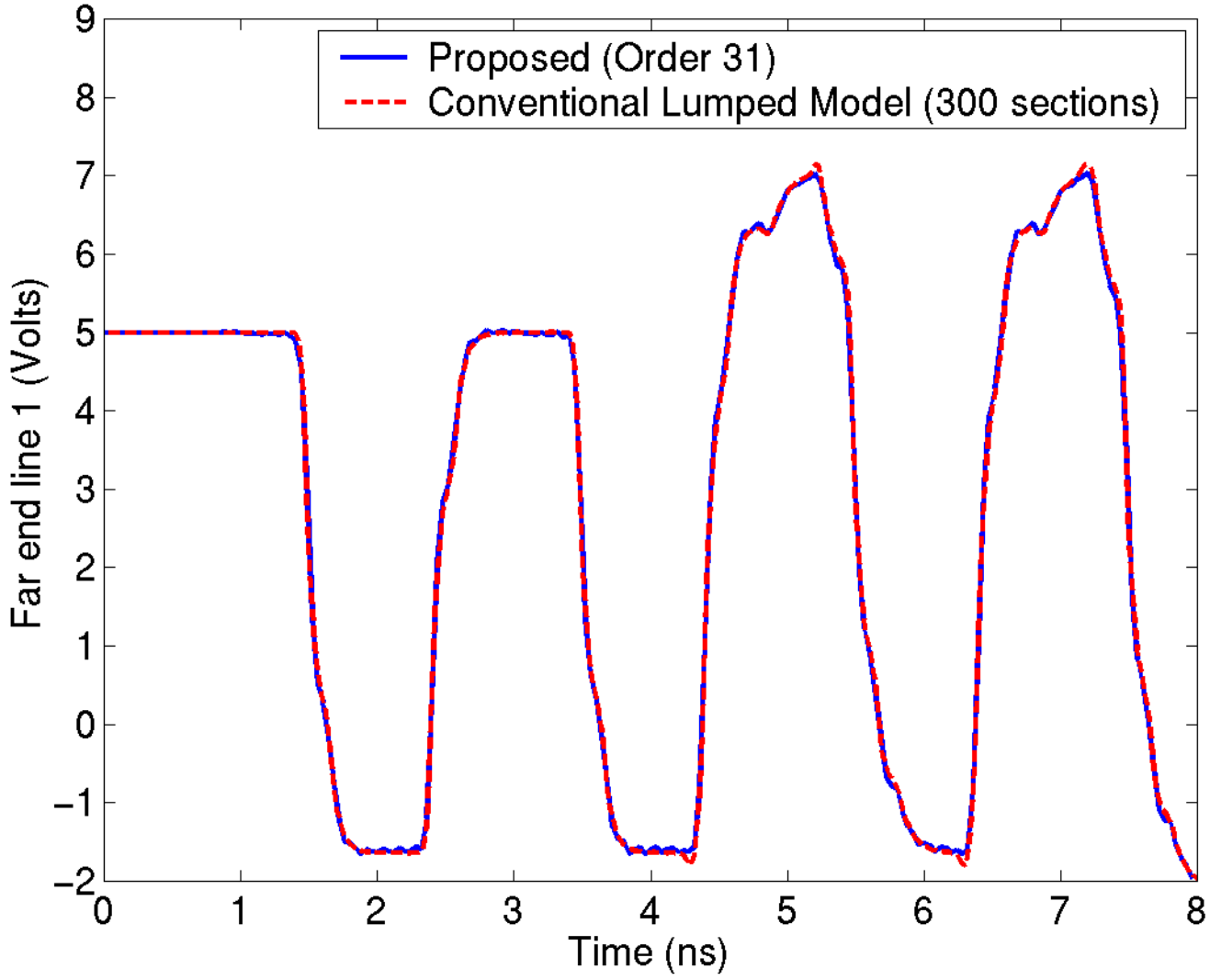
Performance Comparison

Simulations	MRA (MNA size)	Lumped (MNA size)	MNA savings
Example 1	**8281**	**48000**	**83%**
Example 2	**355**	**2 482**	**86%**
Example3 (5cm)	**914**	**6 002**	**85%**
Example 3 (20cm)	**3 650**	**24 002**	**85%**
Example 3 (40cm)	**7 298**	**80 002**	**91%**

Example 3: Nonlinear Terminations



Transient Responses

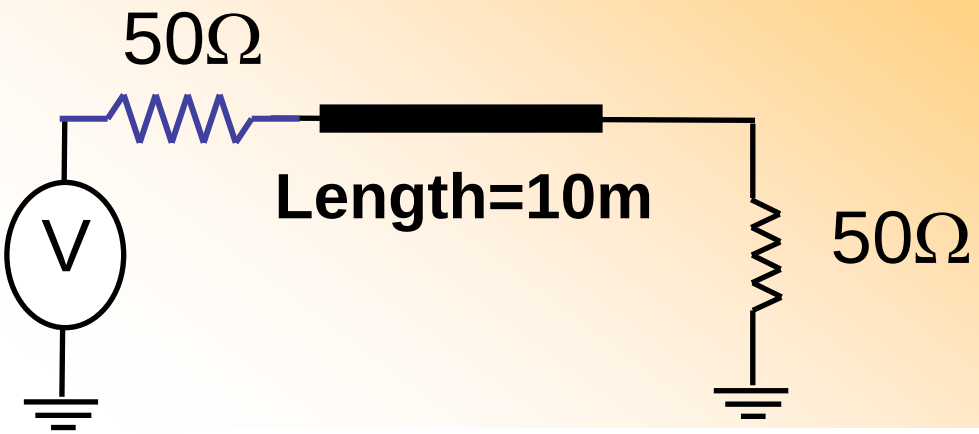


CPU Comparison

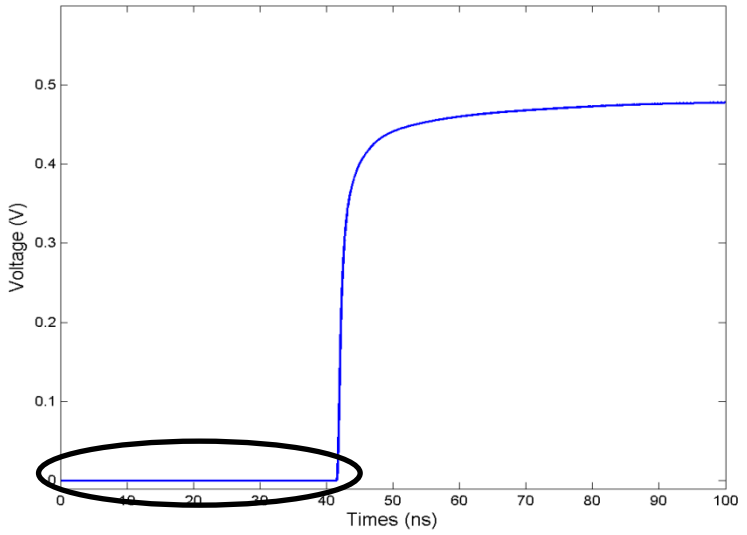
Algorithm	Total number of lumped sections	CPU time (SPARC Ultra 5-10) (seconds)
Conventional Lumped	300	3282
Proposed	31	315

How About Long Low-Loss Lines???

*(Low Loss TL)**

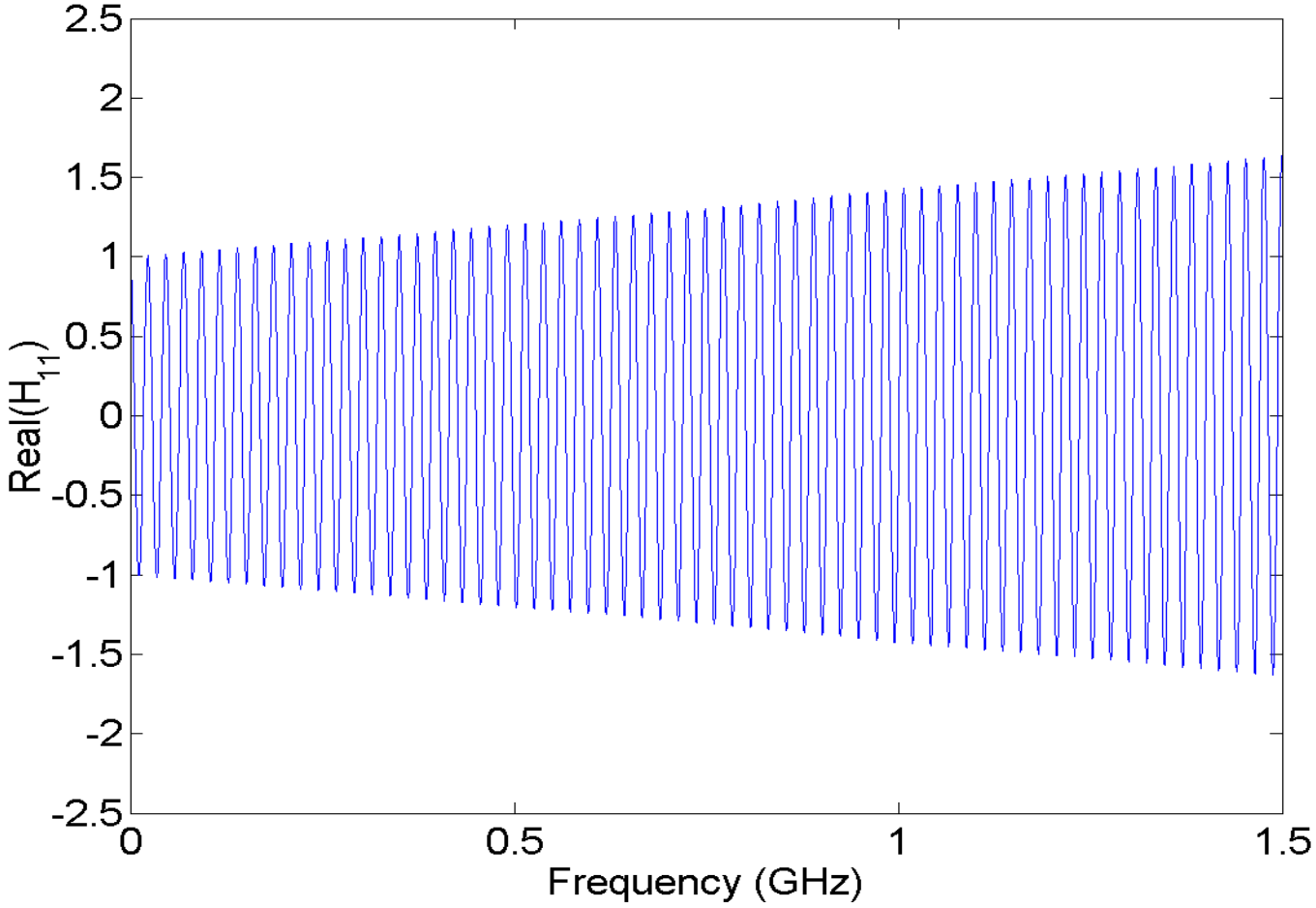


MoC	MRA
Time (s)	Time (s)
4	463



Why?

Without Delay Extraction



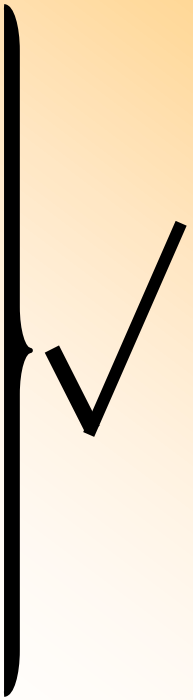
Macromodel: Objectives

1) Closed Form

→ **Large Number of Coupled Lines**

2) Guaranteed Passivity

3) Delay Extraction



Agenda

Advanced Interconnect Modeling Methods

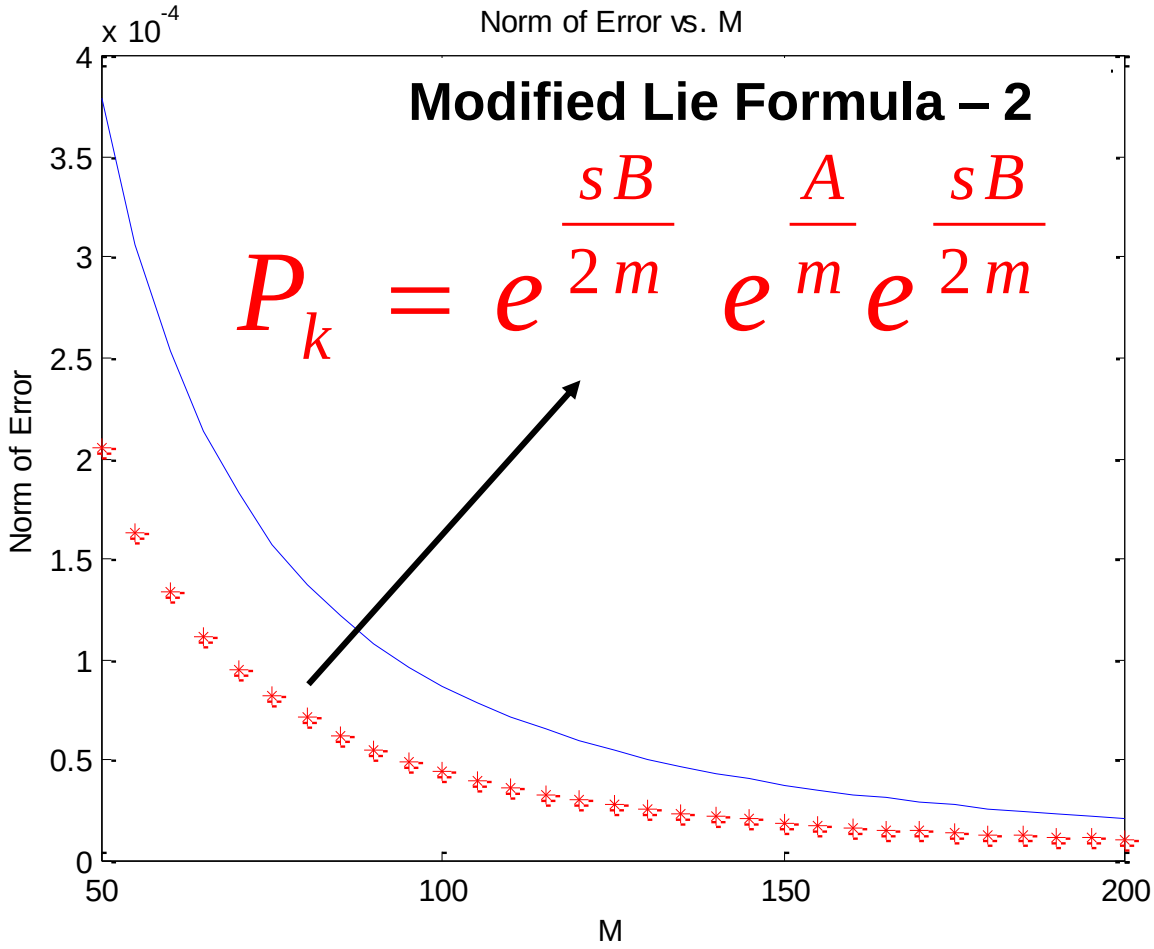
- MoC, MRA
- DEPACT
- WR+TP, EMI
- Tabulated Data Macromodelling, Parallelization

Conclusions

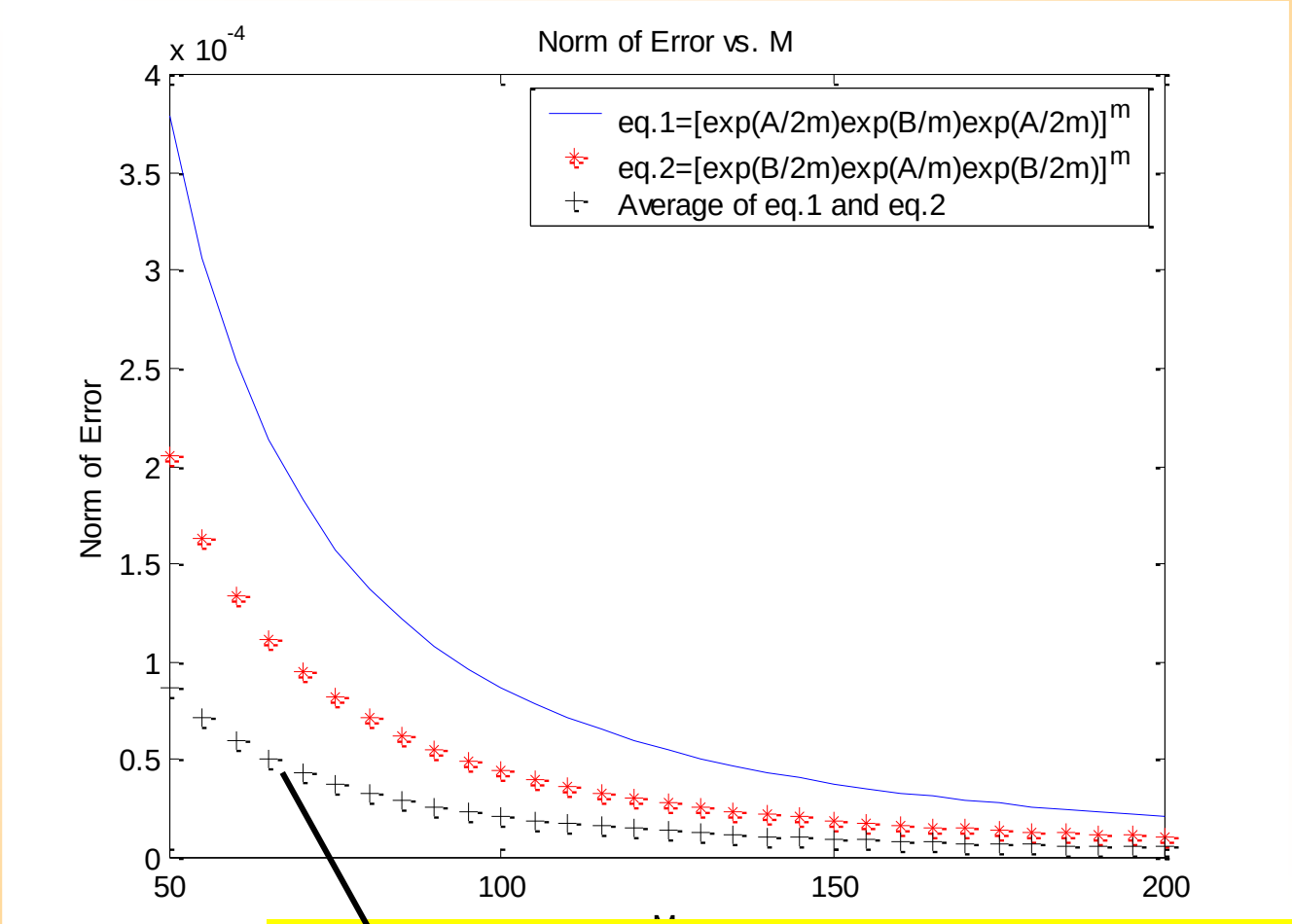
Delay Extraction - DEPACT

- **Extracts pure delay components of equivalent circuit matrix**
- **Pure-delay components can be simulated with existing tline (T)**
- **Highly compact/passive macromodels**

Error Estimates



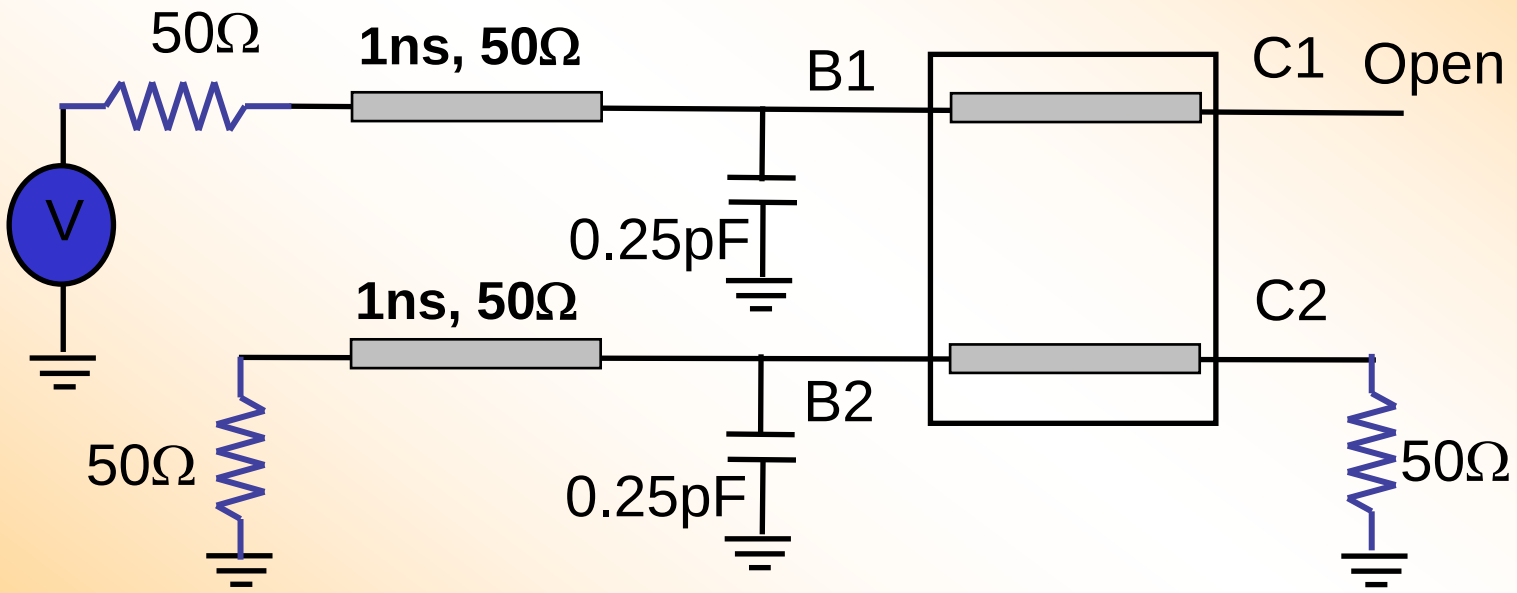
Error Estimates



Average of Modified Lie Formula 1 and 2

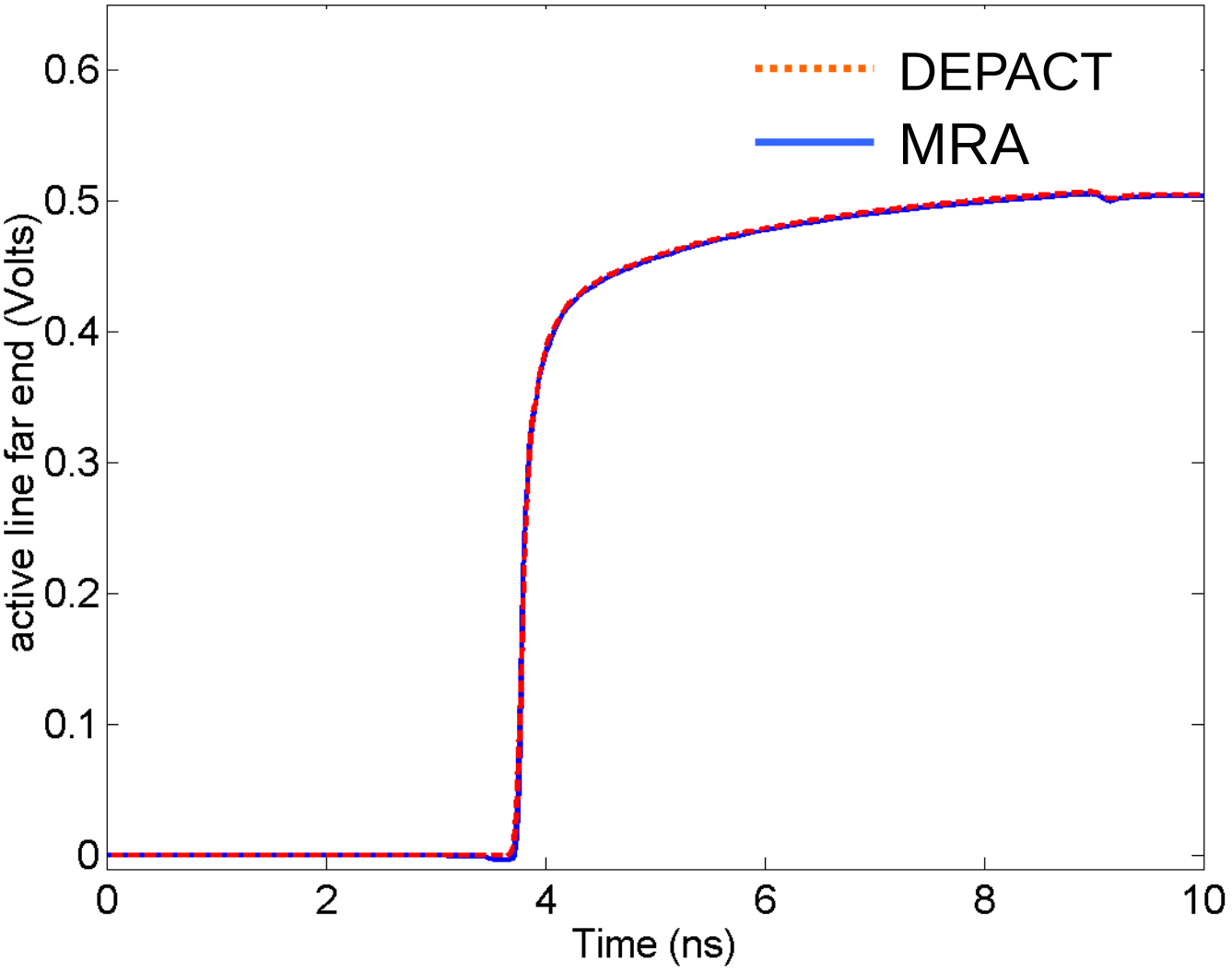
Example: Lossy Coupled TL

5cm, 20cm, 40cm



Input: step response, rise time = 0.035 ns

IBM: Line 6 (40cm)



IBM: Line 6

Simulation	DEPACT	MRA	Lumped
	time (s)	time (s)	time (s)
5cm	**0.89**	**4.16**	**32.4**
20cm	**2.47**	**25**	**292**
40cm	**4.32**	**74**	**4641**

Computer: SUN Blade-1000 workstation with 900MHz UltraSPARC-III CPU.

Problem Addressed so far……

- Limited Bandwidth of Approximation
- Individual numerical fitting of parameters of a matrix function
- Loss of physical properties – such as passivity
- Delay Extraction + Passivity
- ➔ How about large coupled lines?

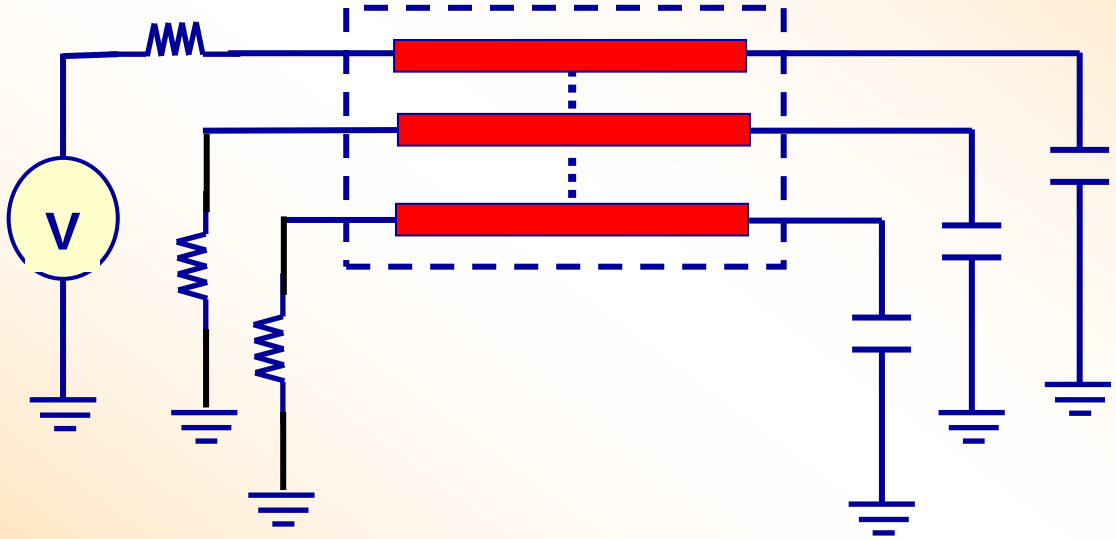
Agenda

Advanced Interconnect Modeling Methods

- MoC, MRA, DEPACT
- WR+TP
- EMI
- Tabulated Data

Conclusions

Large # of Coupled Lines: Traditional approaches

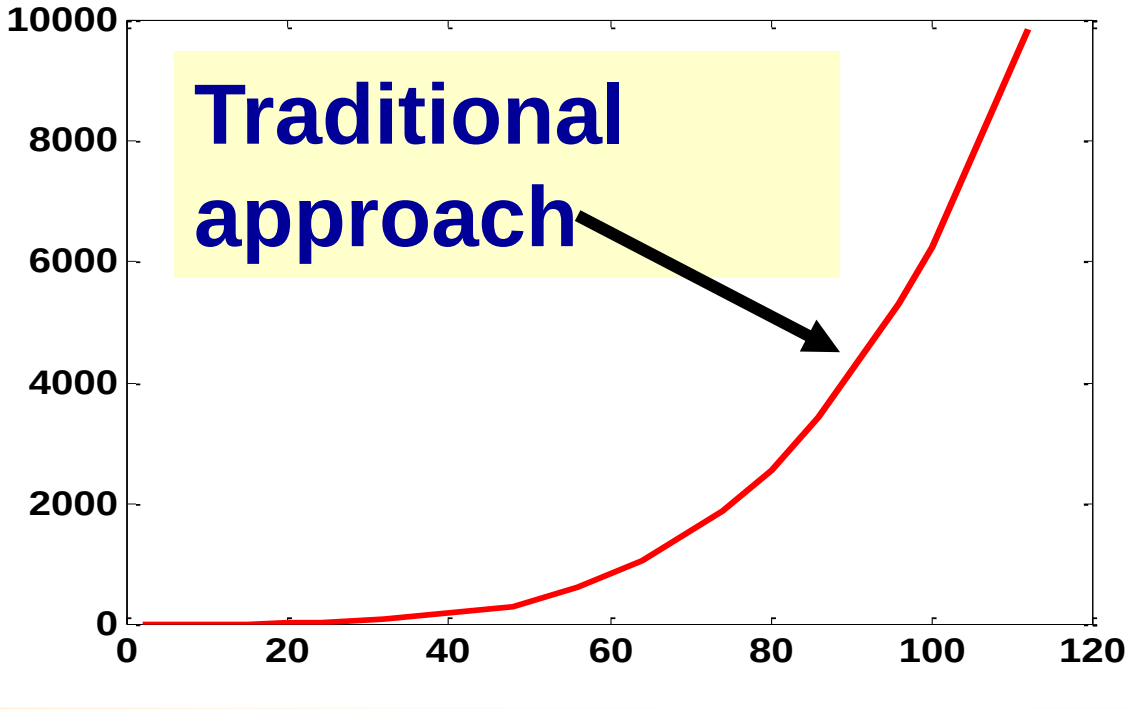


Number of lines	CPU Time
2	2.3 sec
32	78 sec
96	5315.6 sec

1.5 hours!!

Large # of Coupled Lines

CPU Time (Seconds)



N (number of lines)

Average cost of simulating N-coupled lines circuit is proportional to N^{α} , where $3 \leq \alpha \leq 4$

In the literature……

Direct Methods (L/U, F/B)

→*Fast*

→*Memory Inefficient*

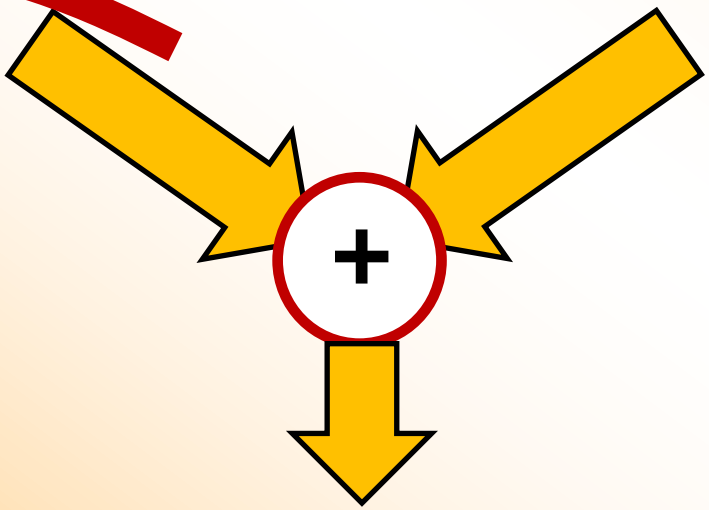
→*Sequential Process*

Iterative Methods

→*Slow*

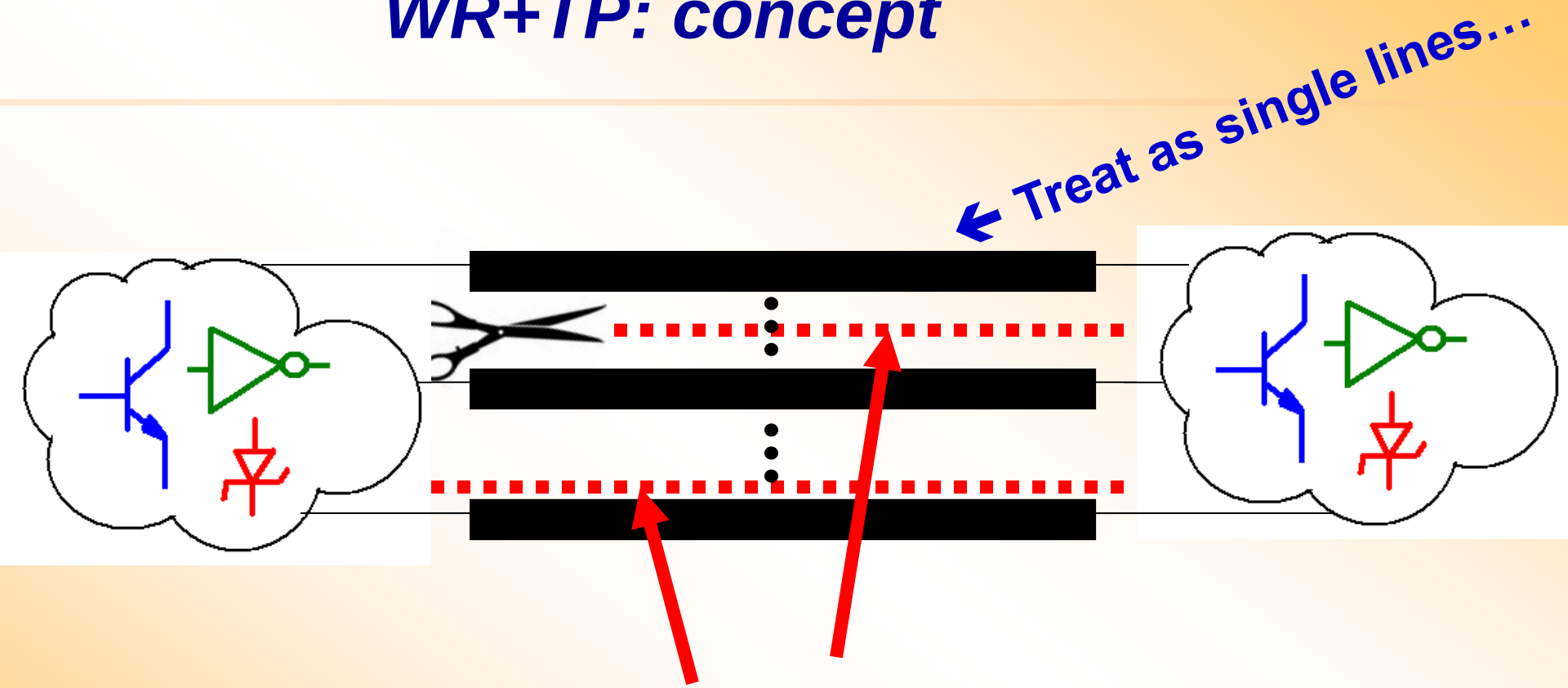
→*Memory Efficient*

→*Parallelizable*

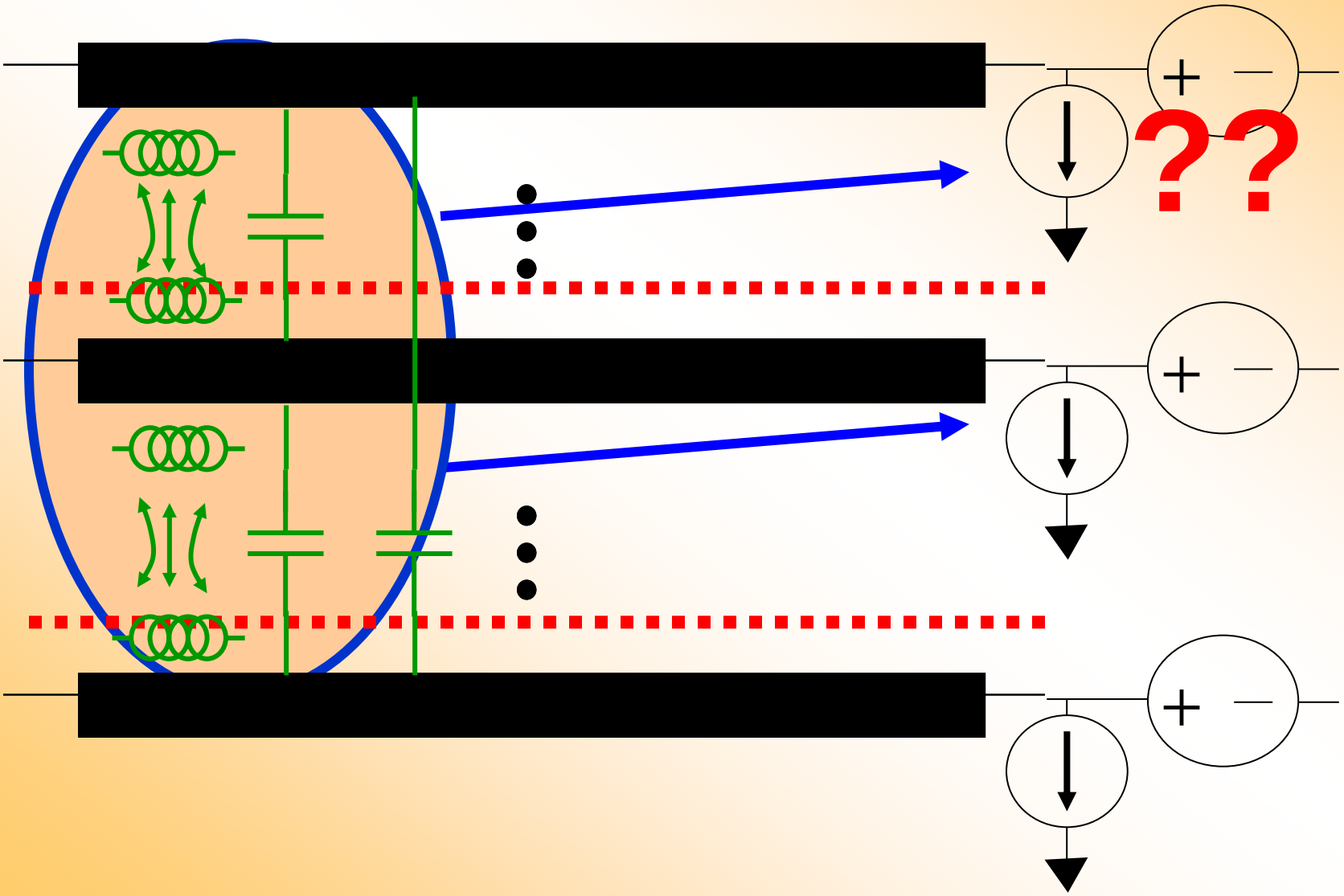


Combine both using ➔ ***Waveform Relaxation***

WR+TP: concept



WR + TP of Unexcited Lines- WR Sources



Computation of WR Source

Homogeneous Telegrapher's Equation

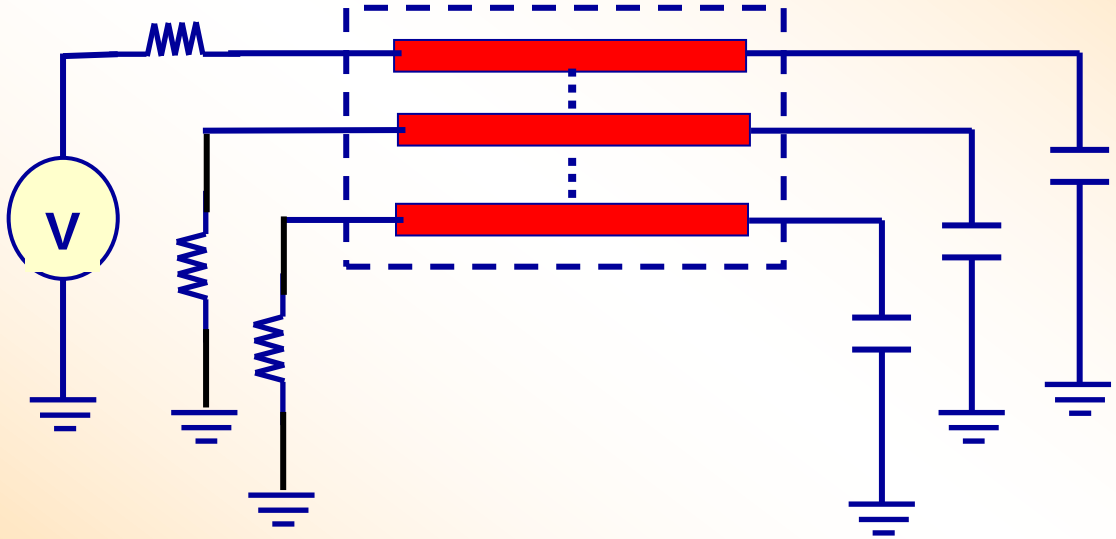
$$\frac{\partial}{\partial z}\begin{bmatrix}\mathbf{V}(z,t)\\ \mathbf{I}(z,t)\end{bmatrix}=\begin{bmatrix}\mathbf{0} & -\mathbf{R}\\ -\mathbf{G} & \mathbf{0}\end{bmatrix}\begin{bmatrix}\mathbf{V}(z,t)\\ \mathbf{I}(z,t)\end{bmatrix}+\begin{bmatrix}\mathbf{0} & -\mathbf{L}\\ -\mathbf{C} & \mathbf{0}\end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix}\mathbf{V}(z,t)\\ \mathbf{I}(z,t)\end{bmatrix}$$

for kth line

$$\frac{\partial}{\partial z}v_k(z,t)=-R_{kk}i_k(z,t)-L_{kk}\frac{\partial}{\partial t}i_k(z,t)-\sum_{\substack{j=1\\ j\neq k}}^{n}\left[\quad\right]+\tilde{e}_k(z,t)$$

$$\frac{\partial}{\partial z}i_k(z,t)=-\hat{G}_{kk}v_k(z,t)-\hat{C}_{kk}\frac{\partial}{\partial t}v_k(z,t)-\sum_{\substack{j=1\\ j\neq k}}^{n}\left[\quad\right]+\tilde{q}_k(z,t)$$

TRANSVERSE PARTITIONING + WR

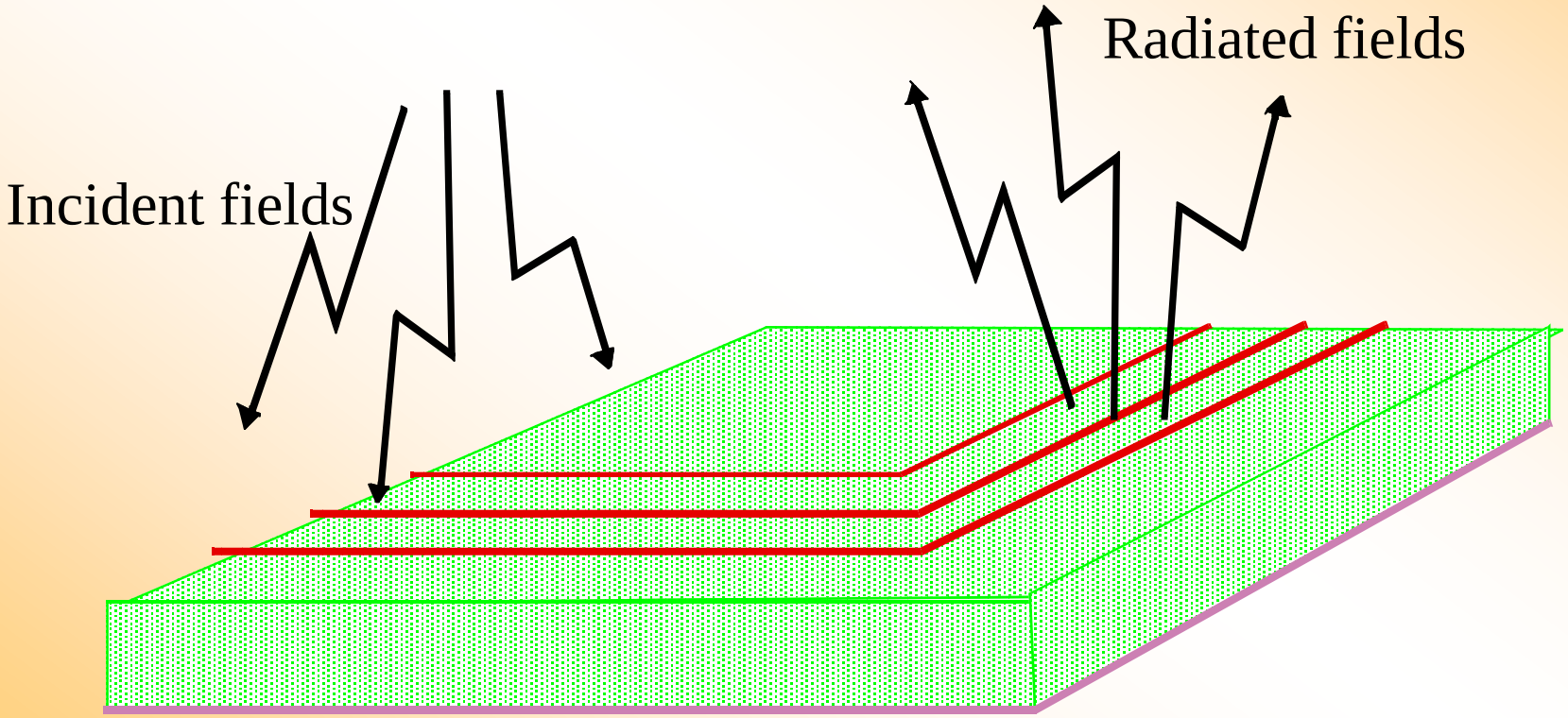


Number of lines	CPU Time
96	1.5 hours

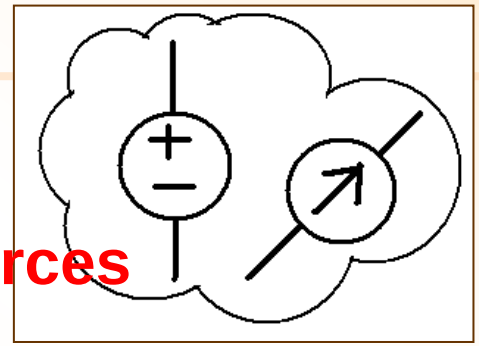
TP

34.5 sec !!

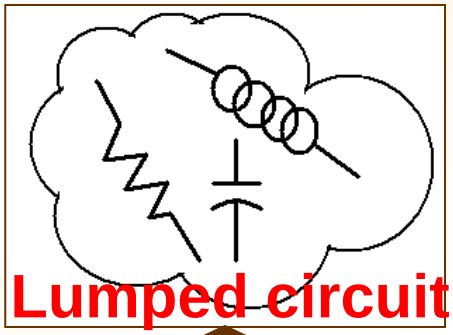
Electromagnetic Interference



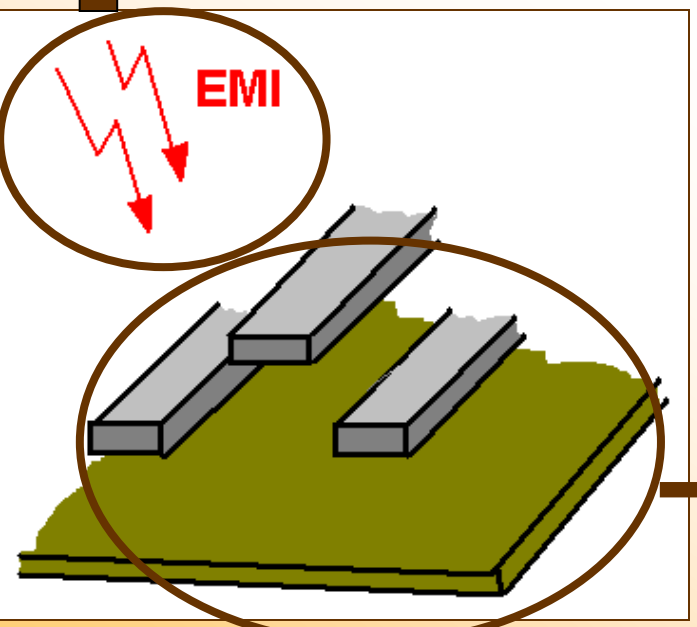
EMI Analysis & High-Speed Interconnects



Sources

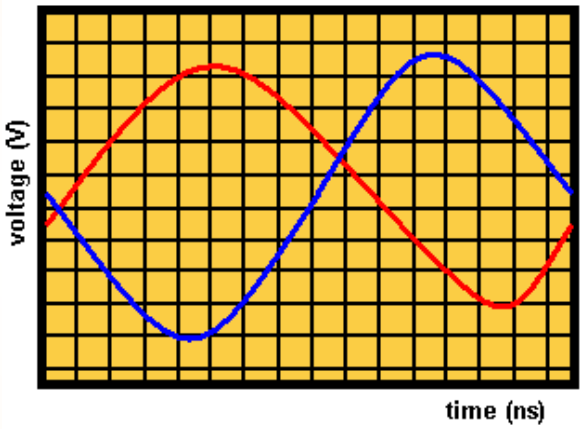


Lumped circuit



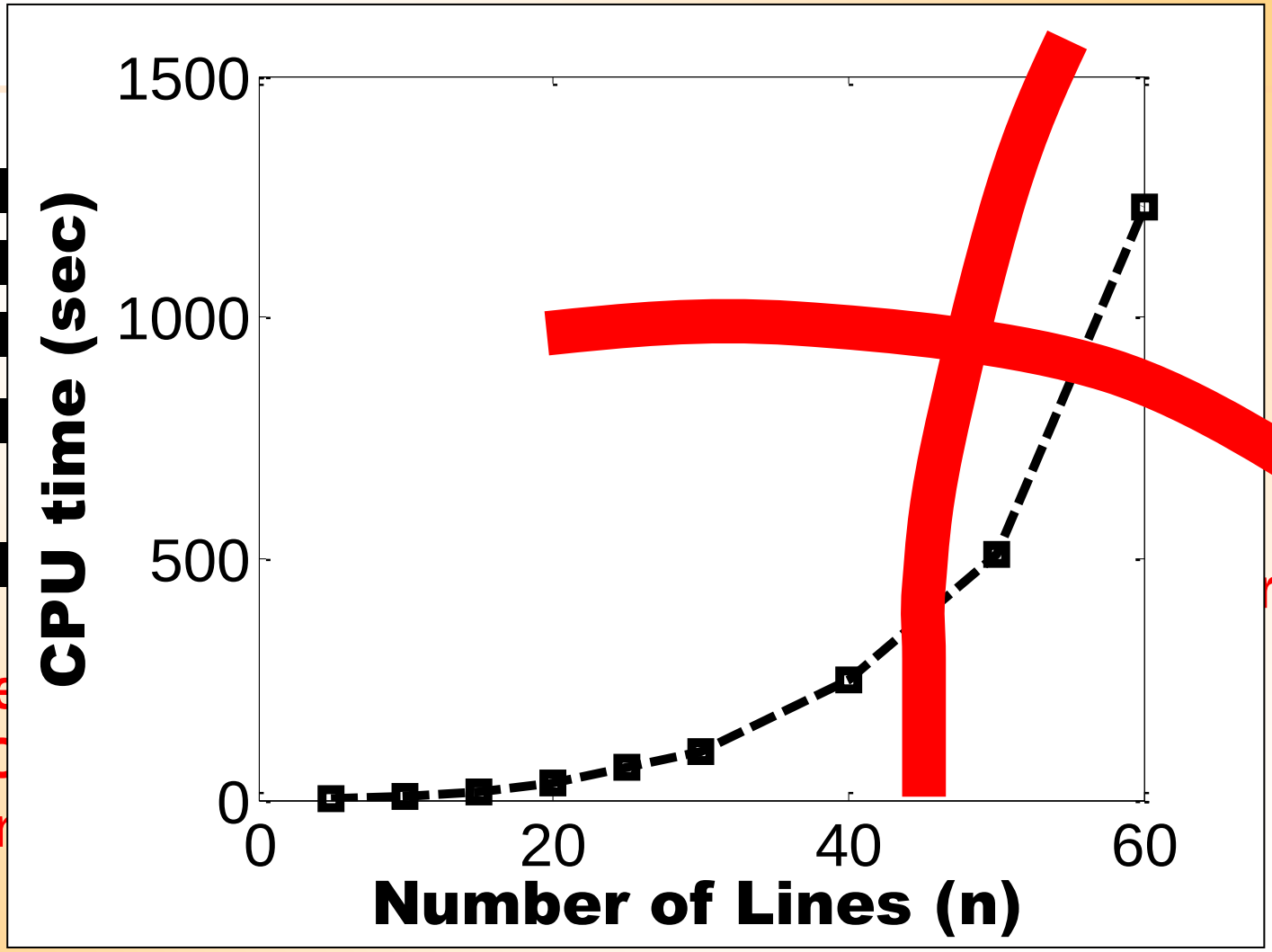
Physical description

Macromodeling



SPICE simulation

Conventional EMI Analysis: Large # of Coupled Lines



Large
of C
Lin

rcuit-

Simulation Time → $O((n^2)^2)=O(n^4)$!!!

WR+TP + EMI

Description of EMI:

$$\frac{\partial}{\partial z}\begin{bmatrix}\mathbf{V}(z,s)\\ \mathbf{I}(z,s)\end{bmatrix}=\begin{bmatrix}\mathbf{0} & -(\mathbf{R}+s\mathbf{L})\\ -(\mathbf{G}+s\mathbf{C}) & \mathbf{0}\end{bmatrix}\begin{bmatrix}\mathbf{V}(z,s)\\ \mathbf{I}(z,s)\end{bmatrix}+\begin{bmatrix}\mathbf{V}_F(z,s)\\ \mathbf{I}_F(z,s)\end{bmatrix}$$

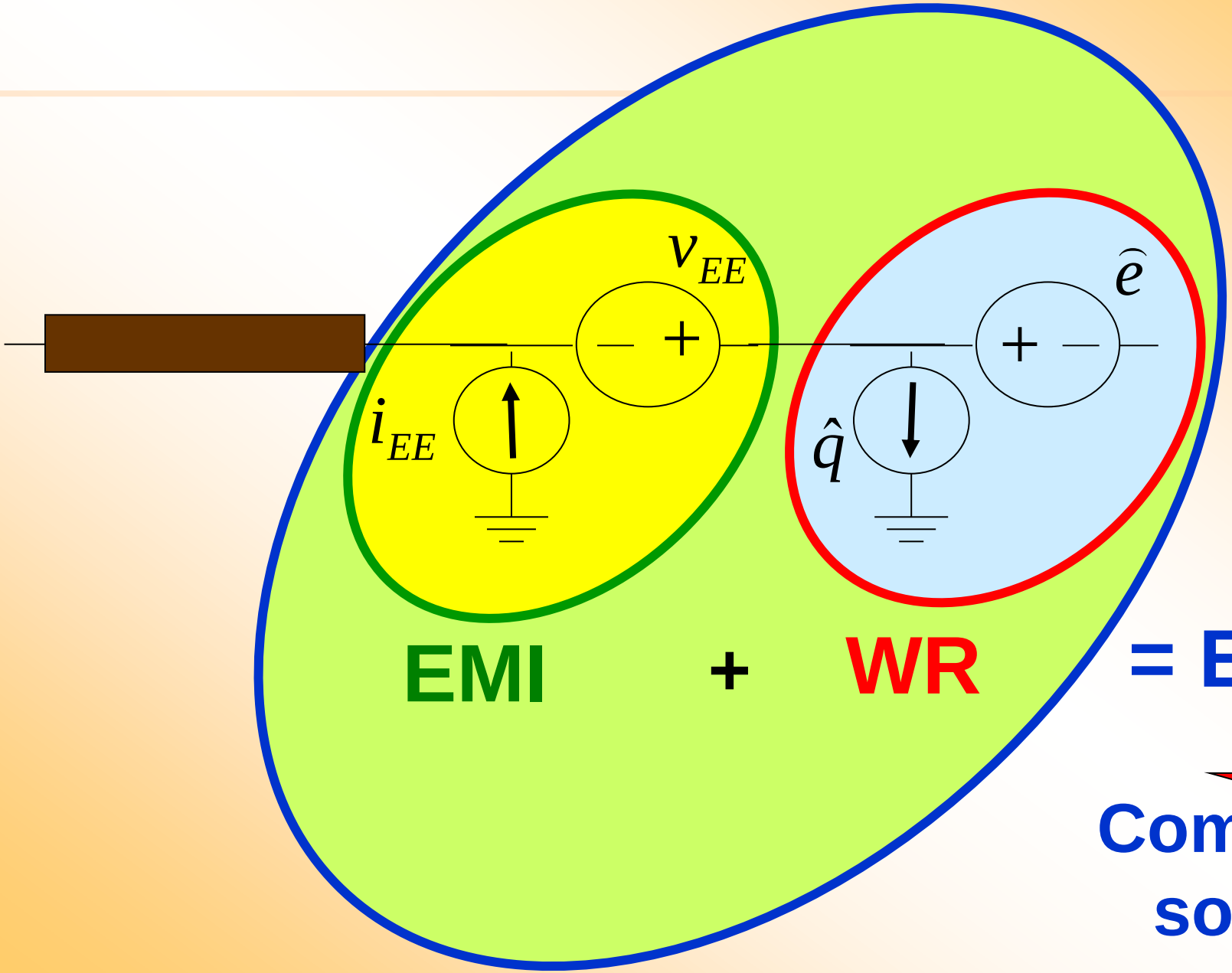
mutually compatible representation POSSIBLE!

Wav

$$\frac{\partial}{\partial z}v_k(z,t)=-R_{kk}i_k(z,t)-L_{kk}\frac{\partial}{\partial t}i_k(z,t)-\tilde{e}_k(z,t)$$

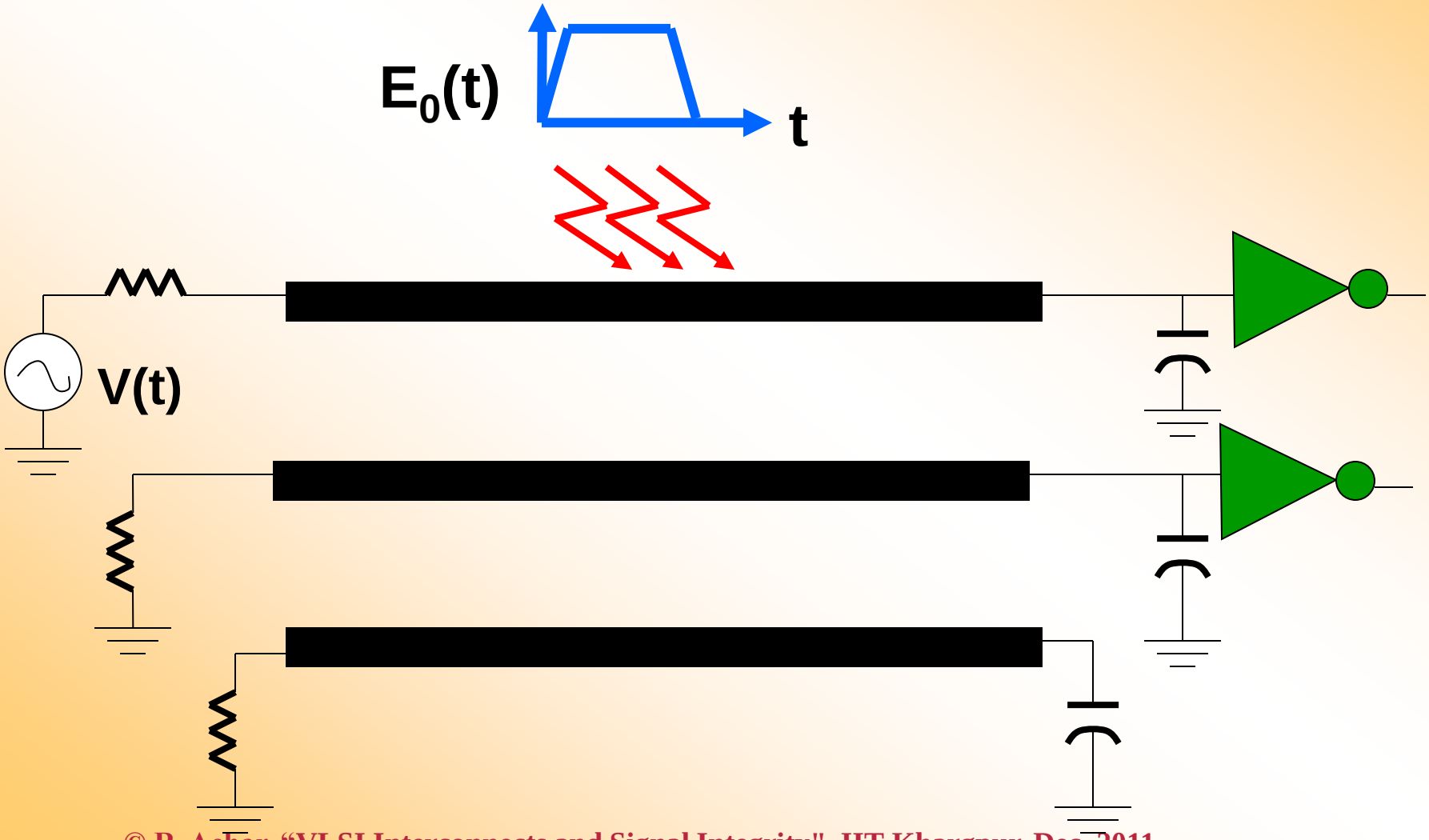
$$\frac{\partial}{\partial z}i_k(z,t)=-\hat{G}_{kk}v_k(z,t)-\hat{C}_{kk}\frac{\partial}{\partial t}v_k(z,t)-\tilde{q}_k(z,t)$$

Combined representation for each iteration

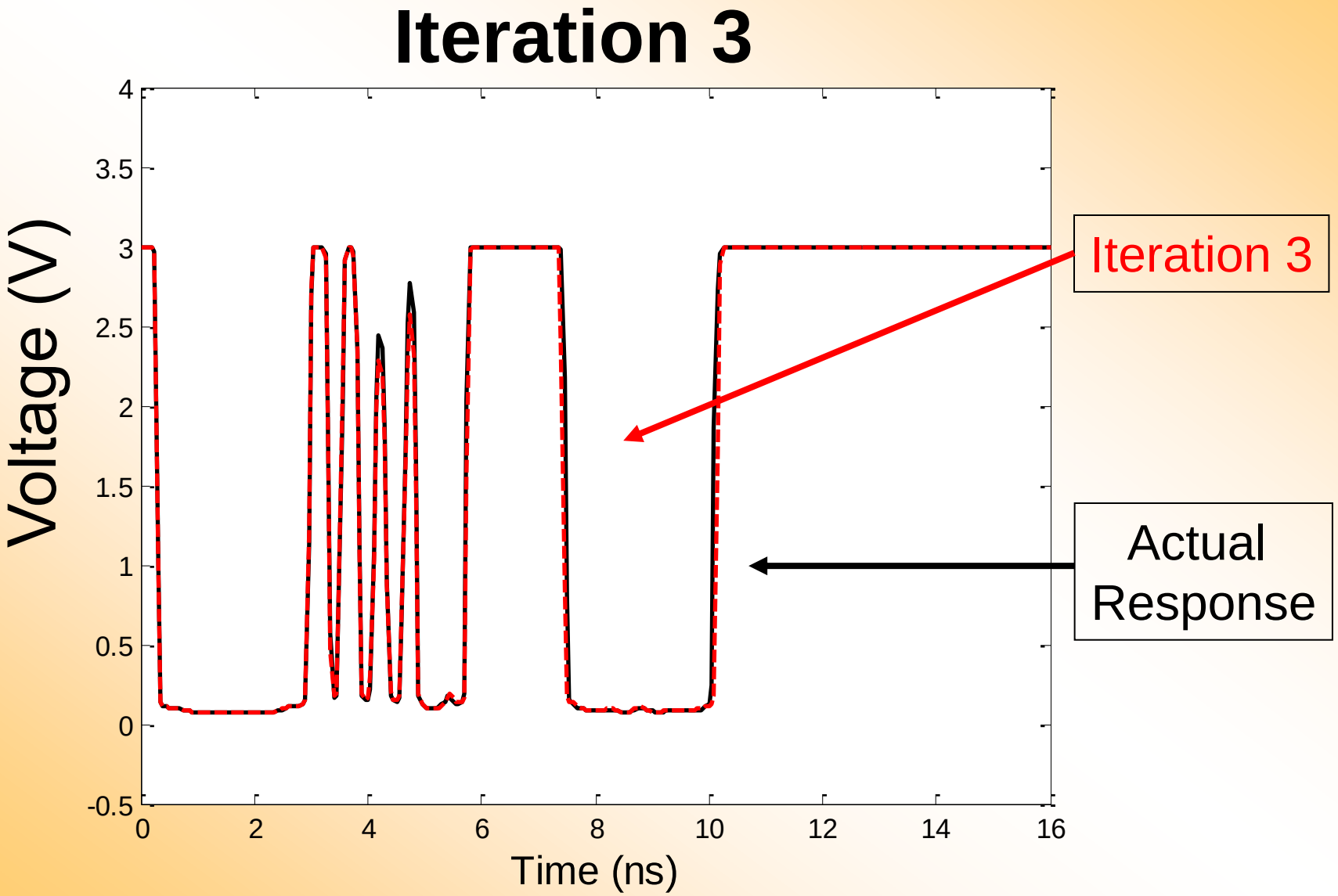


Example: WR+TP + EMI

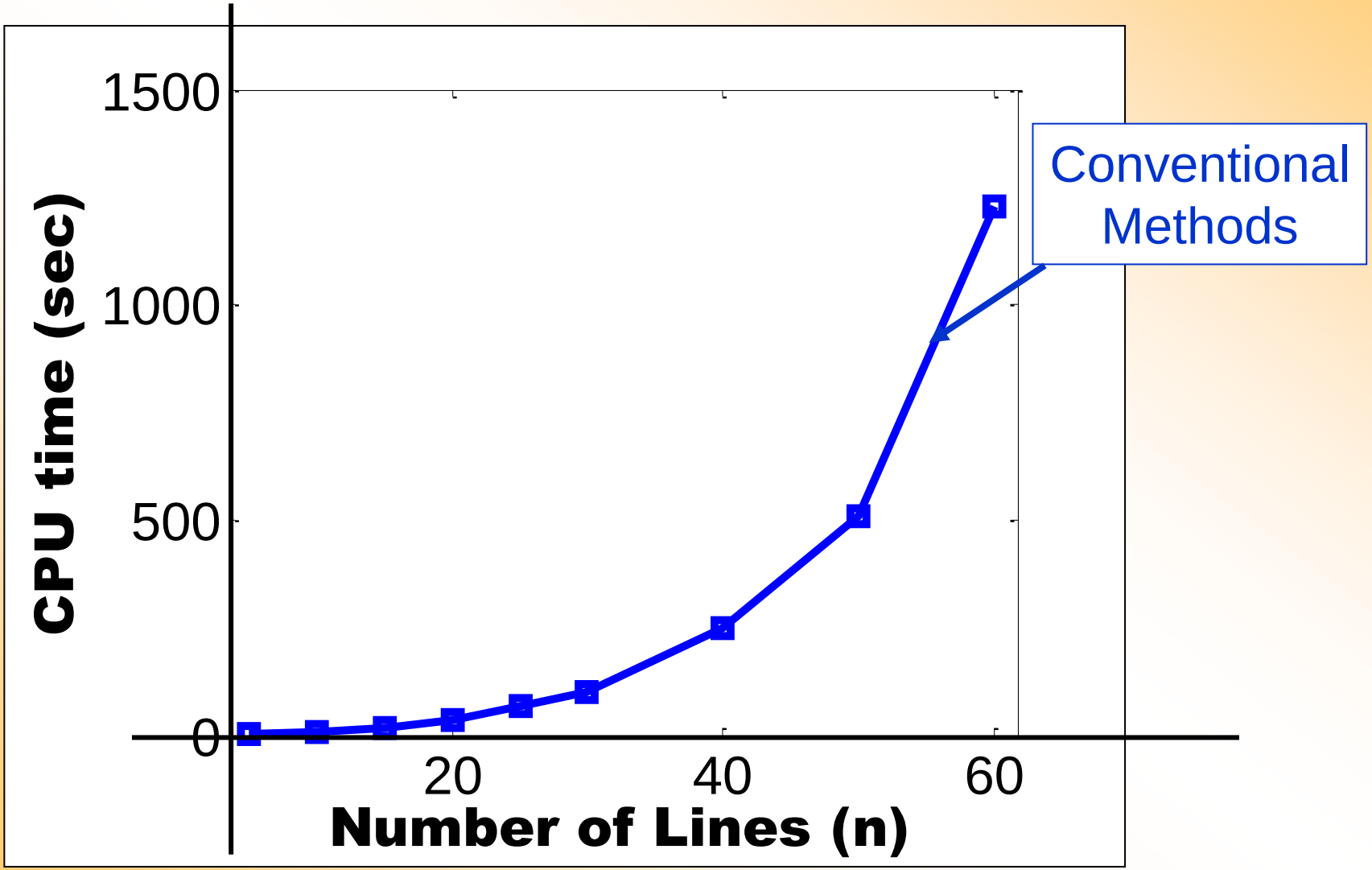
Example 2: 3 Line, Active terminations, Trapezoidal Incidence



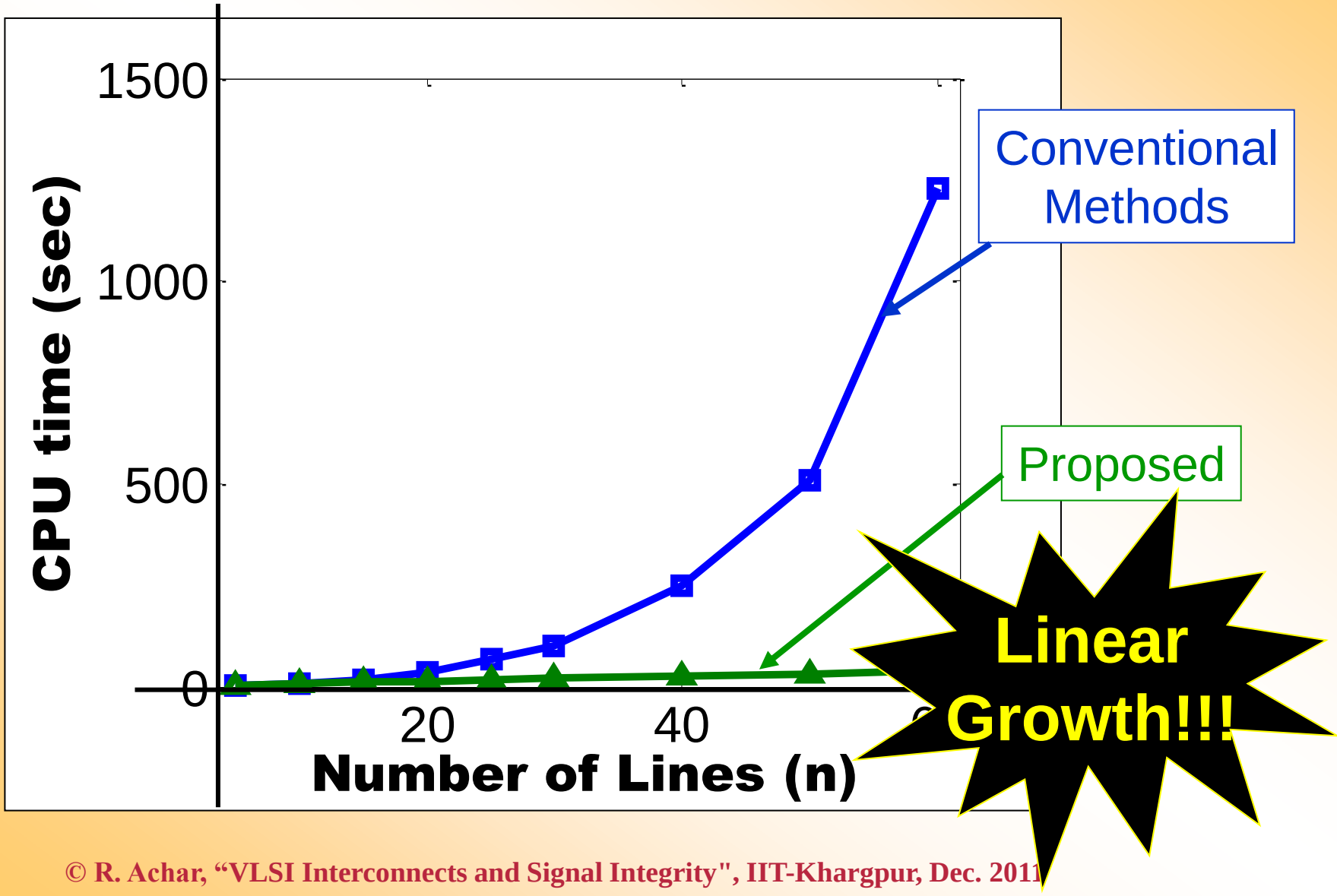
Example: WR+TP + EMI



Example: WR+TP + EMI



Example: Complexity Analysis



Agenda

Advanced Interconnect Modeling Methods

- MoC, MRA, DEPACT
- WR+TP. EMI
- Tabulated Data Macromodeling:
  - Parallelization, GVF

Conclusions

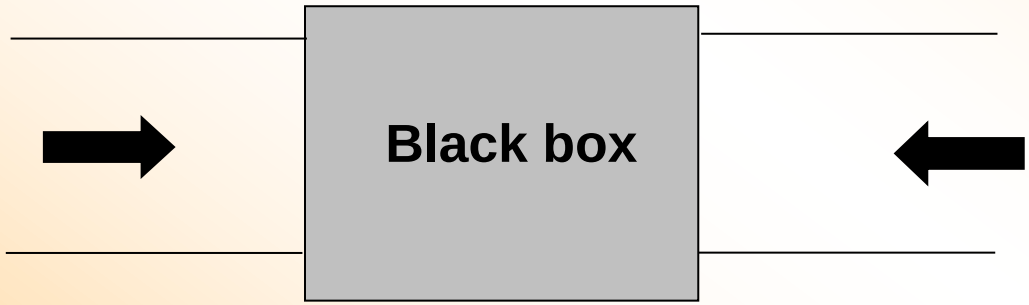
Why measured/simulated data

At high frequencies, many complex electrical devices may have no analytical models

Example: 3D transmission lines, vias, packages
non-uniform transmission lines
on-chip passive devices

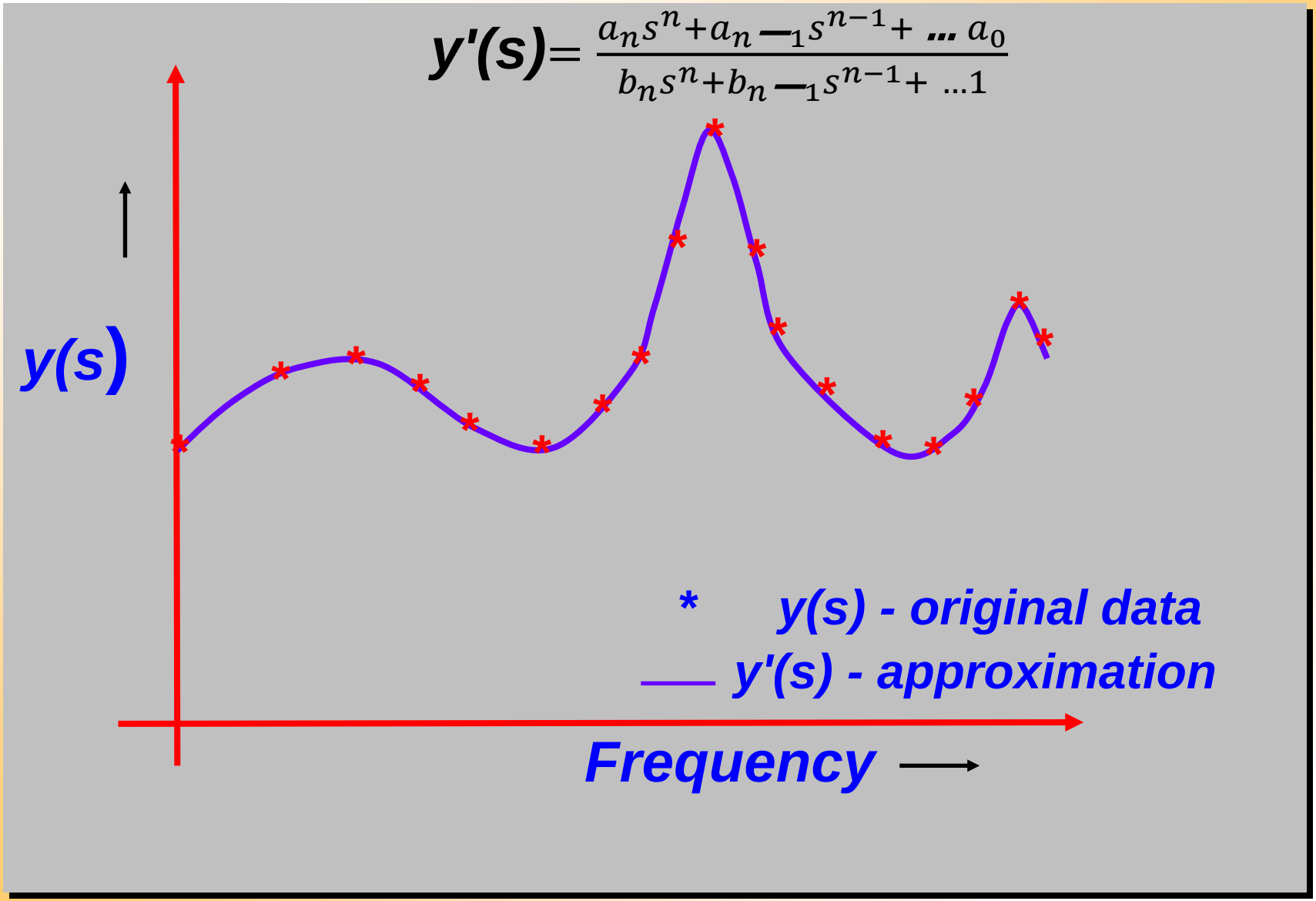
➔ **characterized by tabulated data in terms of multiport Terminal parameters**

To identify a system for circuit simulations



- ***Impedance* parameters *or Z-parameters***
- ***Admittance parameters or Y-parameters***
- ***Hybrid parameters or H-parameters***
- ***Scattering parameters or S-parameters***

System identification via Direct Curve Fitting



System identification via Direct Curve Fitting

$$f(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \ldots a_0}{b_n s^n + b_{n-1} s^{n-1} + \ldots 1}$$

When written for many freq pts

$$\begin{bmatrix} s_1^n & s_1^{n-1} & \ldots 1 & -f(s_1)s_1^n & -f(s_1)s_1^{n-1} & \ldots -f(s_1)s_1 \\ s_2^n & s_2^{n-1} & \ldots 1 & -f(s_2)s_2^n & -f(s_2)s_2^{n-1} & \ldots -f(s_2)s_2 \\ . & . & . & . & . & . \\ . & . & . & . & . & . \\ s_i^n & s_i^{n-1} & \ldots 1 & -f(s_i)s_i^n & -f(s_i)s_i^{n-1} & \ldots -f(s_i)s_i \end{bmatrix} \begin{bmatrix} a_n \\ a_{n-1} \\ . \\ a_0 \\ b_n \\ b_{n-1} \\ . \\ b_1 \end{bmatrix} = \begin{bmatrix} f(s_1) \\ f(s_2) \\ . \\ . \\ . \\ f(s_i) \end{bmatrix}$$

System identification via Direct Curve Fitting

- ill-conditioned
- Can not achieve Higher-Order Approximations

Solution ➔ Vector fitting algorithm

Original paper: **B. Gustavsen and A. Semlyen, "Rational Approximation of Frequency Domain Responses by Vector Fitting, *" IEEE Transactions on Power Delivery,* vol. 14, no. 3, pp. 1052-1061, July 1999.**

$$f(s) = \sum_{n=1}^{N} \frac{\tilde{r}_n}{s - p_n} + d + se$$

➔ **Continuously refined and evolved over last 20+ years**

VF – an Iterative Algorithm

Assume an initial set of poles and a scaling function

Data → $$f(s) = \sum_{n=1}^{N} \frac{\tilde{r}_n}{s - p_n} + d + se$$

initial guess of Poles

Scaling function → $$\sigma(s) = \sum_{n=1}^{N} \frac{c_n}{s - \bar{p}_n} + 1$$

Same Poles

Scaled function → $$\sigma(s) f(s) \cong \sum_{n=1}^{N} \frac{\tilde{c}_n}{s - \bar{p}_n} + d + se$$

Substituting for $\sigma(s)$ **and writing the eq. at k frequency points**

Step1:Computation of Poles

Therefore, for *k* frequency points $AX=b$ **where,**

$$A=\begin{bmatrix} \frac{1}{s_1-\bar{p}_1} & \cdots & \frac{1}{s_1-\bar{p}_N} & 1 & s_1 & \frac{-f(s_1)}{s_1-\bar{p}_1} & \cdots & \frac{-f(s_1)}{s_1-\bar{p}_N} \\ \frac{1}{s_2-\bar{p}_1} & \cdots & \frac{1}{s_2-\bar{p}_N} & 1 & s_2 & \frac{-f(s_2)}{s_2-\bar{p}_1} & \cdots & \frac{-f(s_2)}{s_2-\bar{p}_N} \\ \cdots & & \cdots & \cdots & & \cdots & \cdots & \cdots \\ \frac{1}{s_k-\bar{p}_1} & \cdots & \frac{1}{s_k-\bar{p}_N} & 1 & s_k & \frac{-f(s_k)}{s_k-\bar{p}_1} & \cdots & \frac{-f(s_k)}{s_k-\bar{p}_N} \end{bmatrix} \quad b=\begin{bmatrix} f(s_1) \\ f(s_2) \\ \vdots \\ f(s_k) \end{bmatrix}$$

$$X=\begin{bmatrix} \tilde{c}_1 & \cdots & \tilde{c}_N & d & e \end{bmatrix}\begin{bmatrix} c_1 & \cdots & c_N \end{bmatrix}^T$$

Scaled function residues

Scaling function residues

overcomes ill conditioning !!!

Computation of zeros of $\sigma(s)$: Real Case

With, $X = [\tilde{c}_1 \quad \dots \quad \tilde{c}_n \quad d \qquad e \quad c_1 \quad \dots \quad c_N]^T$ **known from AX=b**

Refined poles for the next iteration can be obtained in terms of the zeros of $\sigma(s)$

Zeros $\bar{z}_n$ of $\sigma(s)$ are the eigenvalues of the matrix

$$\boldsymbol{H = A - B\,C^T}$$

$$\boldsymbol{A} = \begin{bmatrix} \bar{a}_1 & & & \\ & \bar{a}_2 & & \\ & & . & \\ & & & \bar{a}_n \end{bmatrix} \qquad \boldsymbol{B} = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \qquad \boldsymbol{C} = \begin{bmatrix} c_1 \\ c_2 \\ \vdots \\ c_n \end{bmatrix}$$

Computation of Poles: Multiport Case

$$Y(s) = \begin{bmatrix} Y_{11} & Y_{12} & \dots & Y_{1P} \\ Y_{21} & Y_{22} & \dots & Y_{2P} \\ \dots & \dots & \dots & \dots \\ Y_{P1} & Y_{P2} & \dots & Y_{PP} \end{bmatrix};$$

To be modelled through VF

$$Y(s) = \begin{bmatrix} \sum_{n=1}^{N} \frac{\tilde{c}_n^{1,1}}{s-\bar{p}_n} + d^{1,1} & \sum_{n=1}^{N} \frac{\tilde{c}_n^{1,2}}{s-\bar{p}_n} + d^{1,2} & \dots & \sum_{n=1}^{N} \frac{\tilde{c}_n^{1,p}}{s-\bar{p}_n} + d^{1,P} \\ \sum_{n=1}^{N} \frac{\tilde{c}_n^{2,1}}{s-\bar{p}_n} + d^{2,1} & \sum_{n=1}^{N} \frac{\tilde{c}_n^{2,2}}{s-\bar{p}_n} + d^{2,2} & \dots & \sum_{n=1}^{N} \frac{\tilde{c}_n^{2,p}}{s-\bar{p}_n} + d^{2,P} \\ \dots & \dots & \dots & \dots \\ \sum_{n=1}^{N} \frac{\tilde{c}_n^{P,1}}{s-\bar{p}_n} + d^{P,1} & \sum_{n=1}^{N} \frac{\tilde{c}_n^{P,2}}{s-\bar{p}_n} + d^{P,2} & \dots & \sum_{n=1}^{N} \frac{\tilde{c}_n^{p,p}}{s-\bar{p}_n} + d^{P,P} \end{bmatrix}$$

➔ **A. Chinea and S. Grivet-Talocia, "On the Parallelization of Vector Fitting Algorithms", *IEEE Trans. on Components, Packaging and Manufacturing Technology*, vol. 1, no. 11, November 2011.**

Review of Parallel VF for Multi-CPU Environment

$$\begin{bmatrix} \boldsymbol{\Phi}_1 & 0 & \cdots & 0 & \tilde{\boldsymbol{\Phi}}_1 \\ 0 & \boldsymbol{\Phi}_2 & 0 & 0 & \tilde{\boldsymbol{\Phi}}_2 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \boldsymbol{\Phi}_{P^2} & \tilde{\boldsymbol{\Phi}}_{P^2} \end{bmatrix} \begin{bmatrix} \tilde{c}_1 \\ \vdots \\ \tilde{c}_{P^2} \\ \hat{\boldsymbol{c}} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

$$\tilde{A}_1 = \alpha_1 [\boldsymbol{\Phi}_1 \quad \tilde{\boldsymbol{\Phi}}_1] \quad \Rightarrow \quad \textit{Define} \quad A_1 = \begin{bmatrix} real(\tilde{A}_1) \\ Img(\tilde{A}_1) \end{bmatrix}$$

$$\tilde{A}_2 = \alpha_2 [\boldsymbol{\Phi}_2 \quad \tilde{\boldsymbol{\Phi}}_2]$$

$$\vdots$$

$$\tilde{A}_l = \alpha_l [\boldsymbol{\Phi}_l \quad \tilde{\boldsymbol{\Phi}}_l] \quad \Rightarrow \quad A_l = \begin{bmatrix} real(\tilde{A}_l) \\ Img(\tilde{A}_l) \end{bmatrix}$$

$$\boldsymbol{\alpha}_l = {}^{1}/_{\sqrt{\|\boldsymbol{s}_{l,k}\|}}$$

$$l = (i-1)P + j$$

Splitting Strategies

None Splitting

Uses only one Scaling Function for the Entire *S* matrix

➔ **Leads to a common pole-set**

➔ **CPU1:** $A_1 = [Q_1, R_1]$
CPU2: $A_2 = [Q_2, R_2]$
$\vdots$
CPUT: $A_T = [Q_T, R_T]$

➔

Compute $\hat{c}$ in a single CPU

All Splitting

Uses individual Scaling Function for each *S*-Element

➔ **Leads to individual pole sets for each S-element**

➔ **CPU1:** $A_1 = [Q_1, R_1]$ ➔ $\hat{c}_1$
CPU2: $A_2 = [Q_2, R_2]$ ➔ $\hat{c}_2$
$\vdots$
CPUT: $A_T = [Q_T, R_T]$ ➔ $\hat{c}_T$

GVF: GPU Based Vector Fitting

- Emerging Computing Platform of GPUs
- Thousands of Cores
- Exploit massive parallelization potential

**S. Ganeshan, N. Kumar and R. Achar and W. Lee, "GVF: GPU based Vector Fitting for Modelling of Multiport Tabulated Data Networks", IEEE CPMT, pp. 1375-1387, Aug. 2020.

GVF: GPU based parallel Vector Fitting - *None Splitting Strategy*

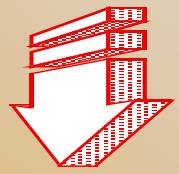
Bulk Transfer from CPU to GPU: S_l, g, α_l

Formulate and transfer to GPU: $\hat{\Phi}$

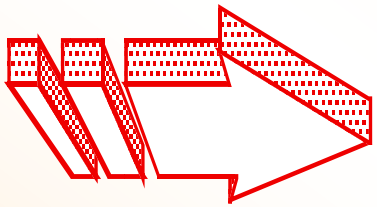
GPU

Formulate: $A_1 \cdots A_{P^2}$

Perform QR: $R_1 \cdots R_{P^2}$ ***(MAGMA)***



Extract: $R_{l_{N\times N}}^{22}$**:** $R_1^{22} \cdots R_{P^2}^{22}$



Collect $R_{l_{N\times N}}^{22}$ **for each** A_l **for evaluation of residues of the scaling function**

GVF: None Splitting Strategy

Approach (a)

Compute: $\hat{c}$

Approach (b)

Bulk Transfer $R_{l_{N\times N}}^{22}$ (P^2elements) from GPU to CPU

GPU

$$\begin{bmatrix} R_1^{22} \\ R_2^{22} \\ \vdots \\ R_{P^2}^{22} \\ \lambda^T \end{bmatrix} \quad [\hat{c}] = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ K \end{bmatrix}$$

CPU

$$\begin{bmatrix} R_1^{22} \\ R_2^{22} \\ \vdots \\ R_{P^2}^{22} \\ \lambda^T \end{bmatrix} \quad [\hat{c}] = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ K \end{bmatrix}$$

Transfer $\hat{c}$ from GPU to CPU

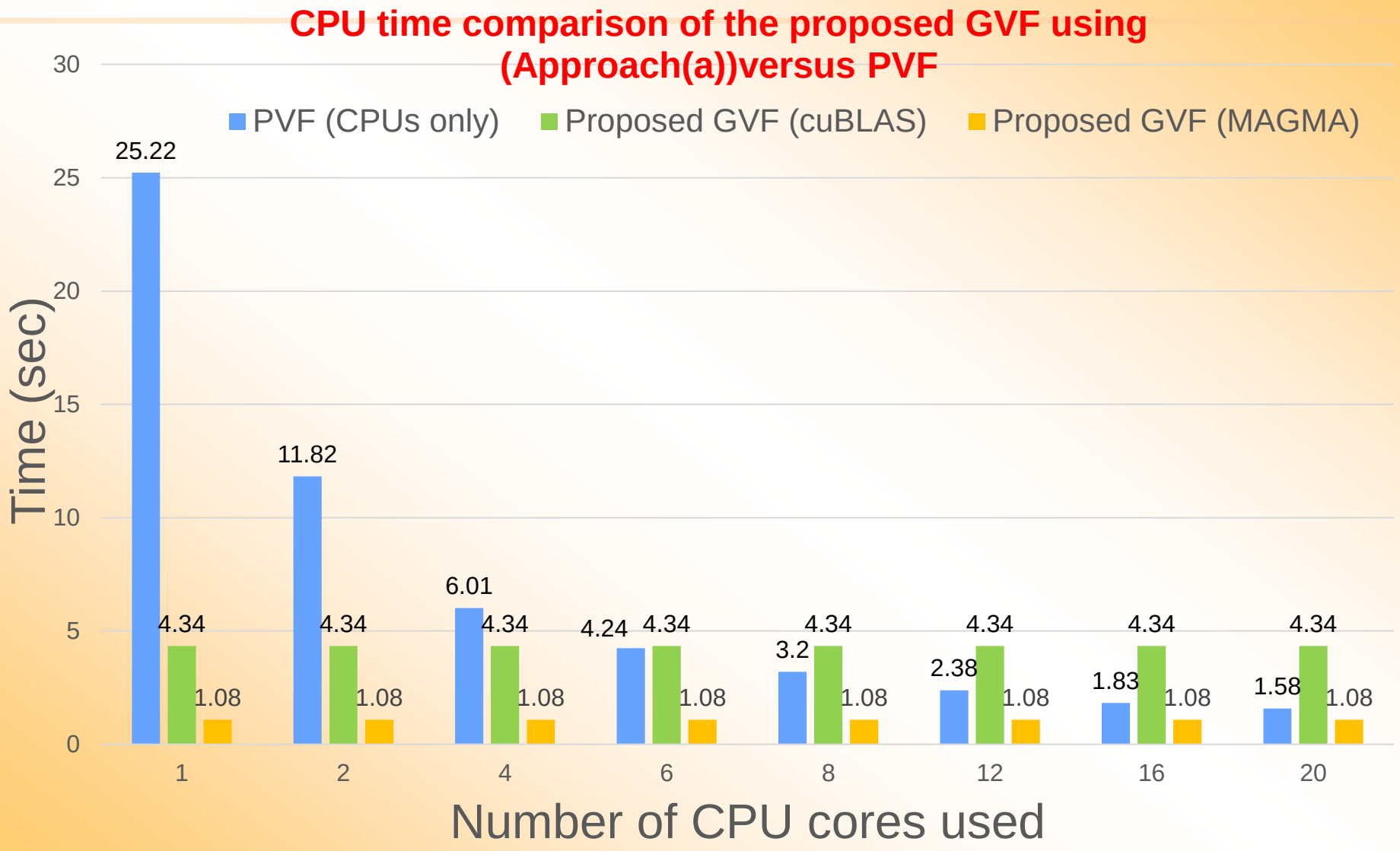
Compute Zeros of the scaling function in a CPU

Example 1 – 60 ports, 70 poles, 1000 Frequency Samples

Size of $\hat{\Phi}$=(1000 x 70) ; $A_l(P^2 = 3600)$ ➔ ***(2000 x 143)***

Cost of individual steps in GVF (Using MAGMA library)	**Time *(msec)*** *(Approach (a))*	**Time *(msec)*** *(Approach (b))*
Transfer of S, g, α from CPU to GPU	20.19	20.19
Formulation of $\hat{\Phi}$ in CPU and transfer to GPU	1.97	1.97
Formulation of A in GPU (*customized)*	0.04	0.04
QR factorization in GPU (MAGMA)	543.09	543.09
R_l^{22} extraction in GPU (*customized)*	0.02	0.02
Transfer back R_l^{22} from GPU to CPU	***56.00***	-
Residue $\hat{c}$ calculation in CPU (LAPACK)	***460.02***	-
Residue $\hat{c}$ calculation in GPU (MAGMA)	-	***562.50***
Transfer back $\hat{c}$ from GPU to CPU	-	***0.03***
Zeros computation in CPU	3.60	3.60
Total Time Taken	***1084.9***	***1131.44***

Example 1 – 60 ports, 70 poles, 1000 Frequency Samples: None Splitting Strategy



GVF: All Splitting Strategy

Bulk Transfer from CPU to GPU:

S_l, g, α_l, p_n

GPU

Formulate: $\hat{\Phi}_1 \cdots \hat{\Phi}_{P^2}$

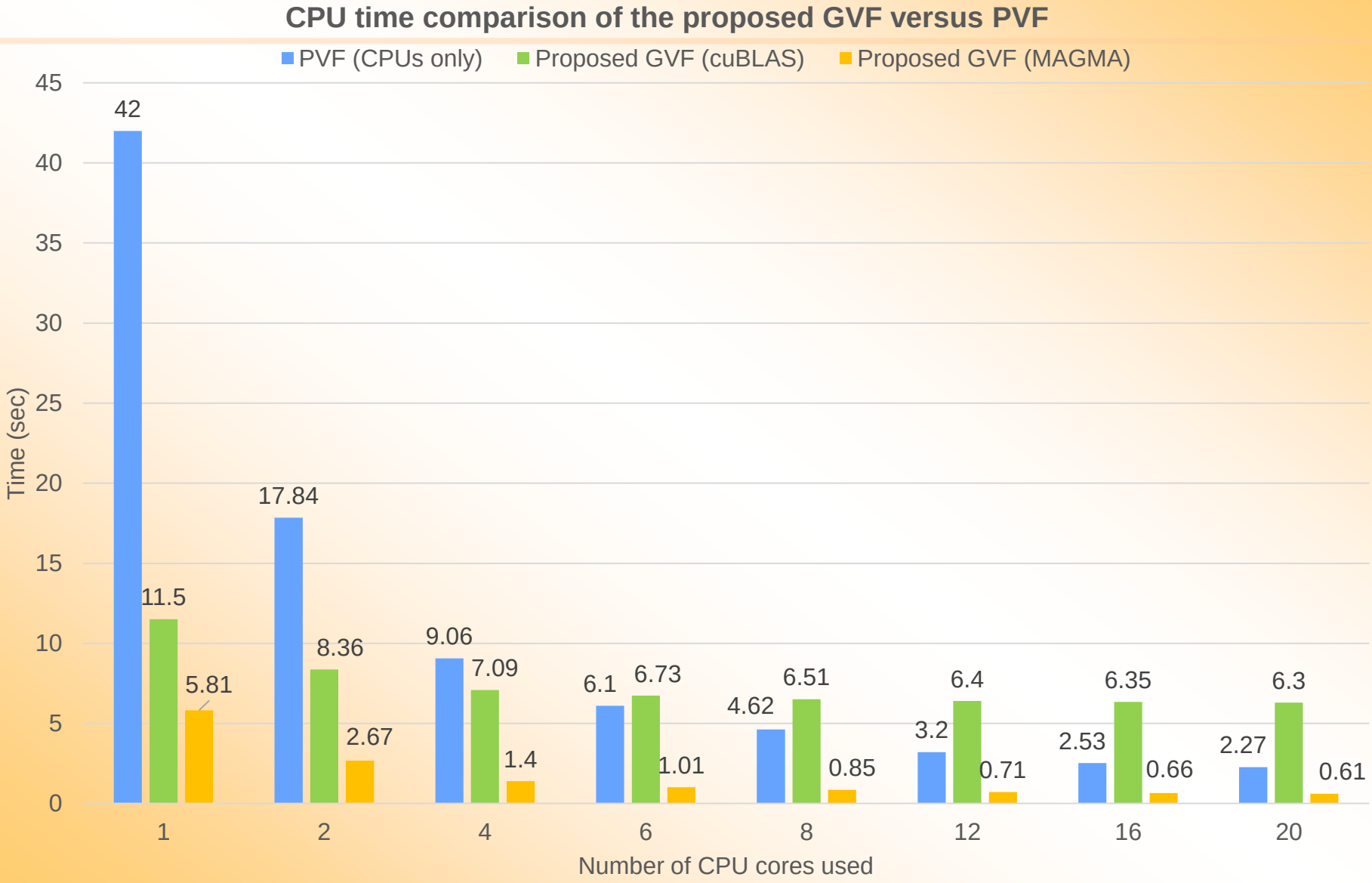
Formulate: $A_1 \cdots A_{P^2}, b_1 \cdots b_{P^2}$

Compute: $A_l^T * A_l, A_l^T * b_l$ ***(MAGMA)***

Evaluate: $\hat{c}_l$

Transfer $\hat{c}_l$ from GPU to CPU

Example 1 – 60 ports, 70 poles, 1000 Frequency Samples: All Splitting Strategy



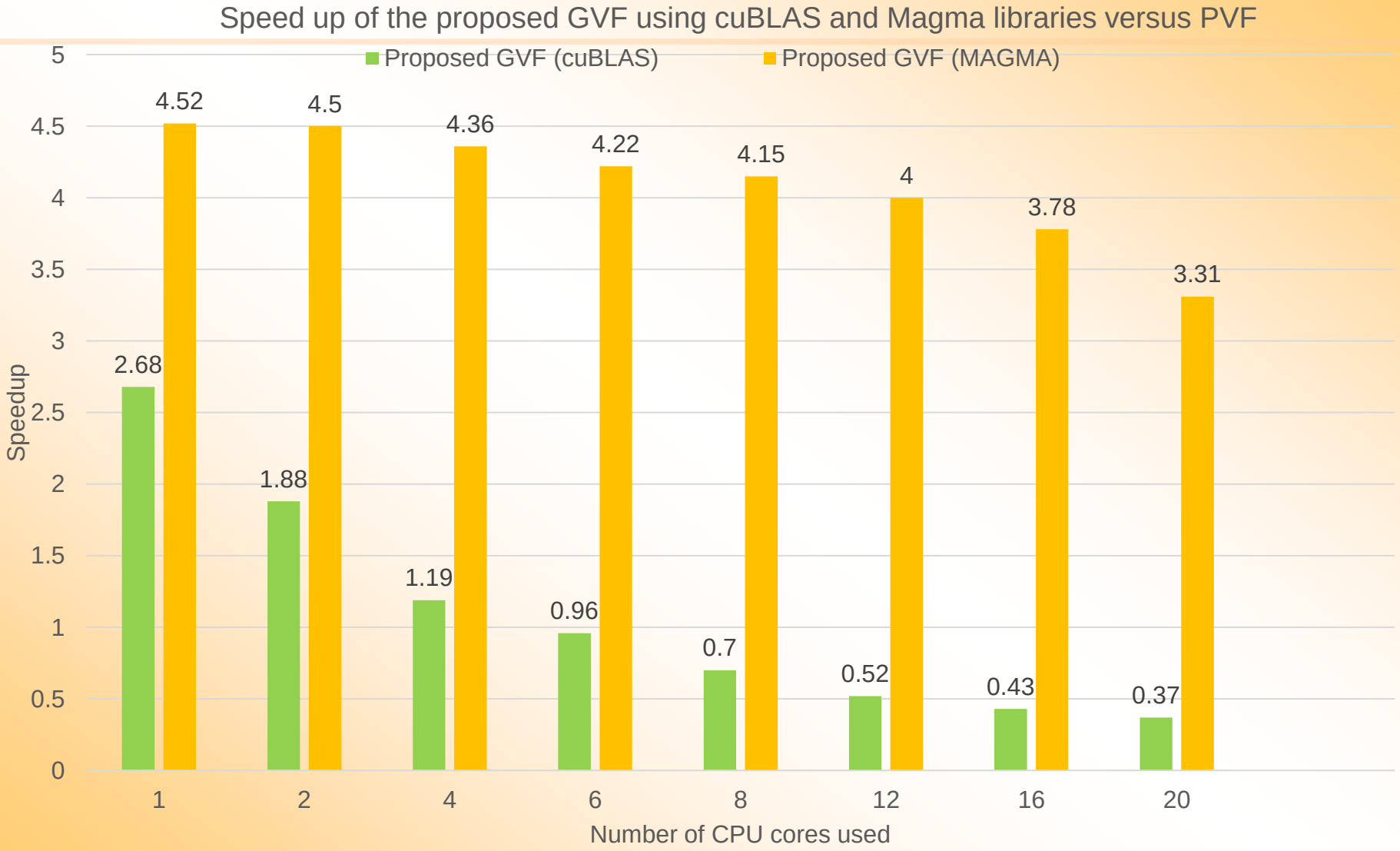
GVF: GPU based Vector fitting algorithm

Example case: 120 ports, 80 poles, 1000 Frequency Samples

All Splitting Strategy

Example	PVF [34] (multi CPU)		Proposed GVF time using *MAGMA* library *(sec)*	Speedup
	# CPU cores used	Time *(sec)*		
#ports = 120 #poles = 80 #fpoints = 1000 #size of $\widehat{\Phi}$=1000 × 80 Total # of Φ_l =14400	1	193.90	**42.86**	**4.52**
	2	95.45	**21.21**	**4.50**
	4	48.40	**11.10**	**4.36**
	6	36.80	**8.72**	**4.22**
	8	25.03	**6.03**	**4.15**
	12	17.71	**4.43**	**4.00**
	16	14.42	**3.81**	**3.78**
	20	12.23	**3.69**	**3.31**

Example 2 – 120 ports, 80 poles, 1000 Frequency Samples: All Splitting Strategy



Conclusions

Advanced Interconnect Modeling and Simulation methods still emerging:

- to meet the fundamental challenges such as passivity
- to be more efficient/accurate
- to meet the high-speed designer's dream of seamless analysis platform for mixed circuit/EM/RF design.