



IEEE Orange County Solid-State Circuits Society (SSCS) Present:
Hardware Security and Safety of IC Chips and Systems
By Professor Makoto Nagata, Kobe University, Kobe, Japan

Day: Tuesday, June 4, 2024

Time: Registration & Networking 6:00 p.m. – 6:30 p.m.
Presentation 6:30 p.m. – 8:00 p.m.
Q&A and Networking 8:00 p.m. – 8:15 p.m.

Fee: Free for all the IEEE & SSCS members, students, engineers in transition, technologists, as well as those who are exploring to join IEEE & SSCS in the future.

Address: Custom Silicon Solutions (CSS), 18021 Cowan, Irvine, CA 92614, USA.

Parking: Free Parking available in the permitted & unmarked spaces.

Abstracts: IC chips are key enablers to a smartly networked society and need to be more compliant to security and safety. For example, semiconductor solutions for autonomous vehicles must meet stringent regulations and requirements. While designers develop circuits and systems to meet the performance and functionality of such products, countermeasures are proactively implemented in silicon to protect against harmful disturbances and even intentional adversarial attacks. This talk will start with electromagnetic compatibility (EMC) techniques applied to IC chips for safety to motivate EMC-aware design, analysis, and implementation. It will discuss IC design challenges to achieve higher levels of hardware security (HWS). Crypto-based secure IC chips are investigated to avoid the risks of side-channel leakages and side-channel attacks, corroborated with silicon demonstrating analog techniques to protect digital functionality. The EMC and HWS disciplines derived from electromagnetic principles are key to establishing IC design principles for security and safety.



Biography: Makoto Nagata (Senior Member, IEEE) received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in electronics engineering from Hiroshima University, Hiroshima, Japan, in 2001.

He was a Research Associate at Hiroshima University from 1994 to 2002, an Associate Professor at Kobe University, Kobe, Japan, from 2002 to 2009, where he was promoted to a Full Professor in 2009.

His research interests include design techniques targeting high-performance mixed analog, RF and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, 2.5D and 3D system integration, as well as their applications for hardware security and hardware safety, and cryogenic electronics for quantum computing.

Dr. Nagata is a Senior Member of IEICE. He has been a member of a variety of technical program committees of international conferences, such as the Symposium on VLSI Circuits (2002–2009), Custom Integrated Circuits Conference (2007–2009), Asian Solid-State Circuits Conference (2005–2009), International Solid-State Circuits Conference (2014–2022), European Solid-State Circuits Conference (since 2020), and many others. He chaired the Technology Directions subcommittee for International Solid-State Circuits Conference (2018–2022) and served for an Executive Committee Member (2023–present). He was the Technical Program Chair (2010–2011), the Symposium Chair (2012–2013), and an Executive Committee Member (2014–2015) for the Symposium on VLSI circuits. He was the IEEE Solid-State Circuits Society (SSCS) AdCom member (2020–2022), the distinguished lecturer (2020–2021 and 2024–present), and currently serves as the chapters vice chair (2022–) of the society. He is an associate editor for IEEE Transactions on VLSI Systems (since 2015).

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Send questions to Farhad Mafie, IEEE-OC SSCS Chairman: FarhadMISC@Gmail.com

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