Compact Modeling of GaN HEMTs for Power and RF Circuit Design

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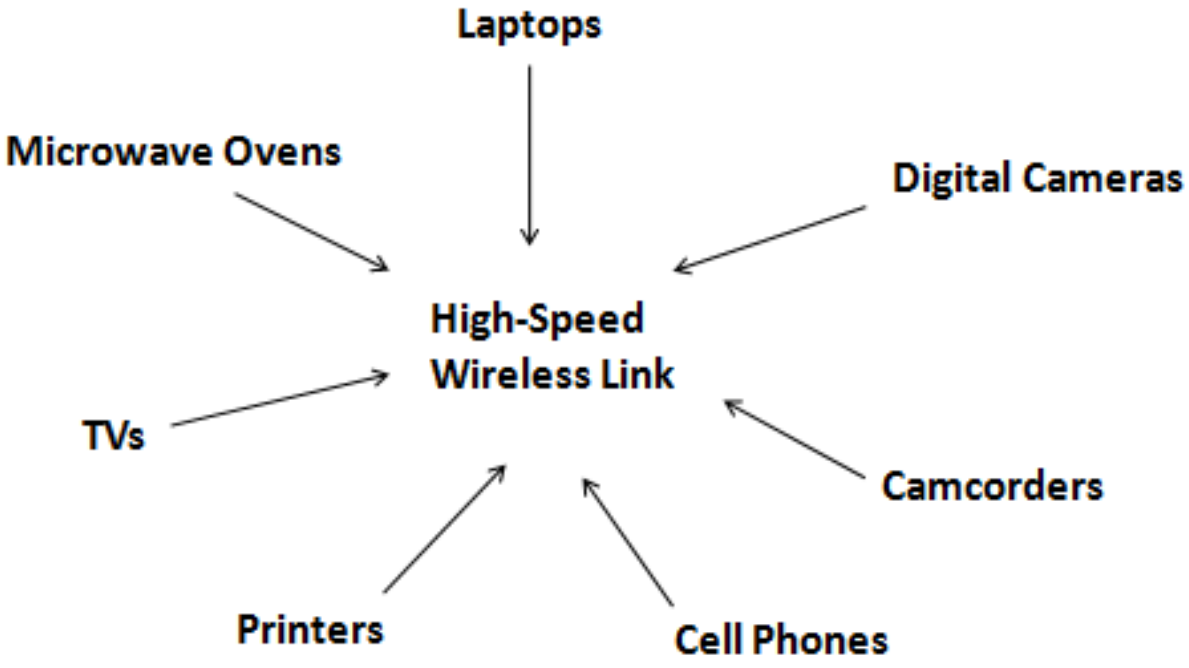
A Wireless World

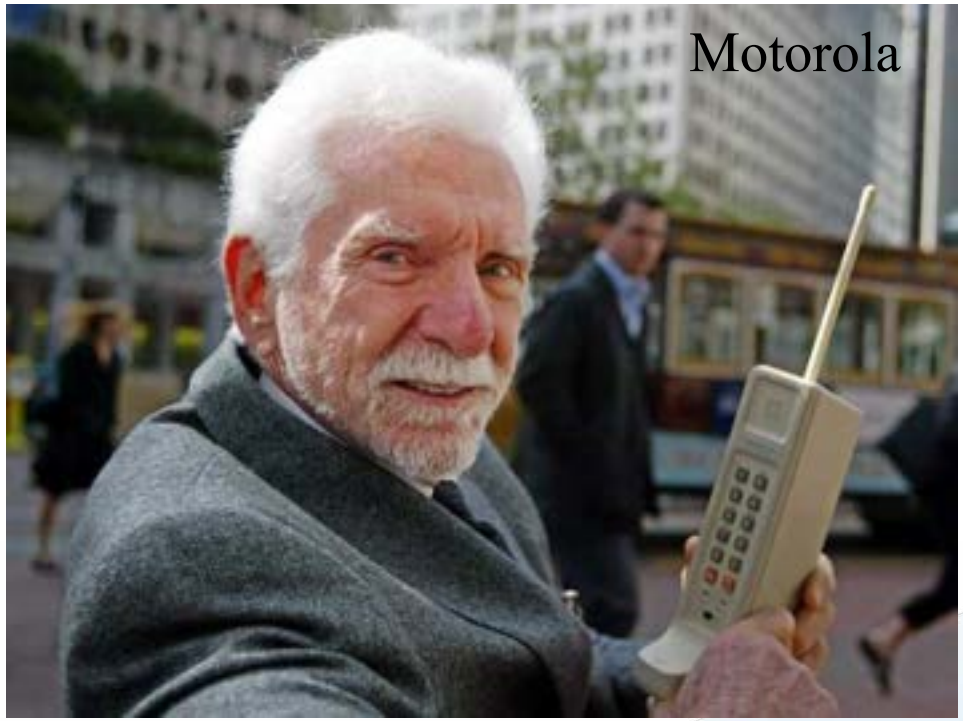


- High-speed wireless links (WiFi, Bluetooth) allow seamless connections among device and appliance.
- Although RF design always talks about wireless transmission, all concepts are valid for wired transmission.

Evolution of Mobile Wireless Communication

Early wireless devices

An old car phone (1940)



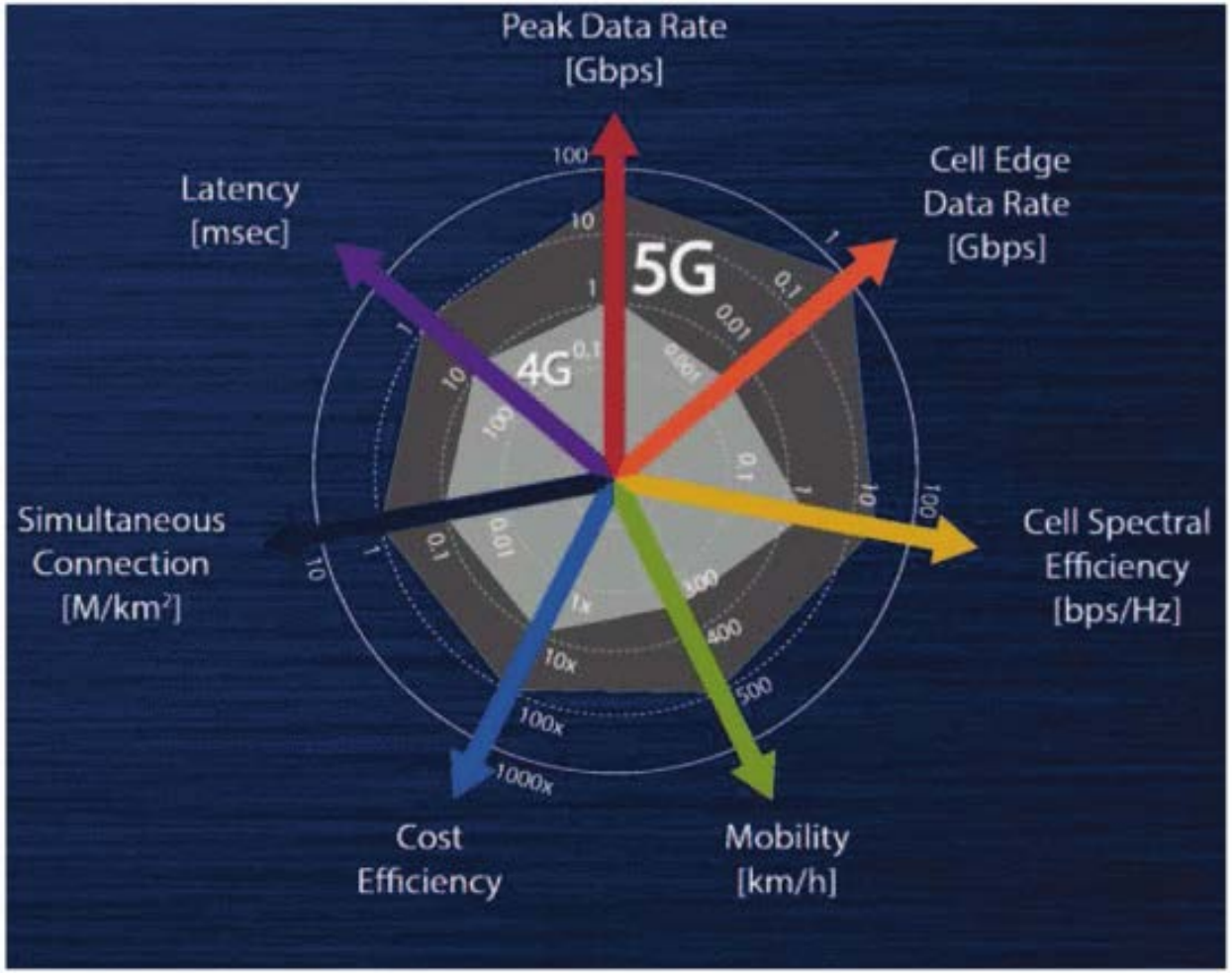
First Hand held cell phone (1973)

Evolution of Mobile Wireless Communication

Generation	Speed	Technology	Key Features
1G (1970 –1980s)	14.4 Kbps	AMPS,NMT, TACS	Voice only services
2G (1990 to 2000)	9.6/ 14.4 Kbps	TDMA,CDMA	Voice and Data services
2.5G to 2.75G (2001-2004)	171.2 Kbps 20-40 Kbps	GPRS	Voice, Data and web mobile internet, low speed streaming services and email services.
3G (2004-2005)	3.1 Mbps 500- 700 Kbps	CDMA2000 (1xRTT, EVDO) UMTS and EDGE	Voice, Data, Multimedia, support for smart phone applications, faster web browsing, video calling and TV streaming.
3.5G (2006-2010)	14.4 Mbps 1-3 Mbps	HSPA	All the services from 3G network with enhanced speed and more mobility.
4G (2010 onwards)	100-300 Mbps. 3-5 Mbps 100 Mbps (Wi-Fi)	WiMax, LTE and Wi-Fi	High speed, high quality voice over IP, HD multimedia streaming, 3D gamming, HD video conferencing and worldwide roaming.
5G (Expecting at the end of 2019)	1 to 10 Gbps	LTE advanced schemes, OMA and NOMA	Super fast mobile internet, low latency network for mission critical applications, Internet of Things, security and surveillance, HD multimedia streaming, autonomous driving, smart healthcare applications.

www.rfpage.com

What's so special in 5G

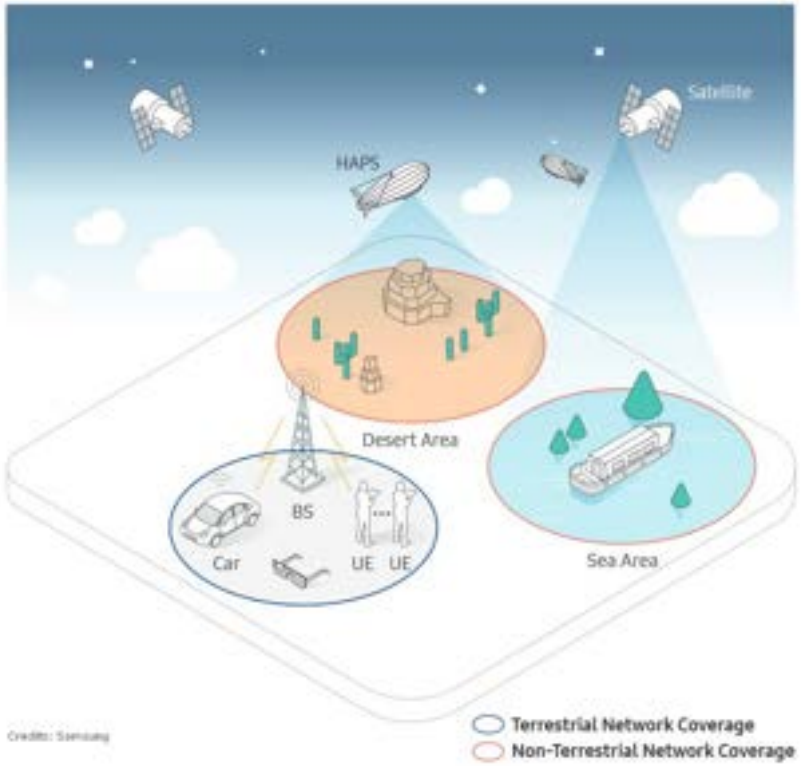


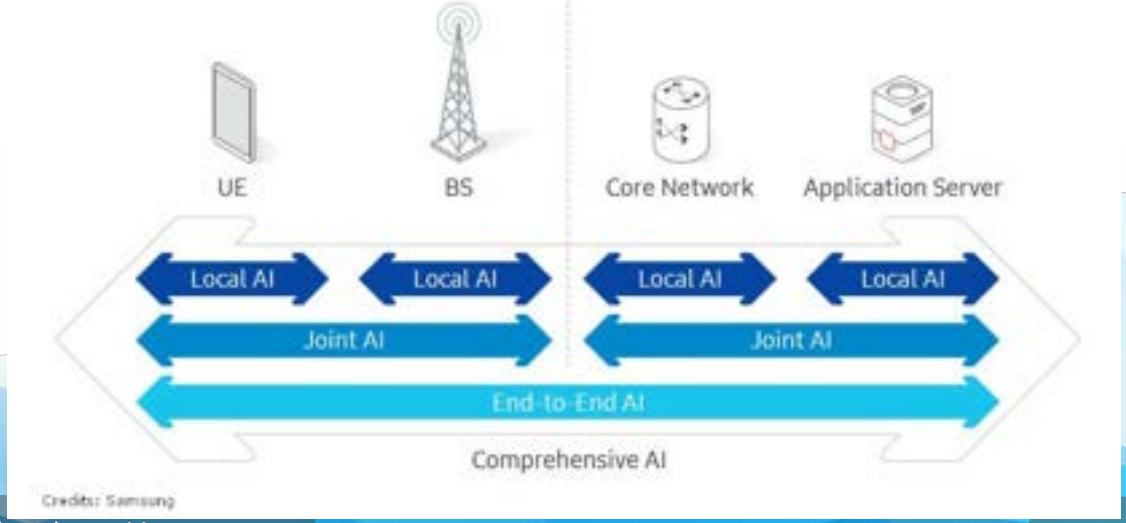
- Frequency bands – sub-6GHz and 28GHz
- 5G small cell
  - Qorvo and Peregrine Semi are offering solutions using SOI technology.
    - Average power of 5-6 W
  - Lower power will limit the coverage area of small cells, restricting its use in cities.
- Solution – GaN technology
  - Enables high power modules for data transmission.

Ref. – A. Niknejad, CICC 2015

6G?

- Research on 6G
- Applications
  - Artificial Intelligence (AI)
  - Extended Reality (XR)
  - Automation
  - Robotics
- 6G requires massive performance improvements as compared to 5G.
- 5G speed - 20 Gbps and frequencies up to 100 GHz
- 6G - 1000 Gbps and may utilize frequencies up to 3 THz





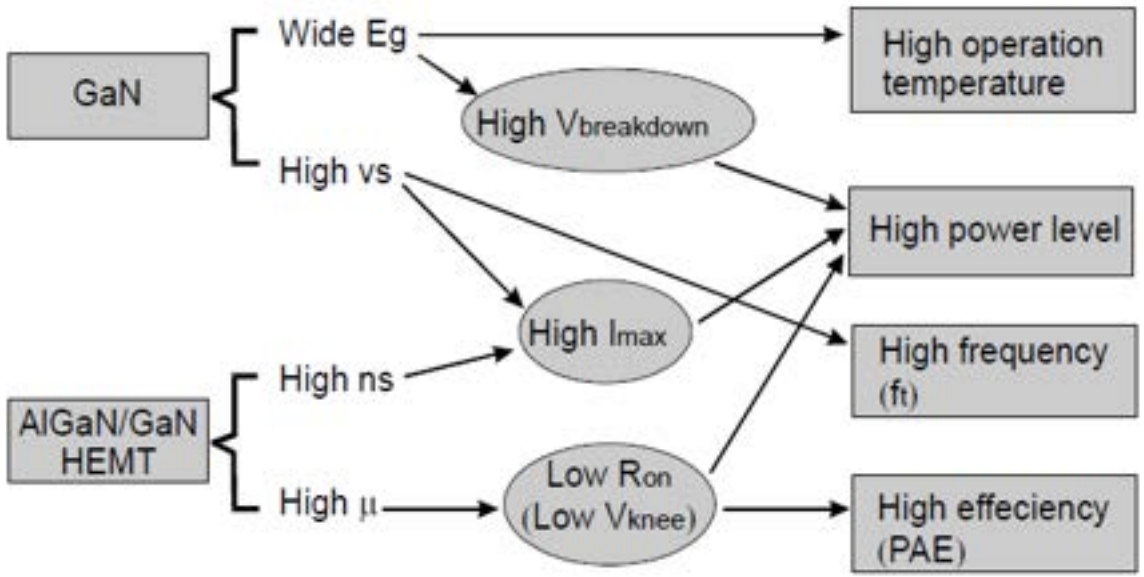
GaN Properties

	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.1	1.42	3.26	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0
μ_n (cm^2/Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)
v_{sat} (10^7cm/s)	1.0	1.0	2.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3
$JM = \frac{E_{br} v_{sat}}{2\pi}$	1	2.7	20	27.5

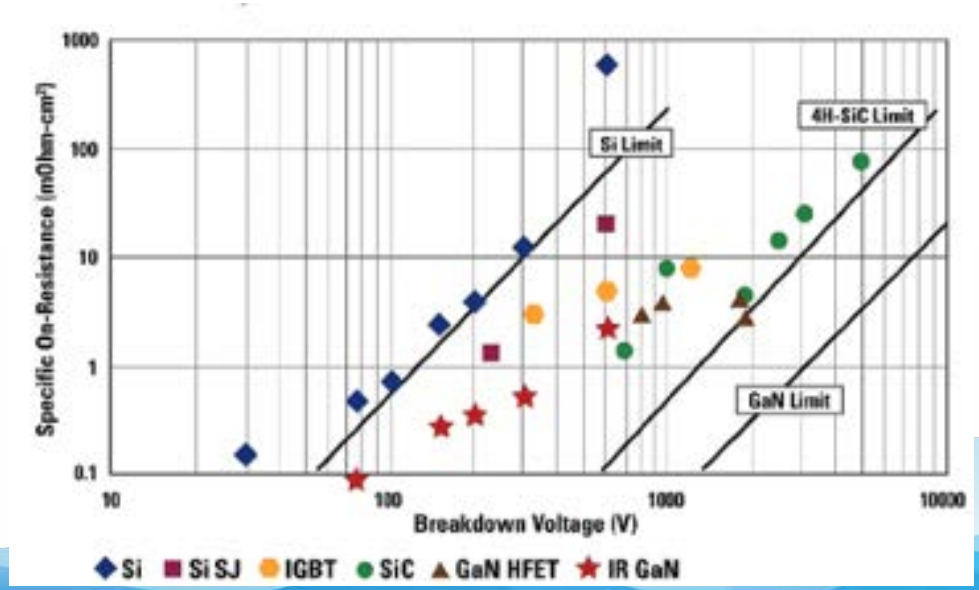
[1]

Johnson's figure of merit (rel. to Si)

Comparison of Material Properties & respective FoMs



[2]



[1] U. K. Mishra *et al.*, *Proc. IEEE*, **96 (2),** [2008]

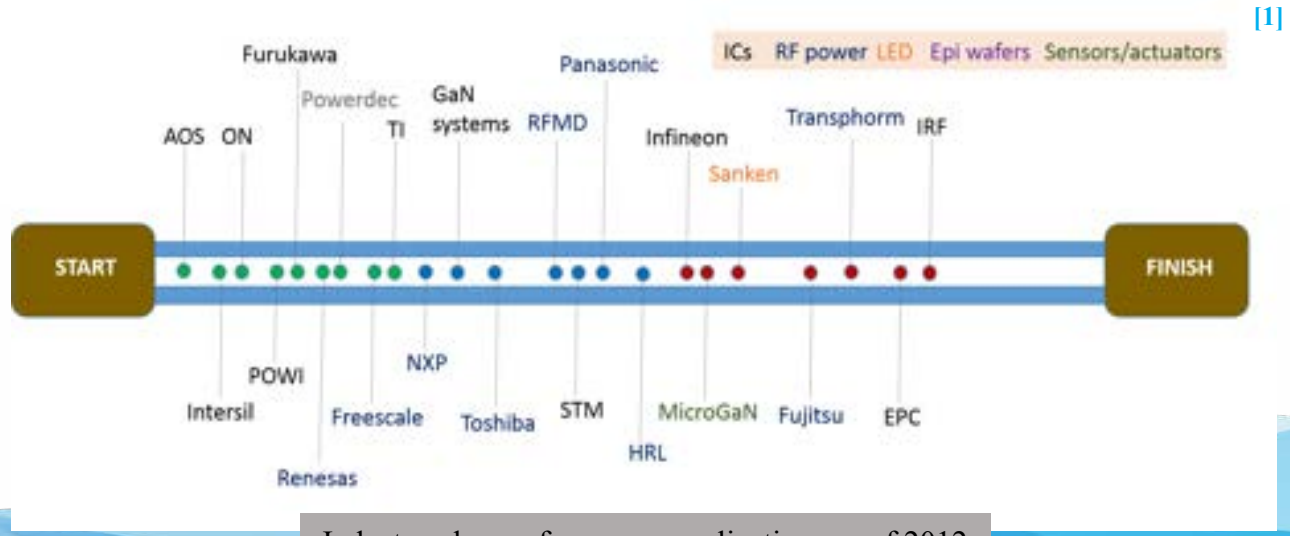
[2] M. A. Briere, Tech. Rep., International Rectifier, Dec. [2008]

GaN Attractions & Avenues

Size comparison of Si power MOSFET with GaN HEMT from EPC for same performance

Size comparison of RF HEMTs based on GaAs and GaN technologies from Qorvo

[1]



Industry players for power applications as of 2012

[1] S. Levin, Tech. Rep., Power Petrov Group, [2013]

Contents

- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
- Modeling Power Devices using ASM-HEMT
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

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Nanolab: Characterization and Modeling Capabilities

- *About Nanolab*
- *Hardware Capabilities*
- *EDA Capabilities*

About Nanolab: Some Stats

Funding

- Government Agencies
- Industry Partners
- Compact Model Coalition (CMC)

Publications

	2020	2019	2018	2017	2016	2015
Books		1				1
Journal	16	14	20	19	18	9
Conference	9	15	19	11	30	30

Current Members

- Postdoc – 5
- Ph.D. – 27
- Ten PhDs graduated

About Nanolab: Collaborations

Berkeley UNIVERSITY OF CALIFORNIA

University of South Florida

Tagore Technology

ims BORDEAUX

अंतरिक्ष विभाग DEPARTMENT OF SPACE

Department of Science & Technology, Government of India

intel

MaxLinear

Applied Materials

AMCAD Engineering
Advanced Modeling for Computer-Aided Design

tsmc

SILVACO

KIT Karlsruher Institut für Technologie

Analog Devices

Texas Instruments

UIC UNIVERSITY OF ILLINOIS AT CHICAGO

Keysight Technologies

Synopsys®

cadence™

About Nanolab: Areas of Research

Atomistic Simulation

Strong compute and storage infrastructure for atomistic simulations - paving the way for first principle studies of materials. Research topics include materials like VO2, V2O5, black phosphoros, TMDs like MoS2, phosphorene, borophene among many others.

DC and RF Device Characterization

State-of-the-art equipment for DC and RF characterization of packaged and on-wafer devices. High power measurement capabilities coupled with pulsed IV/RF and load pull systems allow for characterizations of higher level circuits like power amplifiers.

SPICE/Compact Modeling

Strong collaboration with the industry in terms of model development. Working closely with UC Berkeley to maintain and develop the BSIM standard models. Out ASM-HEMT model for GaN-HEMTs was recently recognized as an industry standard by the Compact Model Coalition (CMC)

RF Circuit Design

Hardware and software capabilities to design and implement prototypes for RF circuits. Power Amplifier and Low Noise Amplifier design using advanced device technologies.

Hardware Capabilities I

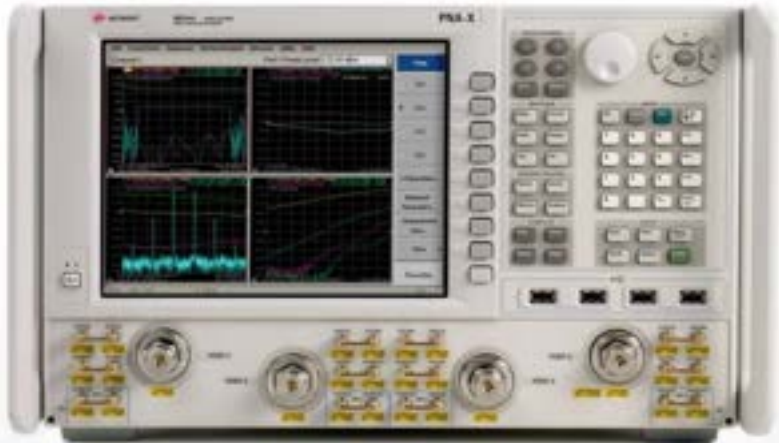
Keysight Semiconductor Device Analyzer (B1500A) Measurement capabilities:

- IV, CV, pulse/dynamic IV range of 0.1 fA - 1 A / 0.5 µV - 200 V
- Evaluation of devices, materials, semiconductors, active/passive components
- AC capacitance measurement in multi frequency from 1 kHz to 5 MHz
- Pulsed IV measurement min 10 ns gate pulse width with 2 ns rise and fall times with 1 µs current measurement resolution

Maury Microwaves/AMCAD AM3221

- Bipolar ±25V/1A (gate) and high-voltage 250V/30A (drain) models
- Pulse widths down to 200ns
- Synchronized pulsed S-parameter measurements
- Connect systems in series for synchronizing 3+ pulsed channels
- Long pulses into the tens and hundreds of seconds for trapping and thermal characterization

Hardware Capabilities II



Keysight ENA (E5071C) 100KHz to 8.5 GHz

- 9 kHz to 4.5/6.5/8.5/14/20 GHz
- 2- or 4-port, 50-ohm, S-parameter test set
- Improve accuracy, yield and margins with wide dynamic range 130 dB, fast measurement speed 8ms and excellent temperature stability 0.005 dB/°C

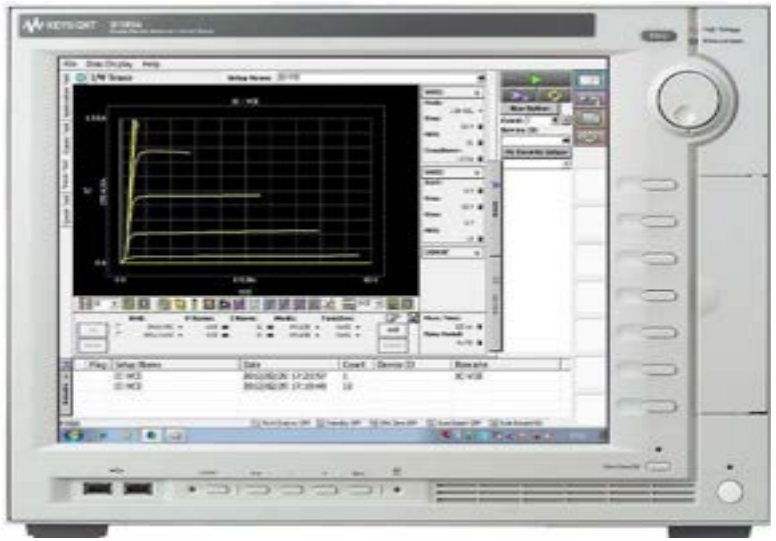
Keysight PNA-X (N5244A) 10 MHz to 43.5 GHz

- High Frequency Device Characterization (Microwave Network Analyzer)
- 100Khz to 8.5 GHz and 10 MHz to 43.5 GHz
- 2-port and 4-ports with two built-in sources
- High output power (+16 dBm)
- Best dynamic accuracy: 0.1 dB compression with +15 dBm input power at the receiver
- Low noise floor of -111 dBm at 10 Hz IF bandwidth

Hardware Capabilities III

Keysight Power Device Characterization System: B1505

- Power device characterization up to 1500 A & 10 kV
- Medium current measurement with high voltage bias (e.g. 500 mA at 1200 V)
- μΩ on-resistance measurement capability
- Accurate, sub-picoamp level, current measurement at high voltage bias
- Fully automated Capacitance measurement at up to 3000 V of DC bias
- High power pulsed measurements down to 10 μs
- High voltage/high current fast switch option to characterize GaN current collapse effect
- Fully automated thermal testing from -50 ℃ to +250 ℃



Keysight N8975B Noise Figure Analyzer

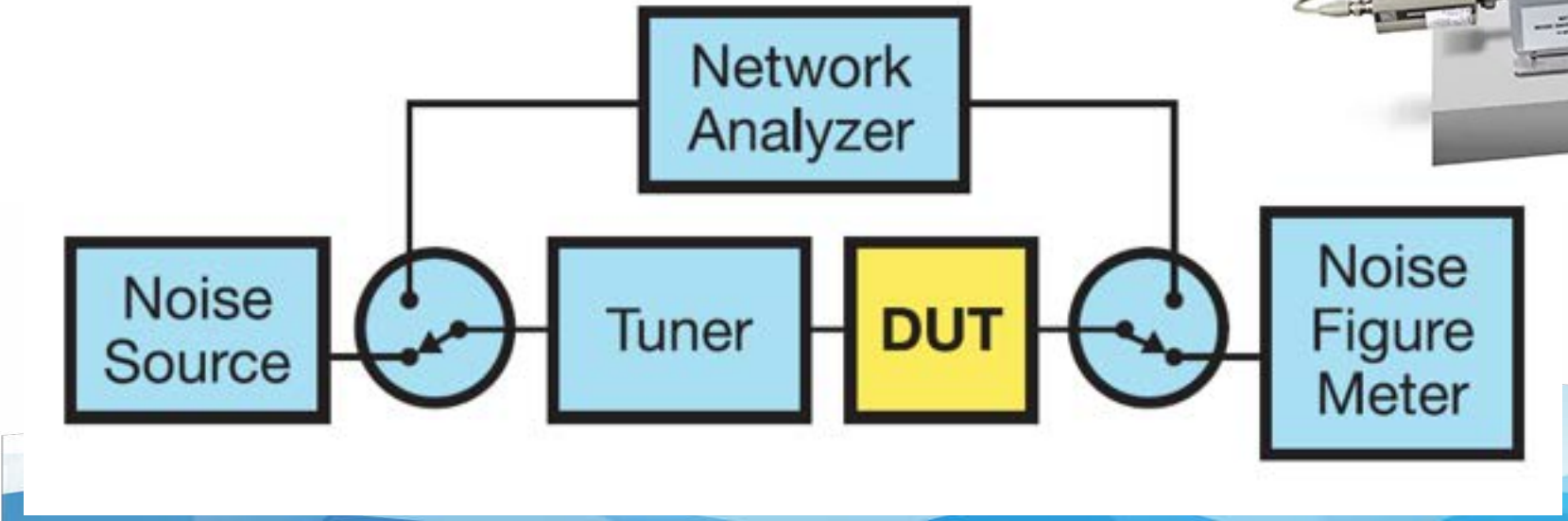
- Frequency range 10 MHz to 26.5 GHz in a one-box solution
- Includes Spectrum Analyzer and IQ Analyzer (Basic) modes
- SNS series noise source N4002A
- U7227C 100 MHz to 26.5 GHz External USB Preamplifier included

Load Pull Characterization

Maury Load Pull Characterization system

- A fundamental passive load pull system capable of performing load pull characterization up to 15W.
- XT982GL01 – 0.6 to 18 GHz Load tuner
- Plan to expand to a 3 harmonic hybrid load pull system soon.

Thermal Noise Characterization



EDA Capabilities

SPICE SIMULATORS

synopsys HSPICE®

cādence

Advanced Design System

cādence

Advanced Design System

Microwave Office

RF

TCAD

COMSOL

SILVACO

synopsys®

IC-CAP

Device Characterization and Modeling Software

Atomistic Simulations

Quantum Wise

nextnano

High-Frequency Characterization

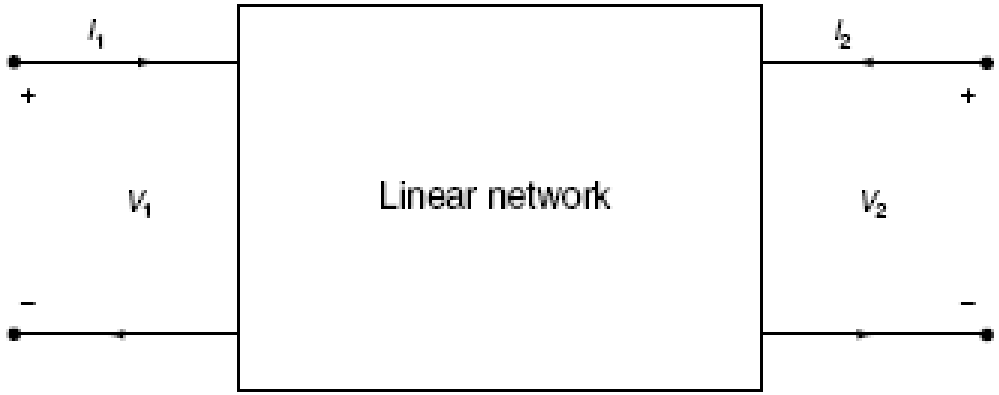
High-Frequency Characterization

- We seek to model the linear (small-signal) behavior of a device subject to a high-frequency test signal

- Such behavior is typically summarized by the N-port network parameters of the device
  - Impedance parameters (Z-Parameters)
  - Admittance parameters (Y-Parameters)
  - Hybrid parameters (H-Parameters)
  - Scattering parameters (S-Parameters)

- Focus on 2-port networks, which we can measure with our lab equipment

Network Analysis basics



Z-Parameters

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$Z_{ij} = \left.\frac{V_i}{I_j}\right|_{I_k=0\, for\, k\neq j}$$

Z_{ij} found by driving port *j* with current I_j, open-circuiting all other ports, & measuring open-circuit voltage at port *i*

Y-Parameters

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0\, for\, k\neq j}$$

Y_{ij} found by driving port *j* with voltage V_j, short-circuiting all other ports, & measuring short-circuit current at port *i*

H-Parameters

$$V_1 = h_{11}I_1 + h_{12}V_2$$
$$I_2 = h_{21}I_1 + h_{22}V_2$$

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

Short-circuit current gain

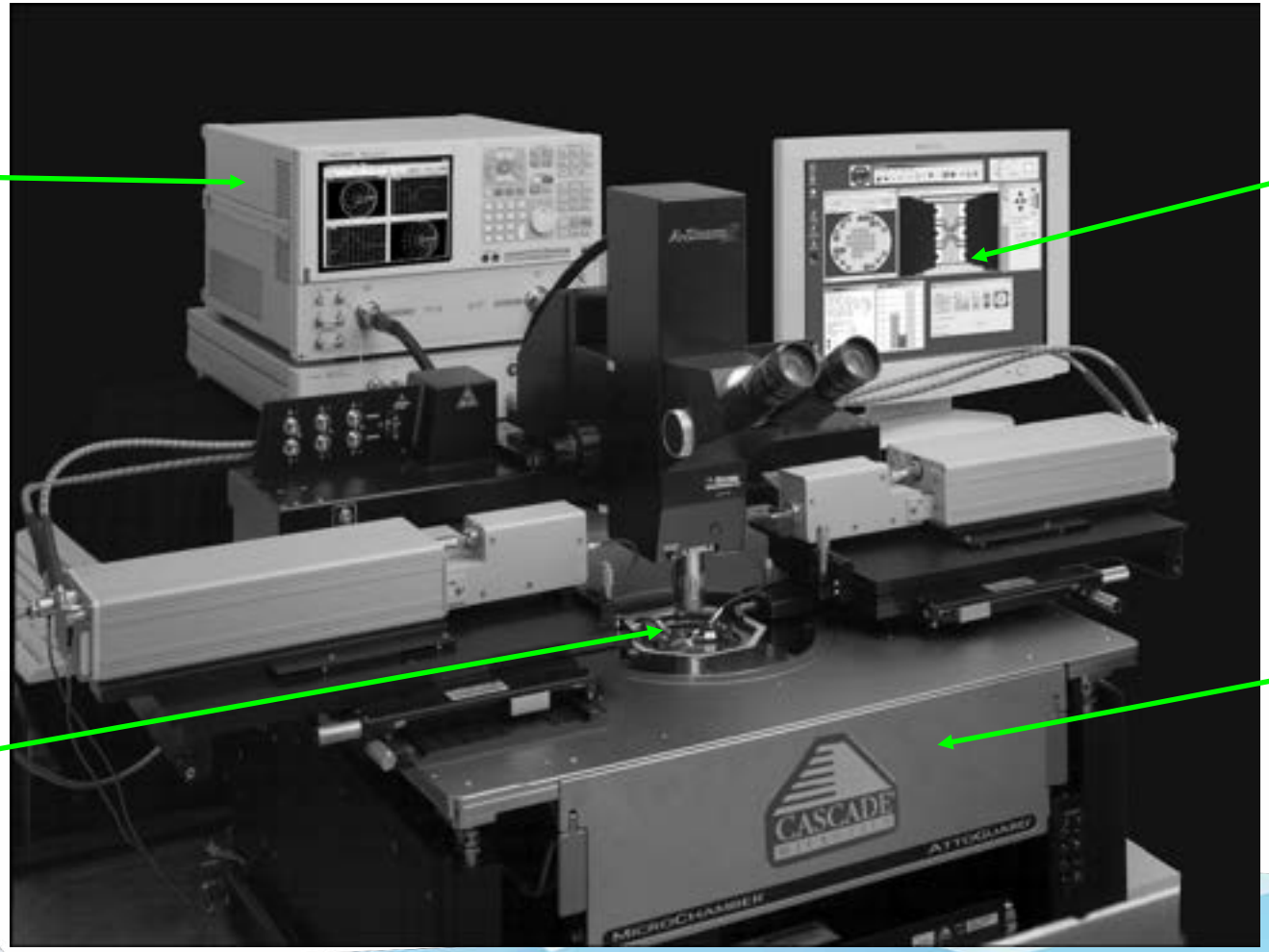
Network Analysis basics contd.

- Z-, Y-, and H-Parameters are an abstraction at high frequencies since voltages, currents, and impedances can not be measured in a direct manner
  - Desired quantities are non-unique for non-TEM modes of propagation
  - Require perfect open and short circuits which are difficult to achieve
- S-Parameters are preferred because they are based on the concept of incident, reflected, and transmitted waves which are more easily measured at high frequencies in terms of amplitude and phase angle of the various waves
- Typically deal with 2-port network parameters for transistor compact modeling work

110GHz S-Parameter Measurement System

Network Analyzer

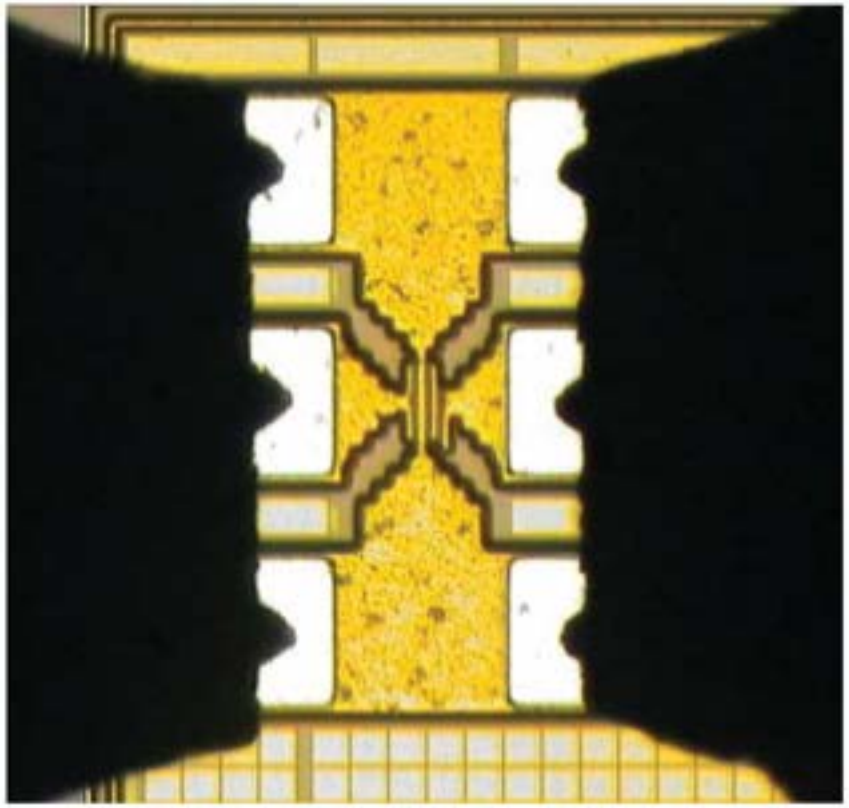
Computer control



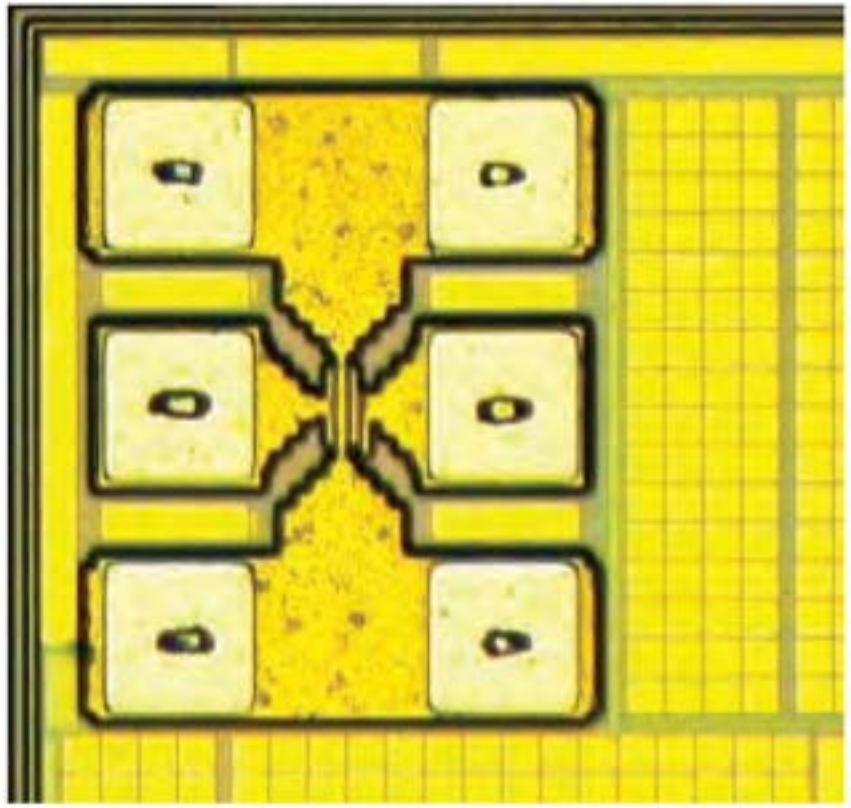
Coplanar probes to DUT

Semi-automatic probe station

RF GSG probes

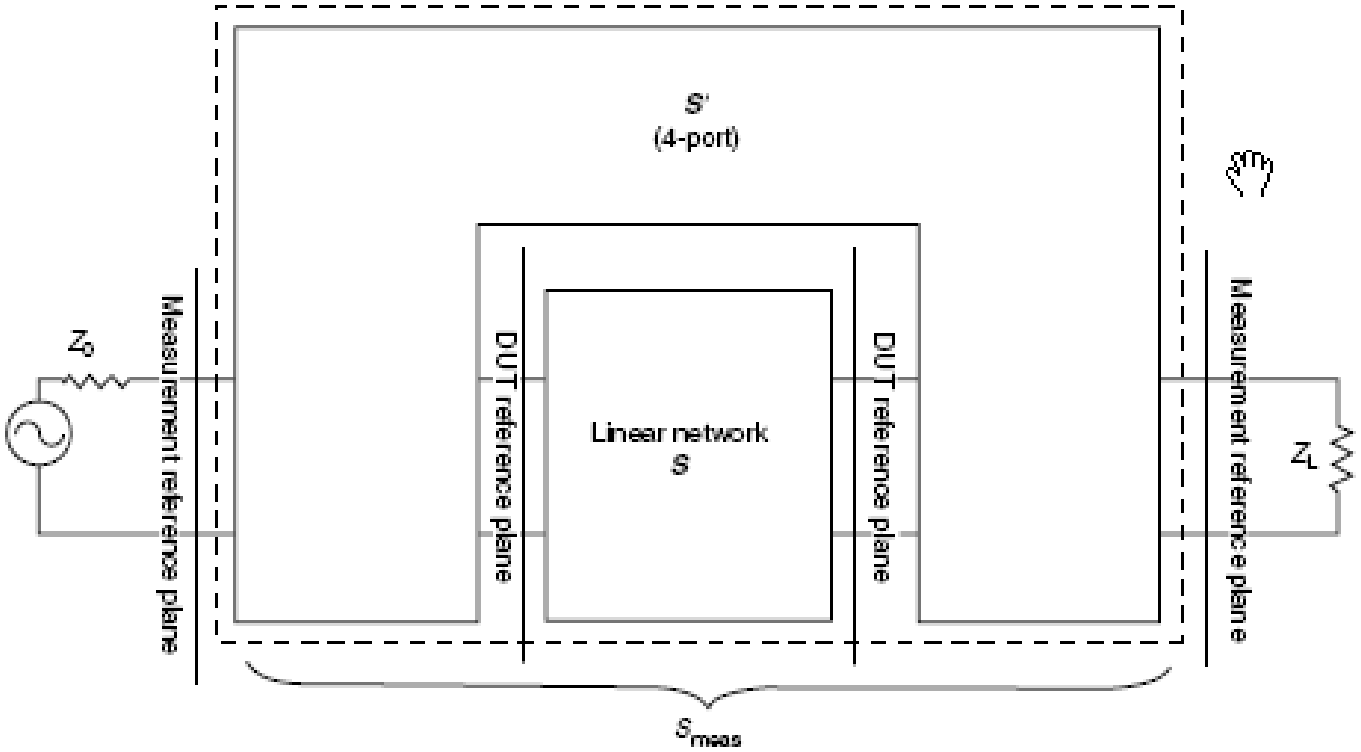


Excellent tip visibility Infinity Probe contacting Silicon RF device



Small contact marks enable contact to small pads

Calibration



- Calibration of measurement setup required to account for parasitics associated with connection of VNA to a DUT
  - Connection results in additional losses, reflective discontinuities, & phase shifts
- 4-port S' matrix implies 16 error terms
  - Passive nature of error network implies that it is reciprocal such that transmission terms are equal and a 12-term error model suffices to describe the S' matrix

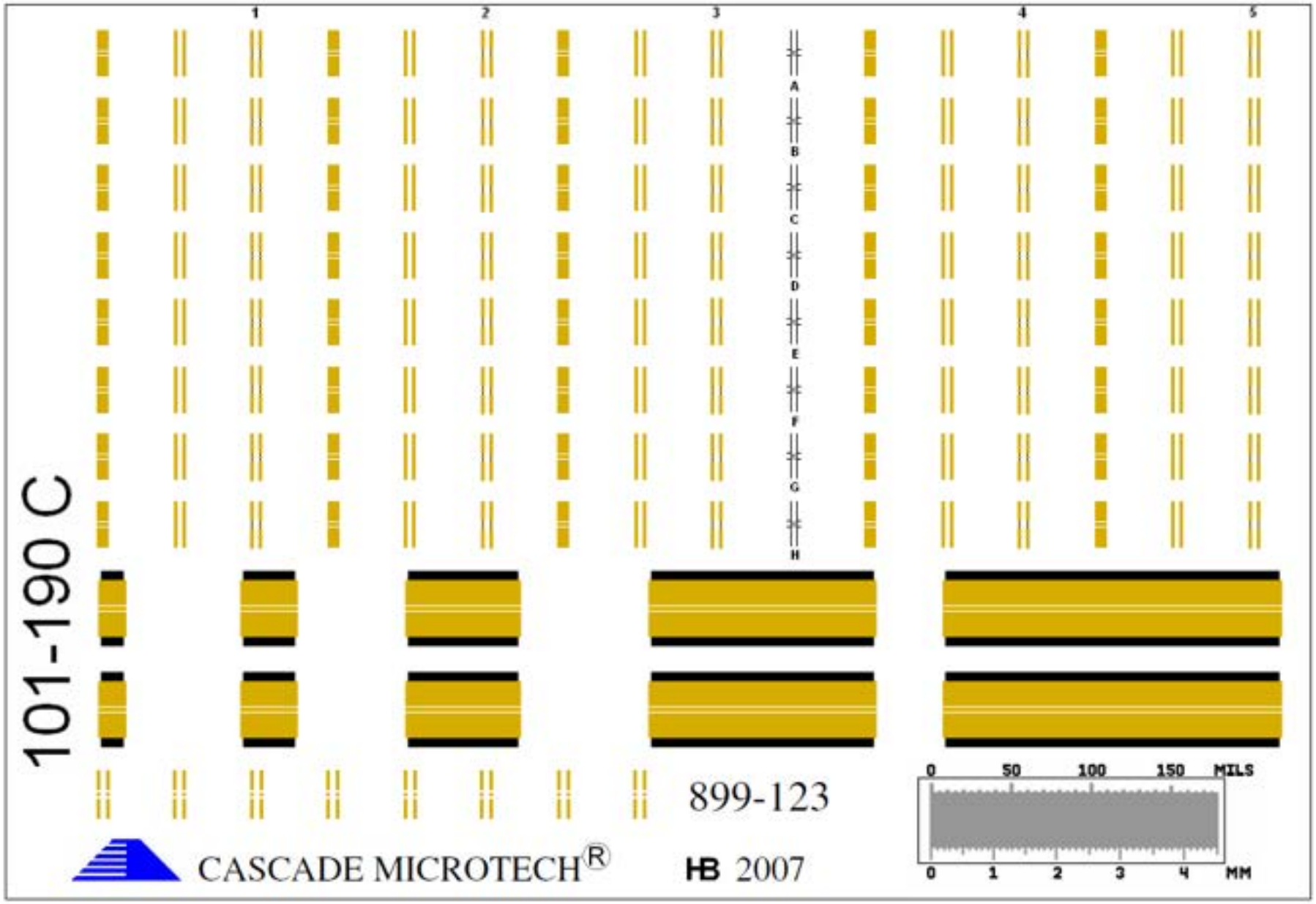
Calibration contd.

- Calibration achieved by measuring known standards located at DUT reference planes (probe tips for on-wafer measurements, and applying algorithms to determine the 12 error terms)
- Several calibration techniques available
  - Open-Short
  - SOLT (Short-Open-Load-Thru)
  - SOLR (Short-Open-Load-Reciprocal)
  - TRL (Thru-Reflect-Line)
  - LRM/LRRM (Line-Reflect-Match/Line-Reflect-Reflect-Match)
- Different standards required for different techniques, but, in general, standards must be precise with very low, known parasitics
- A special Impedance Standard Substrate (ISS) with precisely defined standards is used
  - Typically use SOLT even for 110GHz measurements

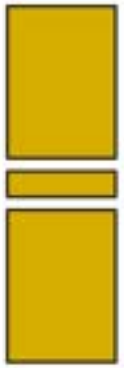
Impedance Standard Substrate

(Pitch: 100 – 250 um, Configuration: Ground-Signal-Ground)

P/N: 101-190, S/N:



Impedance Standard Substrate contd.



Thru

Thru delay: **1.0 ps**

Length: **220 um**

Impedance: **50 Ohm** (Nominal)

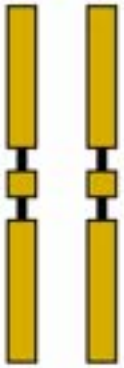
Note: Thru and Verification line lengths are signal conductor edge-to-edge dimension.

Short

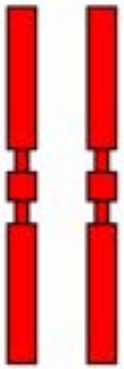
Recommended Overtravel:

ACP
75 - 125 um

Infinity
50 - 75 um



Load



Precision 50 Ohm Load

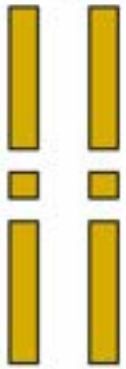
Note: Ensure the bias supply is turned **off** during calibration. Applying bias to the probe during calibration could cause the resistance of the load to change.

DC accuracy:
+/- 0.3 %

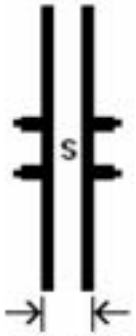
Note: For optimum calibration accuracy **only** the **Red** - marked load standards should be used.

Verification Lines

ps	um
3	450
7	900
14	1800
27	3500
40	5250



Open
(On Substrate)



130 um
Alignment Marks

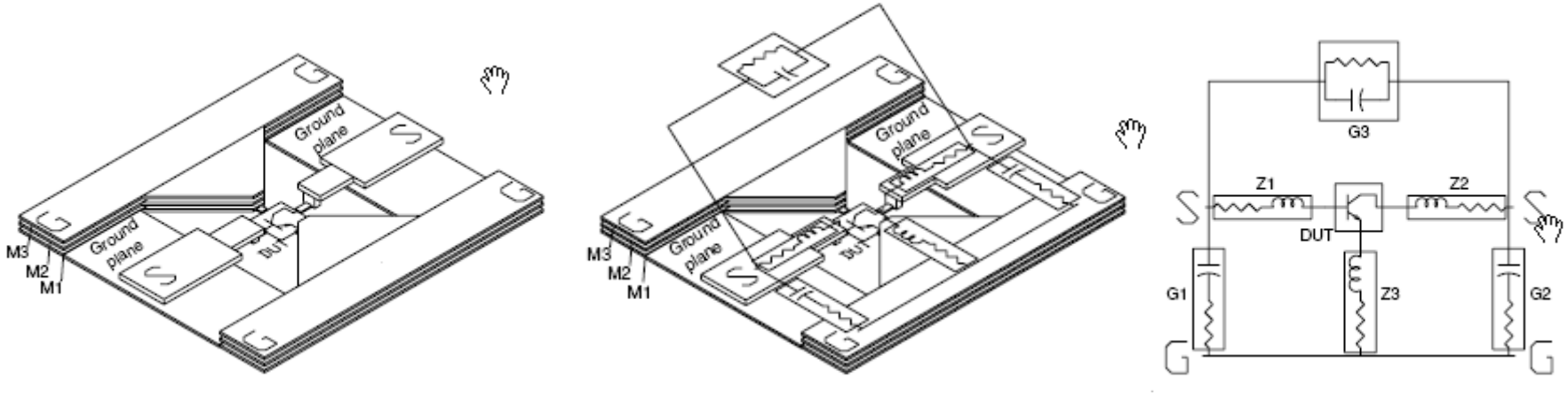
Note: By default, an **Open** is synthesized by raising the probes in air a minimum distance of 250 mm above the chuck surface. A Substrate Open structure is also provided as an alternative.

S-parameter measurement

- S-parameters measured using vector network analyzer (VNA) (e.g. Agilent E5071C ENA with frequency range of 100 kHz–8.5 GHz)

- De-embedding
  - Use de-embedding to remove parasitics
  - Probe/wire parasitics are de-embedded using calibration substrate
  - Pads to device parasitics are de-embedded using OPEN-SHORT de-embedding

De-embedding



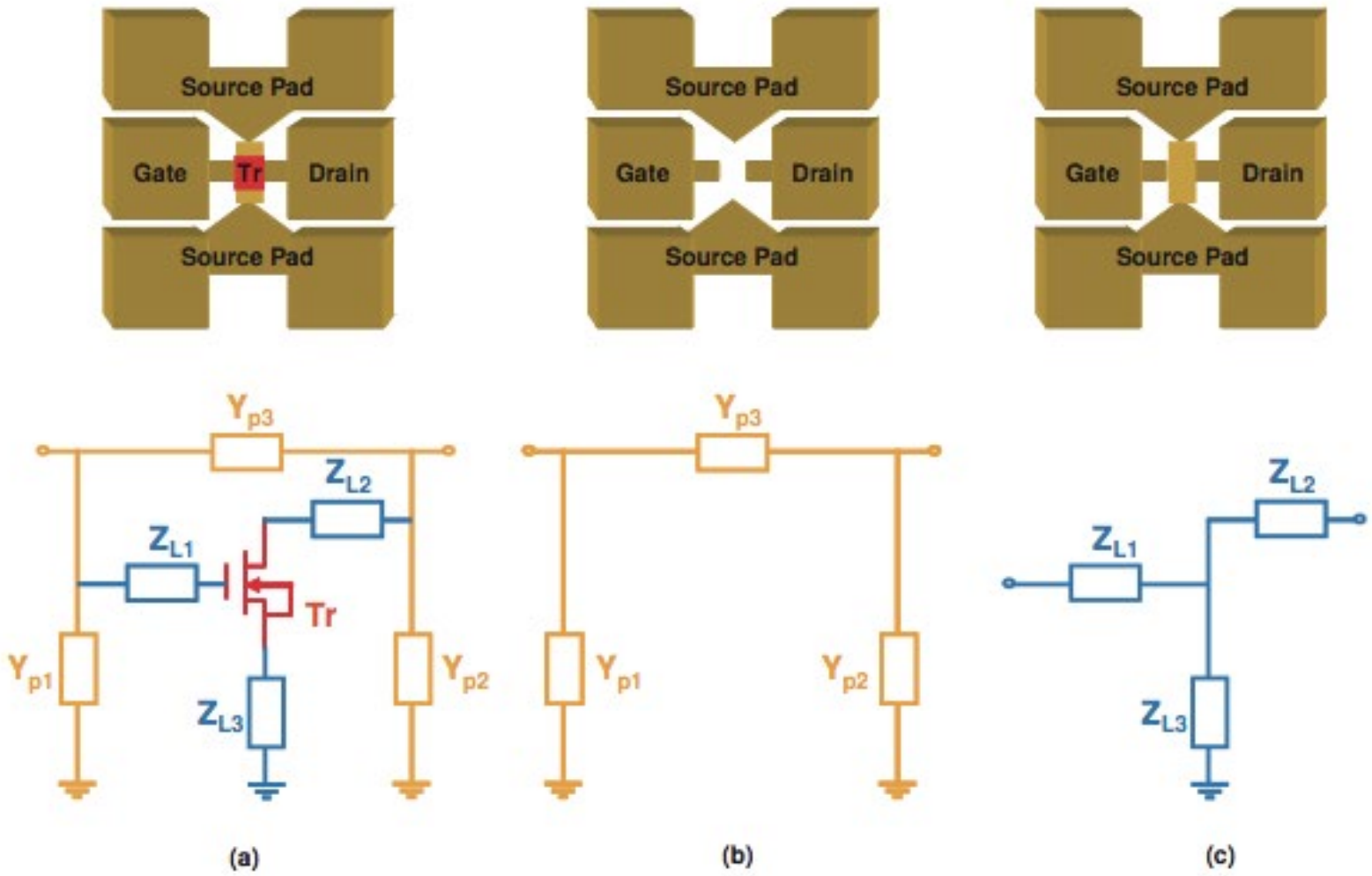
- Even with calibration, reference planes are still not at the boundaries of the intrinsic device due to on-wafer test structure interconnects (probe pads, transmission lines, ground planes, etc.)
  - Must measure additional on-wafer test structures to calibrate out (de-embed) the remaining parasitics

De-embedding contd.

- Most common on-wafer de-embedding technique is the OPEN-SHORT method where
  - OPEN test structure is designed to represent the parallel (G) parasitics
  - SHORT test structure is designed to represent the series (Z) parasitics

- De-embedding results are valid if OPEN, SHORT, and DUT are linear and time invariant (LTI) in nature
  - OPEN and SHORT are passive and, thus LTI
  - DUT is LTI if it behaves linearly with applied input power – care must be taken in choosing power level for S-Parameter measurements

Open-Short De-embedding



De-embed from Open:

$Y_{DUT/Open} = Y_{Total} - Y_{Open}$

$Y_{Short/Open} = Y_{Short} - Y_{Open}$

Convert to Z:

$Z_{DUT/Open} = Z(Y_{DUT/Open})$

$Z_{Short/Open} = Z(Y_{Short/Open})$

De-embed from Short:

$Z_{DUT} = Z_{DUT/Open} - Z_{Short/Open}$

Convert to S:

$S_{DUT} = S(Z_{DUT})$

Courtesy: Agilent Technologies

De-embedding contd.

- OPEN-SHORT De-embedding Method:
  1. Measure the S-parameters of the DUT embedded in the padset (S_{meas}).
  2. Measure the S-parameters of the OPEN and SHORT de-embedding standards (S_{open} and S_{short}, respectively).
  3. Convert S_{open} and S_{short} to Y-parameters (Y_{open} and Y_{short}, respectively). Subtract Y_{open} from Y_{short} to yield Y'_{short} (the Y-parameters of the short standard with the parallel capacitive and resistive contribution from the pads and substrate removed).
  4. Convert Y'_{short} to Z'_{short}. Z'_{short} now represents the combined network consisting of the three series impedances (Z1, Z2, and Z3).
  5. Convert S_{meas} to Y_{meas} and subtract Y_{open} from it. This yields Y'_{meas} (the Y-parameters of the DUT with the parallel capacitive and resistive contribution from the pads and substrate removed). Convert Y'_{meas} to Z'_{meas} which still contains the series impedances associated with Z1, Z2, and Z3 in addition to the desired DUT terminal characteristics.
  6. Subtract Z'_{short} from Z'_{meas} to yield Z''_{meas} (the Z-parameters of the DUT in the absence of all padset parasitics) and finally, convert Z''_{meas} back into fully padset corrected S-parameters (S''_{meas}) for analysis of the DUT terminal characteristics.

Contents

- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
- Modeling Power Devices using ASM-HEMT
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

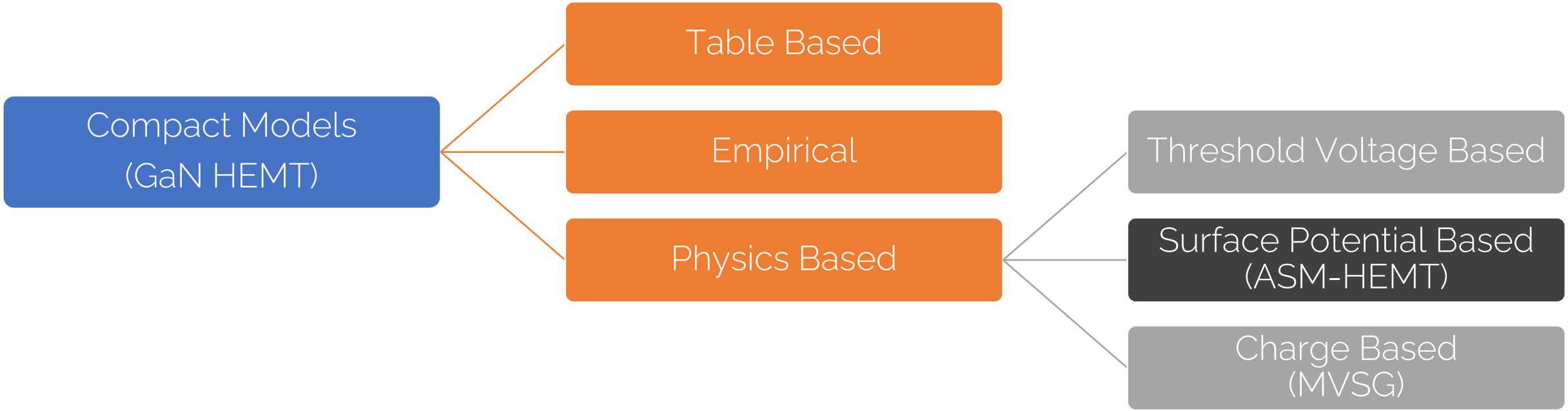
An introduction to ASM-HEMT

- *About ASM-HEMT and its core*
- *Extraction flow*
- *Other models incorporated into the core*
- *Geometric Scaling*

A brief history of HEMT models

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

Various classes of compact models



Advanced **S**PICE **M**odel for GaN **HEMT**s (**ASM-HEMT**)

www.iitk.ac.in/asm

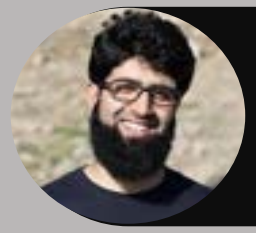
ASM-HEMT Team @ IIT Kanpur

Director

Prof. Yogesh Singh Chauhan

Developers

Present Team



Ahtisham Pampori

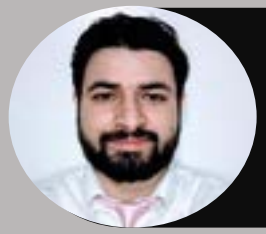
Raghvendra Dangi

Mohammad Sajid

Hasnain Ansari

Past Team

Dr Sudip Ghosh



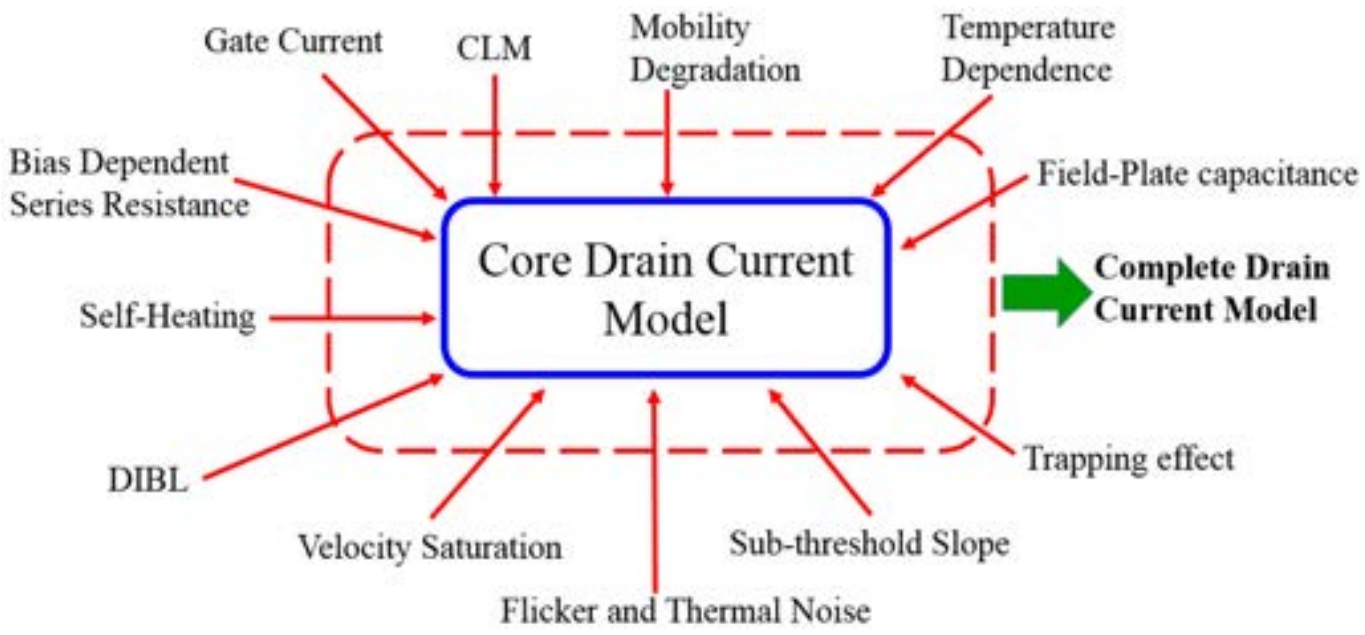
Dr. Aamir Ahsan

Dr. Avirup Dasgupta

ASM-HEMT: Summary

Electrostatics	Analytical Solution of Schrodiger's & Poisson's	→	2-DEG Charge, Ef, Surface Potential
Transport	SP-Based Current & Charge Model	→	I-V, C-V, DIBL, Rd, Rs, Vel. Sat., ...
Higher-order Effects	Noise, Trapping, Self-Heating, Field Plate	→	DC, AC, Transient Harmonic Sim., Noise, ...

ASM-HEMT: Core Model



Real Device Effects Incorporated into the Model

Core Model Parameters

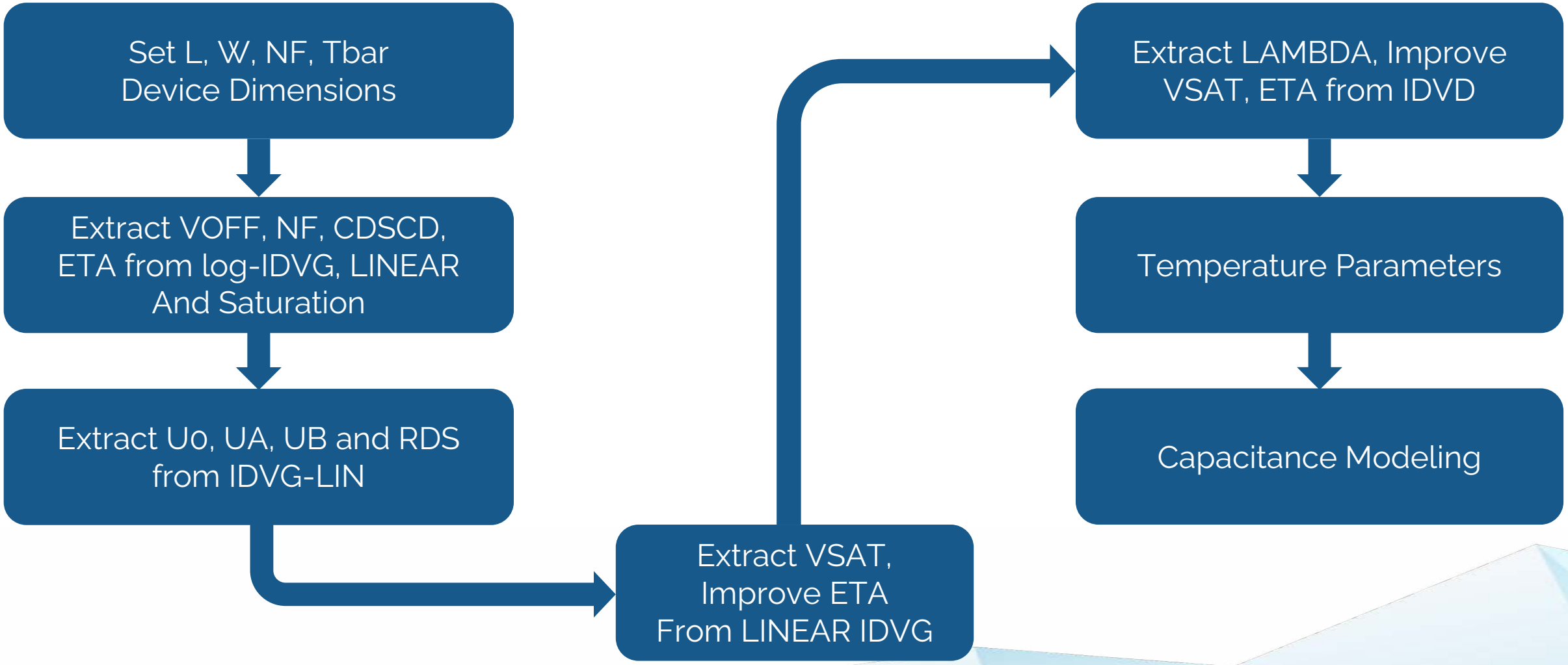
Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	$-2.86\ V$
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	$0.325\ V^{-1}$
η_0	DIBL Parameter	0.117
U_0	Low Field Mobility	$33.29\ mm^2/Vs$
N_{S0ACCS}	AR 2DEG Density	$1.9e+17\ /m^2$
$V_{SATACCS}$	AR saturation velocity	$157.6e+3\ cm/s$
R_{TH0}	Thermal Resistance	$22\ \Omega$

Core drain current expression

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}}\frac{W}{L}C_g N_f\left[V_{go} - \left(\frac{\psi_s+\psi_d}{2}\right) + V_{th}\right] \times \psi_{ds}$$

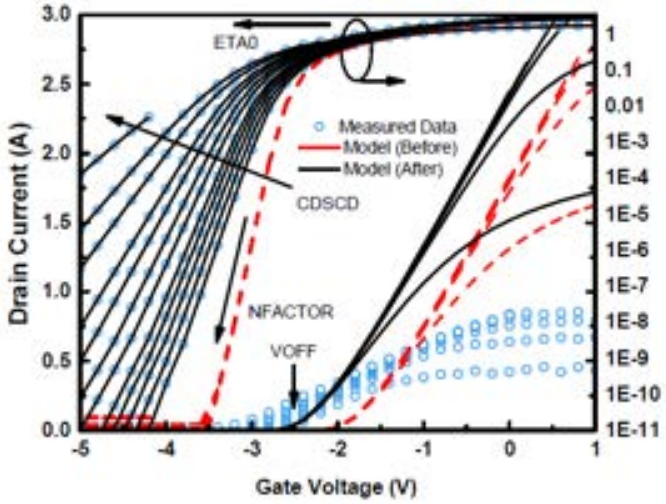
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Extraction Flow I

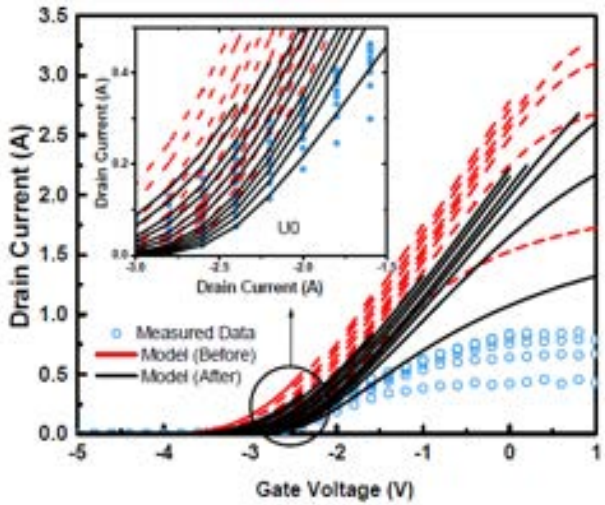


[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

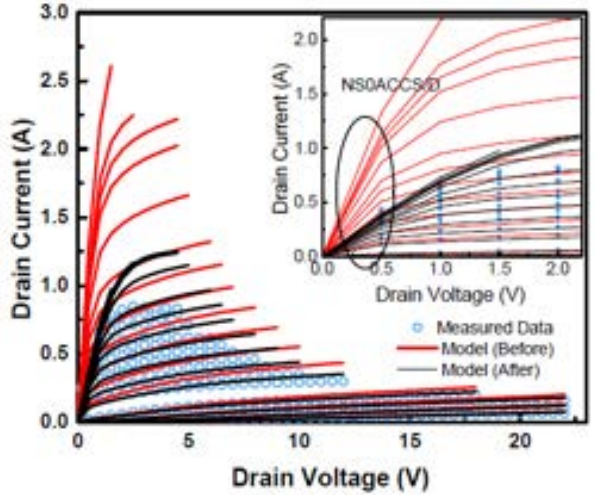
Extraction Flow II



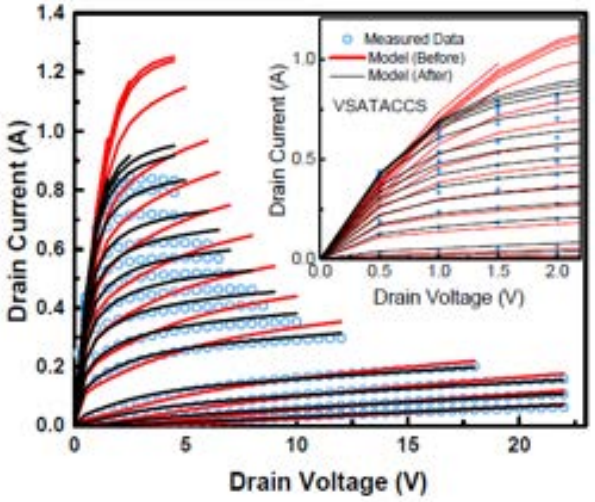
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



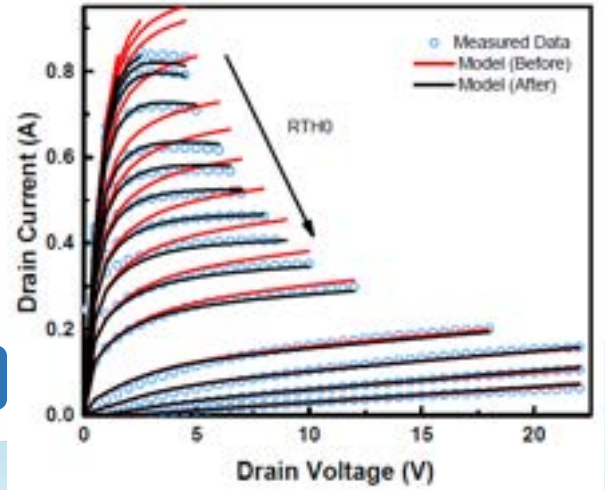
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



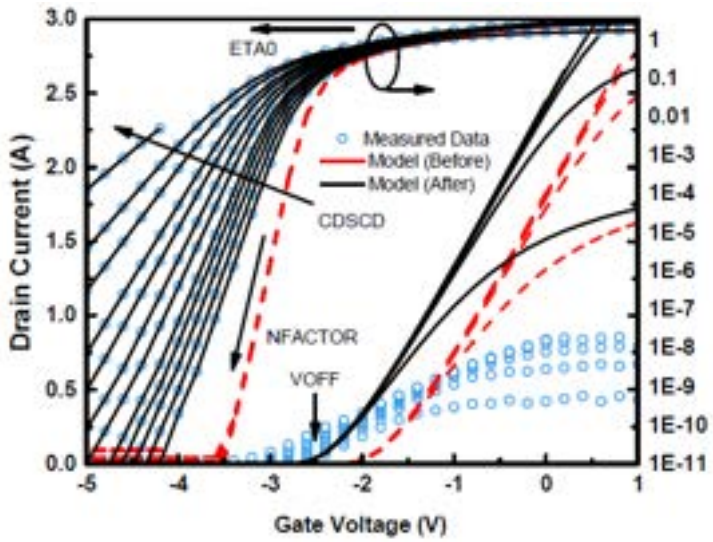
$I_d - V_d$ (Extract $V_{SATACCS}$)



$I_d - V_d$ (Extract R_{TH0})

[1] S. A. Ahsan *et al.*, *MOS-AK Workshop*, Shanghai, [2016]

Extraction from Id-Vg curves



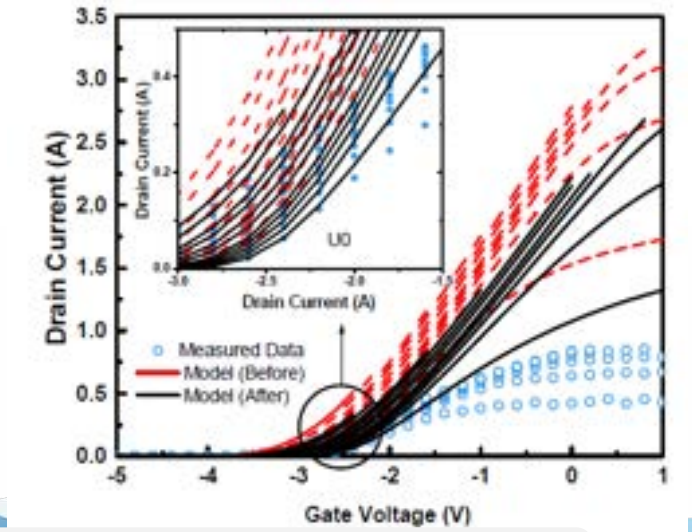
Start with $I_d - V_g$ characteristics in the log scale

$\boldsymbol{ETA0}$ – DIBL Parameter

$\boldsymbol{NFACTOR}$ – Sub-threshold slope parameter

$\boldsymbol{CDSCD}$ – Captures the drain voltage dependence on the sub-threshold slope.

$\boldsymbol{VOFF}$ – Cut-Off Voltage



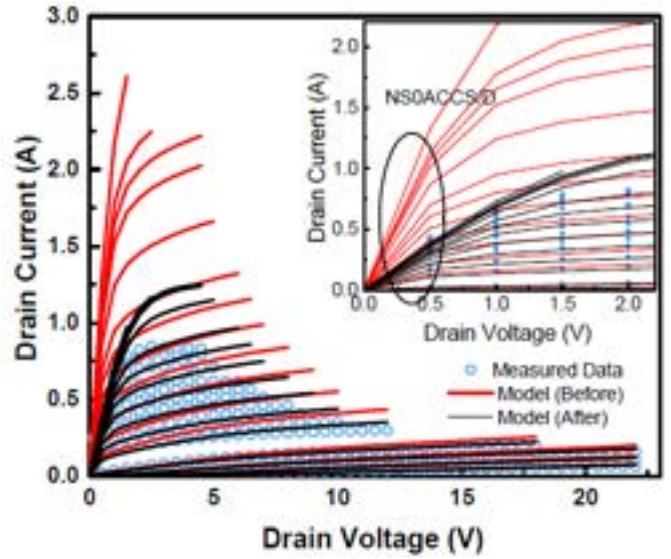
$I_d - V_g$ characteristics in the linear scale

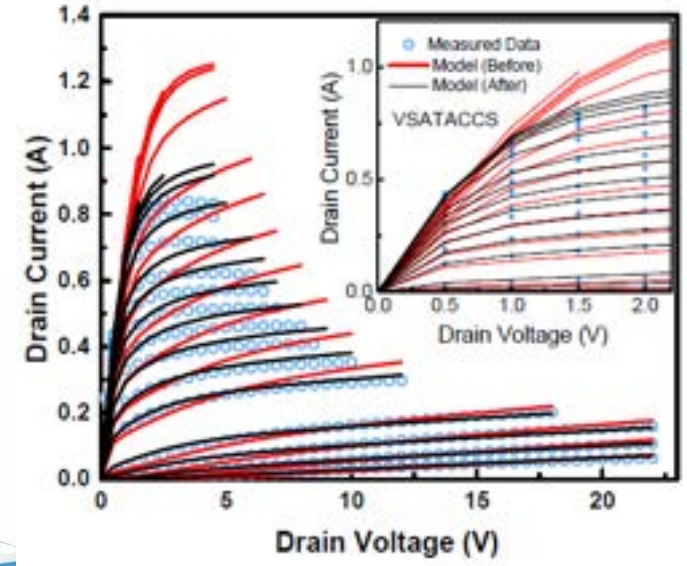
$\boldsymbol{U0}$ – Low field mobility

$\boldsymbol{UA, UB}$ – Mobility degradation parameters

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Extraction from Id-Vd curves





$I_d - V_d$ characteristics

$\boldsymbol{VSAT}$ – Velocity saturation parameter

$\boldsymbol{UA}$, $\boldsymbol{UB}$ – Mobility degradation parameters

Access Region Parameters extracted from $I_d - V_d$ characteristics:

$\boldsymbol{NS0ACCS(D)}$ – 2DEG density in the access region.

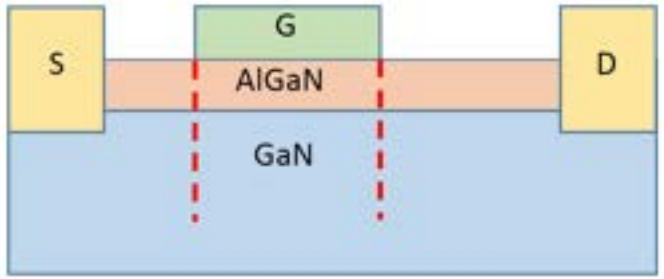
$\boldsymbol{VSATACCS}$ – Saturation velocity in the access region.

$\boldsymbol{U0ACCS(D)}$ – Low field mobility in the access region.

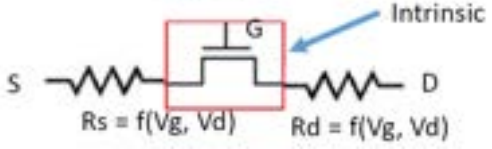
$\boldsymbol{U0ACCS(D)}$ independently tunes the access region resistance around Vds = 0 and helps extract g_{ds} at that point.

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Bias-dependent access region resistance model: Overview



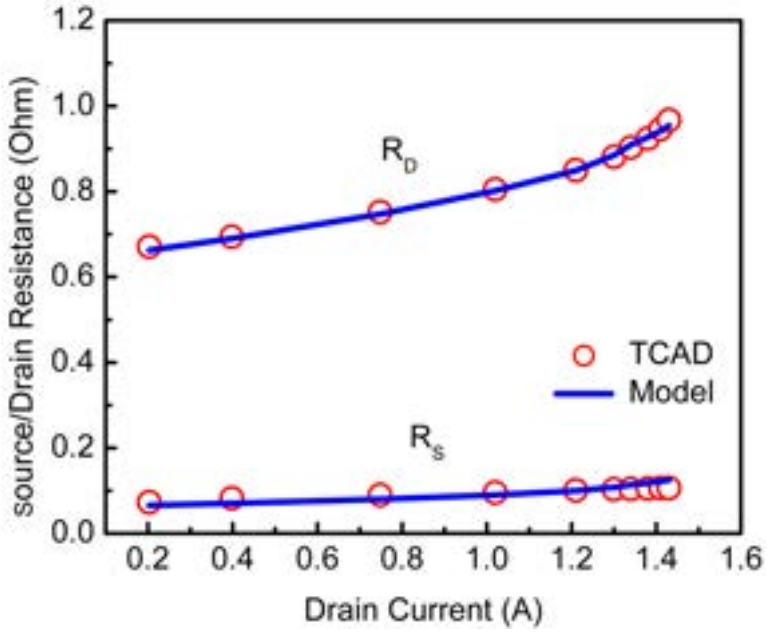
$$R_J = \frac{L_J}{q\mu_n n_{s0}} \qquad J = S, D$$



$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R/V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$I_{ds,acc} = \frac{R_c}{W \cdot N_f} + \frac{L_{acc}}{W \cdot N_f \cdot q \cdot N_{S0ACCS} \cdot U_{0ACCS}} \times \left(1 - \left(\frac{I_{ds}}{W \cdot N_f \cdot N_{S0ACCS} \cdot V_{SATACCS}}\right)^2\right)^{-1/2}$$

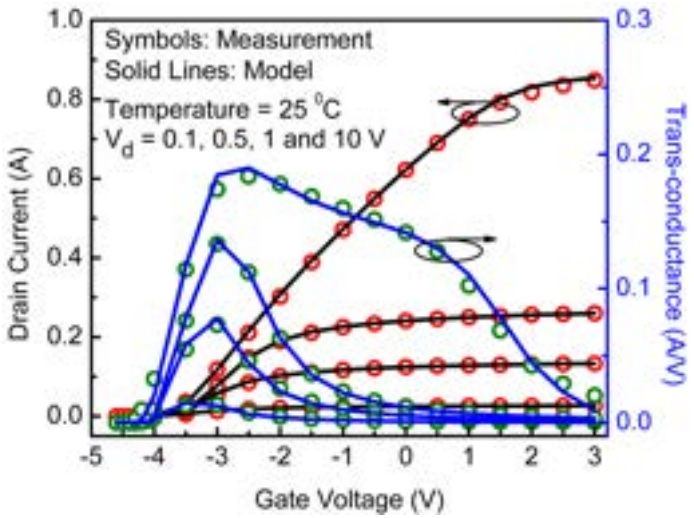


Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

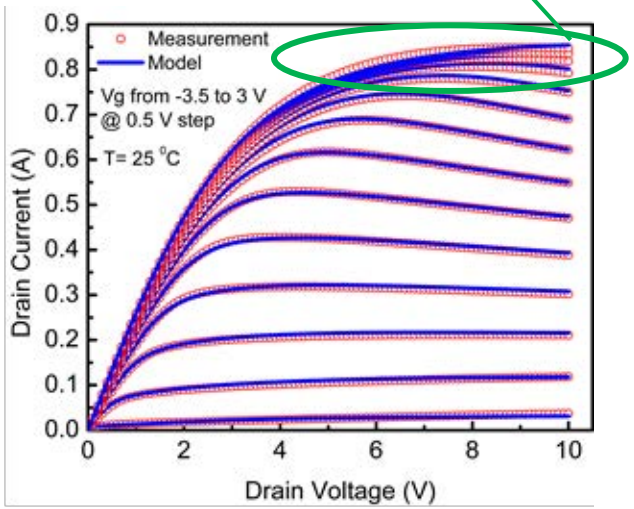
[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

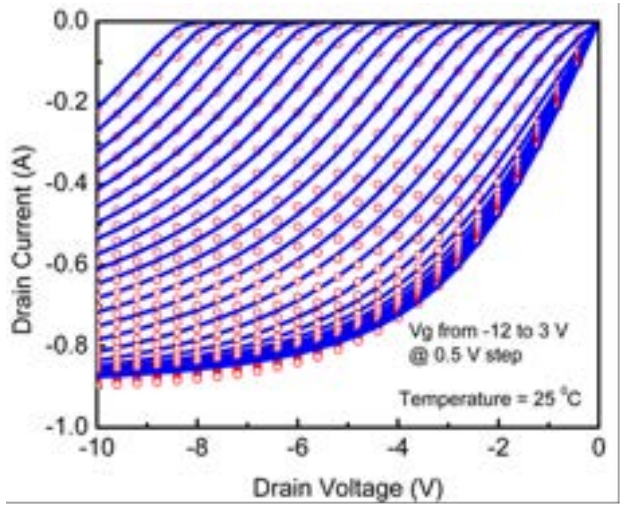
Bias-dependent access region resistance model: Results

Effect of high access region resistance at high V_g



Id - Vg and trans-conductance for the Toshiba power HEMT. Different slopes above Voff in gm-Vg: self-heating governs the first slope while velocity saturation in access region affects second slope.





Ids-Vds and reverse Ids-Vds fitting with experimental data. The non-linear Rs/d model shows correct behavior for the higher Vg curves in the Id - Vd plot; the S-P based model can accurately capture the reverse output characteristics.

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

Bias-dependent access region resistance model: Temperature scaling

The temperature dependence of $R_{d/s}$ model is extremely important as it increases significantly with increasing temperature

Temperature dependence of 2-DEG charge density in the drain or source side access region:

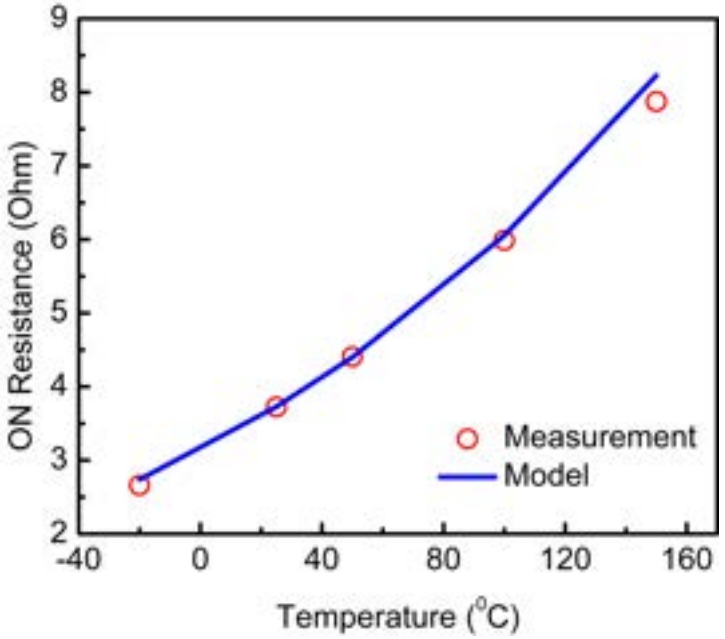
$$n_{s0}(T) = NS0ACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

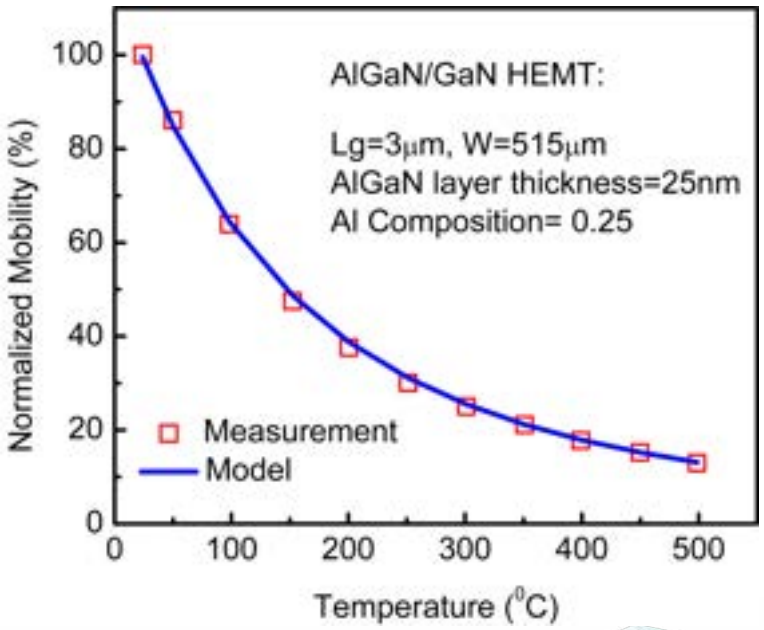
Temperature dependence of Saturation Velocity:

$$V_{sat}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

Temperature dependence of electron Mobility:

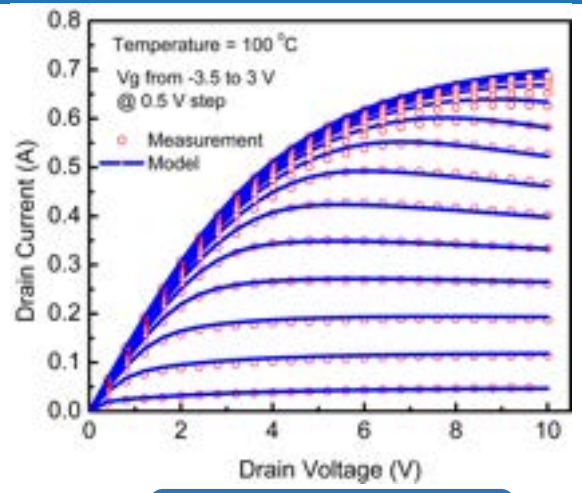
$$\mu_{acc}(T) = U0ACC \cdot \left(\frac{T}{TNOM}\right)^{UTEACC}$$



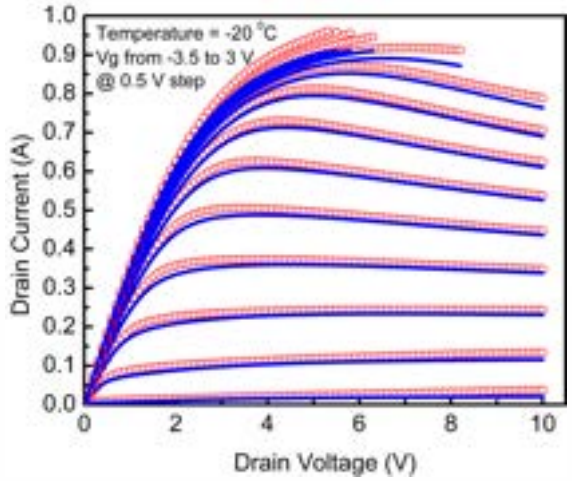


[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

ASM-HEMT: Temperature scaling results



Id - Vd at 100°C



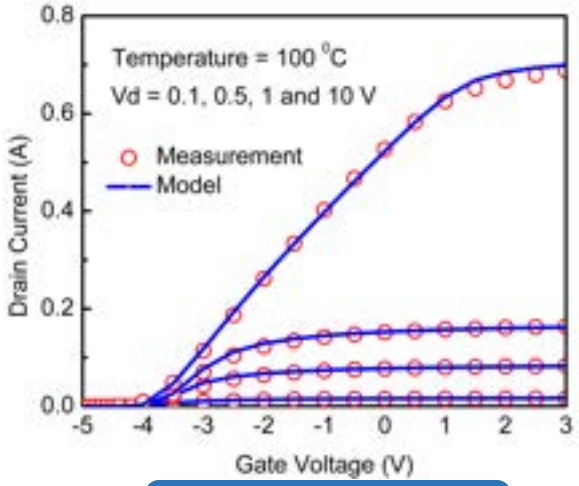
Id - Vd at -20°C

ASM-HEMT features a robust temperature scaling model which has been validated across a broad range of device temperatures.

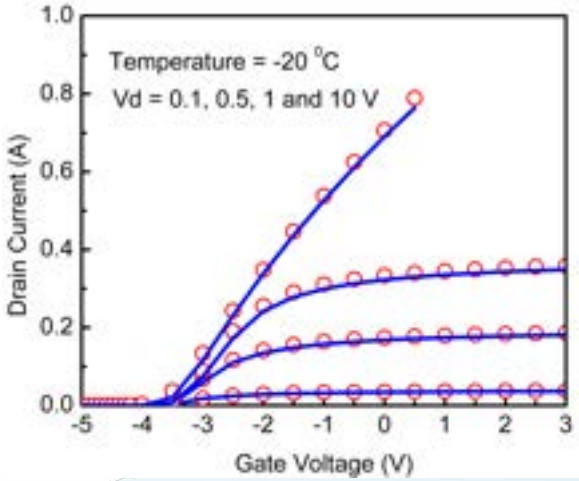
$$V_{off,DIBL}(T) = V_{off,DIBL} - \left(\frac{T_{dev}}{T_{NOM}} - 1\right) \cdot \boldsymbol{KT1} + TRAPVOFF \cdot vcap + voff_{trap}$$

$$U0(T) = U0 \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{UTE}}$$

$$VSAT(T) = VSAT \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{AT}}$$



Id - Vg at 100°C



Id - Vg at -20°C

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

Geometric Scaling I

Charges/Capacitances

$$Q_g = \frac{C_g LW}{V_{g0} - \psi_m + V_{tv}}[V_{g0}^2 + \frac{1}{3}(\psi_d^2 + \psi_s^2 + \psi_d\psi_s) - V_{g0}(\psi_d + \psi_s - V_{tv}) - V_{tv}\psi_m]$$

$$\begin{aligned} Q_d = -\frac{C_g LW}{120(V_{g0} - \psi_m + V_{tv})^2}[&12\psi_d^3 + 8\psi_s^3 + \psi_s^2(16\psi_d - 5(V_{tv} + 8V_{g0})) \\ &+2\psi_s(12\psi_d^2 - 5\psi_d(5V_{tv} + 8V_{g0}) + 10(V_{tv} + V_{g0})(V_{tv} + 4V_{g0})) \\ &+15\psi_d^2(3V_{tv} + 4V_{g0}) - 60V_{g0}(V_{tv} + V_{g0})^2 \\ &+20\psi_d(V_{tv} + V_{g0})(2V_{tv} + 5V_{g0})] \end{aligned}$$

Current Scaling

$$I_d = \frac{W}{L}\mu C_g(V_g0 - \psi_m + V_{th})\psi_{ds}$$

Where $\psi_m = (\psi_d + \psi_s)/2$, $\psi_d s = (\psi_d - \psi_s)$

Access Region Resistance Scaling

$$\begin{aligned} R_{source} = &\frac{RSC(T)}{W \cdot NF} + TRAPRS \cdot vcap \\ &+ \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS(T) \cdot U0ACCS(T)} \\ &\cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCS}\right)^{\frac{-1}{MEXPACCS}} \end{aligned}$$

where

$$I_{sat,source} = W \cdot NF \cdot NS0ACCS(T) \cdot VSATACCS(T)$$

$$\begin{aligned} R_{drain} = &\frac{RDC(T)}{W \cdot NF} + TRAPRD \cdot vcap + R_{trap}(T) + ron_{trap} \\ &+ \frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD(T) \cdot U0ACCD(T)} \\ &\cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCD}\right)^{\frac{-1}{MEXPACCD}} \end{aligned}$$

where $I_{sat,drain} = W \cdot NF \cdot NS0ACCD(T) \cdot VSATACCS(T)$

Geometric Scaling II

Thermal Noise and Flicker Noise Scaling

$$S_{if}(f) = \frac{k_B T}{W L^2 f^{EF}} \frac{I_{DS}^2 K_r}{C_g^2} \Big[NOIAV_{th}C_g \left(\frac{1}{Q_{ch,d}} - \frac{1}{Q_{ch,s}} \right) + (NOIA + NOIBV_{th}C_g) ln \left(\frac{Q_{ch,d}}{Q_{ch,s}} \right) + (NOIB + NOICV_{th}C_g)(-Q_{ch,d} + Q_{ch,s}) + \frac{NOIC}{2}(Q_{ch,d}^2 - Q_{ch,s}^2) \Big]$$

$$S_{it} = \frac{4k_B T_{dev}}{I_D L_{eff}^2} (\mu_{eff,sat} W q C_g)^2 \left(V_{go}^2 \psi_{ds} + \frac{\psi_d^3 - \psi_s^3}{3} - V_{go} \left(\psi_d^2 - \psi_s^2 \right) \right)$$

Gate Current Scaling

$$I_{gs} = W \cdot L \cdot NF \cdot \left[IGSDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[exp\left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

$$I_{gd} = W \cdot L \cdot NF \cdot \left[IGDDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGD \right] \left[exp\left\{ \frac{V_{gd}}{NJGD \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

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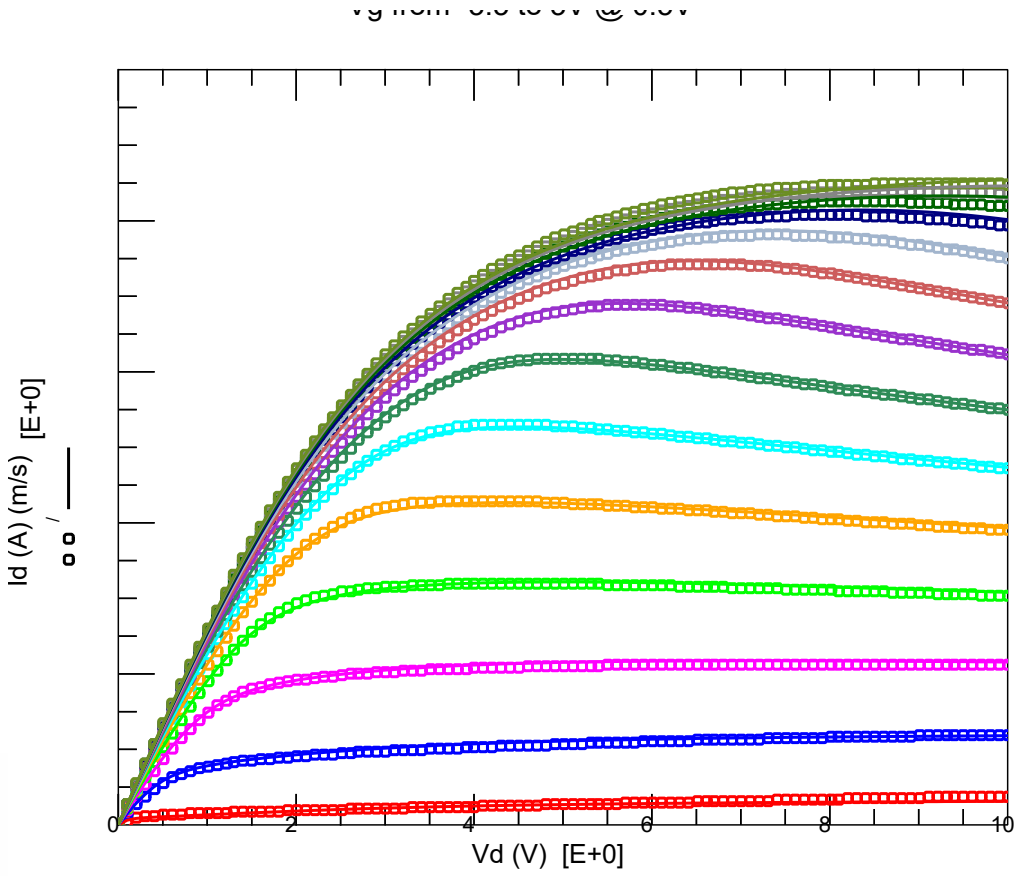
Modeling Power Devices using ASM-HEMT

- *Modeling DC*
- *Modeling field plates*
- *Model comparison with a mixed mode device*

Modeling DC: Room Temperature Output Characteristics

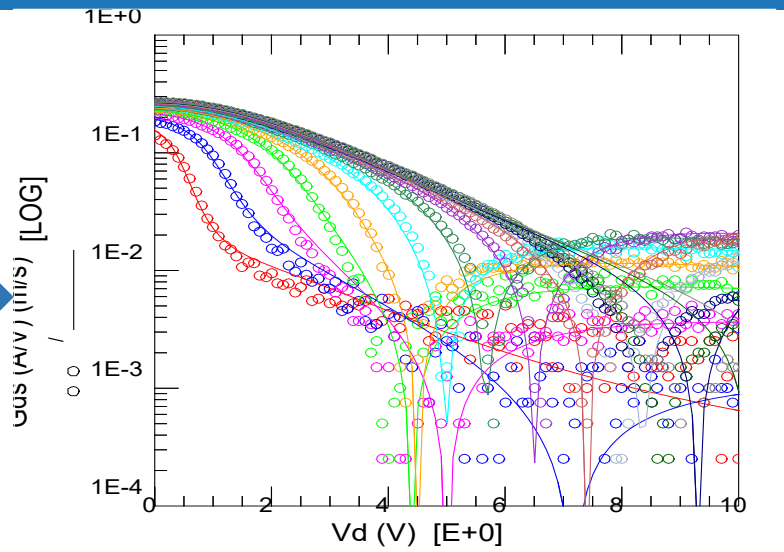


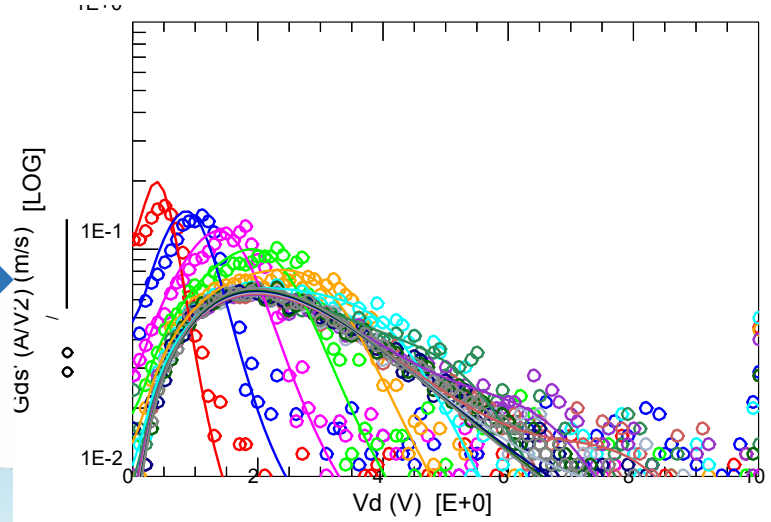
Output Characteristics at T=25°C

Output conductance versus Vd

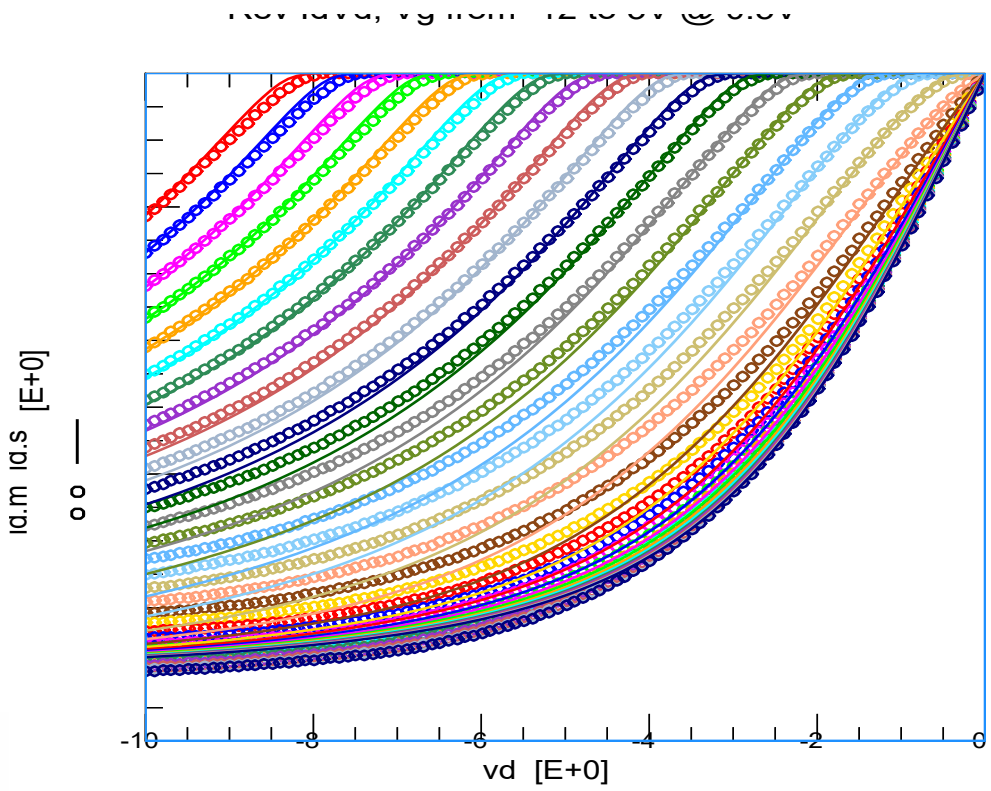
ASM-HEMT accurately captures the IV characteristics of a power GaN HEMT device.

Derivative of output conductance versus Vd



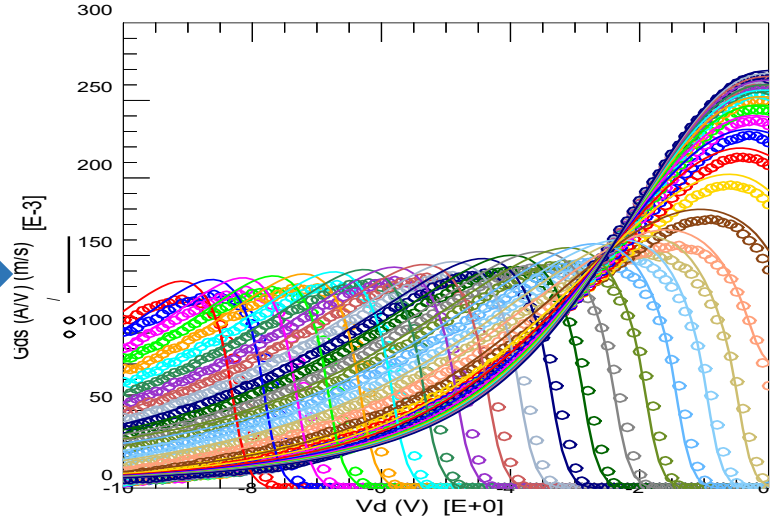


Modeling DC: Room Temperature Reverse Output Characteristics

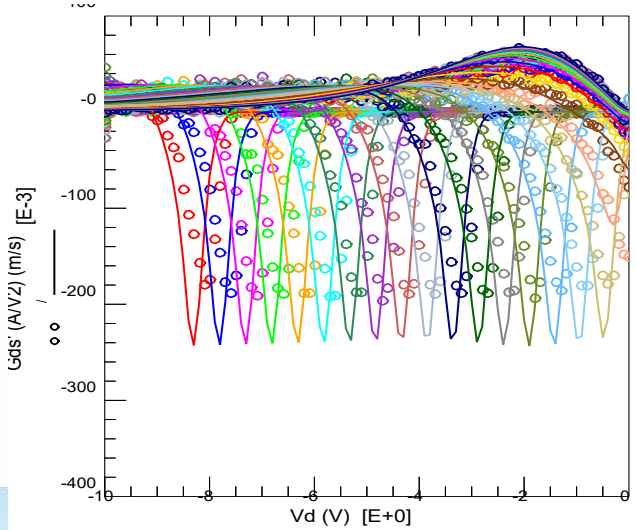


Reverse Output Characteristics at T=25°C

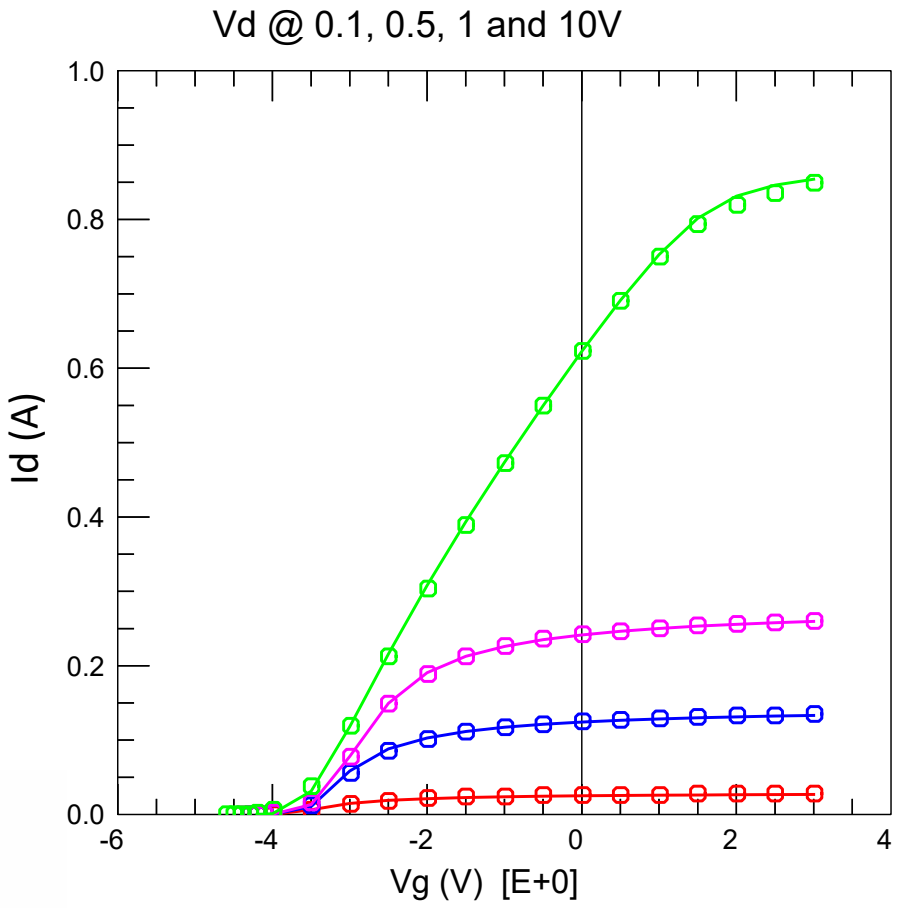
Reverse Output conductance versus Vd



Derivative of reverse output conductance versus Vd

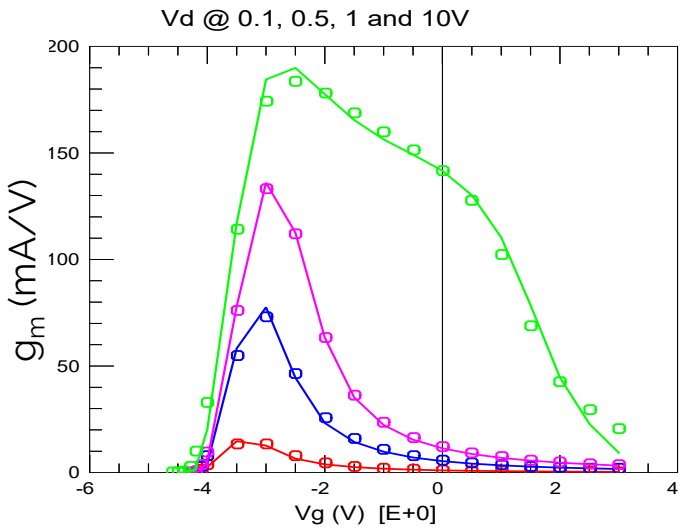


Modeling DC: Room Temperature Transfer Characteristics

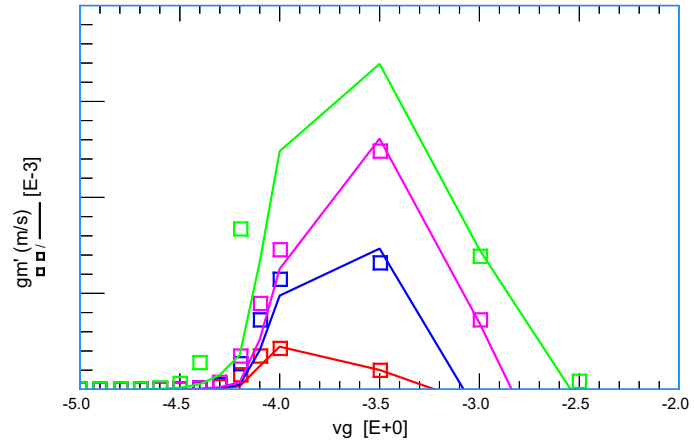


Transfer Characteristics at T=25°C

Transconductance versus Vg

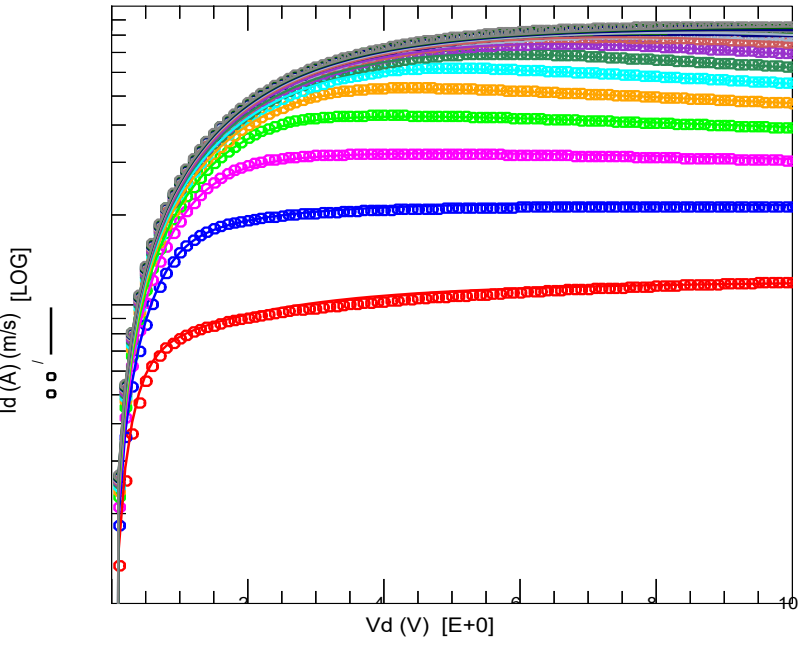


Derivative of transconductance versus Vg

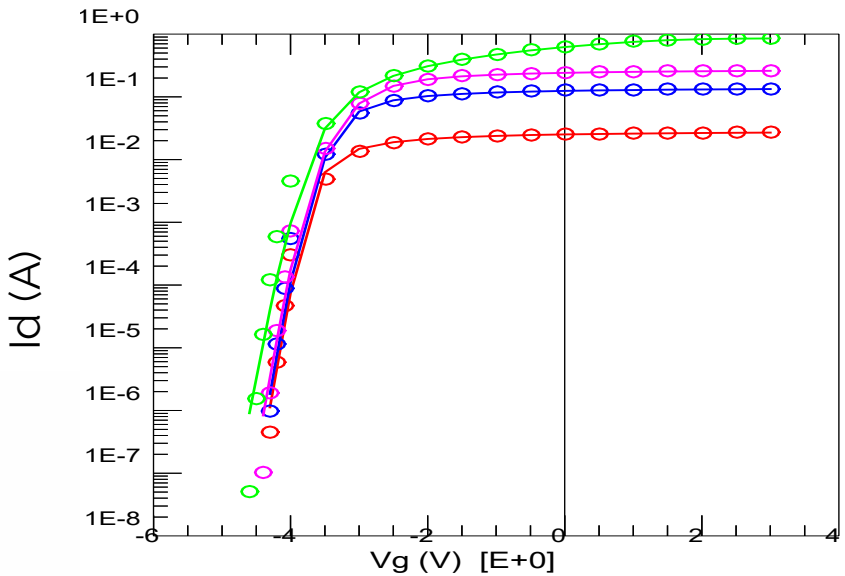


Modeling DC: Room Temperature IV – Log Scale

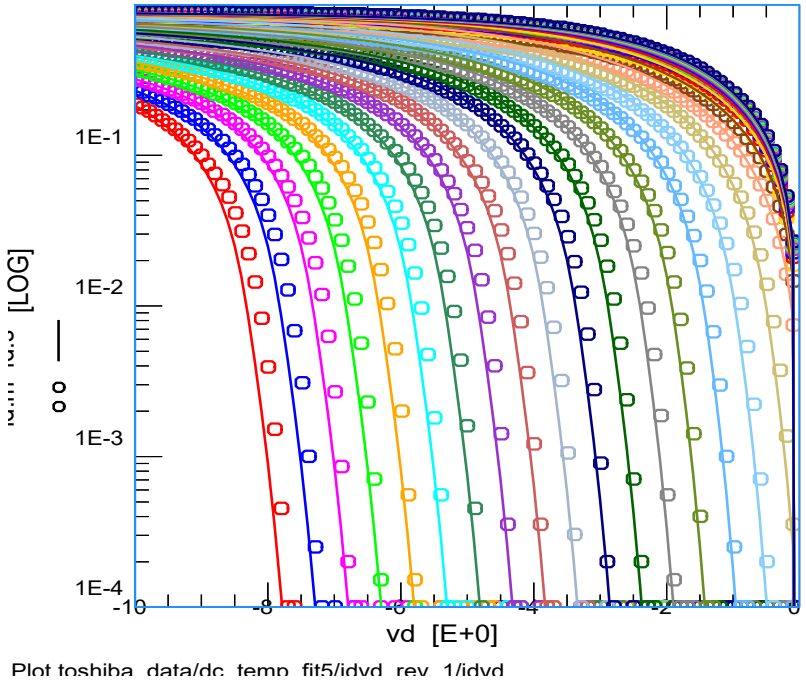
Log (Id) - Vds (Vd>0) T=25°C



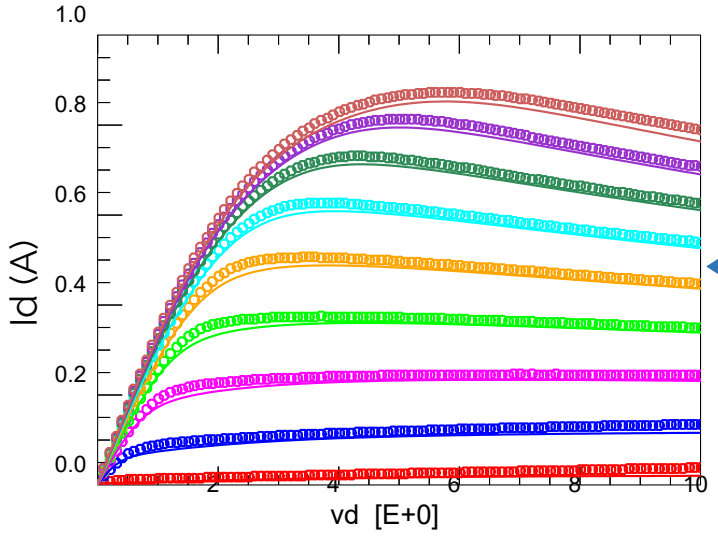
Log (Id) - Vgs T=25°C



Log (Id) - Vds (Vd<0) T=25°C

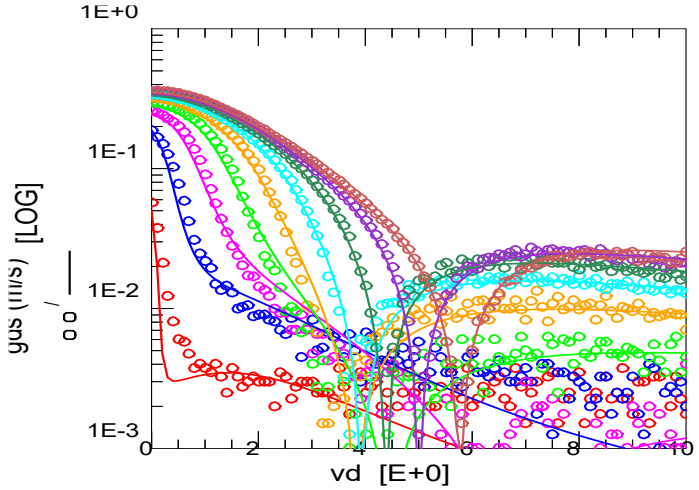


Modeling DC: Output Characteristics @ T=-20°C

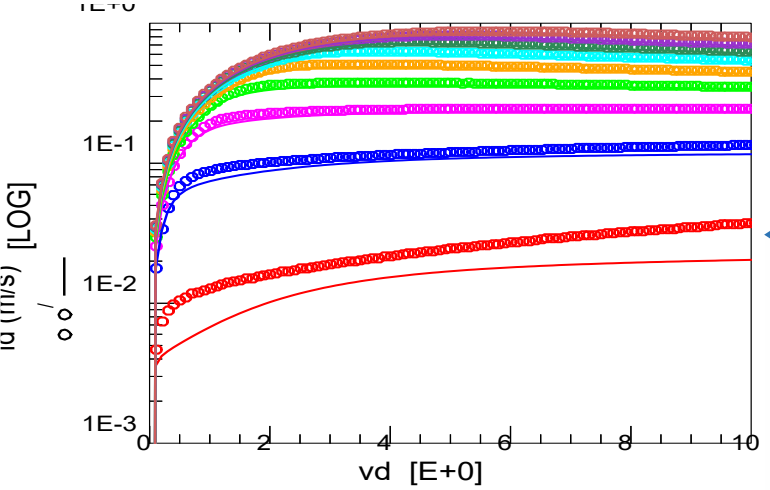


Output Characteristics @ -20°C

Output conductance versus Vd @ -20°C

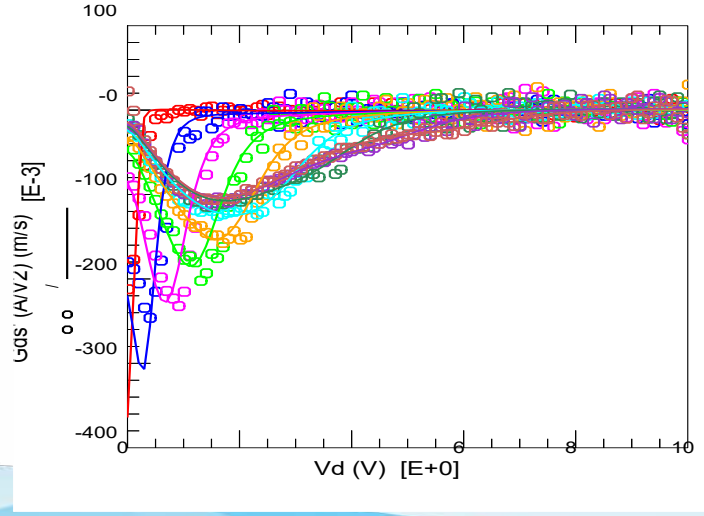


The model scales accurately to sub-zero temperatures.

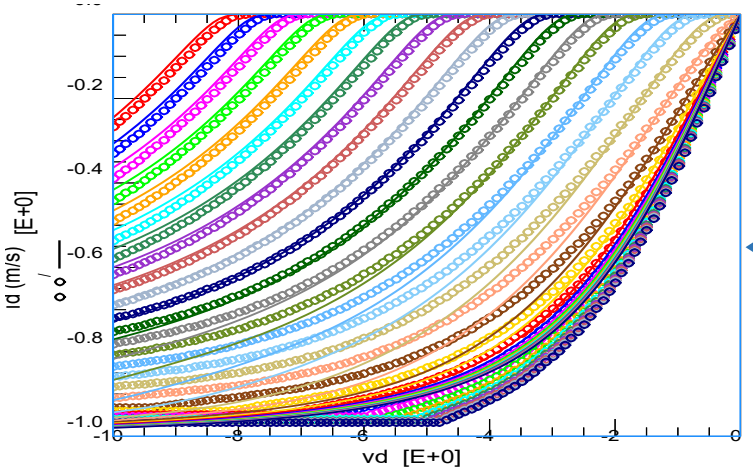


Log Output Characteristics @ -20°C

Derivative of output conductance versus Vd @ -20°C



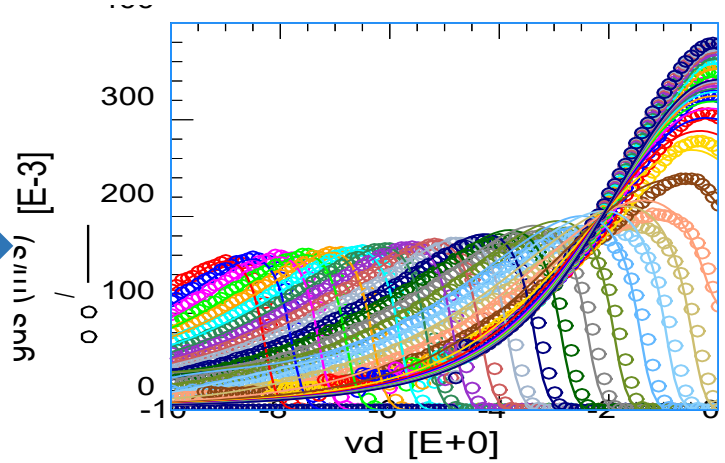
Modeling DC: Reverse Output Characteristics @ T=-20℃



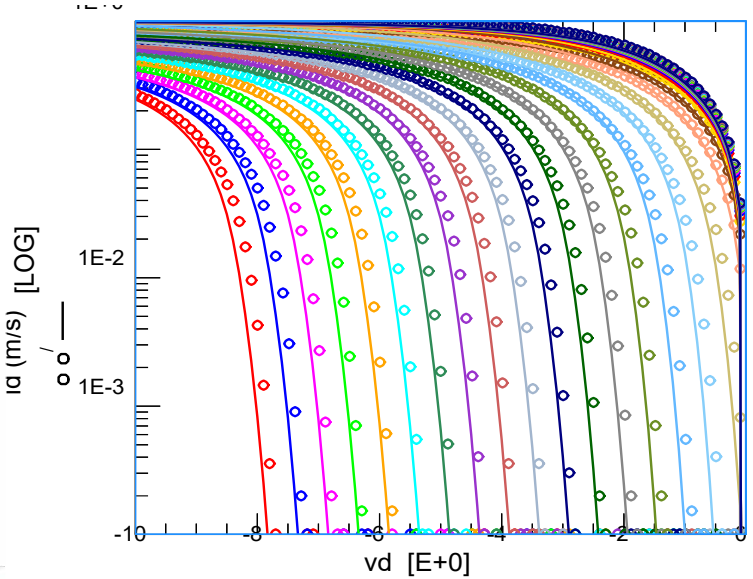
Vg from -12 to 3 V @ 0.5V step

Reverse Output Characteristics @ -20℃

Reverse Output conductance versus Vd @ -20℃

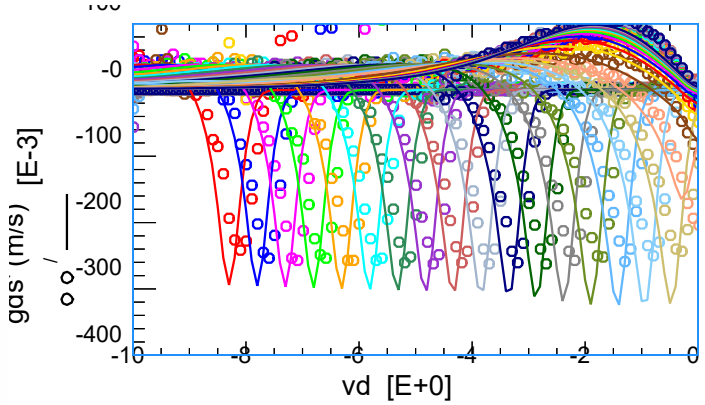


The model scales accurately to sub-zero temperatures.



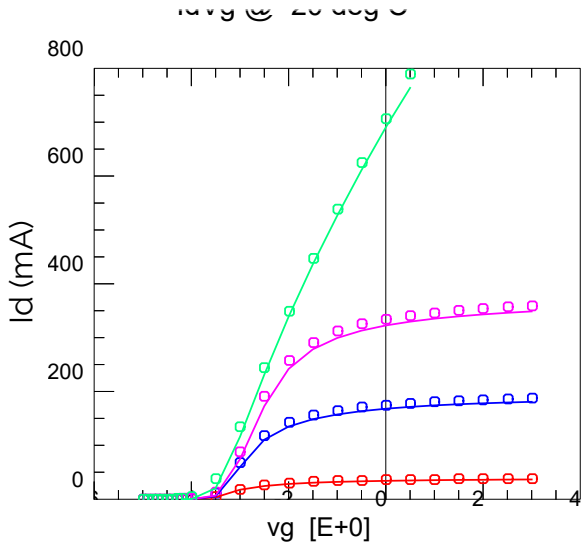
Log Output Characteristics @ -20℃

Derivative of reverse output conductance versus Vd @ -20℃

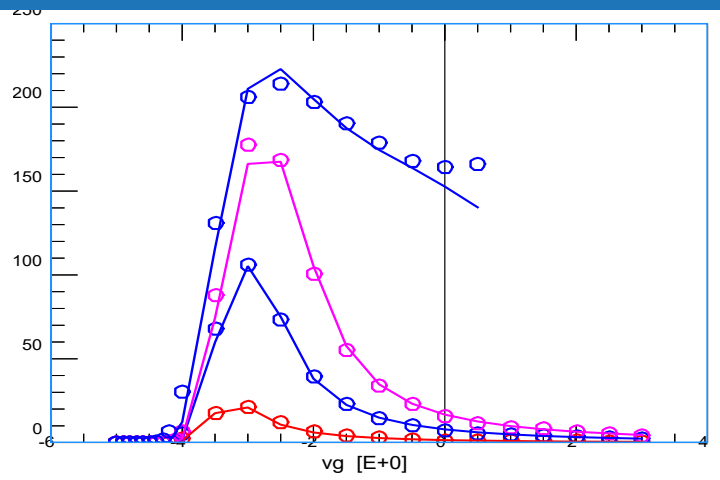


Modeling DC: Transfer Characteristics @ T=-20°C

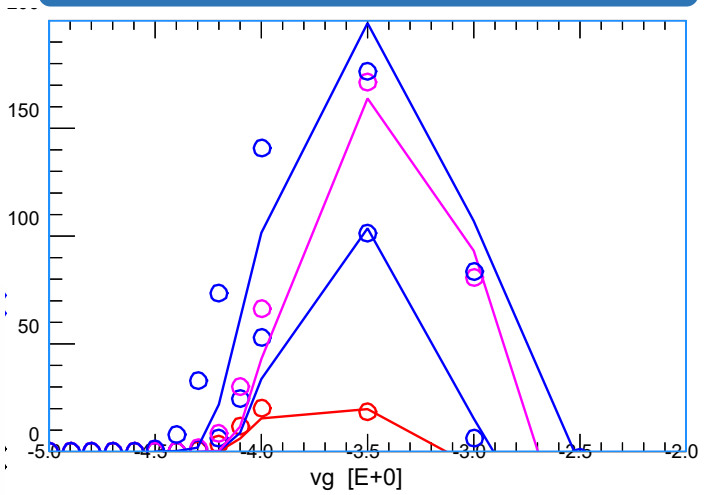
The model scales accurately to sub-zero temperatures.



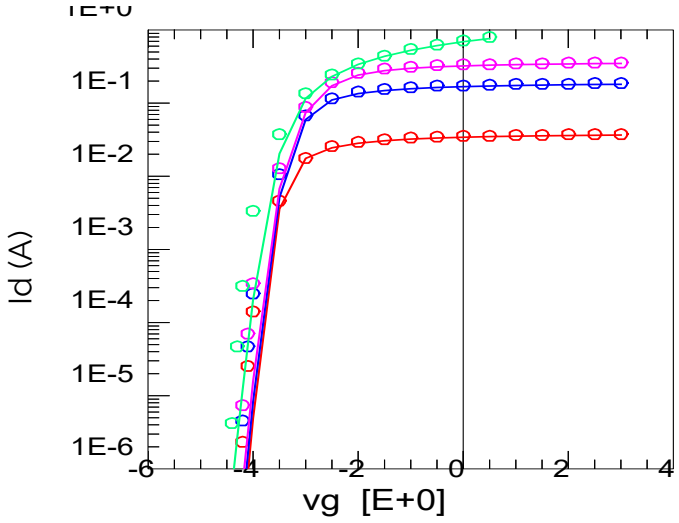
Transfer Characteristics @ T=-20°C



Transconductance @ T=-20°C

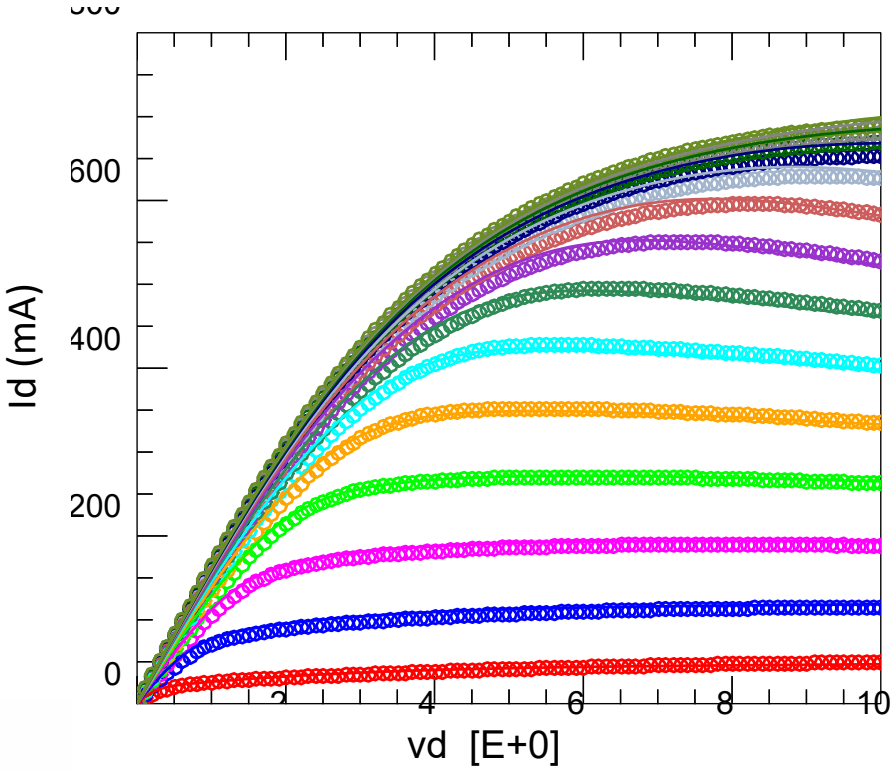


Derivative of Transconductance @ T=-20°C



Transfer Characteristics (Log) @ T=-20°C

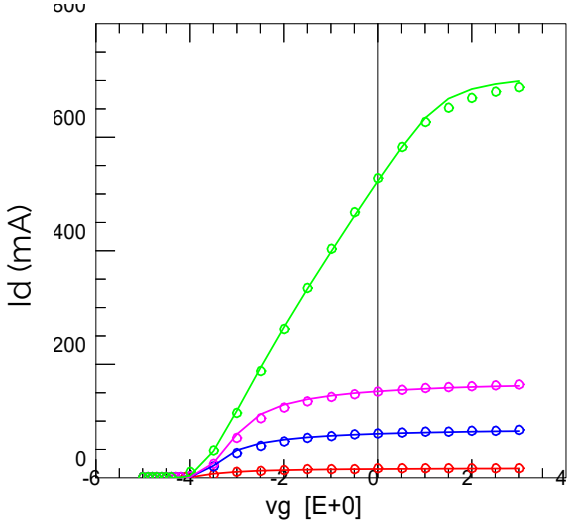
Modeling DC: IV Characteristics @ T=100°C



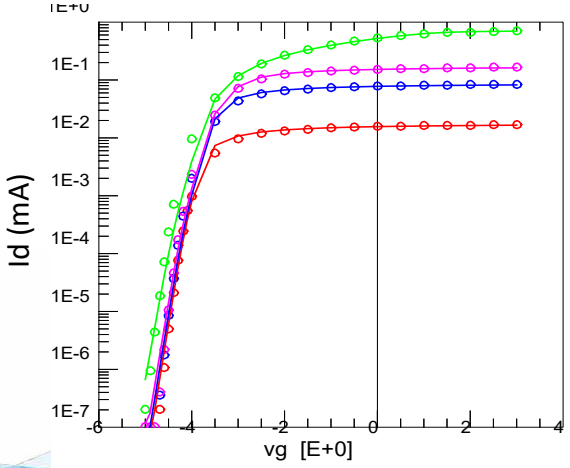
Output Characteristics @ T=100°C

The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.

Transfer Characteristics @ T=100°C

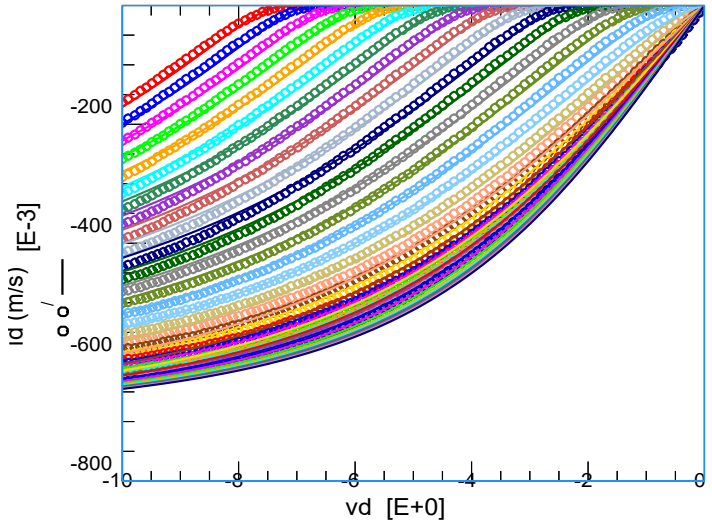


Transfer Characteristics (Log) @ T=100°C



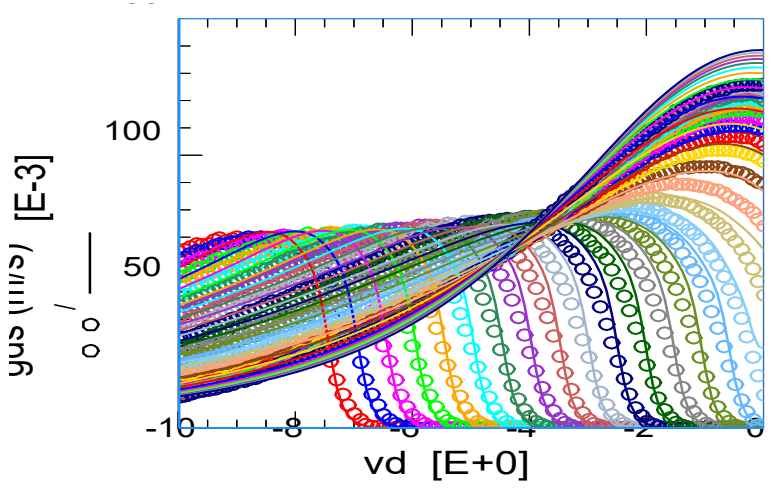
Modeling DC: Reverse Output Characteristics @ T=150℃

Vg from -12 to 3 V @ 0.5V step

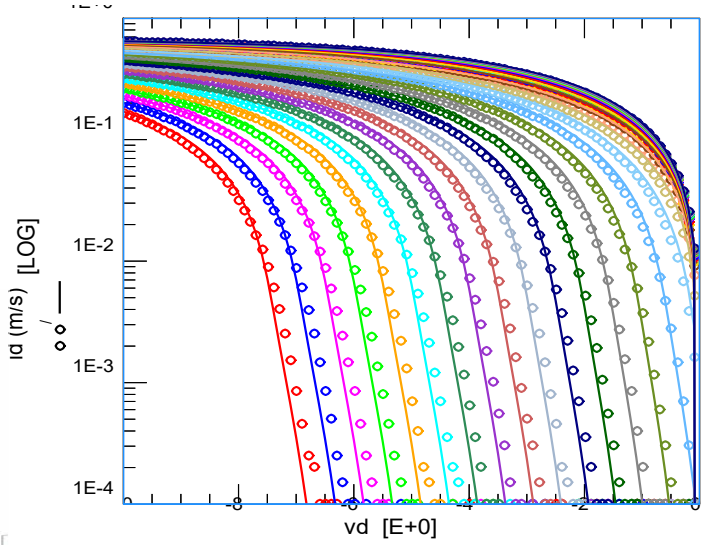


Reverse Output Characteristics @ 150℃

Reverse Output conductance versus Vd @ 150℃

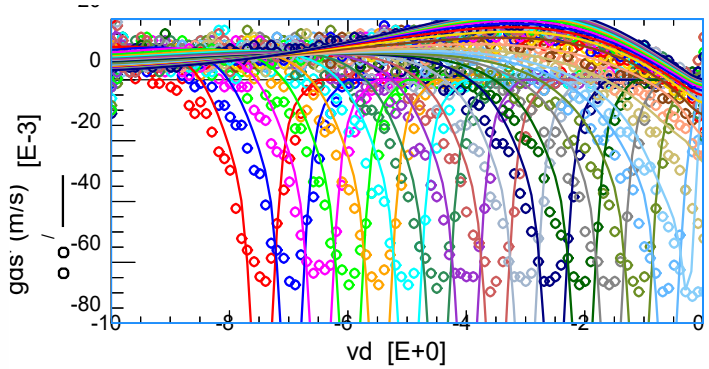


The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.

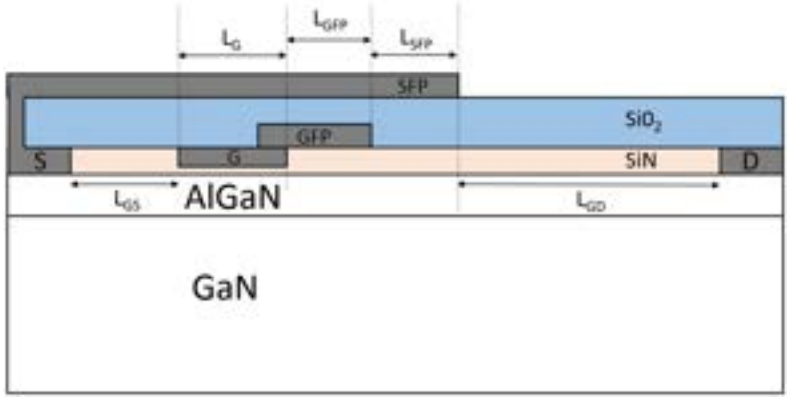


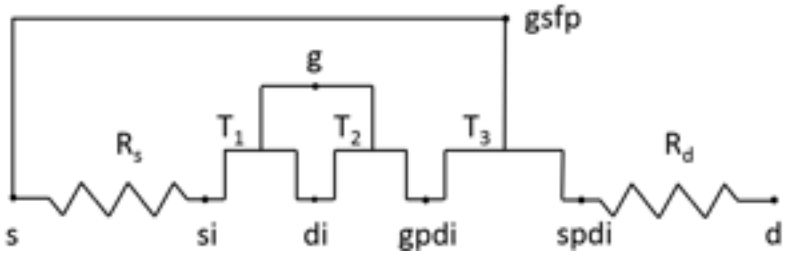
Log Output Characteristics @ 150℃

Derivative of reverse output conductance versus Vd @ 150℃



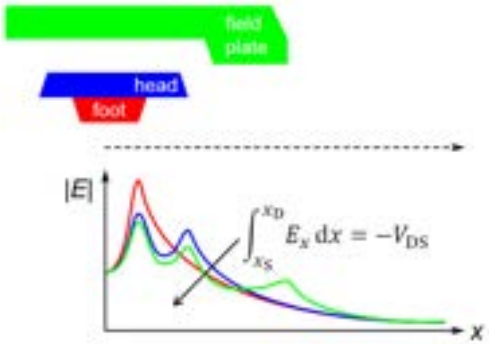
Modeling field plates: Structure





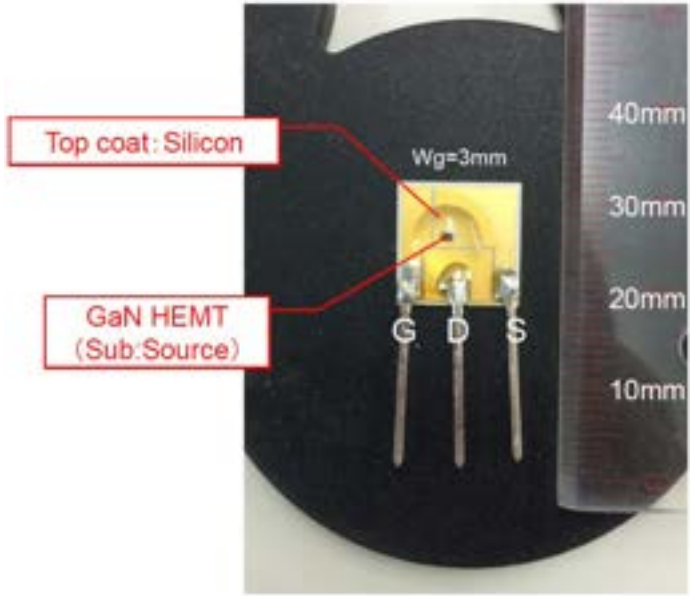
A Gate Field Plate (GFP) and a Source Field Plate (SFP) structure modeled as transistors in series.

Field plates flatten out the peak in the electric field caused by the sudden drop in potential at the gate edge. TCAD showing field fluctuations leading to a distributed field inside the device.

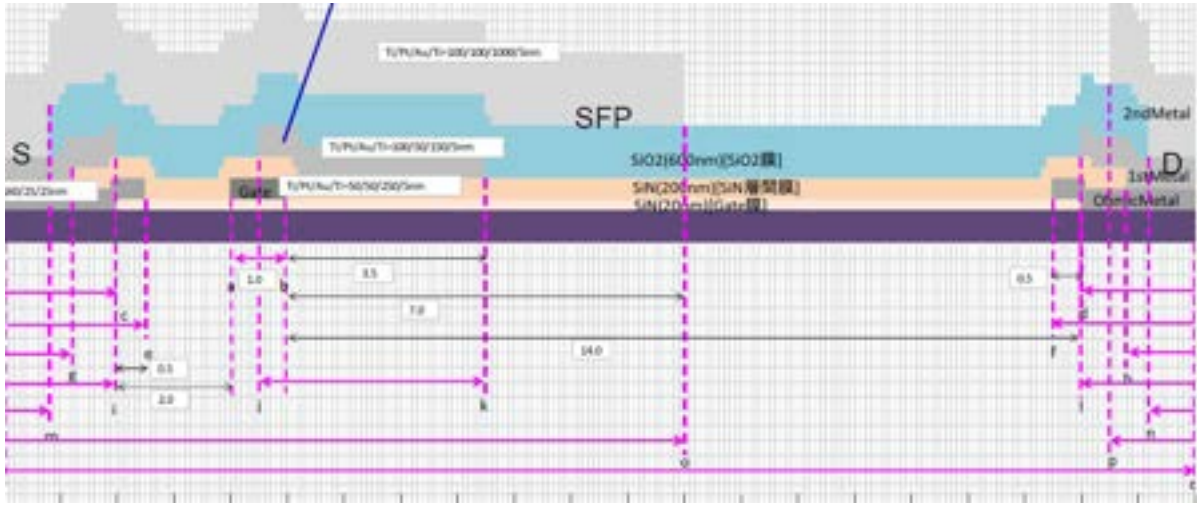


[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

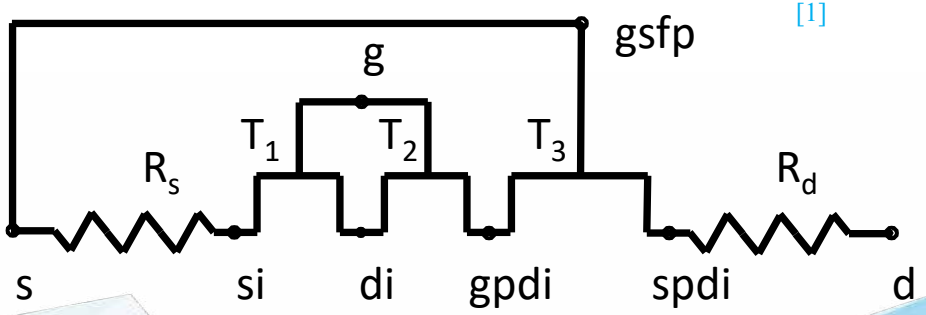
Dual FP GaN HEMT DUT



Picture of the GaN device under test

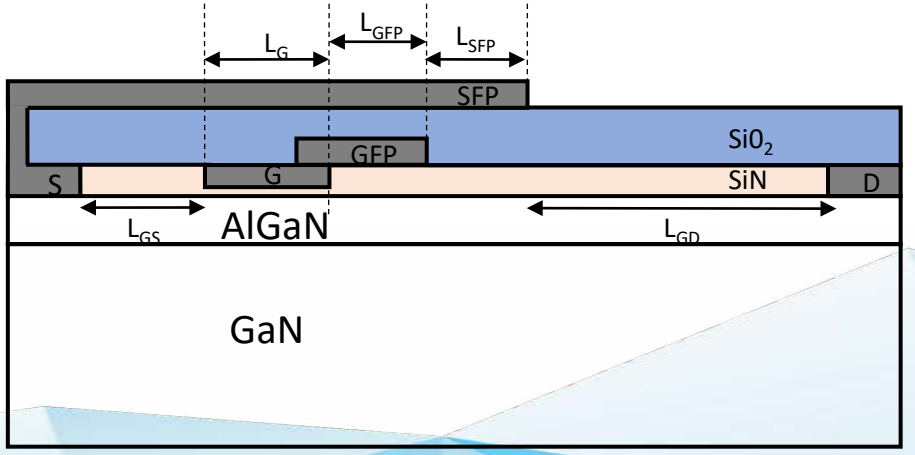


Field-plate configuration as provided by Toshiba



[1]

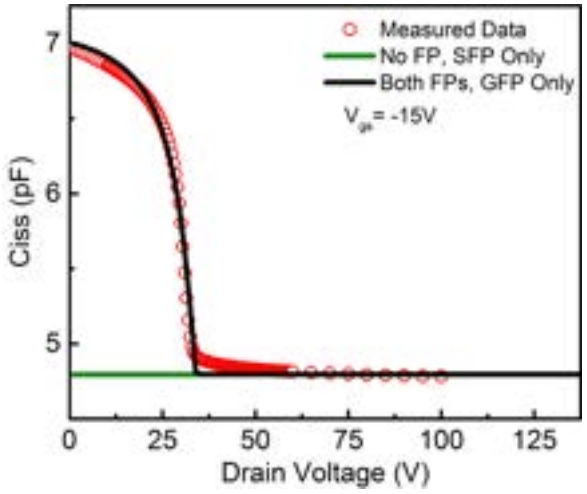
Model representation of the device



Schematic of the dual FP GaN device

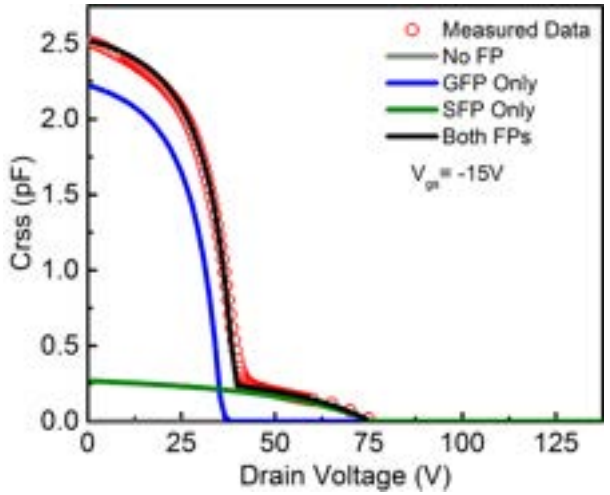
[1] S. A. Ahsan *et al.*, *IEEE Trans. Electron Devices*, **63 (2)**, [2016]

Modeling field plates: Trends w.r.t Drain Voltage

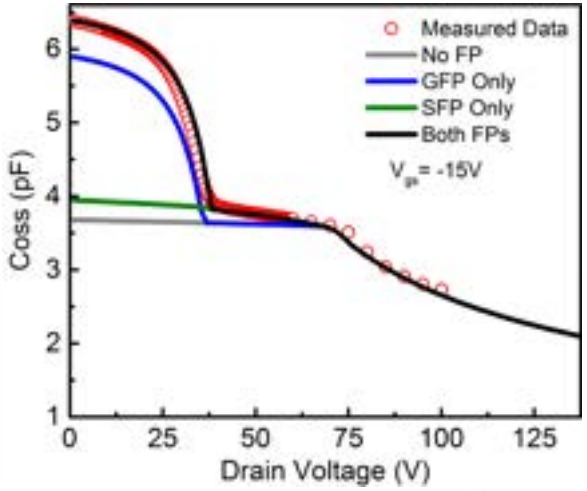


Terminal Capacitance: Input side (Ciss)

Terminal Capacitance: Reverse (Crss)

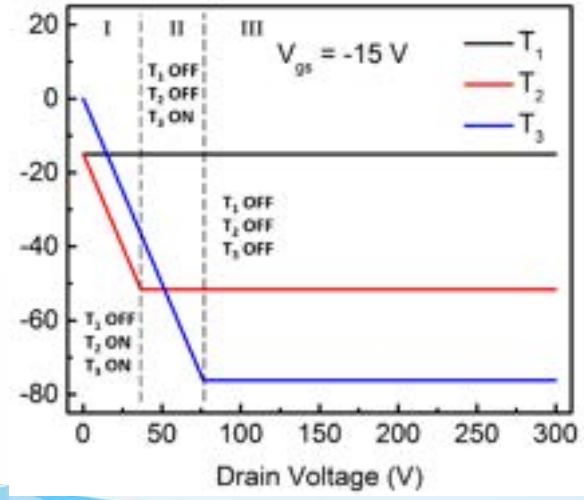


*The plateaus in each capacitance curve denote the **switching-off** of one of the transistors in series as depicted in the previous slide.*



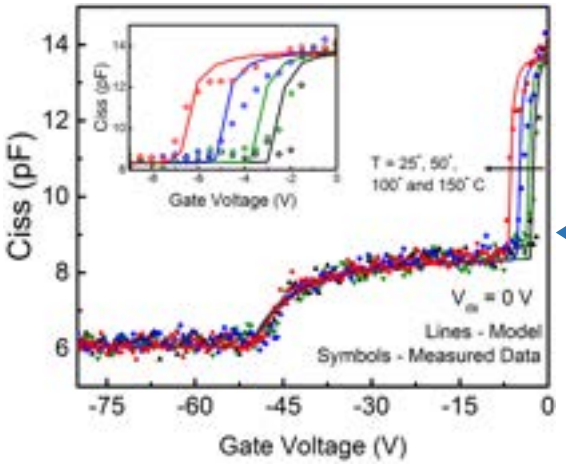
Terminal Capacitance: Output side (Coss)

Activation of different series transistors with increasing drain voltage at a fixed gate bias



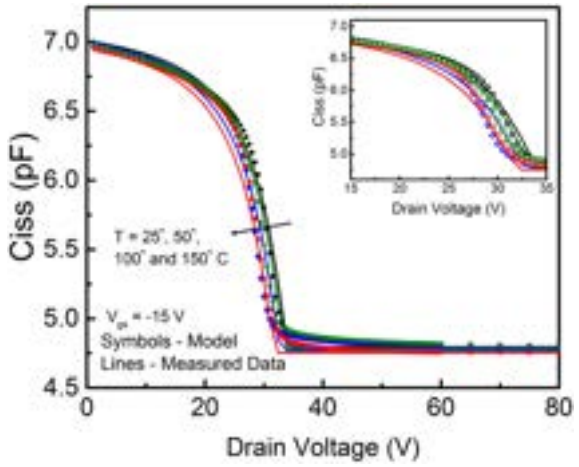
[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Field Plate Models: Trends w.r.t temperature

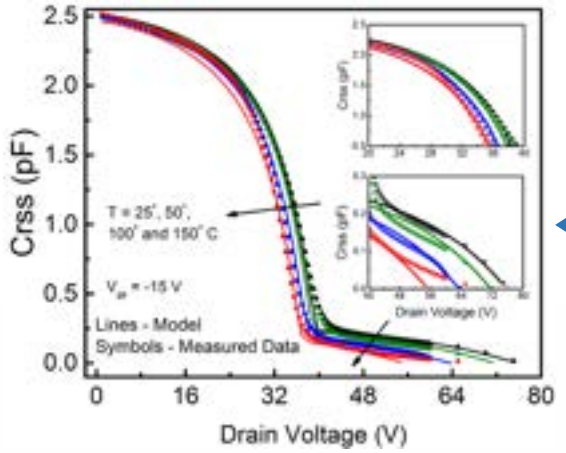


Terminal Capacitance: Input side (Ciss) with gate voltage

Terminal Capacitance: Input side (Ciss) with drain voltage

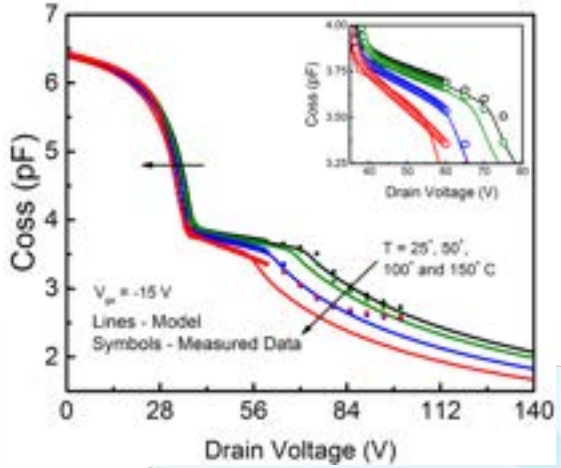


Increasing temperature shifts the threshold voltage in the negative direction – leading to a corresponding shift in the capacitance curves.



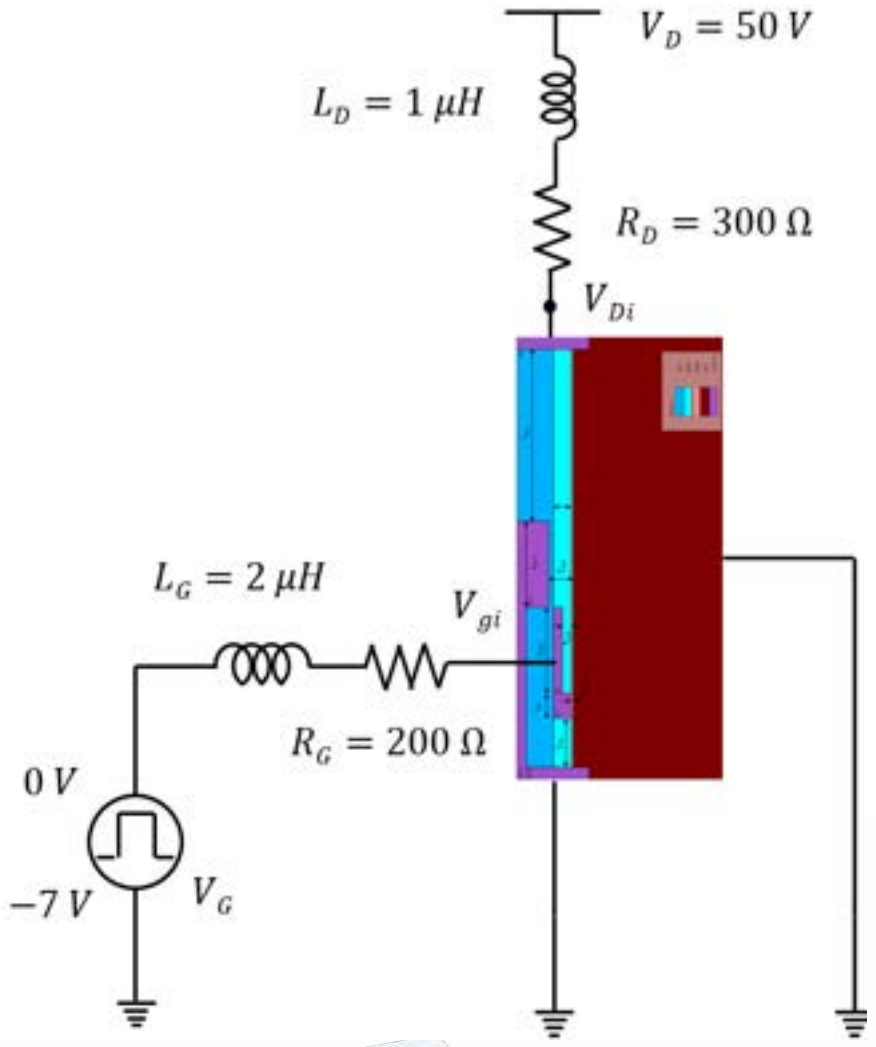
Terminal Capacitance: Reverse (Crss)

Terminal Capacitance: Output side (Coss)



[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

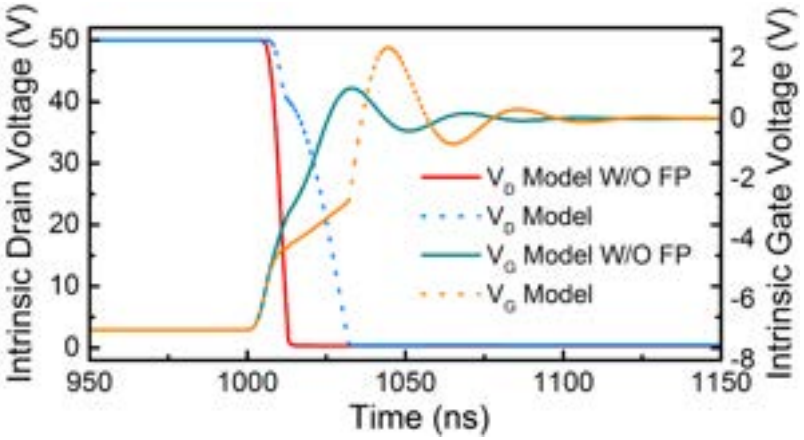
Mixed mode TCAD circuit using ATLAS



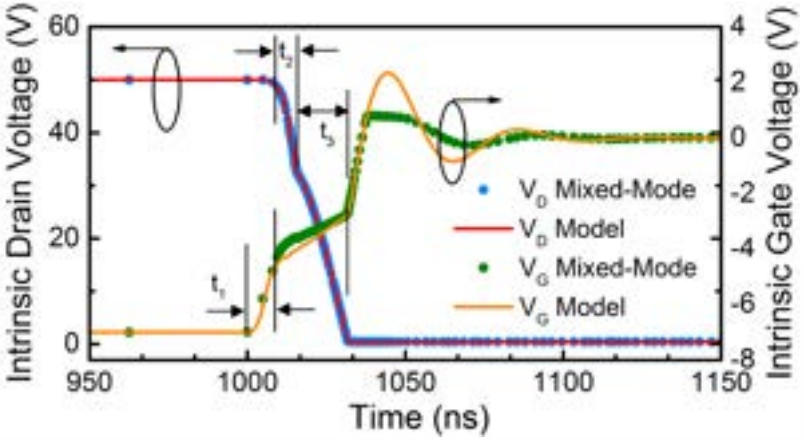
- *Schematic for Mixed-mode simulation using the numerical GaN FP device generated in Atlas.*
- *The FP-HEMT is put as the DUT with 7 V and 0 V pulses of 1 MHz at gate.*
- *The pulse has a pulse-width of 480 ns 20 ns rise and fall times.*
- *Supply voltage of 50 V is chosen to capture the maximum effect of cross coupling capacitances on switching transients while an inductive load is put at the drain.*

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Voltage waveforms

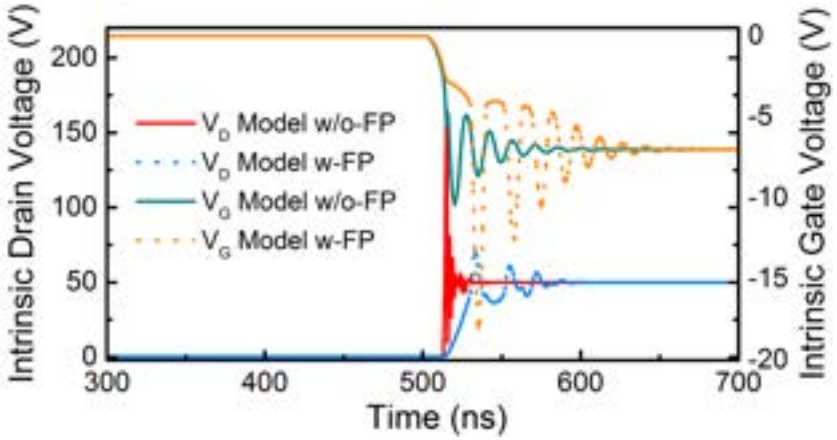


Turn-on by switching applied gate signal from 7 V to 0 V (FP vs no FP)

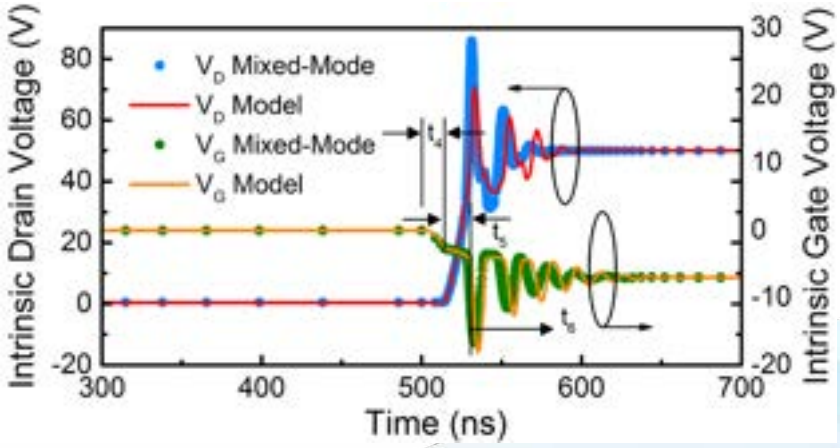


Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)

The model accurately predicts drain overshoots due to LC ringing, Miller plateaus due to accurate prediction in sharing of the gate drive current to charge Cgs and Cgd and the associated gate-drain charge, and the damping of the oscillations.



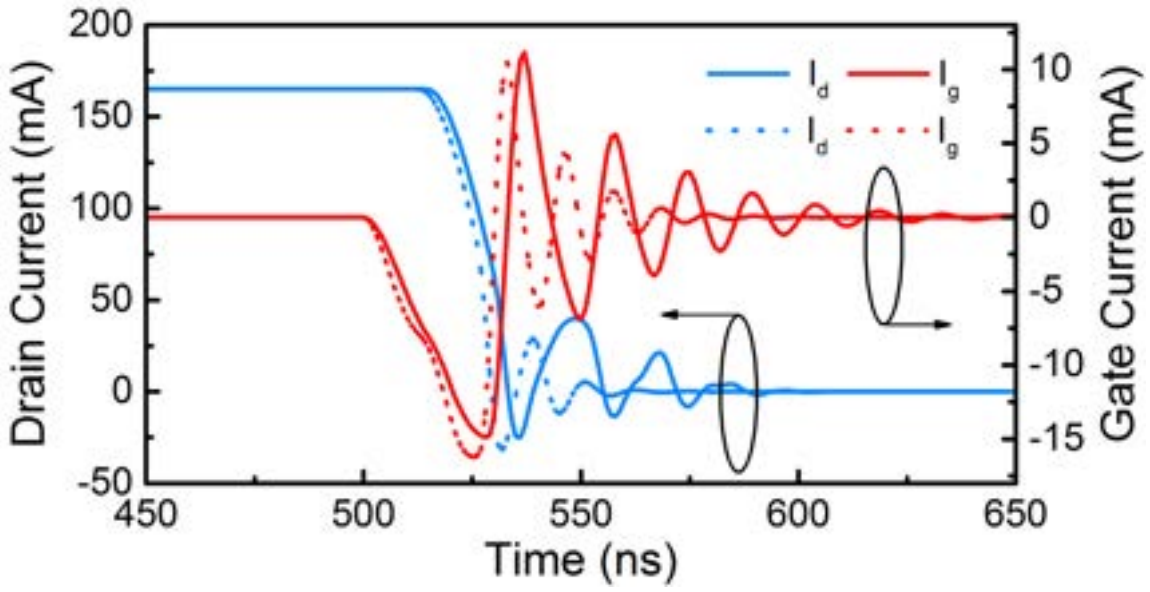
Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (FP vs No FP)



Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed-mode vs Model)

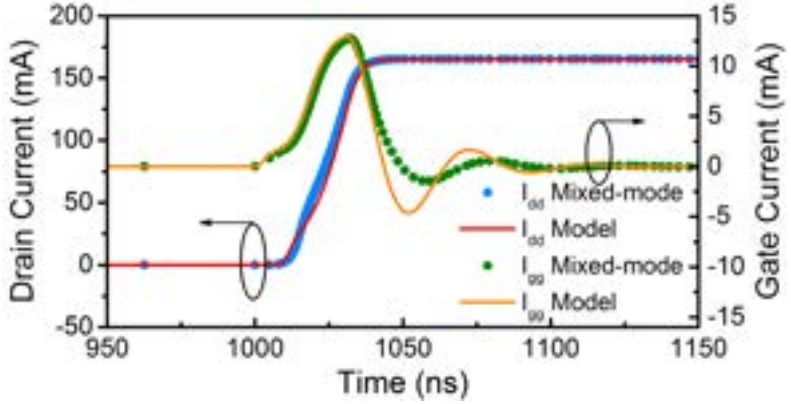
[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Current Waveforms

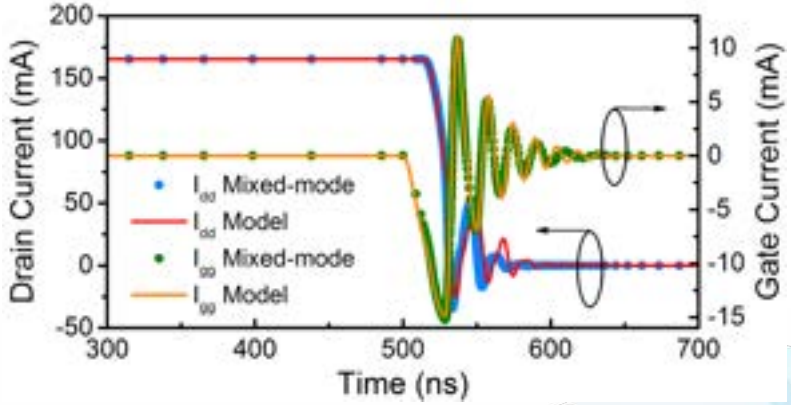


Comparison of modeled time-domain waveforms during turn-off with and without cross-coupling and substrate capacitances.

Solid lines = Cross-Coupling(CC) and substrate model included
Dotted lines = CC and substrate model excluded.



Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)



Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed-mode vs Model)

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

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- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
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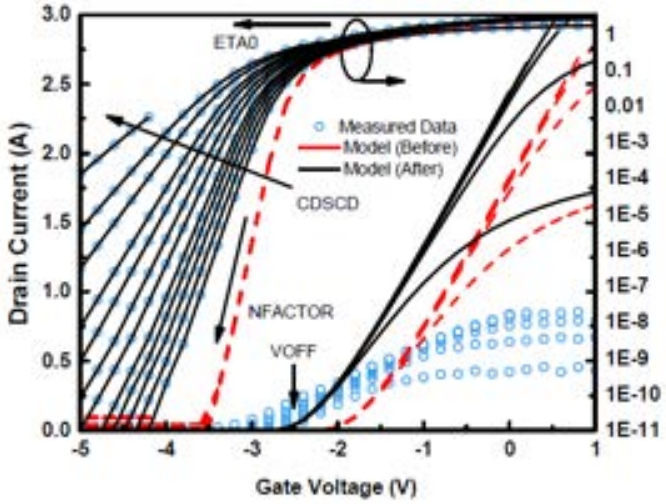
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

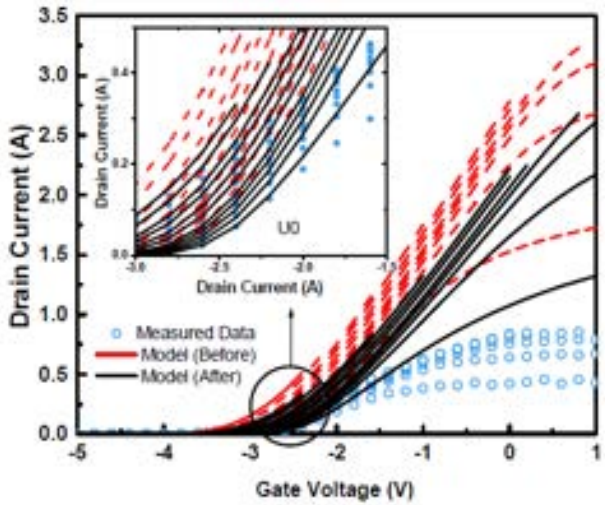
Modeling RF Devices using ASM-HEMT

- *Extracting DC Parameters*
- *RF Model Extraction*
- *Large signal simulations*
- *Load Pull Simulations*

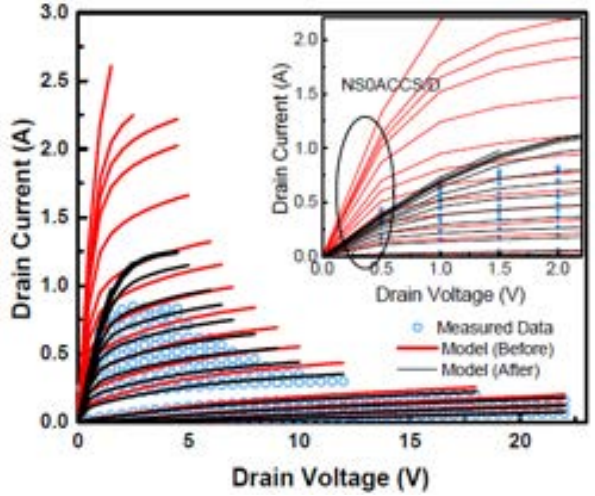
Extracting DC Parameters



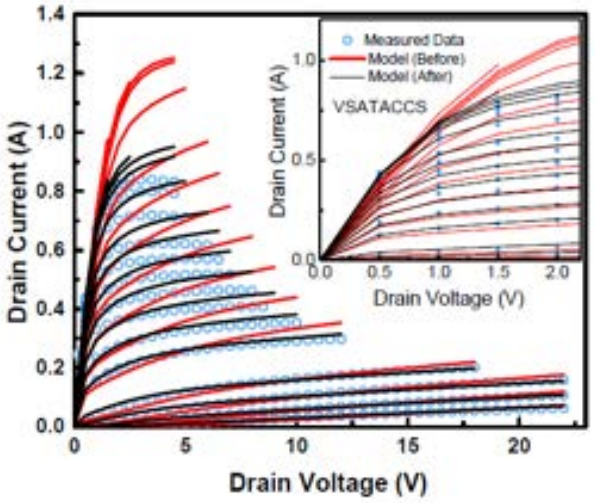
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



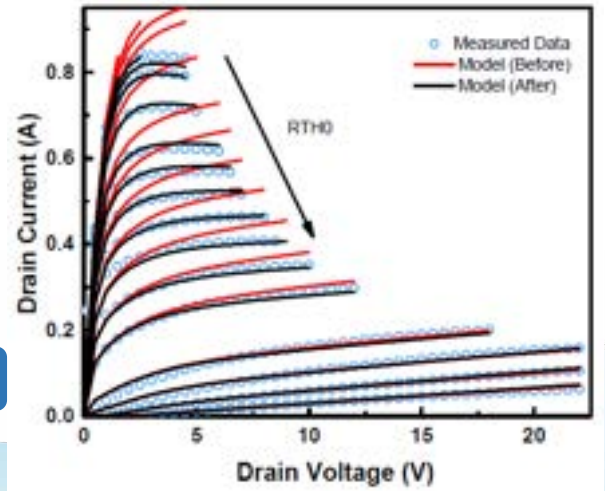
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



$I_d - V_d$ (Extract $V_{SATACCS}$)



$I_d - V_d$ (Extract R_{TH0})

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

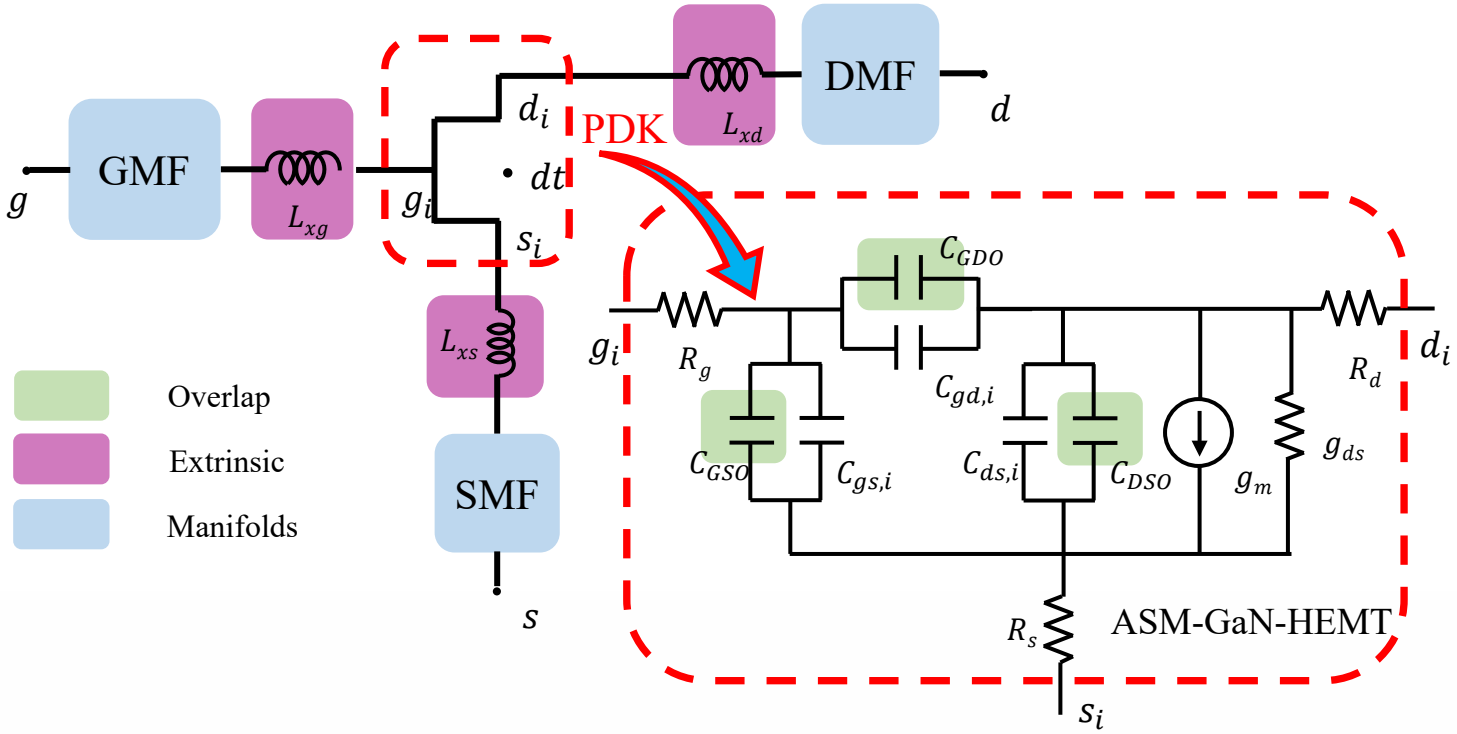
RF Model & Extraction I

Three step methodology

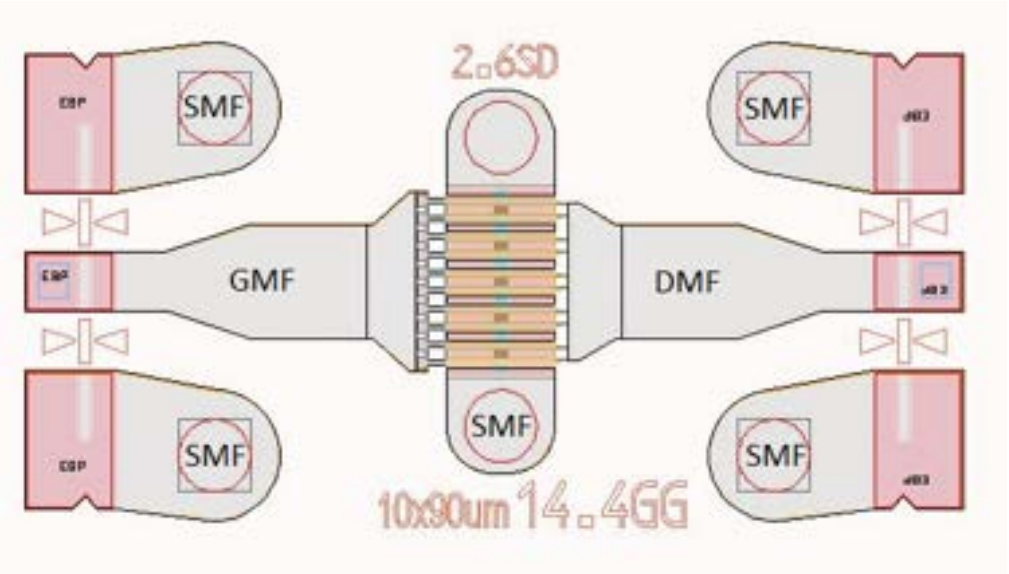
- De-embed manifolds
- Extract the intrinsic core model - Using low frequency Y-parameters
- Extract Inductances - Using high frequency Y-parameters

Model

- Core surface potential based PDK
- Access region resistances included in core
- Bus-inductances in extrinsics



Pad-level Small Signal Equivalent Circuit Model



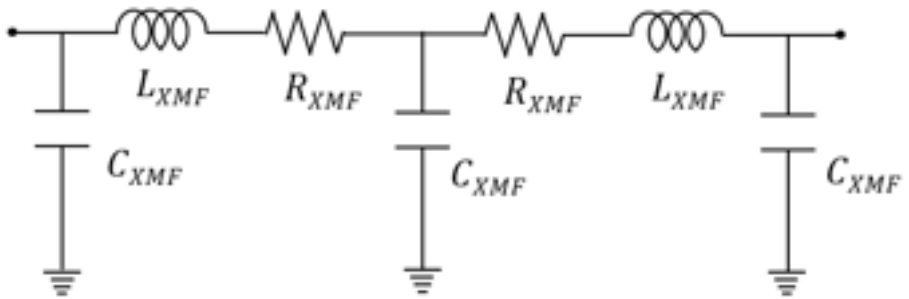
Device Layout

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

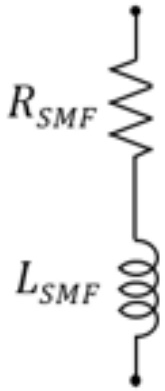
RF Model & Extraction II: Pad Parasitics

Manifolds/Pads

- Used to probe the device
- Feed the signal to gate, drain & source bus-inductances
- Measurements obtained using TRL Calibration
- Transmission line type model
- Reciprocal (may/may not be symmetric)
- De-embedded using "deembed" s2p components in ADS

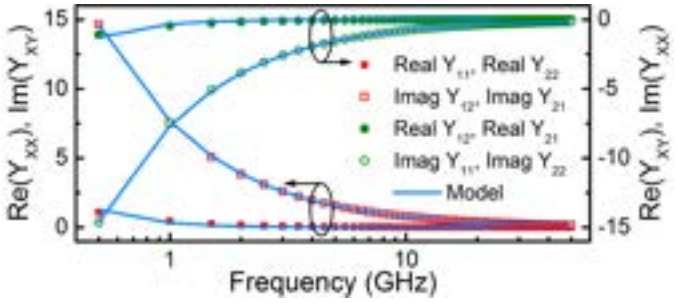


Symmetric network used for GMF/DMF

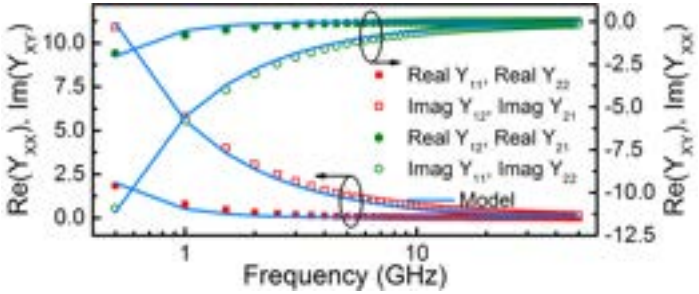


Single port SMF network

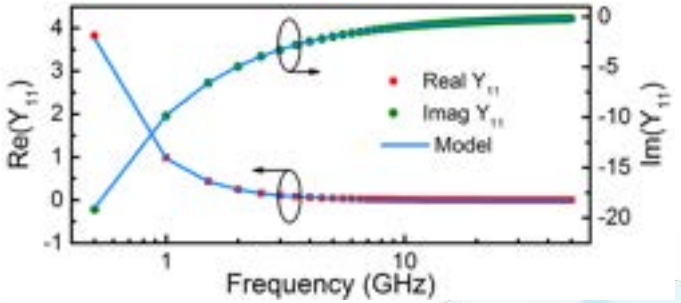
Y-parameters for DMF



Y-parameters for GMF



Y-parameters for SMF



[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

RF Model & Extraction III: Bus Inductances

$$Y_{11} = \frac{\omega^2 C_{gg}{}^2 R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} + \frac{j\omega C_{gg}}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{12} = -\frac{\omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} - \frac{j\omega C_{gd}}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{21} = \frac{g_m - \omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} - \frac{j\omega (C_{gd} + g_m C_{gg} R_g)}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{22} = g_{ds} + \frac{\omega^2 (C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg} (1+g_m R_g))}{1+\omega^2 C_{gg}{}^2 R_g^2} + j\omega C_{ds} + \frac{j\omega C_{gd}(1+g_m R_g) + j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

Key Pointers

- The effect of bus-inductances is ignored at low frequencies (assumption)
- Drain & Source access region resistances ignored from hand analysis (not an assumption, it is an advantage)
- Ignore some terms at low frequency (~ 10 GHz) (assumption)
- Very simple – only need to adjust overlap capacitances & gate finger resistances (advantage)

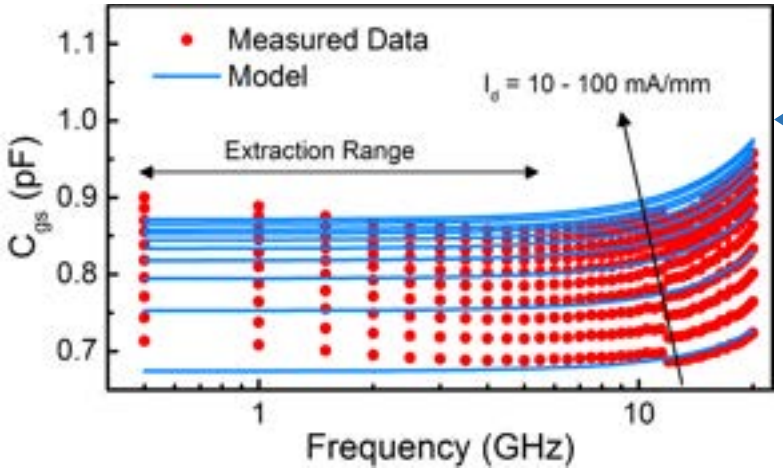
$$[Y] \approx \begin{bmatrix} \omega^2 C_{gg}{}^2 R_g + j\omega C_{gg} & -\omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd} \\ g_m - j\omega (C_{gd} + g_m C_{gg} R_g) & g_{ds} + j\omega (C_{ds} + C_{gd}(1+g_m R_g)) \end{bmatrix}$$

$$\begin{bmatrix} C_{gs} & C_{gd} & C_{ds} \\ g_m & g_{ds} & R_g \end{bmatrix}$$

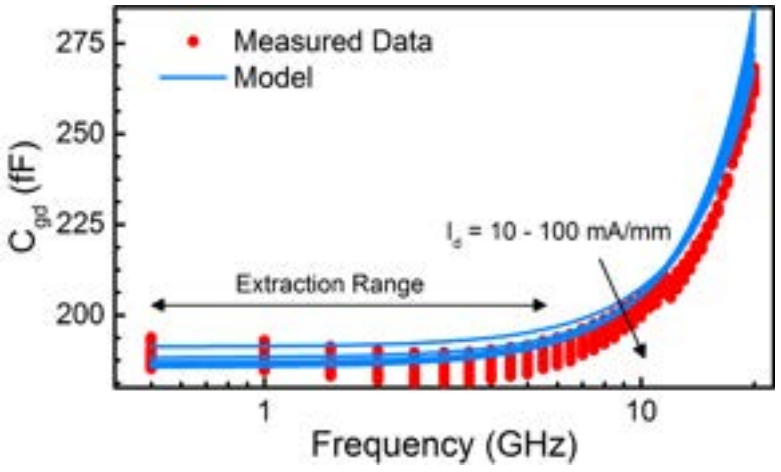
$$\begin{bmatrix} (\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}])/\omega & -\mathrm{Im}[Y_{12}]/\omega & \mathrm{Im}[Y_{22}]/\omega - C_{gd}(1+g_m R_g) \\ \mathrm{Re}[Y_{21}] & \mathrm{Re}[Y_{22}] & \mathrm{Re}[Y_{11}]/(\omega^2 C_{gg}^2) \end{bmatrix}$$

[1] I. Kwon et al., IEEE Trans. Microw. Theory Techn., 50 (6), [2002]

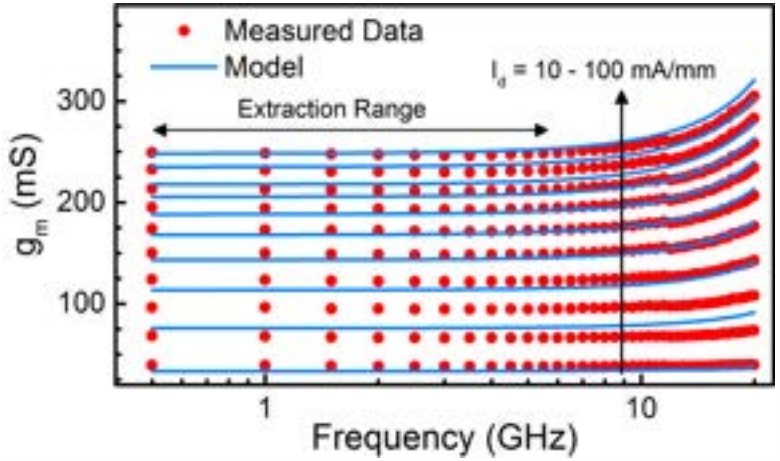
Fitting core model parameters using ADS



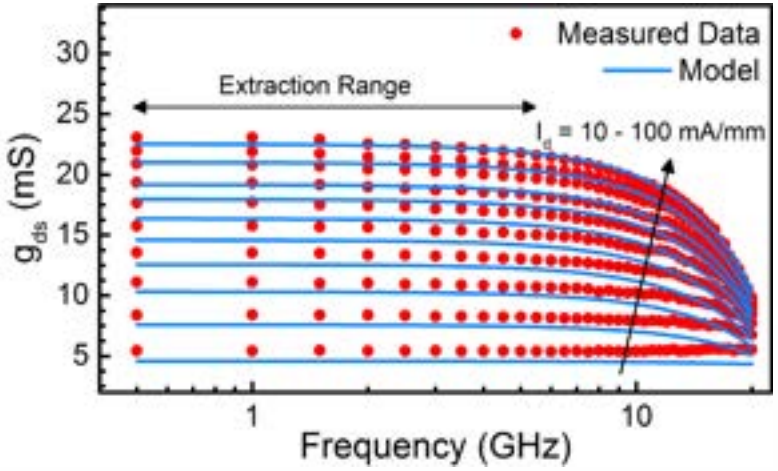
Extract C_{GSO}



Extract C_{GDO}



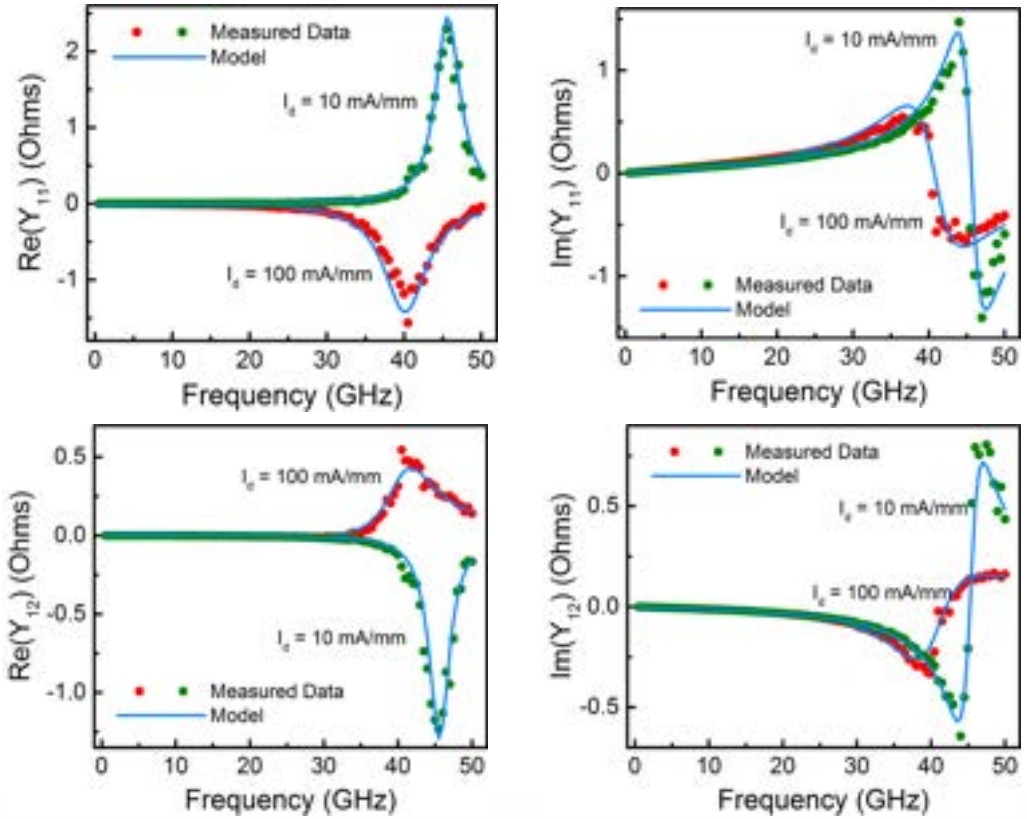
g_m dispersion handled by trap model



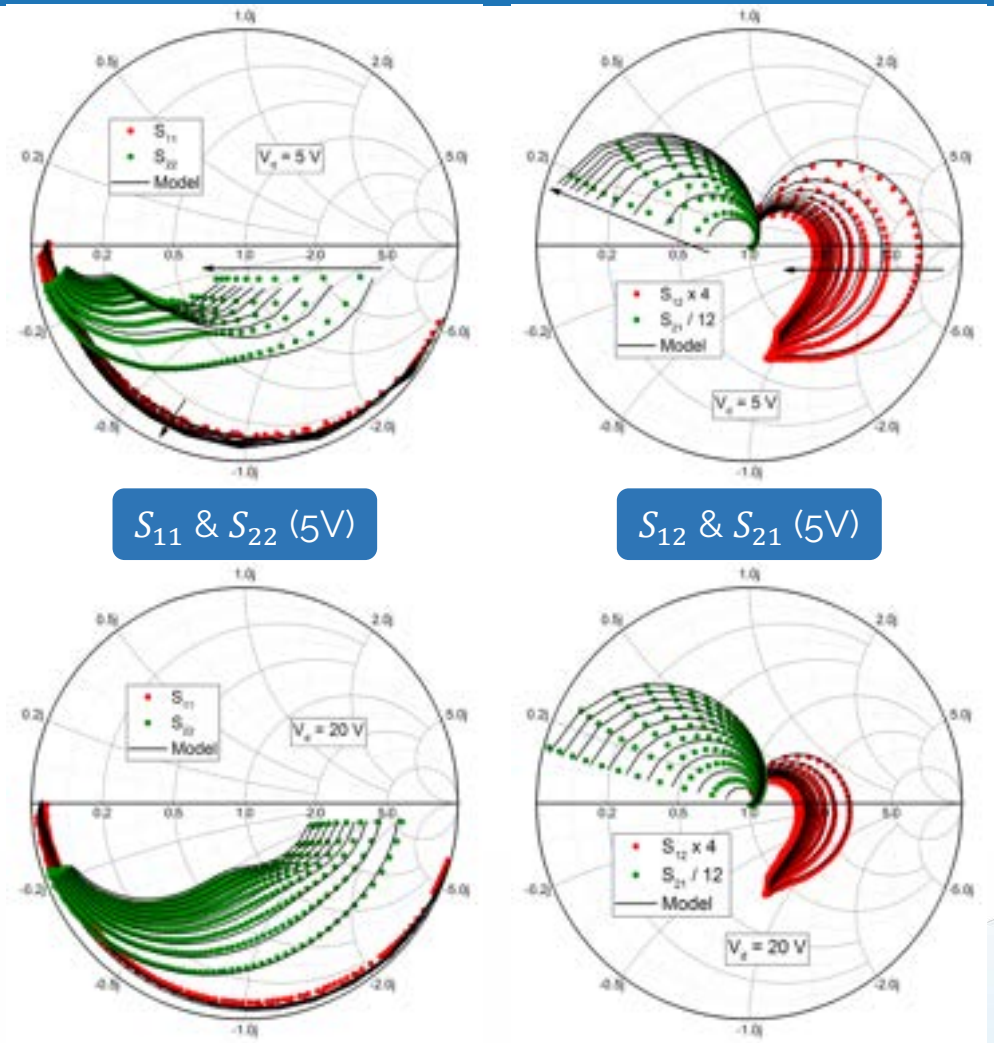
g_{ds} dispersion handled by trap model

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Bus Inductance fitting



Resonant peaks due to interaction of inductances with intrinsic capacitances



S_{11} & S_{22} (5V)

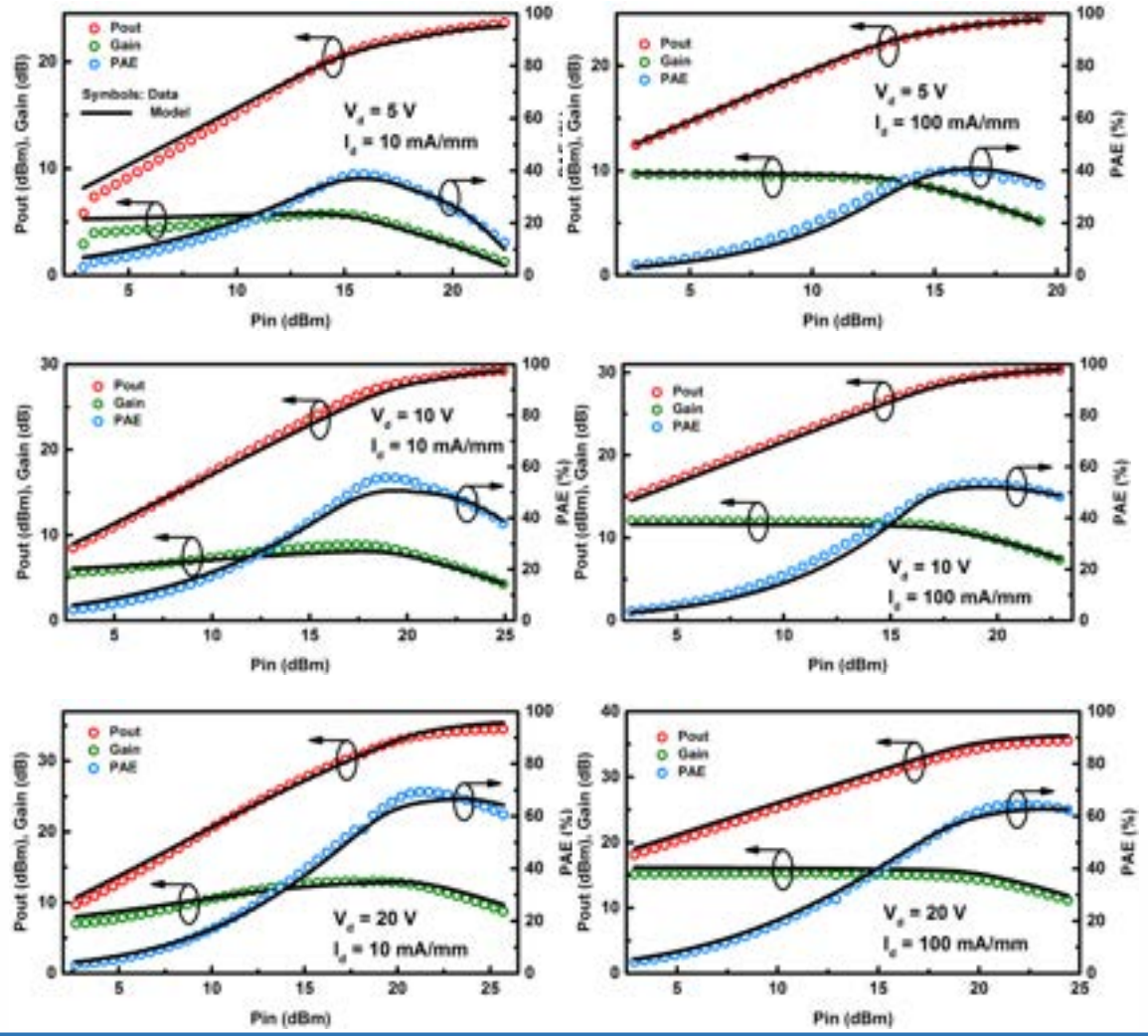
S_{12} & S_{21} (5V)

S_{11} & S_{22} (20V)

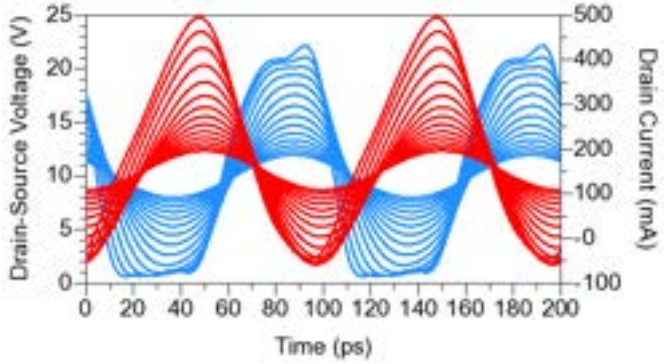
S_{12} & S_{21} (20V)

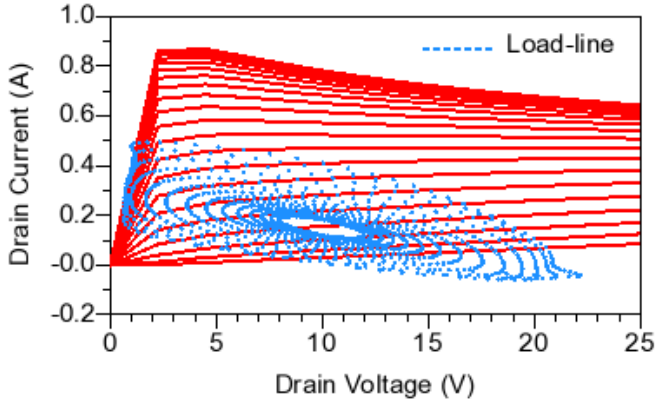
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Large Signal HB Simulations



Harmonic balance drive-up characteristics showing Pout, PAE & Gain



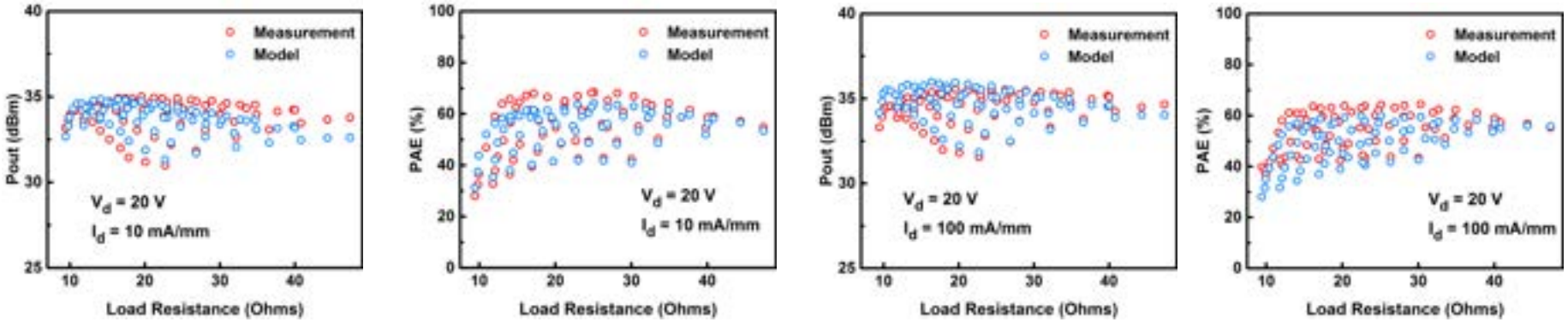


Time domain waveforms of drain voltage & current. Load line contours spanning the IV plane

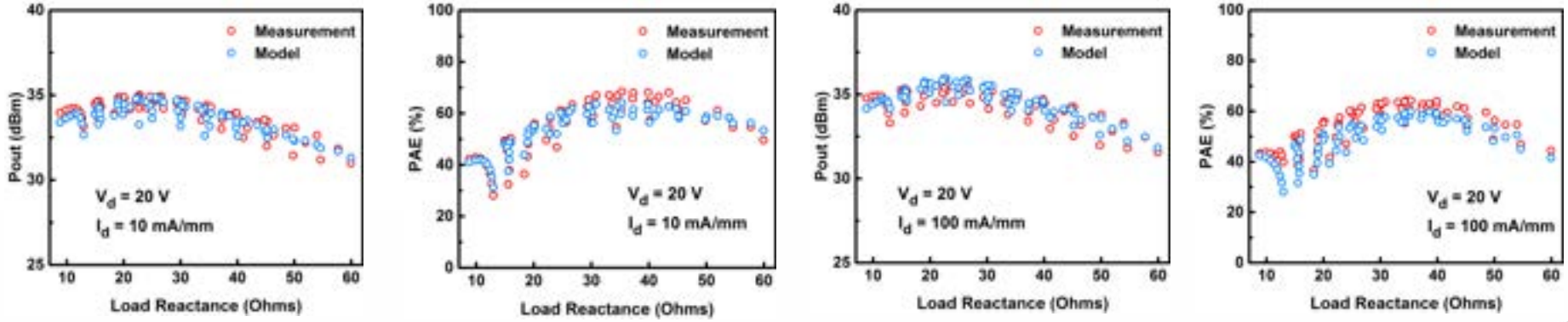
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Validation – Real and Imaginary Loads

Fairly accurate in predicting the maxima for Pout & PAE



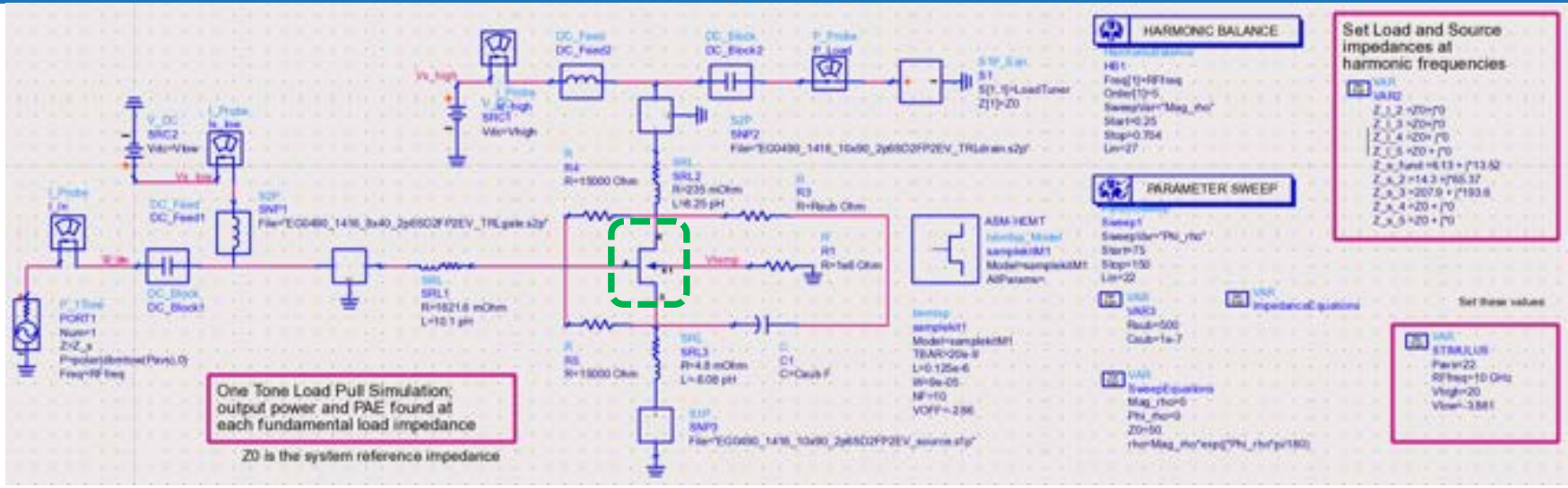
Pout & PAE against load resistance (real load)



Pout & PAE against load reactance (imaginary load)

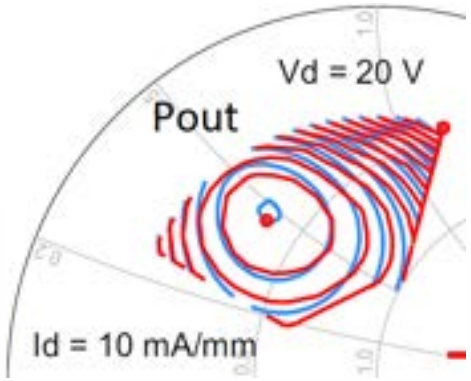
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

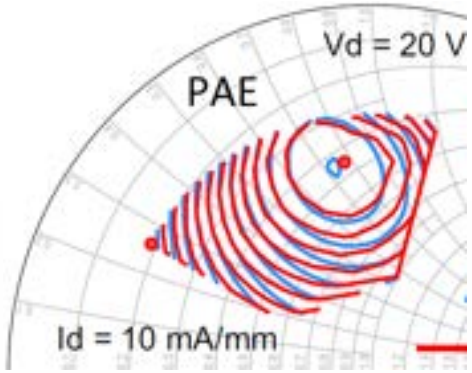
Load Pull simulations using ASM-HEMT

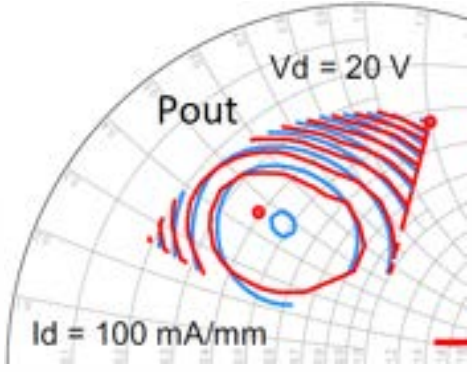


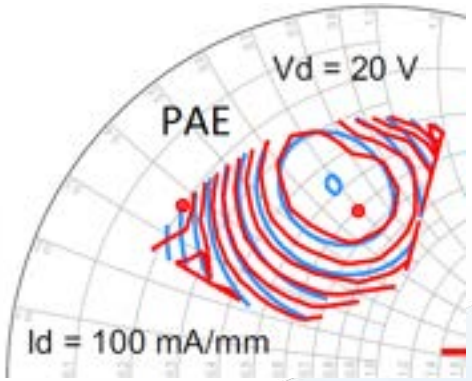
ADS Schematic for simulation of load-pull contours

22 dBm signal @ 10 GHz









Pout & PAE load pull contours for 10 mA/mm

Pout & PAE load pull contours for 100 mA/mm

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

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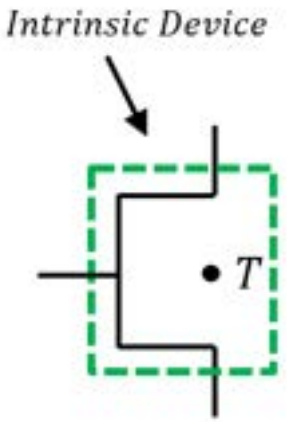
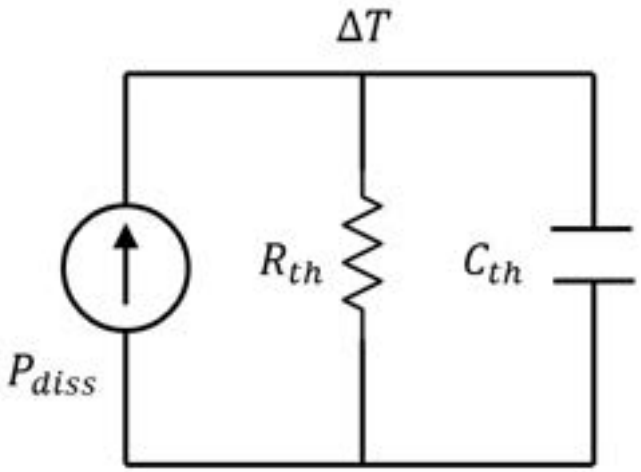
Characterizing Self Heating and its Modeling

- *Self heating Model*
- *Characterization*

Self- Heating Model



$T = T_{NOM} + \Delta T$



$P_{diss} = I_d \times V_d$

Self-Heating Effect

- The self-heating circuit is defined in a thermal discipline.
- For the thermal discipline, power is the equivalent of "current" and temperature is the equivalent of "voltage"

Under these conditions, applying KCL on the thermal subcircuit, we have:

$$P(R_{th}) = \frac{Temp(R_{th})}{RTH0}$$

$$P(R_{th}) = \frac{d}{dt}(Temp(R_{th}) \cdot CTH0)$$

Characterization

$$T_{J1} = T_{NOM,1} + R_{th} \times P_{diss1}$$

$$T_{J2} = T_{NOM,2} + R_{th} \times P_{diss2}$$

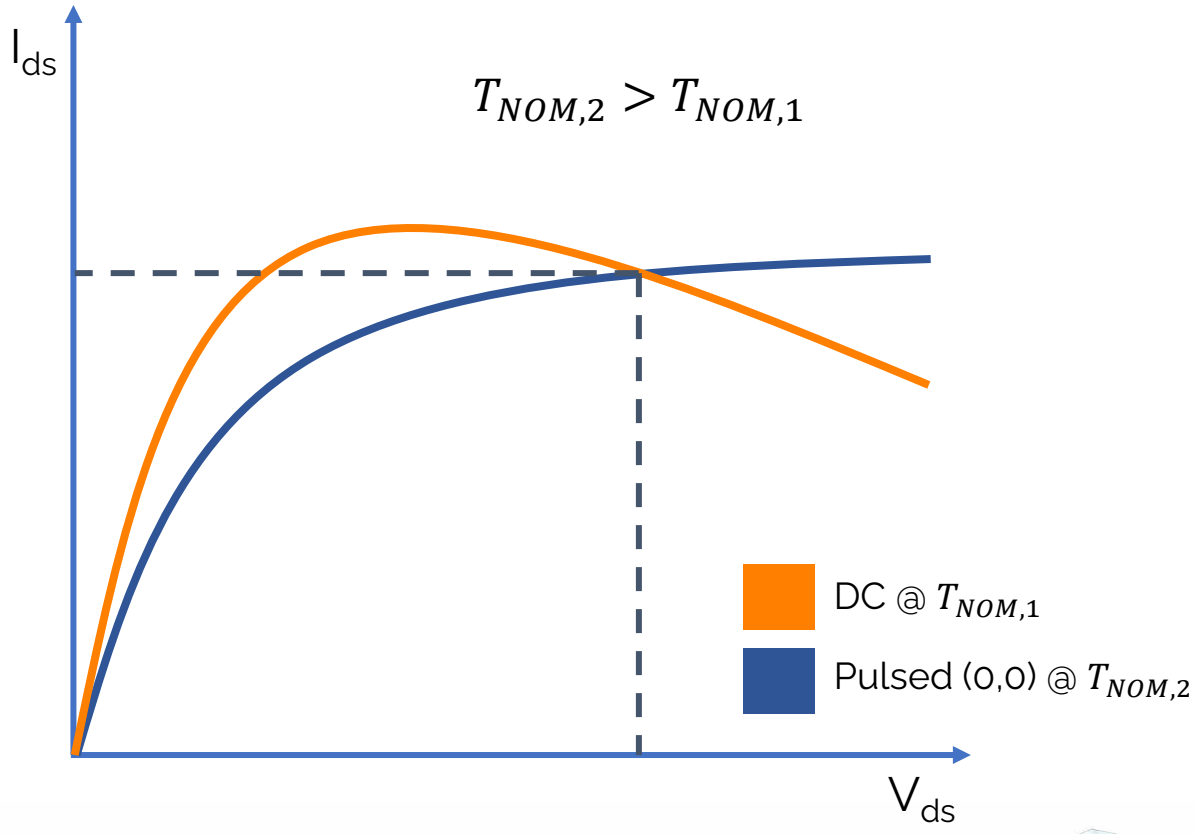
At the intersection point:

$$T_{J1} = T_{J2}$$

And $P_{diss2} = 0$ (Pulsed at (0,0))

$$\Rightarrow R_{th} = \Delta T_{NOM} / \Delta P_{diss}$$

With the ASM-HEMT model, the parameter **RTH0** is tuned till the simulated intersection point overlaps with the measured intersection point after thermal parameters like **UTE**, **AT** and **KT1** have been extracted.



Extracting R_{th} – Both curves are measured at the same Vgs. The intersection point denotes a common junction temperature.

Our model has been recently implemented in Keysight ICCAP.

[1] T. Peyretaillade et al.,1997 IEEE MTT-S International Microwave Symposium Digest, Denver, CO, USA, 1997. doi: 10.1109/MWSYM.1997.596619.

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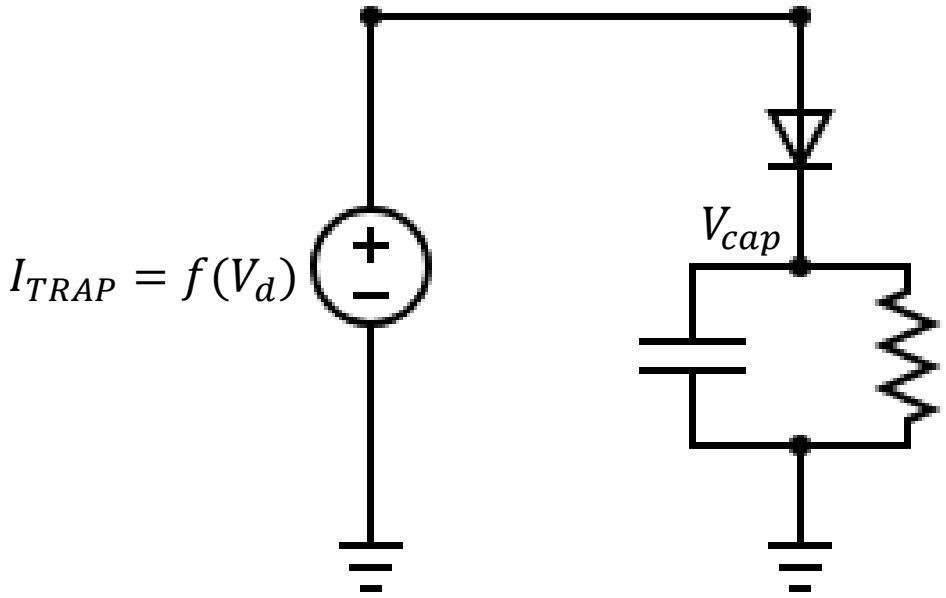
Trapping models in ASM-HEMT

- *Trapping Models in ASM-HEMT*
- *Extraction using pulsed measurements*

Trapping Models in ASM-HEMT: TRAPMOD I



Key highlights

- Dependent on drain voltage only
- Bias-dependent and bias-independent options
- Scales with signal power levels
- Suitable for RF
- Affects threshold voltage, DIBL, AR Resistance.

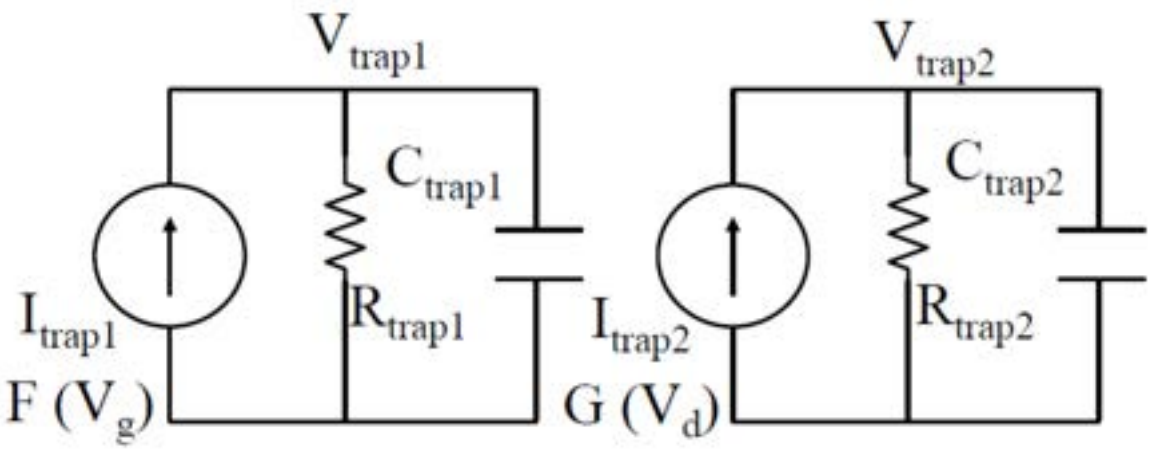
$$V_{OFF}(Trap) = V_{OFF} + (ATRAPVOFF + BTRAPVOFF \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_S(Trap) = R_S + (ATRAPRS + BTRAPRS \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_D(Trap) = R_D + (ATRAPRD + BTRAPRD \cdot e^{-\frac{1}{V_{cap}}})$$

$$\eta_0(Trap) = \eta_0 + (ATRAPETA0 + BTRAPETA0 \cdot e^{-\frac{1}{V_{cap}}})$$

Trapping Models in ASM-HEMT: TRAPMOD II



Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance
- Suitable for PIV simulation
- Affects threshold voltage, DIBL, Subthreshold Slope, AR Resistance.

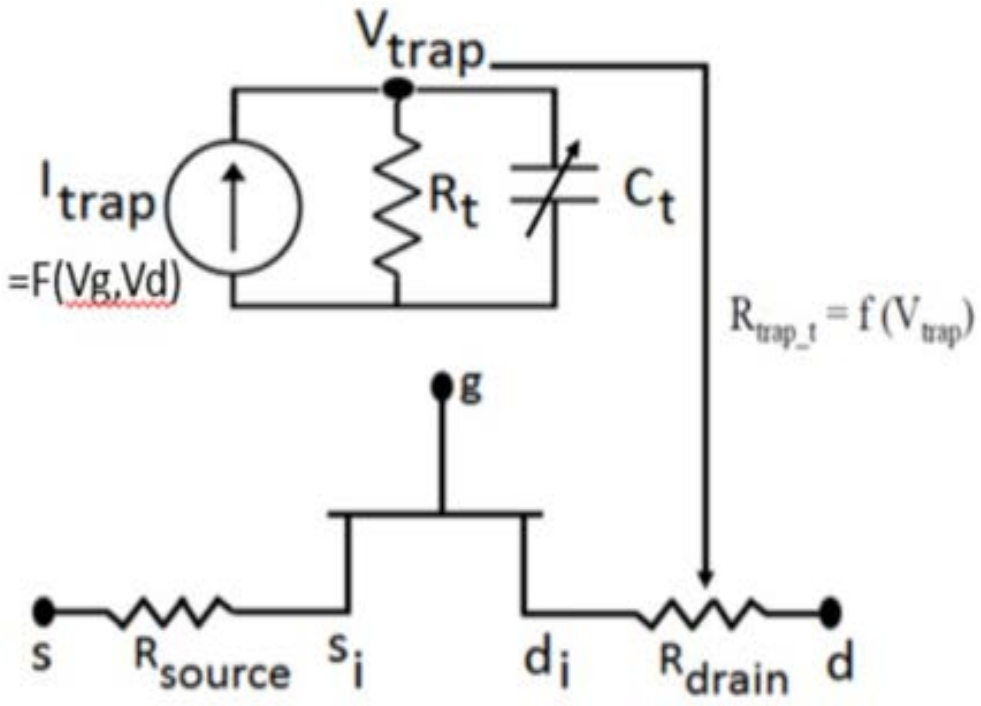
$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$

$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$

$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$

$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$

Trapping Models in ASM-HEMT: TRAPMOD III

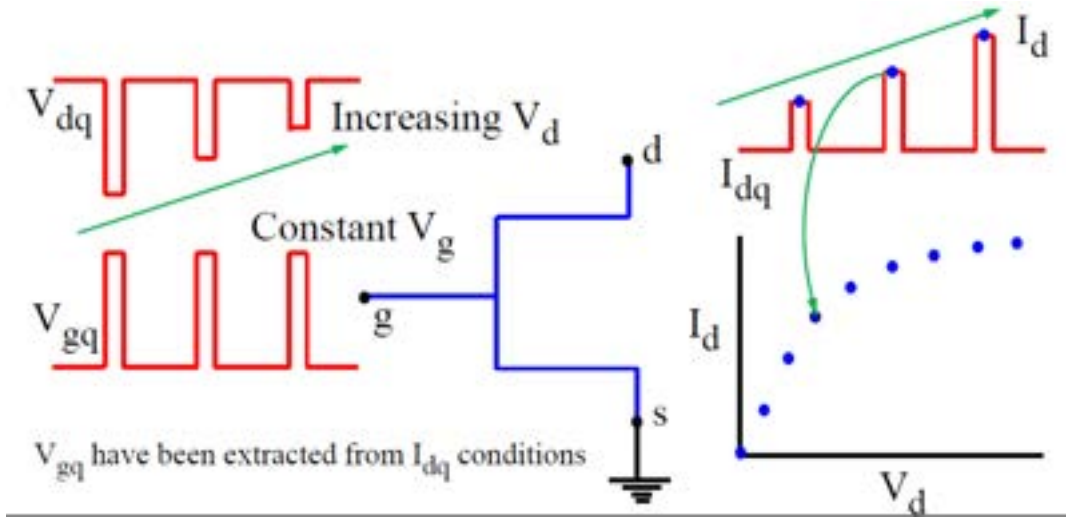


Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance for dynamic Ron
- Suitable for simulating Power Devices
- Incorporates temperature dependence.

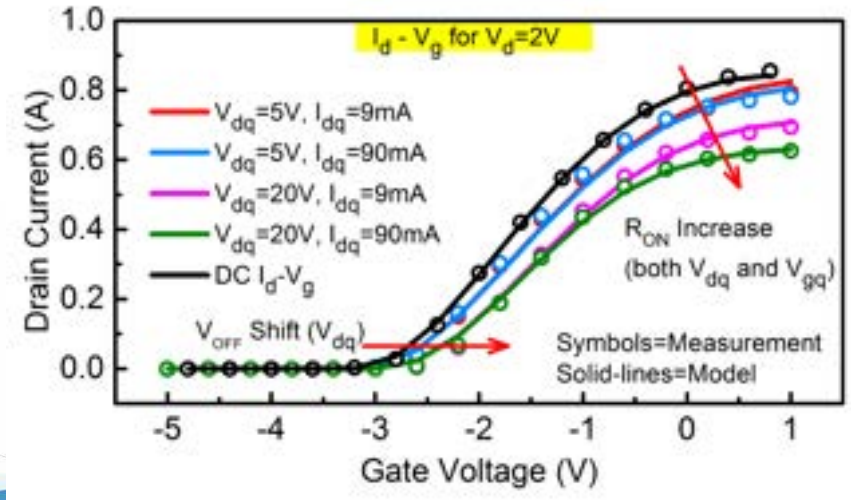
$$R_D(Trap) = R_D + \frac{V(trap1)}{VATRAP} \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{TALPHA}$$

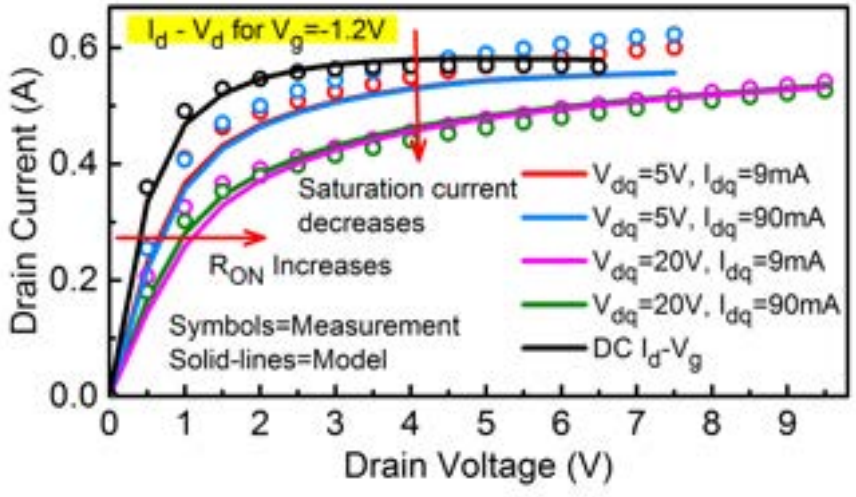
Extraction using pulsed measurements



Pulsed-IV Scheme used to simulate the P-IV Characteristics

- Pulsed IV characterization in dual-pulse mode at a pulse frequency of 1000 Hz with a duty-cycle of 0.02 % is performed under multiple quiescent drain and gate bias conditions such that both the gate and the drain voltages are pulsed simultaneously from the quiescent bias point.
- The pulse width of 200 ns and the measurement window of 40 ns within these 200 ns is short enough to ensure iso-thermal and iso-dynamic measurement of the pulsed-IV characteristics.



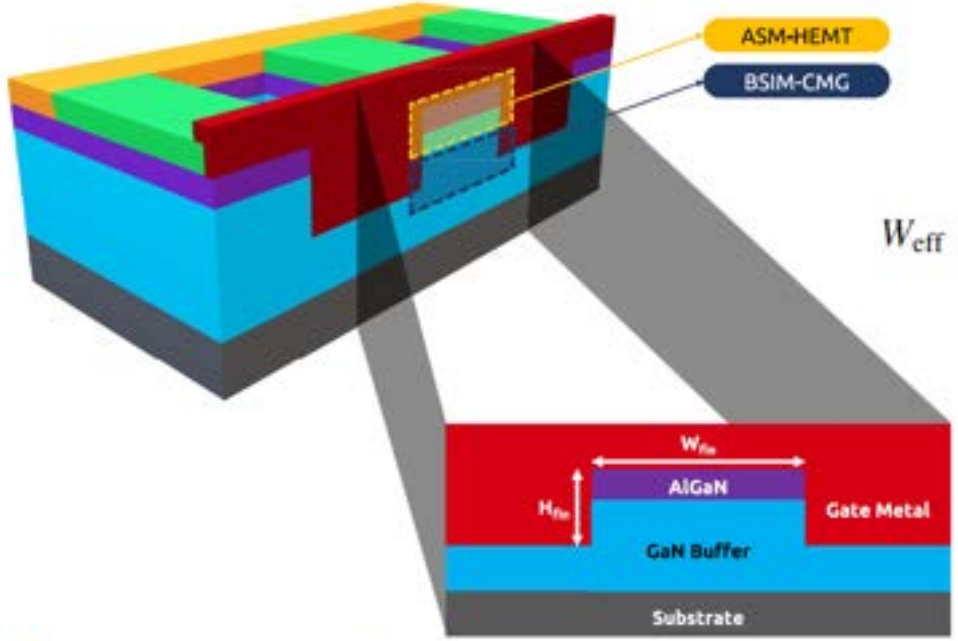


Pulsed – IV chacteristics for multiple quiescent conditions – using TRAPMOD II

Our Recent Works

Modeling the Impact of Dynamic Fin-width on the I–V, C–V and RF Characteristics of GaN Fin–HEMTs

- New model handles the effective width of the 2DEG channel by considering its depletion due to the presence of gates on the sidewalls of the fin.
- ASM-HEMT models 2DEG while BSIM-CMG models the bias-dependent width-modulation due to the sidewalls.



$$W_{\text{eff}} = W_{\text{fin}} - \overbrace{2\sqrt{\frac{2\epsilon_S(\phi_i - V_A)}{qN_D}}}^{\Delta W}$$

Fig. 4. Schematic of the GaN Fin–HEMT (cross section along gate). The gate covers the fin up-to a depth of H_{fin} in the GaN buffer. Also shown is the modeling approach of treating the structure as two transistors in parallel-the 2DEG portion (shown in yellow) using the ASM-HEMT model and the remaining part between the fin walls (shown in blue) using the BSIM-CMG model.

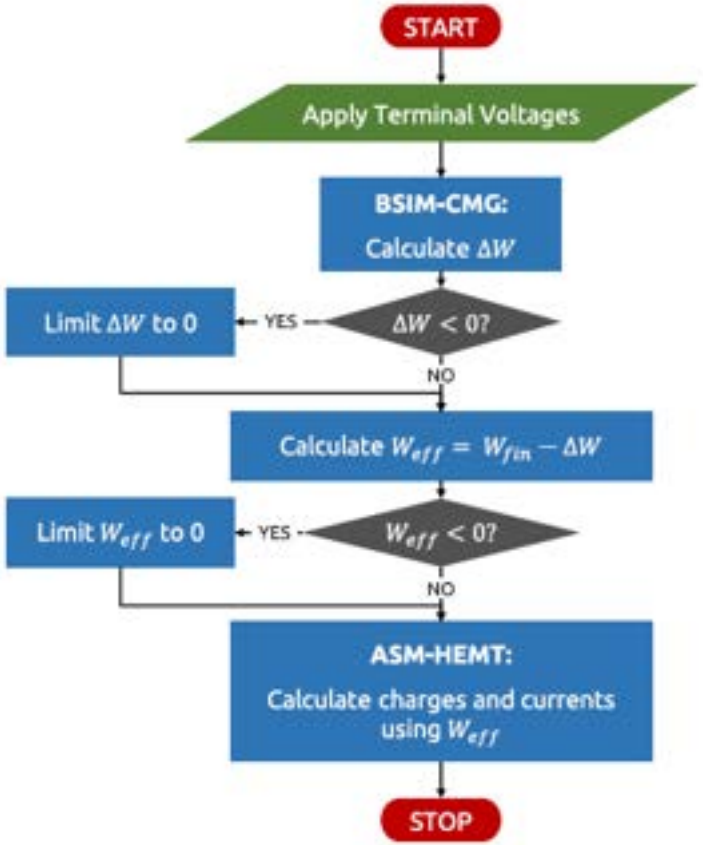


Fig. 5. Flowchart summarizing the modeling strategy adopted in this article. The purpose of the smoothing functions is to prevent any discontinuities in the model, ensuring model convergence and robustness.

A. U. H. Pampori, S. A. Ahsan, and Y. S. Chauhan, "Modeling the Impact of Dynamic Fin-width on the I–V, C–V and RF Characteristics of GaN Fin–HEMTs", IEEE Transactions on Electron Devices, Vol. 65, Issue 5, pp. 2275-2281, May 2022.

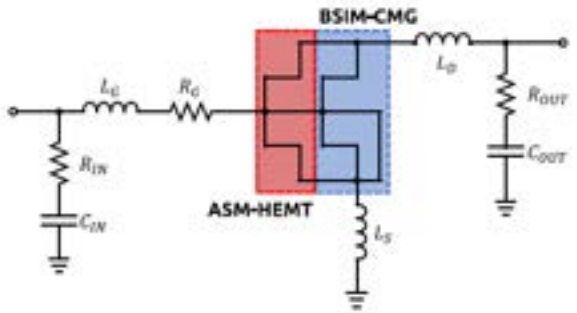


Fig. 13. Small-signal model used to simulate the S-parameters of the device. The bias-dependent and parasitic capacitances are modeled as part of the ASM-HEMT and BSIM-CMG models. The *RC* sections used at the gate and drain provide a rough approximation for the manifolds in the absence of any de-embedding data.

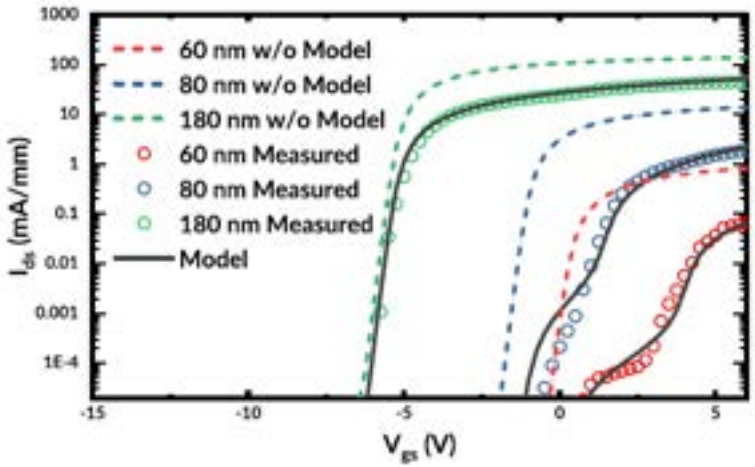


Fig. 6. Subthreshold characteristics with fin-width scaling. The measurements [4] are shown as symbols. The shift in threshold voltage and current levels is accurately captured using the modified $V_{th,eff}$ and μ_{eff} expressions. The dotted lines represent the output without the width-depletion model. The kinks in the subthreshold slope at lower fin-widths are modeled using the depletion effect. All curves are for a drain voltage of 0.1 V.

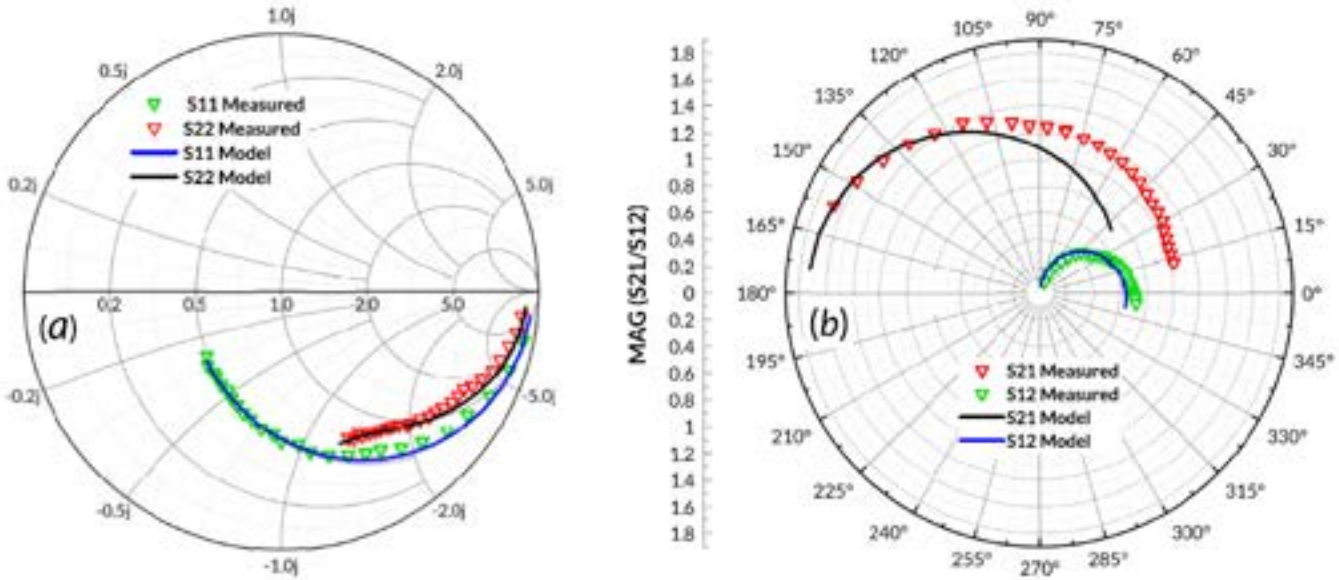


Fig. 12. S-parameter validation of the model in the frequency range of 1–40 GHz for the device defined in Section II-B. (a) Modeled reflection S-parameters S_{11} and S_{22} show a perfect overlap with the measured data. Additional sub-circuits were added to the small-signal model to compensate for the manifolds in the device. (b) Modeled transfer S-Parameters S_{12} and S_{21} have been scaled by a factor of 2.5 and 0.6, respectively, to fit them on a single chart. Both S_{12} and S_{21} show a decent fit at low frequencies. The mismatch at high frequencies can be attributed to the lack of any de-embedding data, the measurements [28] have been shown as symbols and the model is denoted by lines.

A Geometry-scalable model for self-heating in GaN HEMTs

$$R_{th,W} = R_{th0}(1/W + a * W)$$

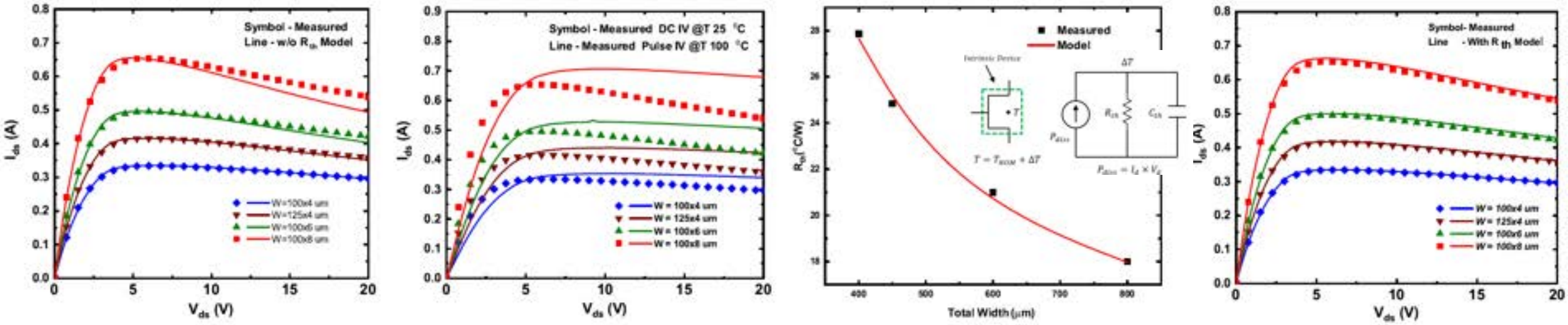


Fig. 1: (a) The output characteristics at $V_g = 0\,V$ for all four gate peripheries are not captured with existing self-heating model in ASM-HEMT. (b) DC and PIV output characteristics at $V_g = 0\,V$ for all four gate peripheries. Lines represent PIV measurements and symbols represent DC measurements. (c) R_{th} calculated using the coincidence method for all four gate peripheries and (d) DC output characteristics at $Vg = 0\,V$ for all four gate peripheries after implementing the self-heating model.

R. Dangi, A. Pampori, P. Kushwaha, E. Yadav, S. Sinha, and Y. S. Chauhan, "A geometry-scalable SPICE compact model for self-heating in GaN HEMTs", 80th Device Research Conference (DRC), Ohio, USA, June, 2022.

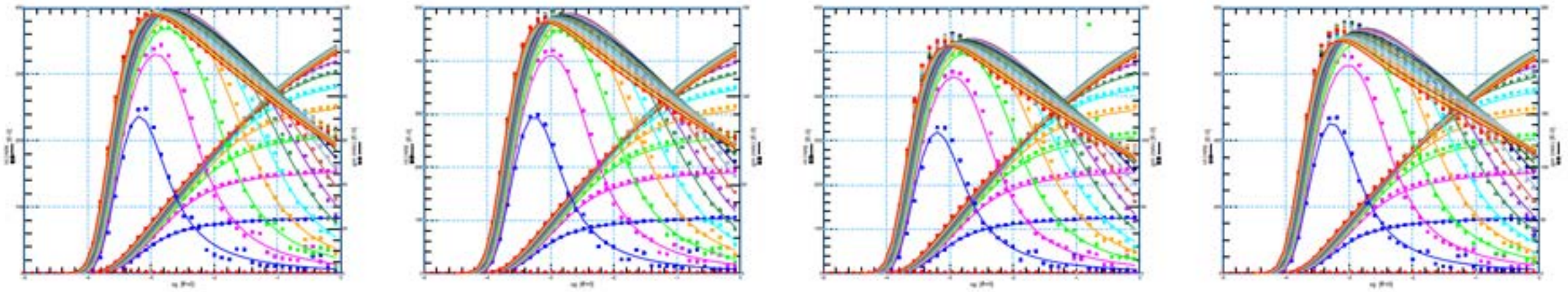


Fig. 2: The transfer characteristics are accurately captured by the revised model for device peripheries (WxNF): (a) $4 \times 100\ \mu m$ (b) $4 \times 125\ \mu m$ (c) $6 \times 100\ \mu m$ and (d) $8 \times 100\ \mu m$.

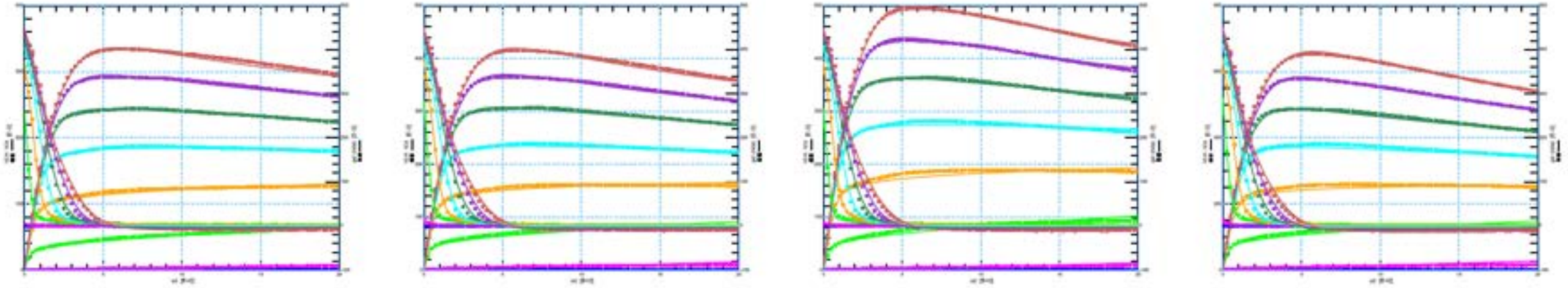


Fig. 3: The output characteristics are accurately captured by the revised model for device peripheries (WxNF): (a) $4 \times 100\ \mu m$ (b) $4 \times 125\ \mu m$ (c) $6 \times 100\ \mu m$ and (d) $8 \times 100\ \mu m$.

S-parameter validation for different gate peripheries

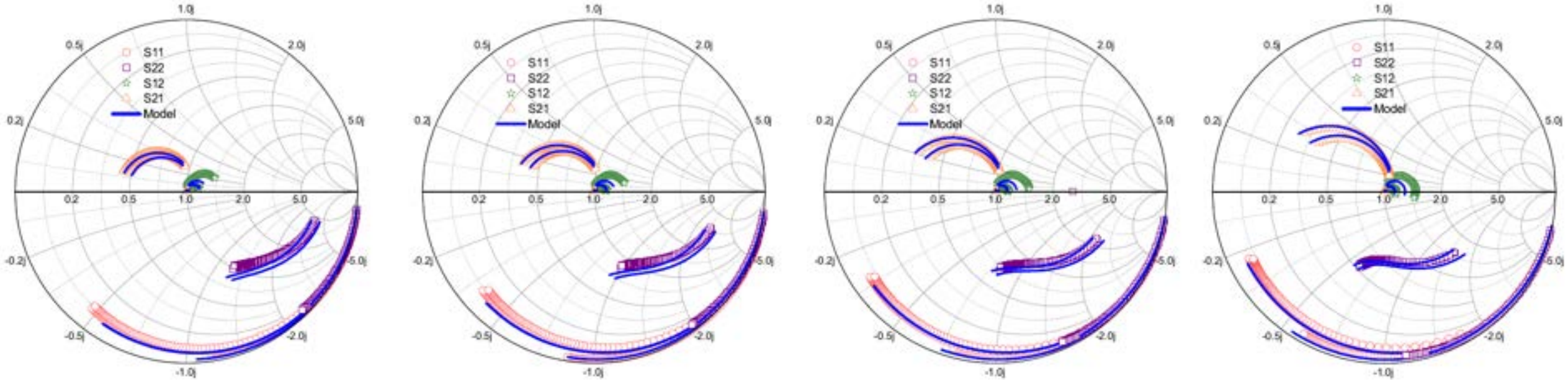


Fig. 4: The model is able to capture the RF characteristics from 1 GHz to 8 GHz with high fidelity at $V_d = 20\ V$ for different gate peripheries (WxNF): (a) $4 \times 100\ \mu m$ (b) $4 \times 125\ \mu m$ (c) $6 \times 100\ \mu m$ and (d) $8 \times 100\ \mu m$.

A Width-Scalable SPICE Model of GaN-HEMTs for X-band Applications

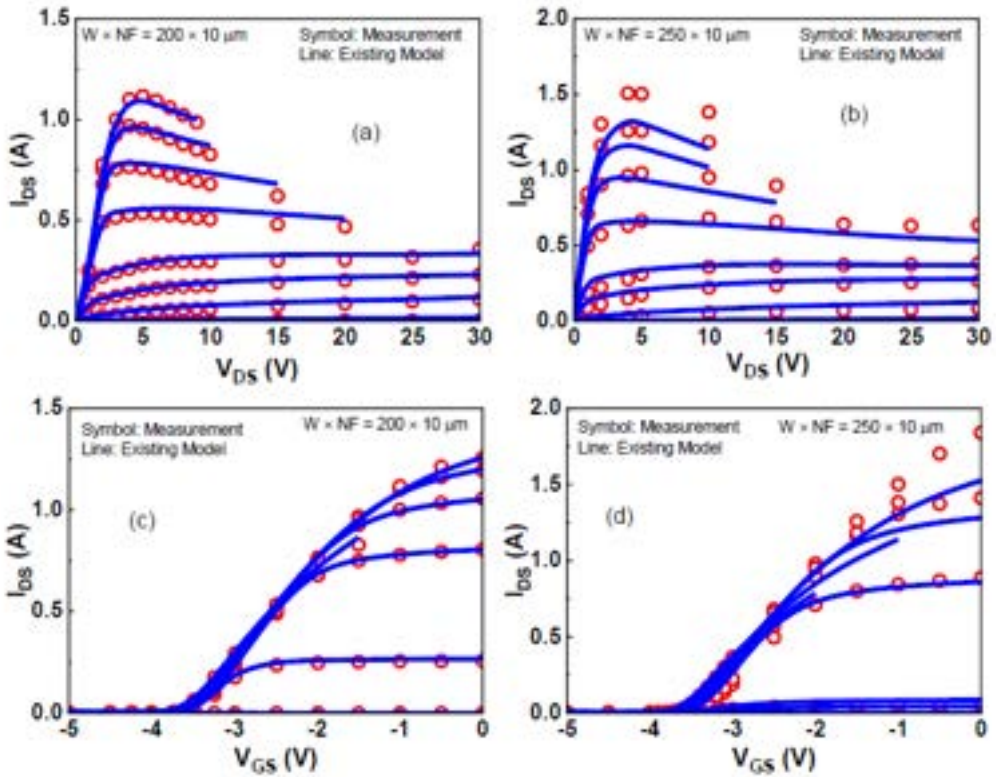
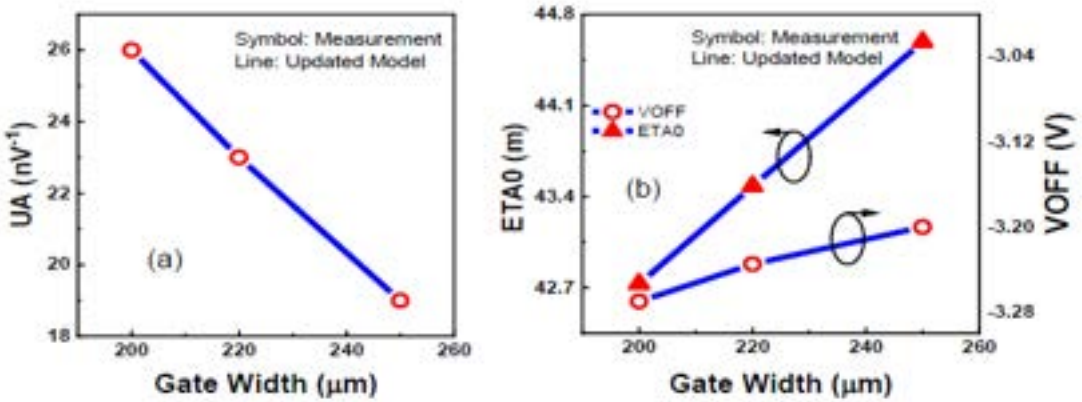


Fig. 2: (a)-(b) Current - Voltage ($I_{DS} - V_{DS}$) characteristics at V_{GS} = -7V to -1V, step = 0.5V for different gate widths (c)-(d) Current - Voltage ($I_{DS} - V_{GS}$) characteristics at V_{DS} = 0 V to 30 V for different gate widths. With increasing device width, the measured data (symbols) cannot be captured by the existing ASM-HEMT model (lines). A larger deviation can be noticed between measured and modeled characteristics where the relative width difference is high between the devices (i.e., 200×10 μm and 250×10 μm).

$$UA_{eff} = UA - UA_W \times W \quad (1)$$

$$VOFF_{eff} = VOFF + VOFF_W \times W \quad (2)$$

$$ETA0_{eff} = ETA0 - ETA0_W \times W \quad (3)$$



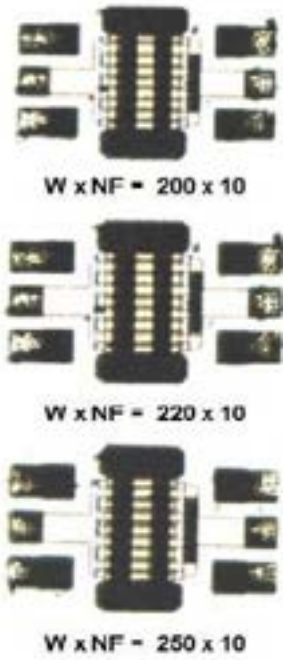


Fig. 3: Model parameters (*UA*, *ETA0*, and *VOFF*) calculated for different gate widths.

M. H. Ansari, R. Dangi, A. Pampori, P. Kushwaha, E. Yadav, S. Sinha, and Y. S. Chauhan, "A Width-Scalable SPICE Model of GaN-HEMTs for X-band RF Applications", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Seoul, Korea, Mar. 2023.

Width scalability for large gate peripheries

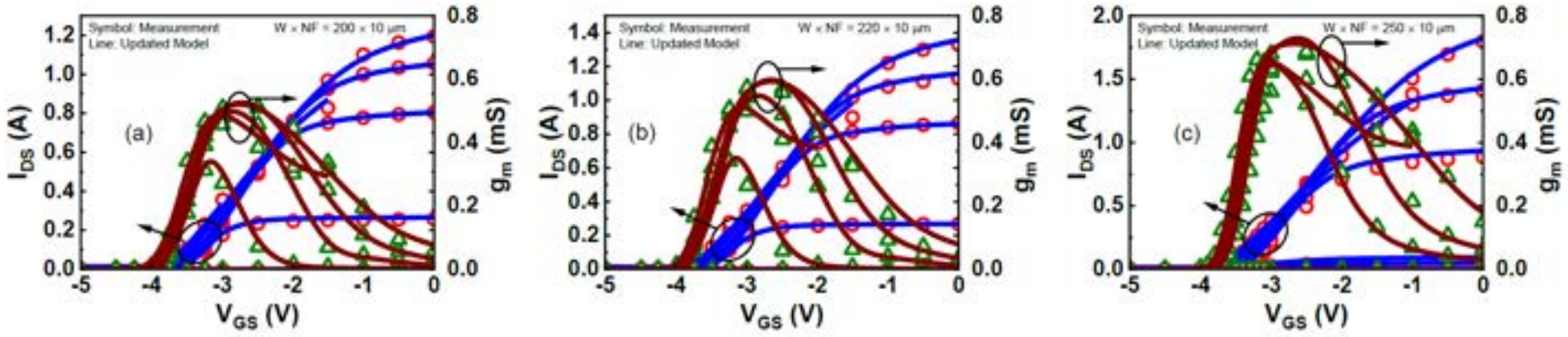


Fig. 4: Current - Voltage (I_{DS} – V_{GS}) and transconductance characteristics at V_{DS} = 0 V to 30 V for different gate widths. The measured data (symbols) is well captured using the updated ASM-HEMT model (lines).

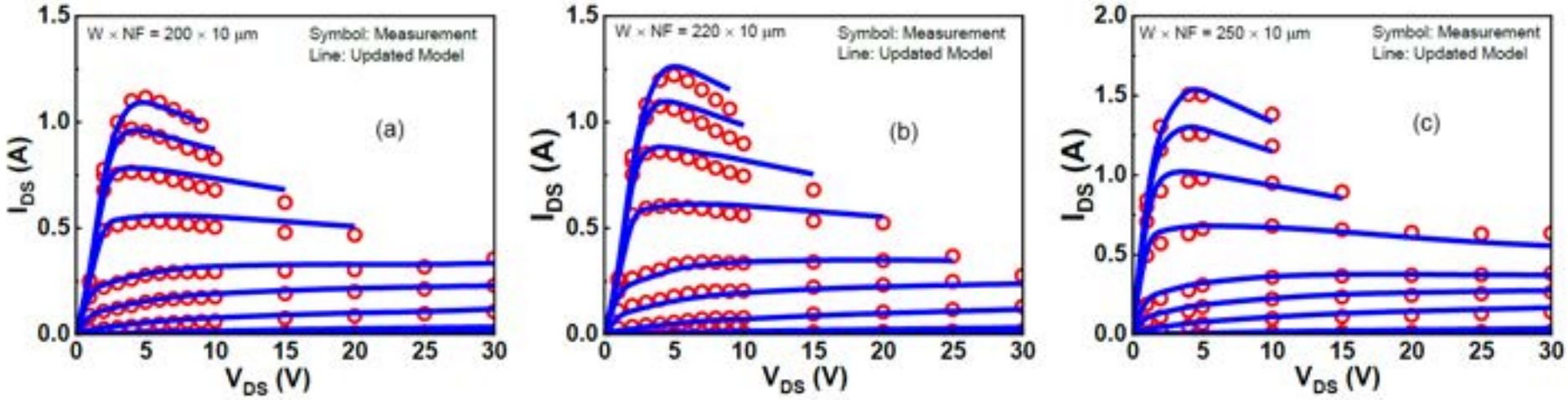


Fig. 5: Current - Voltage (I_{DS}– V_{DS}) characteristics at V_{GS} =–7 V to -1 V, step = 0.5 V for different gate widths. The measured data (symbols) is well captured using the updated ASM-HEMT model (lines).

Small and large signal RF validation for different gate peripheries

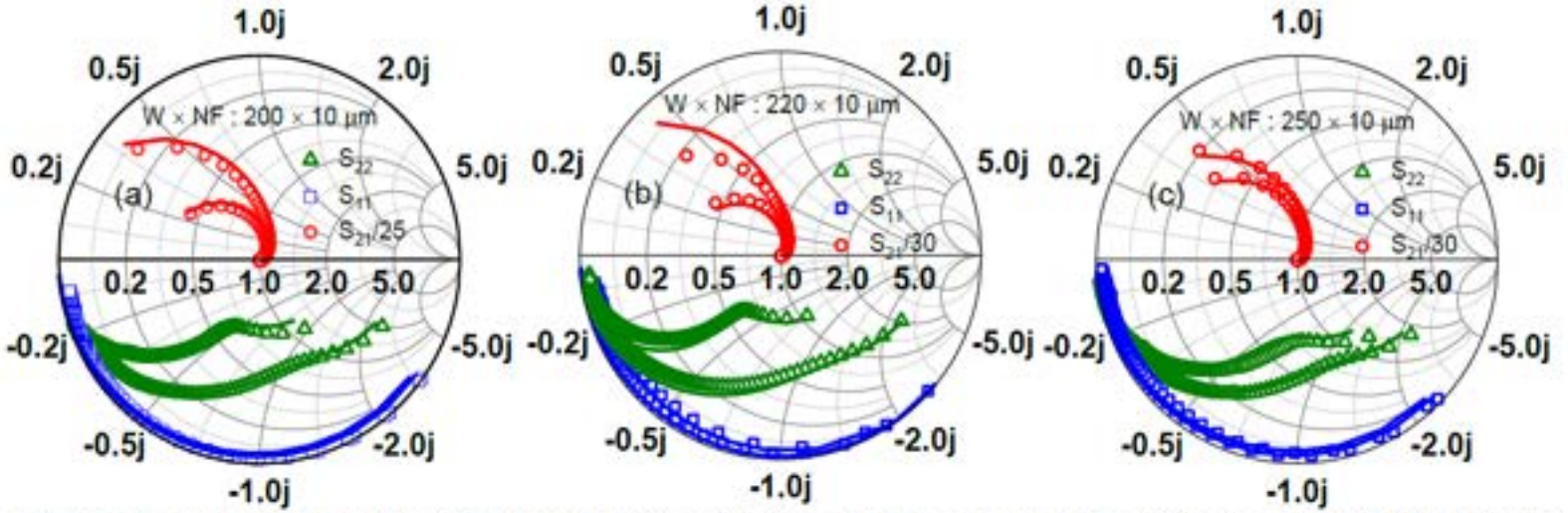


Fig. 6: Measured (symbols) and simulated (lines) S-parameters at V_{DS} = 30 V, V_{GS} = -3.25 V, -3.75 V and freq = 0.5 GHz to 43.5 GHz for (a) $W \times NF = 200 \times 10$ μm (b) $W \times NF = 220 \times 10$ μm (c) $W \times NF = 250 \times 10$ μm. S_{21} has been scaled with a suitable number to improve visibility.

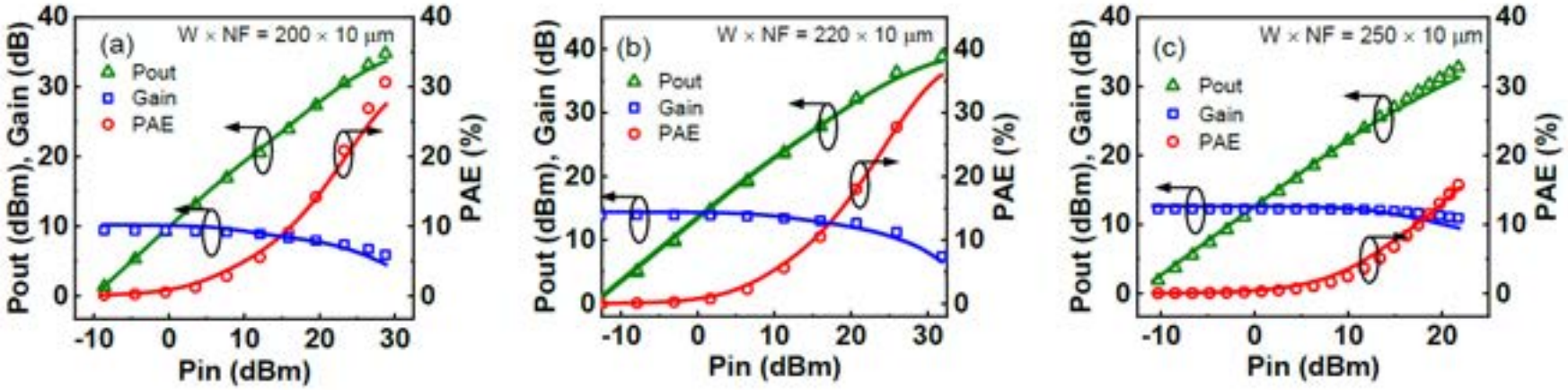


Fig. 7: Measured (symbols) and simulated (lines) values of Gain, Pout, and PAE for different device widths obtained for large-signal simulations at (a) 9 GHz, V_{GS} = -3.5 V and V_{DS} = 20 V (b) 9 GHz, V_{GS} = -3.5 V and V_{DS} = 30 V (c) 9.6 GHz, V_{GS} = -3.3 V and V_{DS} = 30 V.

Modeling of Bias-Dependent Effective Velocity and Its Impact on Saturation Transconductance in AlGaN/GaN HEMTs

- There is progressive decrease in the saturation velocity in GaN HEMTs with increasing Vgs.
- This is predominantly due to the scattering of electrons, forming the high-density 2DEG, by optical phonons at high overdrive voltages.
- This dependence differs from the traditional mobility degradation models.

$$v_{\mathrm{eff}} = v_{\mathrm{eff0}} \times \left(N_q \frac{V_{\mathrm{go}} + V_{\mathrm{th}}[1 - \ln(\beta V_{\mathrm{gon}})] - \frac{\gamma_0}{3}(N_q)^{2/3}}{V_{\mathrm{go}}\left(1 + \frac{V_{\mathrm{th}}}{V_{\mathrm{god}}}\right) + \frac{2\gamma_0}{3}(N_q)^{2/3}} \right)^{-\beta_{\mathrm{veff}}}$$

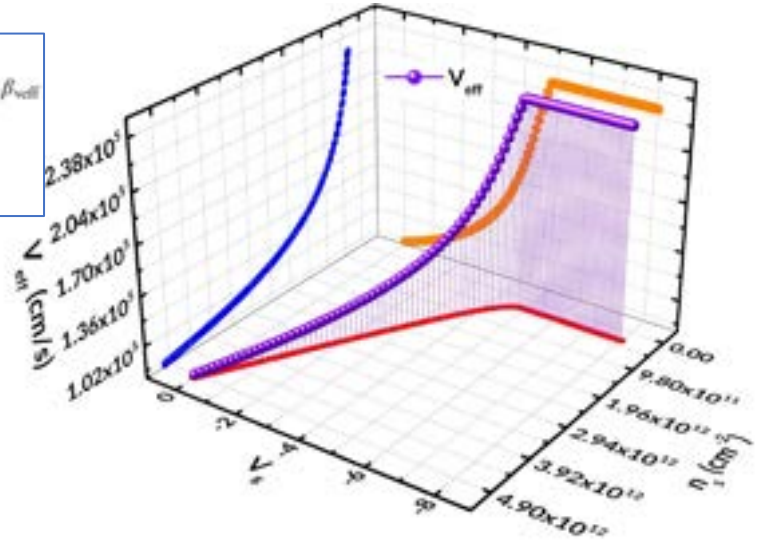
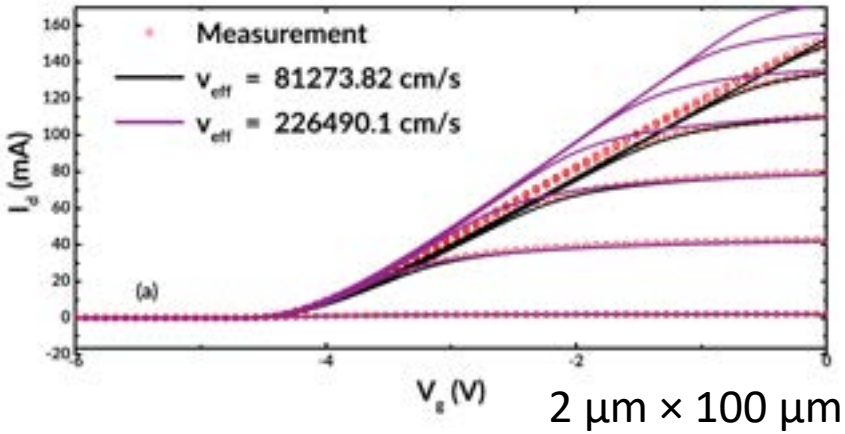
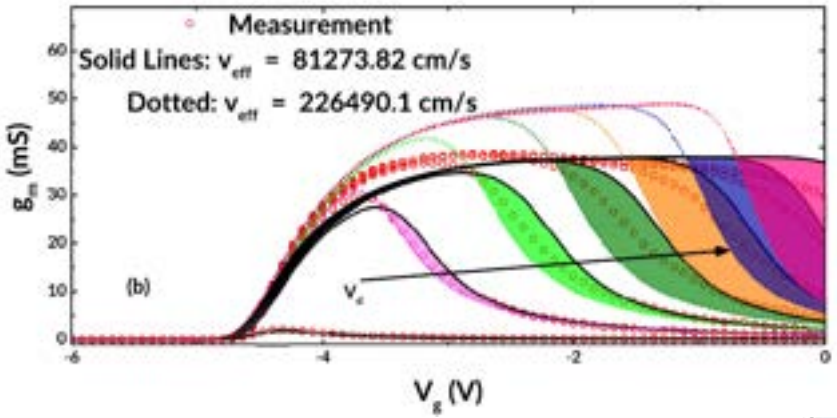


Fig. 3. v_{eff} and n_s as extracted from the model for the 2 μm × 100 μm device after fitting, plotted against V_g. The dependence of v_{eff} on n_s (blue projection) follows a similar trend as in [30].



2 μm × 100 μm device



The difference in the modeled slope (colored areas) increases with increasing drain bias. This is overcome by considering a bias-dependent v_{eff}.

A. U. H. Pampori, S. A. Ahsan, R. Dangi, U. Goyal, S. K. Tomar, M. Mishra and Y. S. Chauhan, "Modeling of Bias Dependent Effective Velocity and its Impact on Saturation Transconductance in AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 68, Issue 7, pp. 3302 - 3307, July 2021.

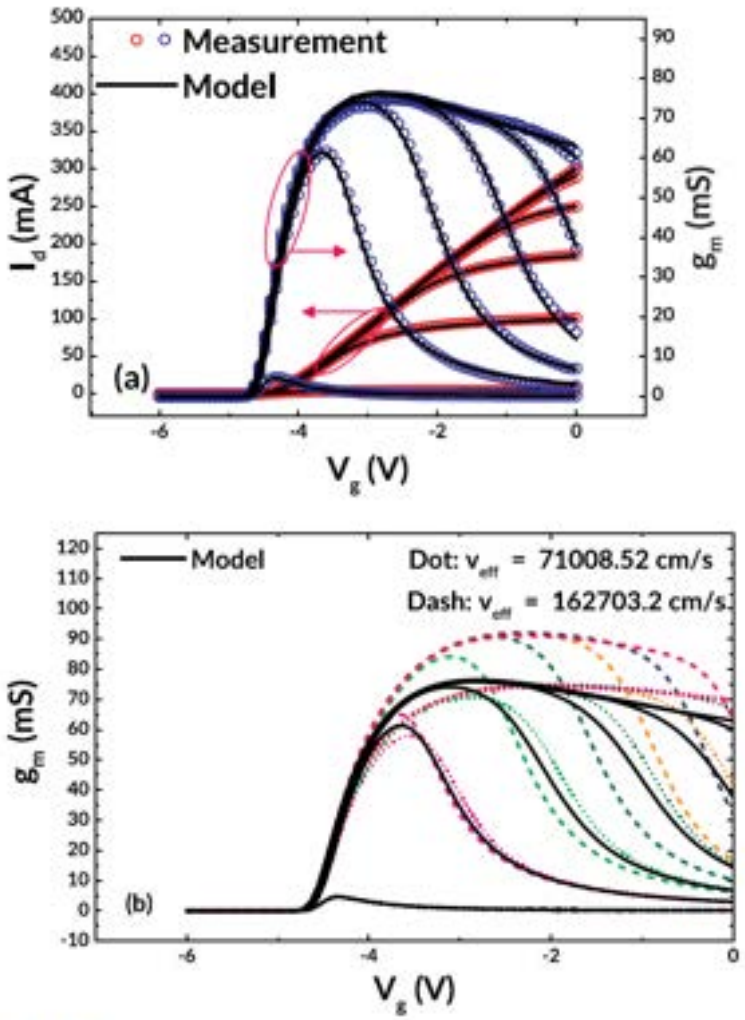


Fig. 5. (a) Transfer *I–V* characteristics of a 200 μm × 2 μm device. The drain voltage was swept from 50 mV to 6 V with a step of 1 V. (b) Model is able to closely follow the changes in the slopes of the g_m characteristics. The dotted and dashed lines represent the minimum and maximum v_{eff}, extracted from the model, used independently.

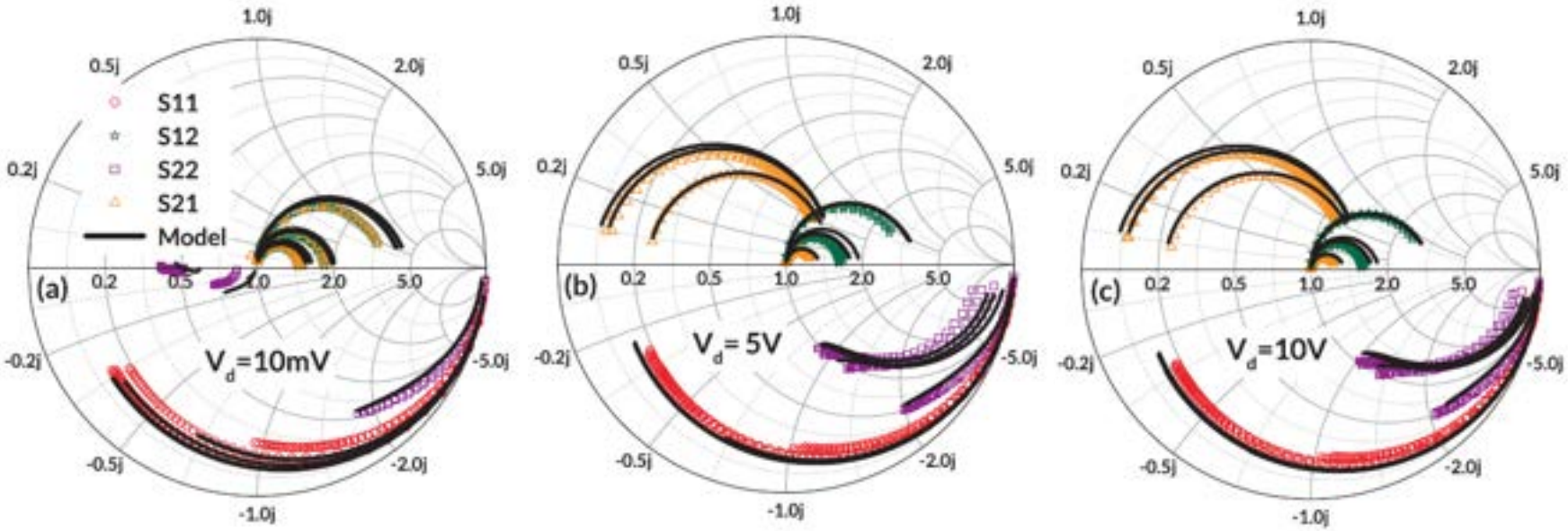


Fig. S-parameters (500 M0Hz–10 GHz) for three different drain-bias conditions [(a) *Vd* =10mV, (b) *Vd* = 5V, and (c) *Vd* = 10V] and multiple gate bias conditions [−6 (OFF-state) to −2 (Class A bias) with a step of 1 V]. Symbols – measurement, model – lines. S21 for 5 and 10 V has been scaled by a factor of 4.5.

Device size: 2 μm × 100 μm.

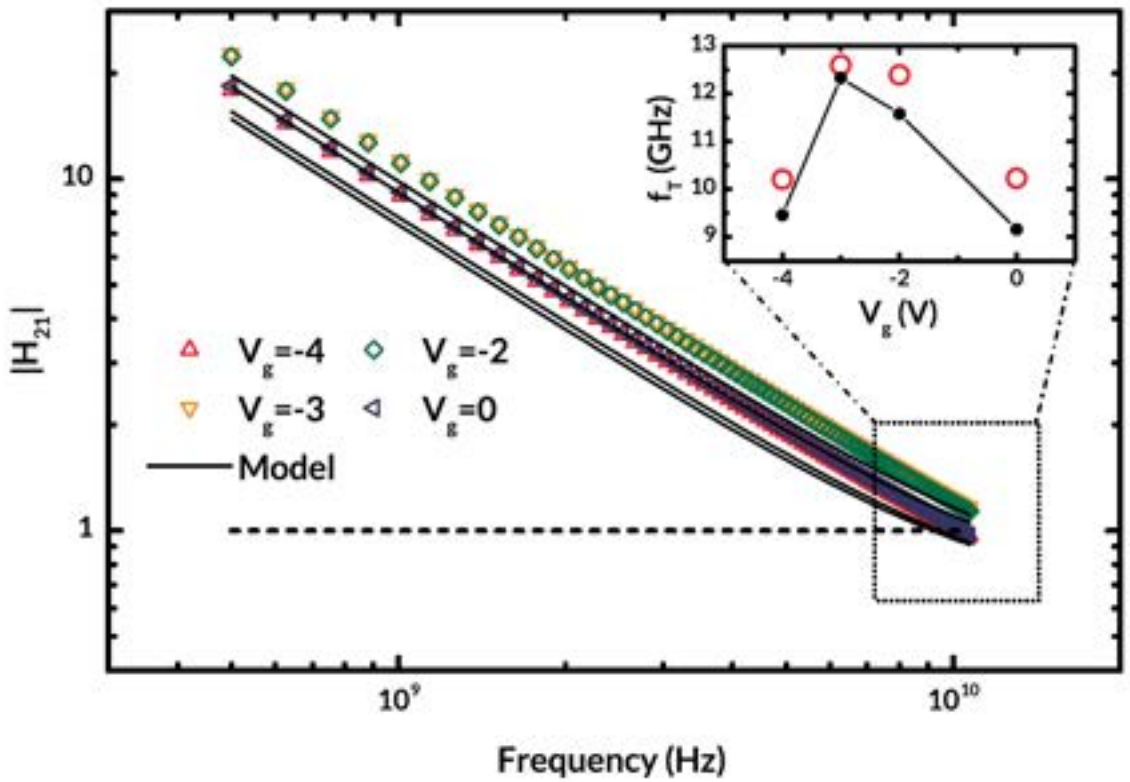


Fig. 7. $|H_{21}|$ plotted against frequency to evaluate f_T for the 2 μm × 100 μm device. The dotted line represents the unity gain. The inset represents the change in f_T with increasing gate bias. Measured data are represented using symbols, while the model is represented using lines.

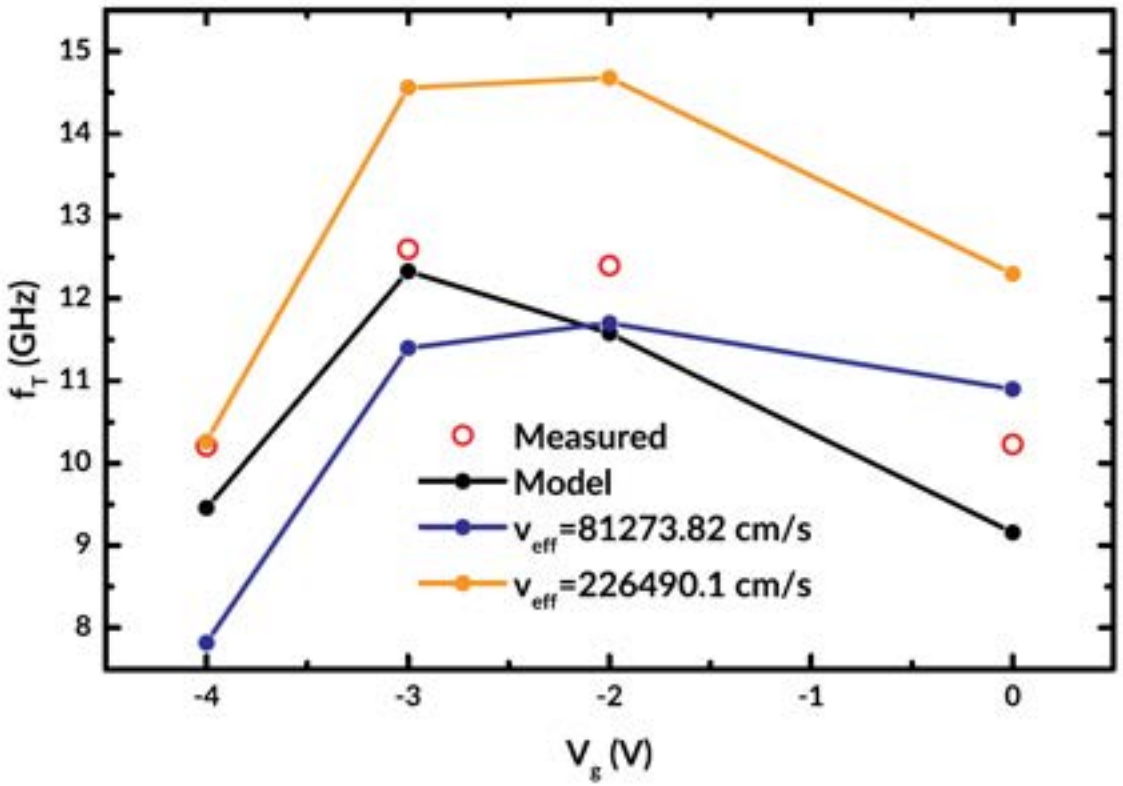


Fig. 8. Model is closely able to follow the trends in f_T at low gate voltages (where v_{eff} is higher), as well as at high gate voltages (where v_{eff} is lower). Data are shown for the 2 μm × 100 μm device.

Modeling Cryogenic effects in GaN HEMTs

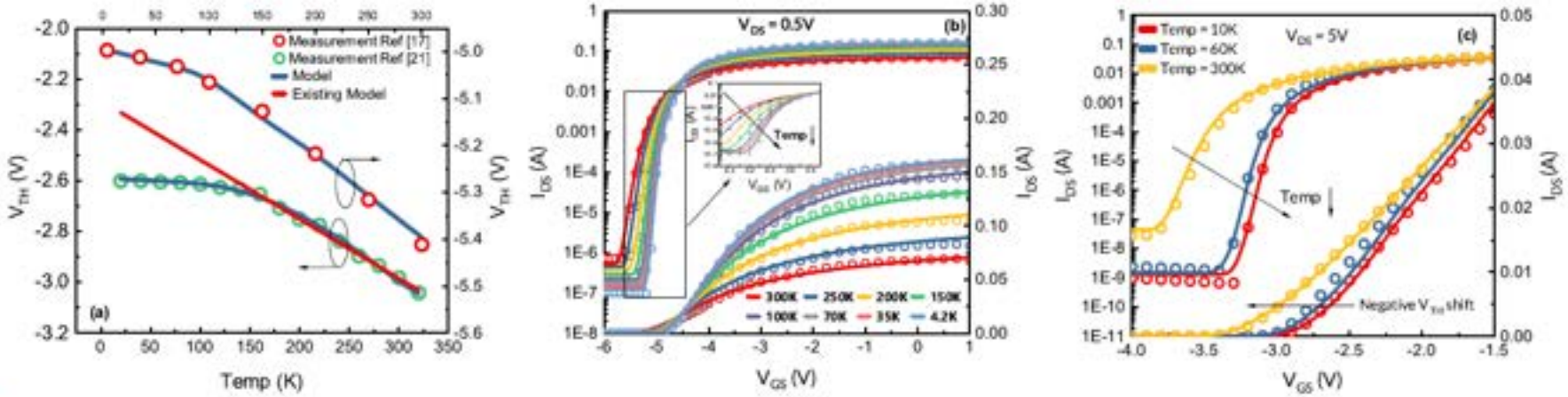


Fig. 3: Measurement (Symbols) and Simulated (Solid lines): (a) Threshold voltage dependence on temperature down to cryogenic temperatures (b) Measurement [17]: I_{DS} - V_{GS} characteristics at V_{DS}=0.5V. (c) I_{DS} - V_{GS} characteristics at V_{DS} = 5V for DUT. Log scale show decrease and saturation of SS at low temperatures and negative V_{TH} shift

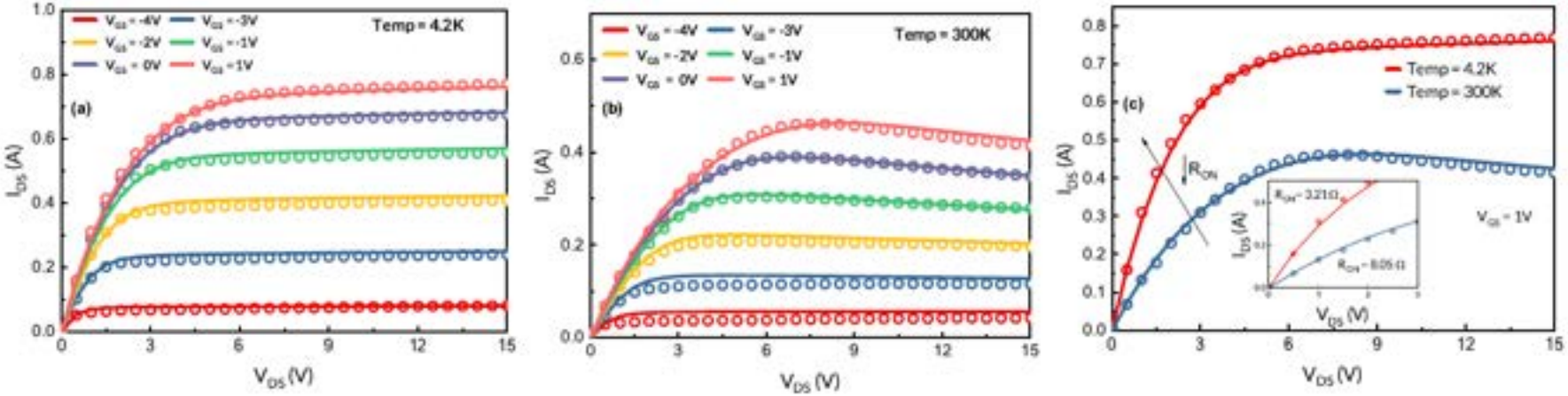


Fig. 4: Measurement (Symbols) [17] and Simulated (Solid lines) for V_{GS} values shown in legends: (a) I_{DS} - V_{DS} characteristics at 4.2K (b) I_{DS} - V_{DS} characteristics at 300K (c) I_{DS} - V_{DS} characteristics at temperature values shown in legends at V_{GS} of 1V. The plot shows maximum current level difference and change in R_{ON}.

M. S. Nazir, P. Kushwaha, A. Pampori, S. A. Ahsan, and Y. S. Chauhan, "Electrical Characterization and Modeling of GaN HEMTs at Cryogenic Temperatures", IEEE Transactions on Electron Devices, Vol. 69, Issue 11, November 2022.

Kink effect at cryogenic temperatures

$$V_{k,s} = \frac{1}{2}\left(1 + \tanh\left(\frac{V_{DS} - V_{DS,KINK}}{V_{dk}}\right)\right)$$

where,

$$V_{DS,KINK} = \frac{-a_K exp\left(-\left(\frac{V_{GS}-b_K}{c_K}\right)^2\right) + d_K}{1 + e_K abs(V_{GS})}$$

$$K_m = \frac{1}{V_{gk}} \exp\left(-\frac{V_{GS} - v_0}{V_\sigma}\right)^2$$

$$V_{k,t} = \frac{1}{1 + \alpha_{11} exp\left(t1 \cdot \frac{T_{EFF}}{T_{NOM}}\right)}$$

$$V_{KINK} = k_m \cdot V_{k,s} \cdot V_{k,t}$$

Final expression for v_{TH} with inclusion of kink is

$$V_{TH,K} = V_{TH} - \alpha_k V_{KINK}$$

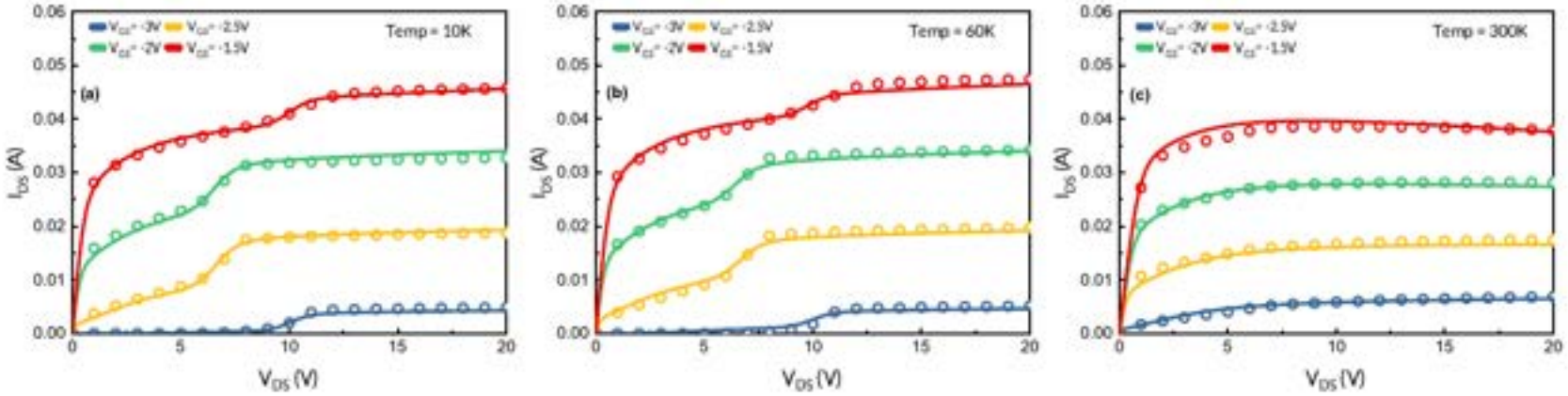


Fig: Measurement (Symbols) and Simulated (Solid lines) for V_{GS} values shown in legends: (a) I_{DS} - V_{DS} characteristics at 10K with observable kink (b) I_{DS} - V_{DS} characteristics at 60K with observable kink (c) I_{DS} - V_{DS} characteristics at 300K with no significant kink.

Kink effect at 3 different biases and temperatures

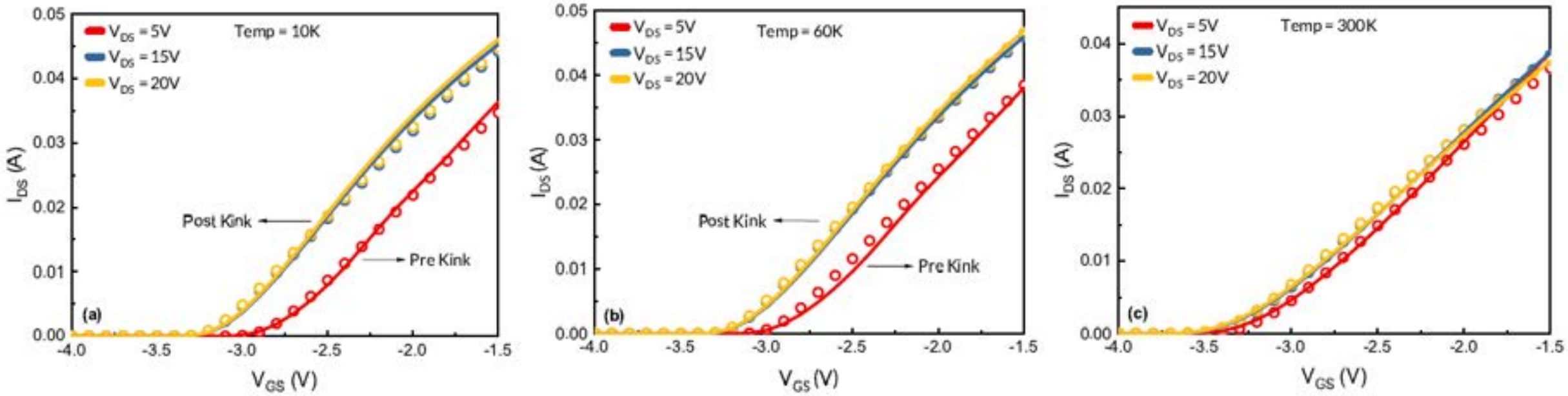
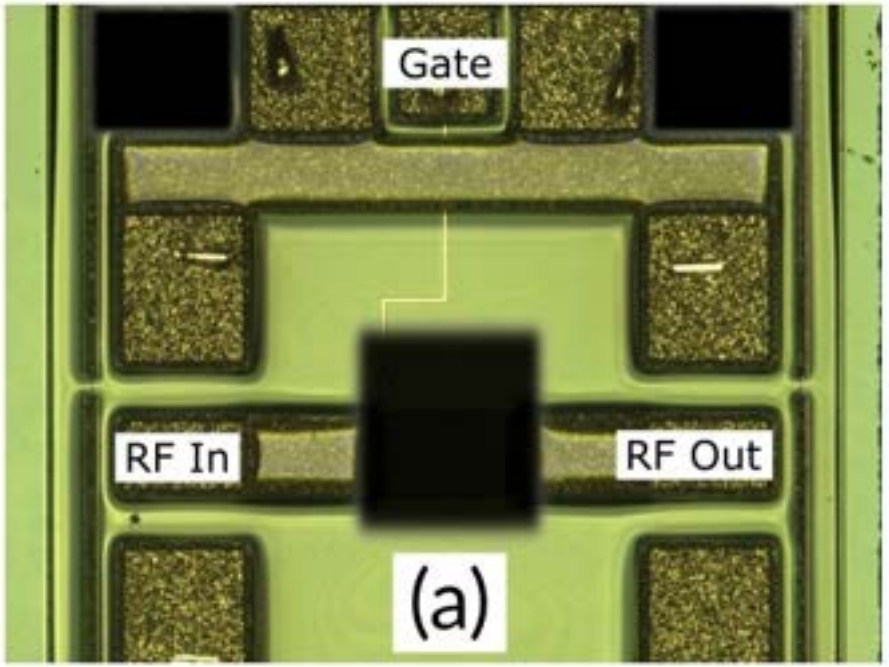


Fig: Measurement (Symbols) and Simulated (Solid lines) for VDS values shown in legends: VDS = 5V denotes the pre-kink region and VDS = (15V and 20V) denote the post-kink region (a) IDS - VGS characteristics at 10K. (b) IDS - VGS characteristics at 60K. (c) IDS - VGS characteristics at 300K with no significant kink observed.

RF Switch Modeling



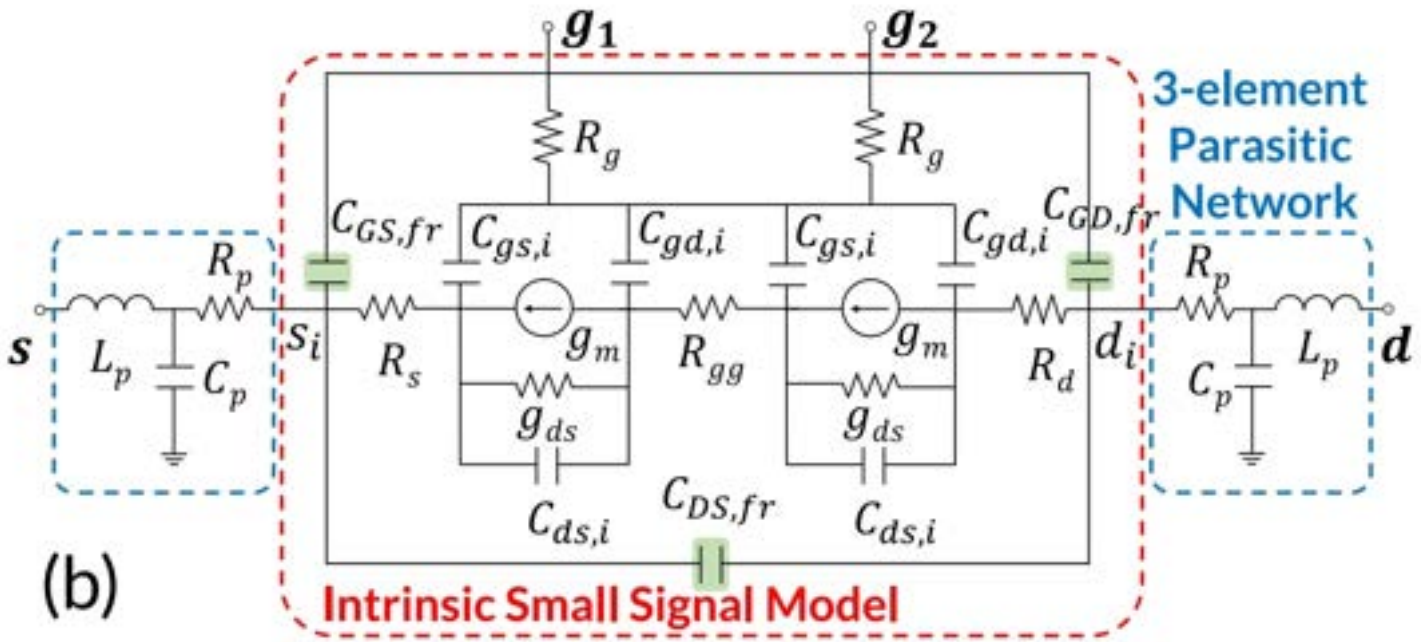


Figure. (a) Die micrograph of the 0.5 um node, 10 x 100 um dual- gate depletion-mode GaN-on-Si switch. (b) The equivalent small-signal model of the dual-gate GaN switch device. The intrinsic model is shown in red and the parasitic components are shown in blue. Elements with 'i' subscripts denote intrinsic capacitances, ‘fr’ subscripts denote fringing capacitances and p subscripts denote parasitic elements.

IV and RF modeling for dual-gate GaN Switch

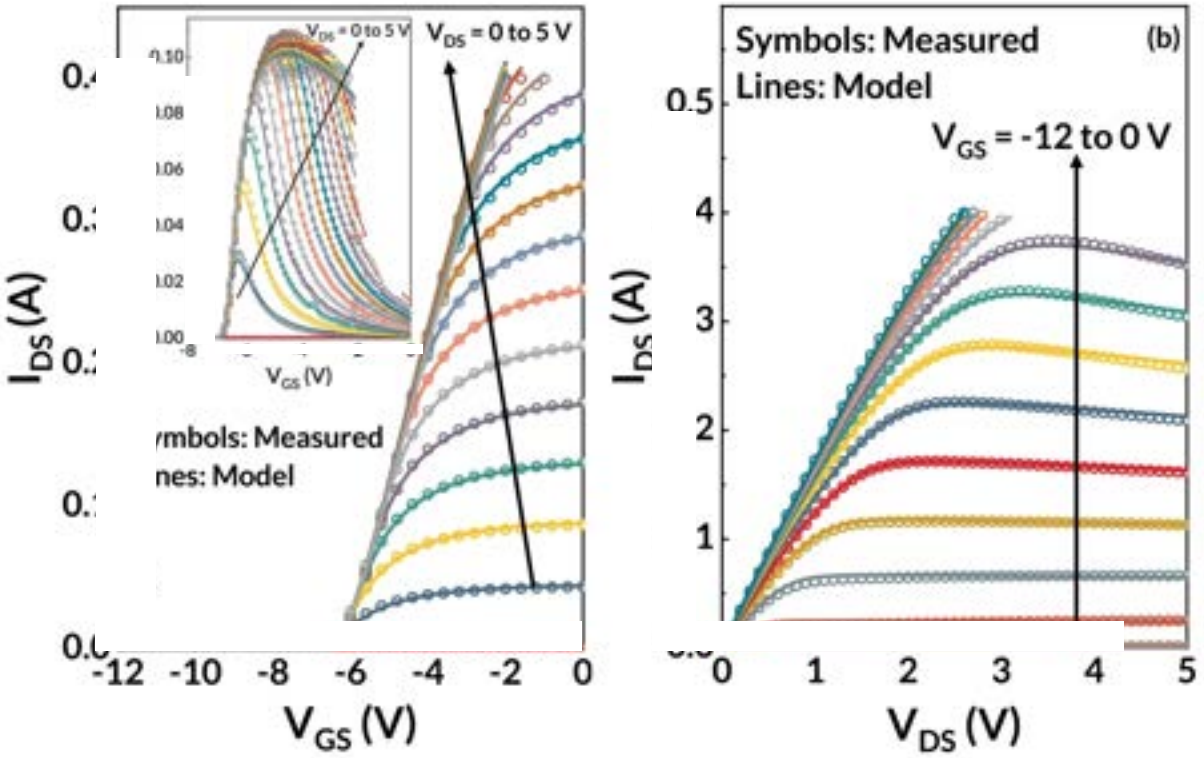


Figure 2. Model extraction results for the 0.5 μm node, 10 × 100 μm dual-gate depletion-mode GaN-on-Si switch, showing the (a) Transfer Characteristics and (b) Output Characteristics. Device characterization was limited to a DC current of $400mA$.

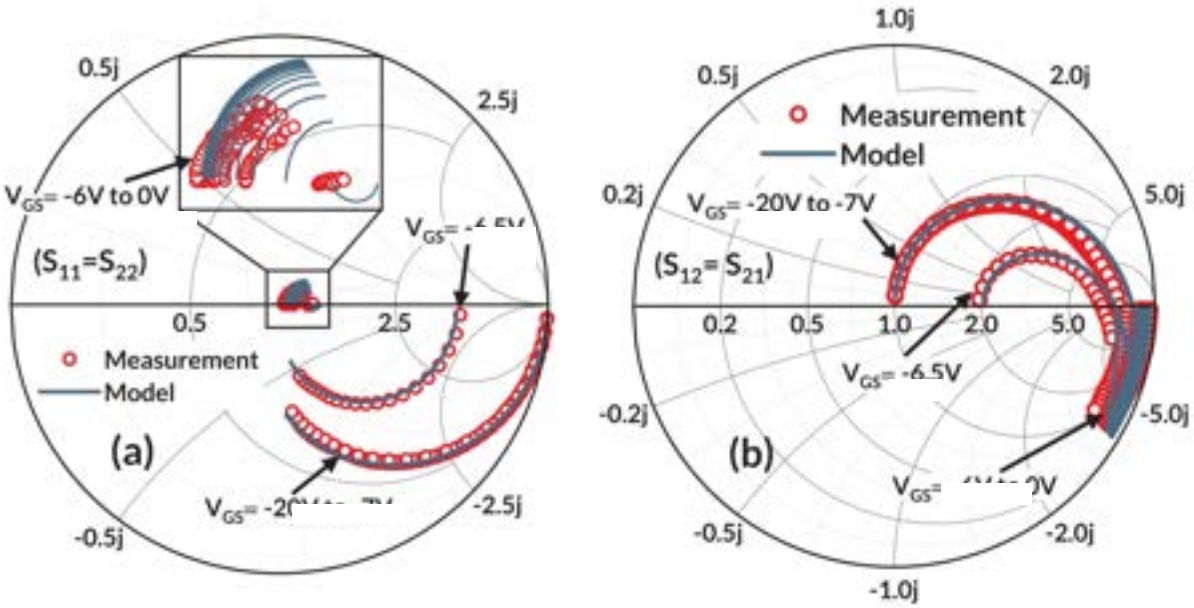
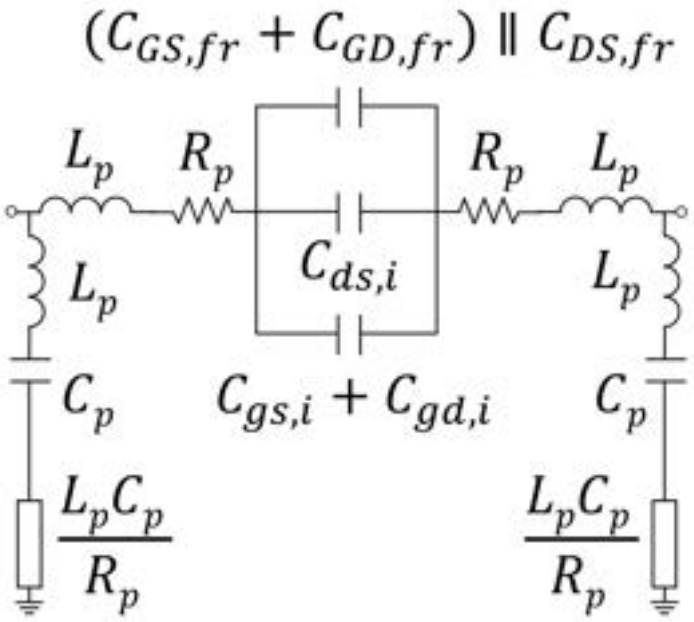


Figure 3. (a) Reflection and (b) Transmission S-Parameters of the 0.5 μm node, 10 × 100 μm dual-gate switch in the common-gate mode from 500 MHz to 20 GHz with the parasitic network embedded. Gate bias was swept from $-20V$ to $0V$ with a step of $0.5V$ at $V_{ds} = 0V$.

Small signal model including parasitic components



$$C_{gd,fr} = W \cdot NF \cdot (CGDO - CGDL \cdot \sqrt{1e^{-6} + Vdse^2} - CGDL2H \cdot Vdse^{2N} - CGDL3H \cdot Vdse^{3N}) \quad (3)$$

Figure 4. The equivalent π-network of the parasitic components shown in Fig. 1(b). The real part of the series components is used to extract R_p while the imaginary part gives L_p at high frequencies. C_p is extracted from the shunt branch at low frequencies.

Modeling harmonics and insertion loss for a switch

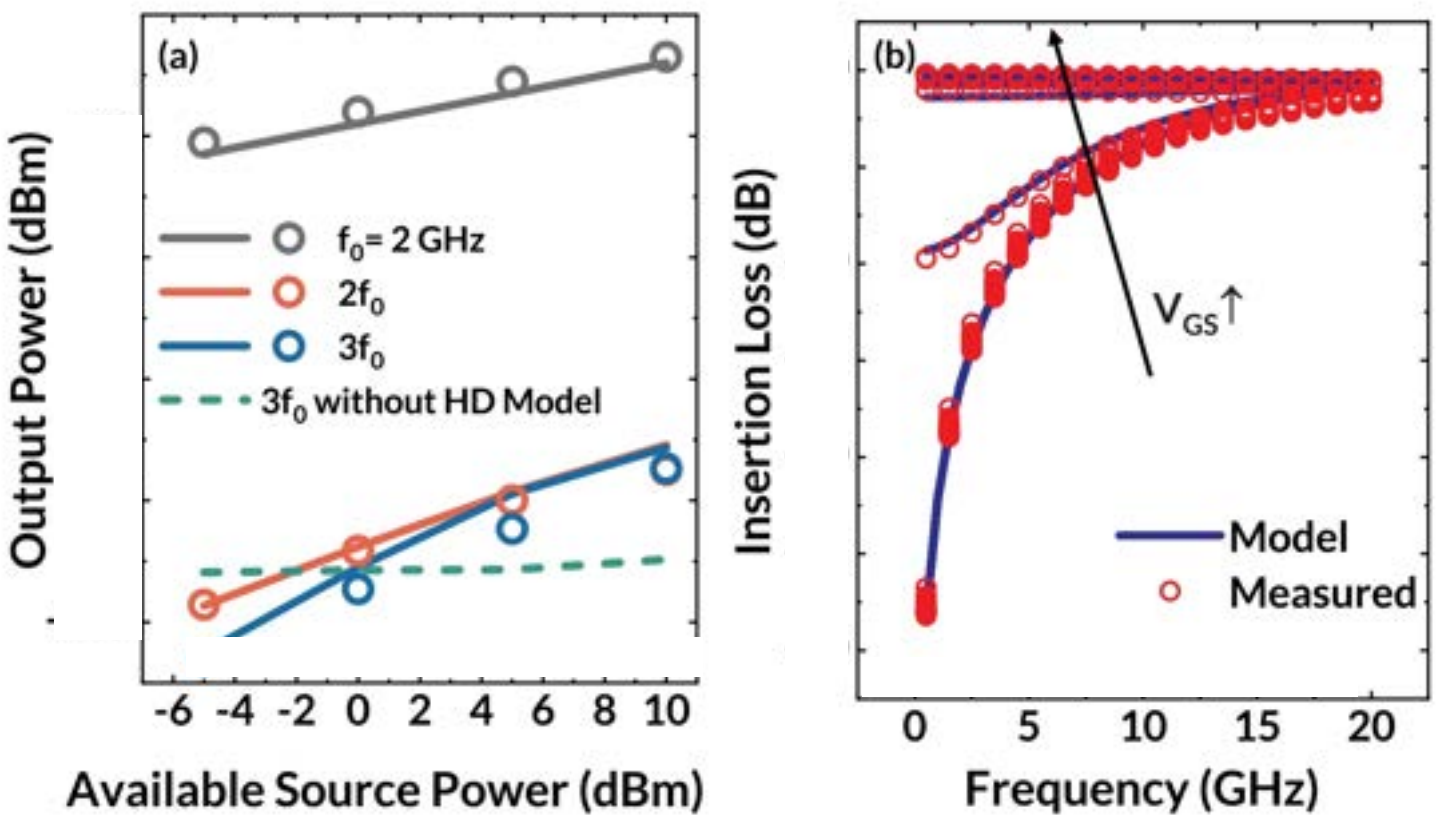
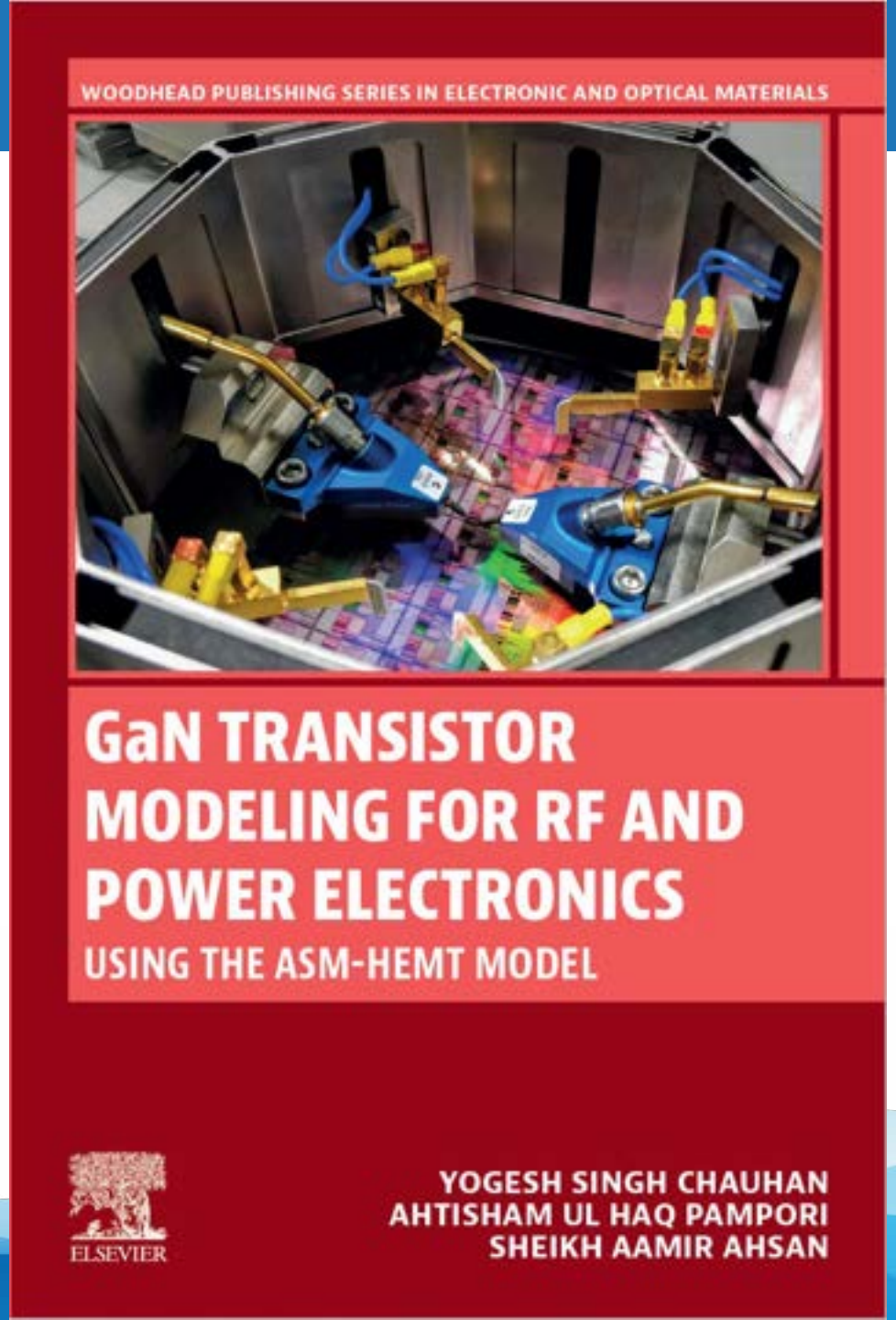


Figure 5. (a) The impact of the developed model on the OFF-state ($V_{gs} = -9V$) harmonics is clearly observed. The dotted line represents the standard ASM-HEMT model while the solid lines represent the new Harmonic Distortion (HD) sub-model. (b) Insertion Loss for the measured device vs. the extracted model. V_{gs} is swept from $-20V$ to $0V$ in steps of $0.5V$.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Related Publications

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23	K. Sharma, S. Ghosh, A. Dasgupta, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Capacitance Analysis of Field Plated GaN HEMT", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
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Thank You!

Questions