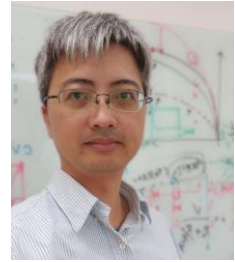


Intelligent Memory in Future High-Performance Computing

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Abstract:

Memory technology is not only the pillar of the present semiconductor industry, but it also plays a critical role in various innovation forefronts of future, such as big data storage/processing, AI acceleration, neuromorphic computing, hardware security, combinatorial optimizer, etc. Memory-centric architectures and computing systems promise to provide unprecedented parallelism, energy efficiency, and density beyond the conventional von Neumann architectures. In this intelligent memory era, breakthroughs in the memory device, circuit, and architecture are required. We will talk about the latest ferroelectric and magnetic memory development in NYCU, including BEOL-compatible ferroelectric transistors, ferroelectric tunnel junctions, and compact STT-MRAM neuron devices. Demonstrations of high energy-efficiency in-memory computing and in-memory annealing will also be highlighted, and the challenges and potential solutions in computing precision, device/circuit variation, and area/energy efficiency will be addressed. Our approach is showcased using a recent SRAM-based in-memory computing macro achieving unprecedentedly high energy efficiency of 20943 TOPS/W.

Biography

Dr. Hou received his Ph.D. in electrical and computer engineering from Cornell University in 2008. In 2000, he joined the Taiwan Semiconductor Manufacturing Company (TSMC). In 2008, he joined the Department of Electronics Engineering, National Chiao Tung University (NCTU) (as National Yang Ming Chiao Tung University (NYCU) since 2021), where he is currently a Chair Professor. Dr. Hou is also the Program Director of Angstrom Semiconductor Initiative, one of the largest national research programs for advanced semiconductors. In 2022, Dr. Hou became the Director General of Taiwan Semiconductor Research Institute (TSRI), one of the National Applied Research Laboratories in Taiwan focusing on semiconductor technology. He was the Associate Vice President for Research & Development at NYCU and the R&D Director of the Electronic and Optoelectronic System Research Lab at the Industrial Technology Research Institute (ITRI). His research interests include the emerging nonvolatile memory for embedded and high-density data storage, electronic synaptic device and neuromorphic computing systems, and heterogeneous integration of silicon electronics with low-dimensional and low-temperature nanomaterials.

Dr. Hou has published more than 300 technical papers with citations >7600 and H-index 44, delivered more than 40 invited conference talks, and held 23 U.S. patents. He was also a recipient of the IEEE Electron Device Society (EDS) Ph.D. student fellowship, EDMA Outstanding Youth Award, CIEE Outstanding Electrical Engineering Professor Award, Micron Teacher Award, Micron Chair Professor Award, MOST Ta-You Wu Memorial Award, and MOST Outstanding Research Award (twice). He served on the technical program committees of major conferences, including VLSI, IEDM, IRPS, DRC, EDTM, ISCAS, etc. He is currently the Regional Editor of IEEE EDS Newsletter. He is also a Member of the Board of Directors of the IEEE Taipei Section and Advisor of the IEEE EDS NCTU student branch chapter.