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IEEE / NE ESDA Meeting

ESD Device Level Testing Standards Review, and Die to Die and Direct Pin Injection Testing Impacts

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Abstract

As device technologies evolve and continue to shrink, manufacturing methods are also being stressed, which can impact yields due to ESD performance. ESD test standards are continuing to evolve as well to meet these changes. However as complex devices such as 3D packing with 1000s of Die-to-Die interconnects become more widely used, this is challenging the "standard" way ESD testing is performed.

Another point of interest for system level testing, is call for a Direct Pin Injection test method. Although the most widely used system level testing standard, IEC 61000-4-2 standard recommends not performing testing on pins of a connector, many manufacturers are being forced to perform this test. We'll discuss the Industry Council on ESD Target Levels approaches to this testing requirement.

Device Level Testing – highlighting the different models

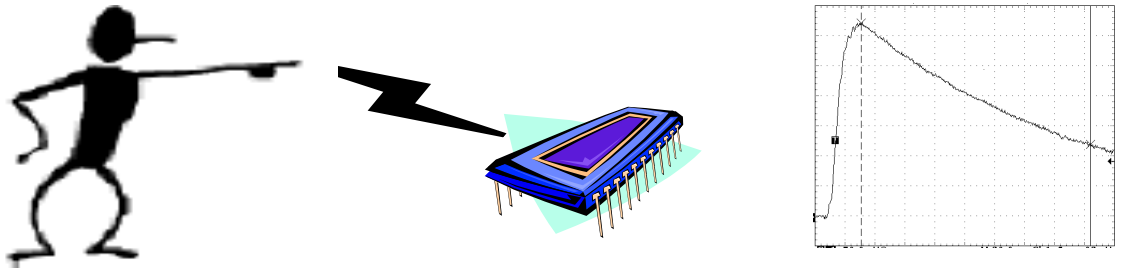
ESD – Electrostatic Discharge

A person or charged object discharging into or out of a sensitive electronic component or circuit can cause a device to fail or a circuit to be upset

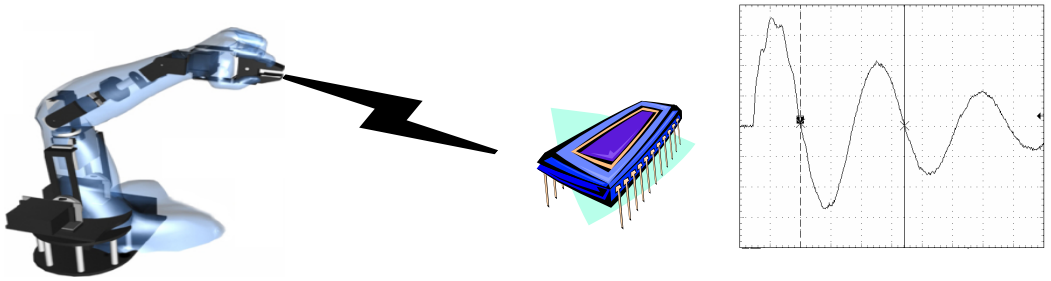
The threshold of feeling is 2kV to 4kV

Everyone can feel 5kV*

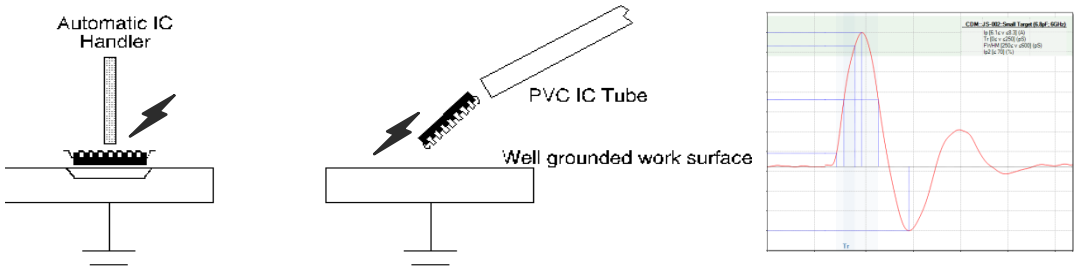
15kV is a ***memorable*** event!!!



Human Body Model Event (HBM) - 100pF/1500 ohm



Machine Model Event (MM) - 200pF/0 ohm



Charged Device Model Event (CDM) - Device Capacitance

Device Level Testing

Qualifying devices to determine their ESD withstand threshold level

The ESD withstand threshold level

This is the highest ESD event (HBM or CDM) a device can withstand without the ESD protection structure being damaged

The Industry Council on ESD Target Levels (https://www.esdindustrycouncil.org/ic/en/) was formed to assist industry with setting appropriate design target levels for today and tomorrow's devices

For HBM, 2000V was once the norm, the Council now recommends 1000V and is leaning towards 500V

For CDM, 500/750V was once the norm, the Council now recommends 250V and is looking at much lower design levels for new technologies

The ESD withstand threshold levels are required for several reasons

- Device manufacturing purposes, to ensure the ESD protection factory controls are sufficient to allow a device to be manufactured and handled without causing any failures. This is especially important when manufacturing at multiple locations!
- Product marketing – data sheet definitions, higher thresholds may mean a higher selling price
- Customer satisfaction – meaning no field failures, which can be very costly and can also ruin a company's reputation

Device Level Testing

Qualifying devices to determine their ESD withstand threshold level

There are many different standards, even duplicates of standards across different Standards bodies. This of course has caused confusion and, in some cases, doubled testing requirements.

- The ESDA and JEDEC committees have eliminated some of this confusion/multiple work by joining together to develop single documents for the HBM (Human Body Model) and CDM (Charged Device Model) testing methods
  - ANSI/ESDA/JEDEC JS-001, Human Body Model (HBM), Component Level
  - ANSI/ESDA/JEDEC JS-002, Charged Device Model (CDM), Device Level

- The committees are also working with other Standards Bodies, such as JEITA (Japanese), AEC (Automotive Electronics Council) to get them to adopt the JS-001 and JS-002 standards

Device Level Testing

Qualifying devices to determine their ESD withstand threshold level

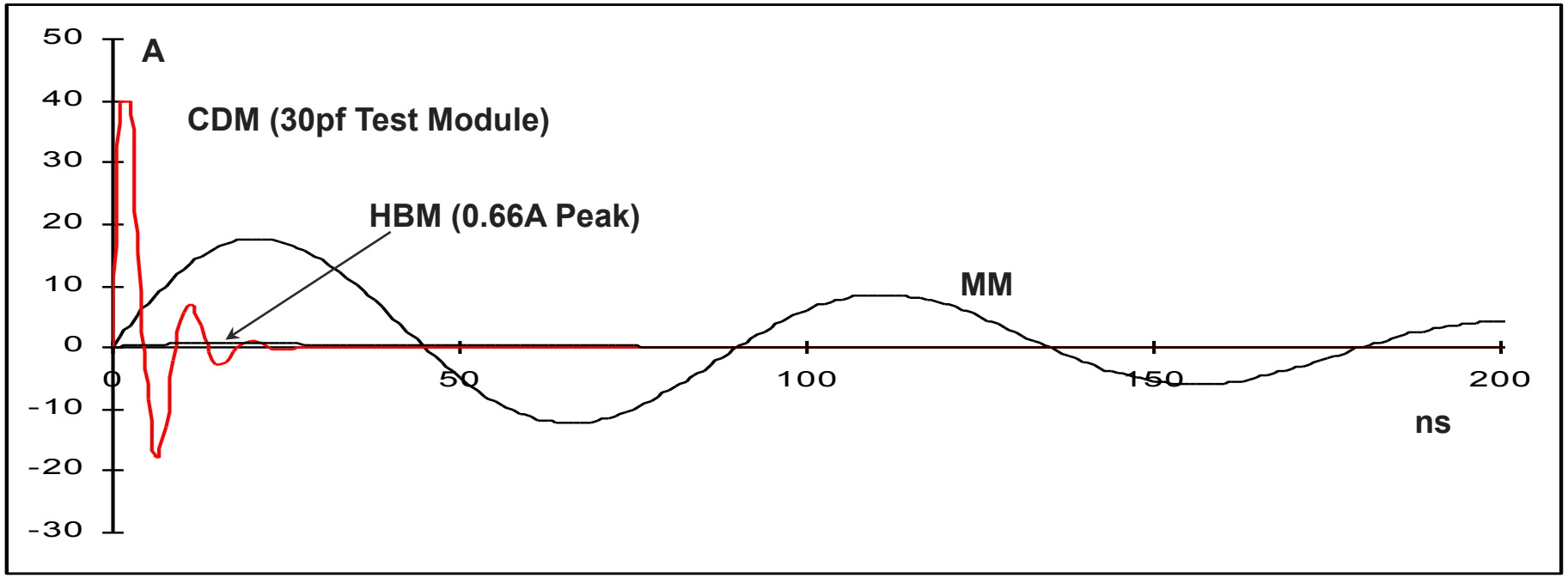
- To qualify a device and determine it's ESD susceptibility threshold level, JEDEC specifies the use of HBM and CDM as the only methods required
    - *JESD47L STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS*

- *MM (Machine Model), which was once required, is no longer required to qualify a device!*
    - The use of Machine Model to qualify a device was being driven by the Japanese and the automotive industry. However, studies have shown that the failure signatures of the HBM and MM events are similar, so there is no need to duplicate testing
        - However, the method is still being used and specified by some companies – there's no way to get away from it ☺

- There are many different test methods that are in use today, HBM and CDM are the required methods for determining a devices ESD withstand threshold level
    - The following pages highlight some of the device level test methods available today

Overlay of Network Models – highlighting the different models

Comparison of 1kV CDM, HBM and MM discharges



- The CDM discharge is 100x faster than HBM or MM
- The peak current can be 40x that of an HBM pulse

Device Level Testing – highlighting the different models

Joint JEDEC and ESD Association standard

- JS-001-2023 Human Body Model (HBM)
- JS-002-2022 Charged Device Model (CDM)
- *SP5.3.3-2018 Low Impedance Contact CDM (LI-CDM)*
- *SP5.3.4-2022 Capacitively Coupled TLP CDM (CC-TLP)*

Electrostatic Discharge Association (ESDA)

- ESDA STM5.1 Human Body Model (HBM)
  - Superseded by JS-001
- ESDA SP5.2 Machine Model (MM)
  - Dropped from an STM to an SP in 2019
- ESDA STM5.3.1 Charged Device Model (CDM)
  - Superseded by JS-002
- ESDA SP5.4 Transient Latch-up (TLU)
- ESDA SP5.5 Transmission Line Pulse (TLP/VF-TLP)
- ESDA SP5.6 Human Metal Model (HMM) 2 pin testing
- ESDA 14.5 Near-field Immunity Scanning
- WG 23 Electrical Overstress (EOS)
- WG 25 Charged Board Event (CBE)
- WG 26 ESD Modeling
- WG 27 Electrical Overstress (EOS) in Automotive
- WG 28 Electrostatic Attraction
- WG 29 HealthCare

WG 14 *System Level / Cable Discharge Event (CDE)*
System Level Direct Pin ESD (SL-DPE)
Work in progress

Joint Electron Device Engineering Council (JEDEC)

- JEDEC JESD22-A114 Human Body Model (HBM)
  - Superseded by JS-001
- JEDEC JESD22-A115 Machine Model (MM)
  - Decommissioned
- JEDEC JESD22-C101 Charged Device Model (CDM)
  - Superseded by JS-002
- JEDEC JESD78 Latch-up
  - Presently at Rev F.01

Automotive Electronics Council (AEC)

- AEC-Q100-002 Human Body Model (HBM)
- AEC-Q100-003 Machine Model (MM)
  - Decommissioned
- AEC-Q100-011 Charged Device Model (CDM)
- AEC-Q100-004 Latch-up

Links:

EOS/ESD Association
https://www.esda.org/standards/

JEDEC
https://www.jedec.org/

AEC
http://www.aecouncil.com

Device Level Testing – Questions and Concerns

With all test methods, there are some issues when trying to replicate a real-world event in a controlled manner!

- *This is what test methods and testers are trying to do!*

Although the HBM test method has been around for a long time, there are still questions and concerns about the method and whether it is still a useful test

- Tester artifacts have been reported over time, which on previous technologies weren't a problem but on new technologies they do have an impact
    - Users should be aware of these, and standards highlight them for reference
- Questions on system interaction with the device under test – do parastics within the tester effect the determination of your device ESD threshold level?
    - Use of a 2pin tester is allowed when results are brought into question
- Is the device being overstressed due to the number of stress combinations required by the standard?
    - Standards have changed over time to try and address some of these concerns

Device Level Testing – Questions and Concerns

The CDM test method has been in use for a long time as well, however many feel it is more important than HBM for device qualification

- This is due to the fact that manufacturing facilities and protection designers know how to protect against HBM, besides humans don't touch devices during manufacturing. However, unintended CDM events in manufacturing continue to be an issue!
- Another reason is, as device geometries continue to shrink and the desire for performance increases, device ESD protection designers are limited in the amount of real-estate they're given for protection!!

Device Level Testing – Questions and Concerns

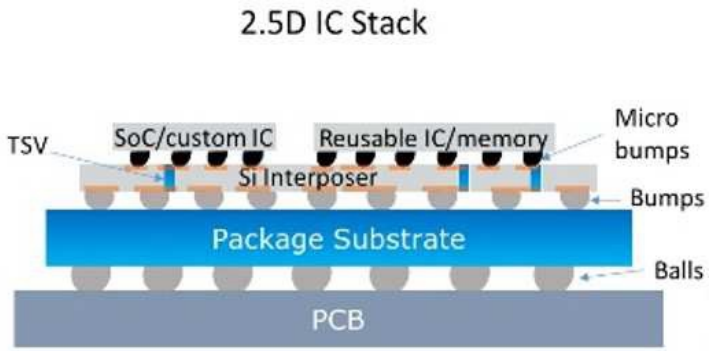
Some of the issues with today's CDM Field Induced test method

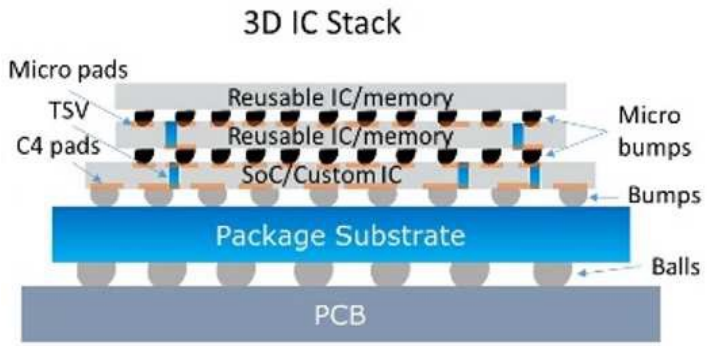
- Air discharge – this causes so many problems during testing, due to its non-repeatability and reproducibility issues. This is being made even worse by the desire to have lower threshold levels on devices, lower voltage makes the non-repeatability even worse!!
  - The Joint CDM Working Group is developing two different Contact CDM methods
    - *Low Impedance Contact CDM (LI-CCDM)*
    - *Capacitively Coupled TLP (CC-TLP)*

- Lack of knowledge about CDM events in manufacturing and misconceptions about whether designs need to address the event
  - It's interesting to note, that most device data sheets either don't include CDM levels or even worse don't include HBM levels, so how do you know they're protected????
    - The ESDA developed a standard practice document which outlines recommendations for data sheets, regarding the reporting of ESD threshold levels

CDM Testing for the Future

In addition, as devices shift to “die level only” or 2.5 and 3D packaging with 1000s of “die-to-die” interconnects, threshold levels may be below 10 volts, testing of these extremely small “micro bumps” is impossible with the present Field Induced CDM test methods





There are still several questions regarding the testing of “micro bumps”

- Is the protection of these components more of a factory control problem?
- If testing is required, what percentage of testing would be realistic?
  - How many bumps would have to be tested?

Field-Induced CDM (FICDM)

The Industry Council on ESD Target Levels, White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements and its follow-up, WP2 Part II: Die-to-Die Interfaces discuss the need for lowering the CDM design threshold level from 500V to 250V. However, it is also noted that many new designs may require levels at 125V or below.

The most common CDM test method is ANSI/ESDA/JEDEC JS-002, which specifies the use of a field-induced method for performing the test. This method recreates or closely replicates a real-world event.

Real-world CDM event

- The device acquires a charge during processing
- The device gets in close proximity to a metal surface at a different potential
- A CDM event is produced

Field-induced CDM testing

- The device acquires a charge through a HV field plate
- A grounded pogo pin (ground plane) is brought in close proximity to a pin on the device
- A CDM event is produced
  - Automation allows testing of each individual pin on the device

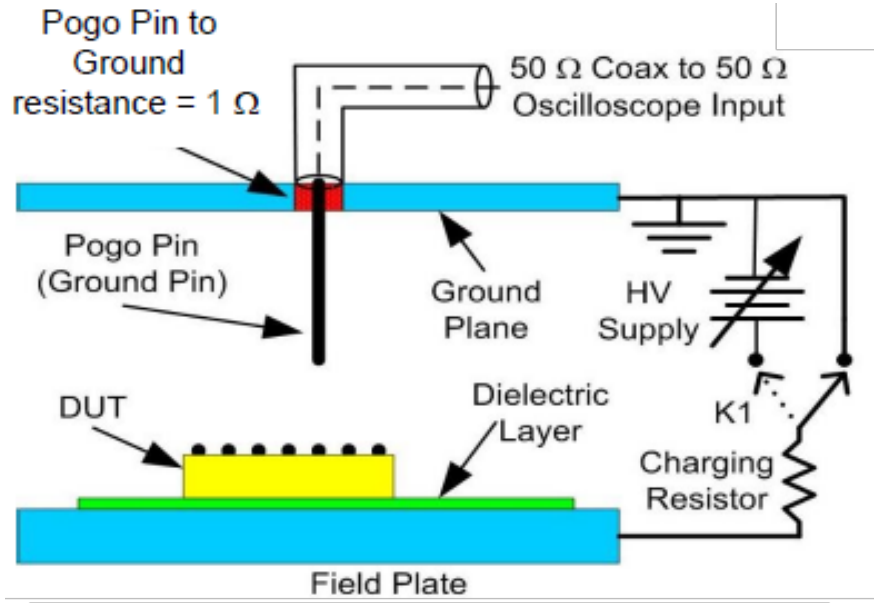
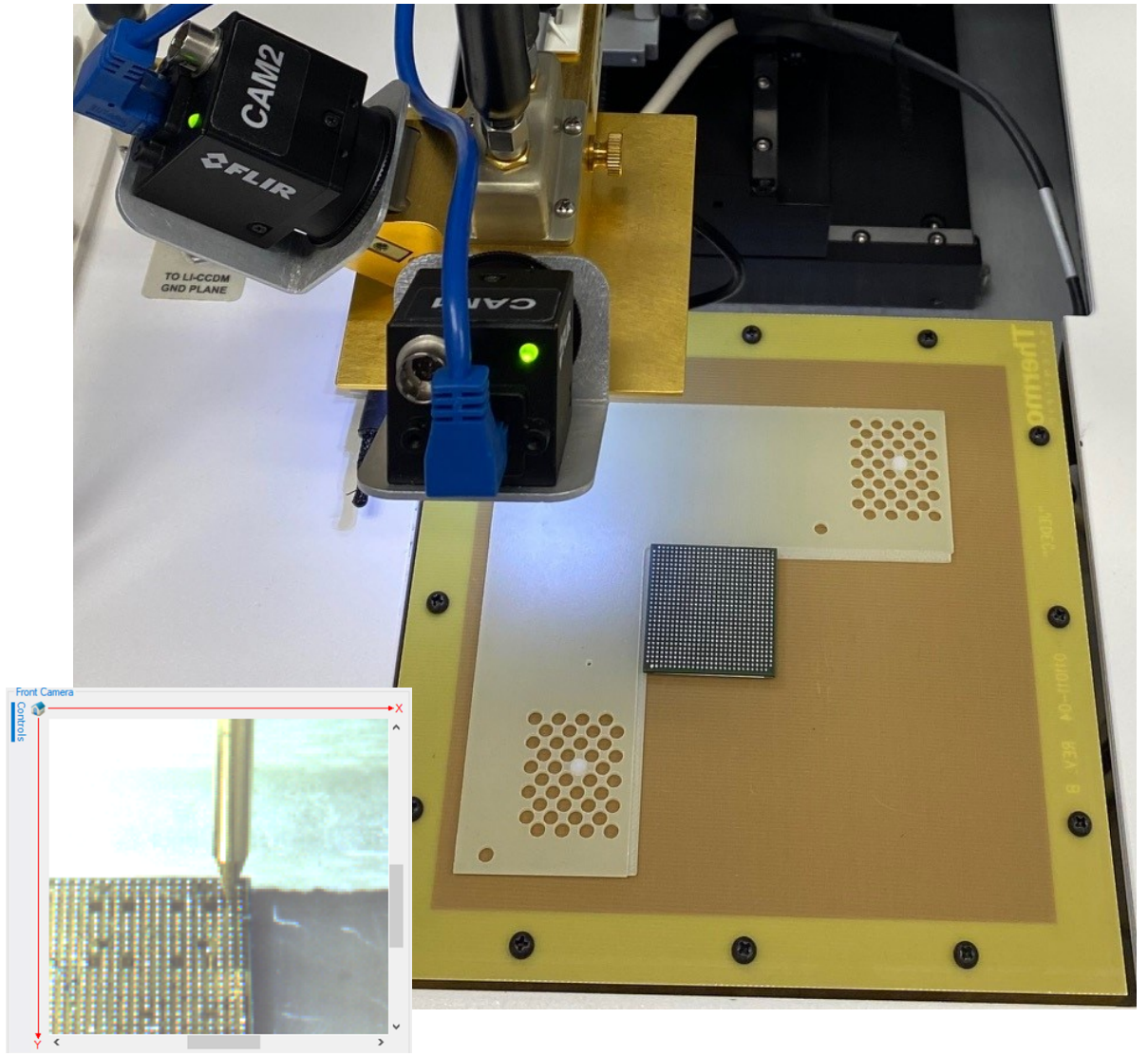


Figure 1: Simplified CDM Tester Hardware Schematic

FICDM Simulator

- Device is placed on a dielectric (specified with a thickness of 0.381 mm)
- Under the dielectric, a metallic plate is connected to a HV supply
- A robotic arm moves a grounded probe with a pogo pin in the center
  - Cameras are used to confirm alignment of the pogo to the DUT pins
- The pogo pin touches one of the pins of the device
- A 1-ohm resistor around the pogo pin is used to capture the CDM event voltage
  - The actual resistance is used to convert the voltage to current amplitude



Two camera views used for alignment

Field-Induced CDM (FICDM)

Although the field-induced method closely replicates a real-world event, there are a number of issues with this method which makes it non-repeatable, especially at lower test voltages

A test method should closely replicate the real-world event; however, it should be repeatable and reproducible

- Air discharge, same as real world event, but with same issues as a spark in air
- Field changes due to geometry, affect CDM event (*type of pogo pin being used*)
- Environmental conditions affect the spark, thus the CDM event
  - Thermo Fisher Scientific was the first company to publish data showing the relationship between humidity and FICDM waveform repeatability

The best way to over come these issues is to use a contact method, such as low-impedance contact CDM (LI-CCDM) or Capacitively Coupled TLP (CC-TLP)

Low-impedance Contact CDM (LI-CCDM)

- LI-CCDM uses a TLP pulse and transmission line to produce a waveform that closely matches FICDM waveforms specified in JS-002 (as well as other FICDM waveforms)
- Because it is a contact method, it is extremely repeatable
- Has a very high bandwidth measurement capability and the ability to switch rise time

Advantages of the LI-CCDM method

- Impervious to environmental conditions
- Since event does not happen in air, field strengths are the same and they do not depend on pogo pin geometry
- Ability to use small geometry, pointed pogo pins during device testing
- Very repeatable, even allowing evaluation of waveforms as a means of failure detection
- Better correlation from device to device and simulator to simulator
- Better resolution for single device pin performance

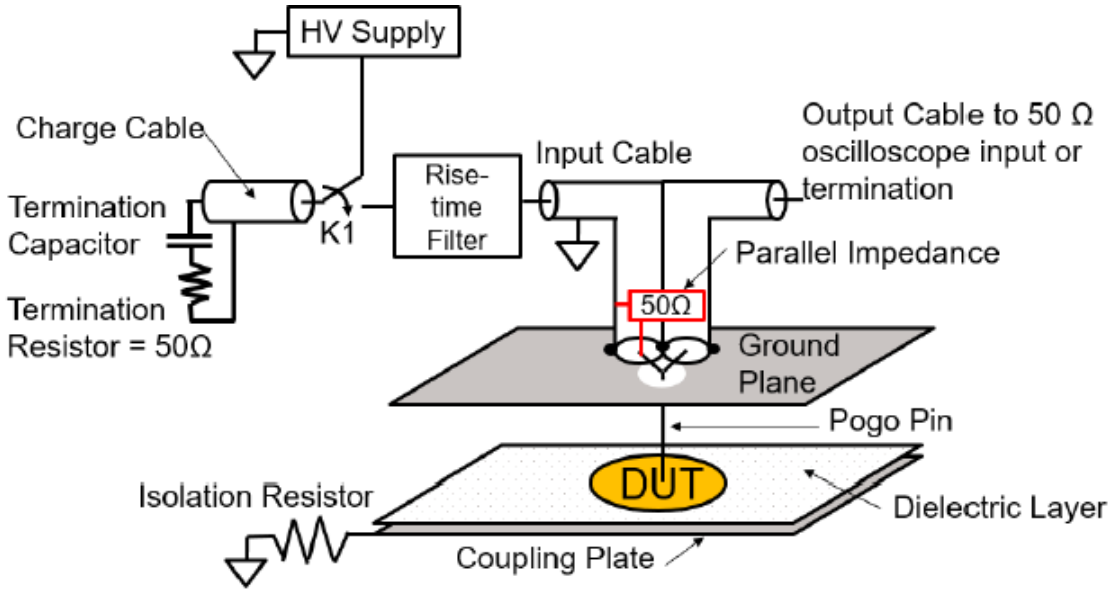


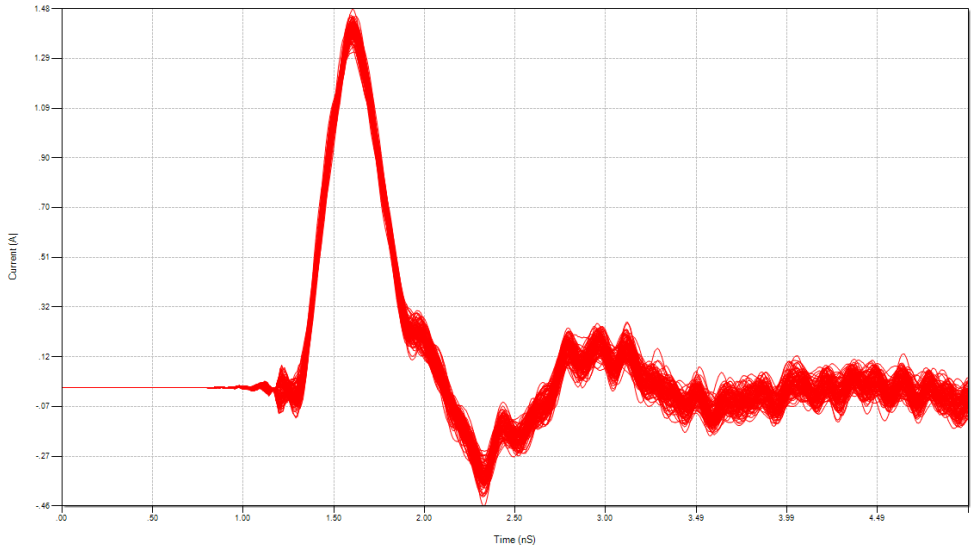
Figure 1: Simplified Hardware Schematic for Low-Impedance CCDM

LI-CCDM Waveform Repeatability Compared to FICDM

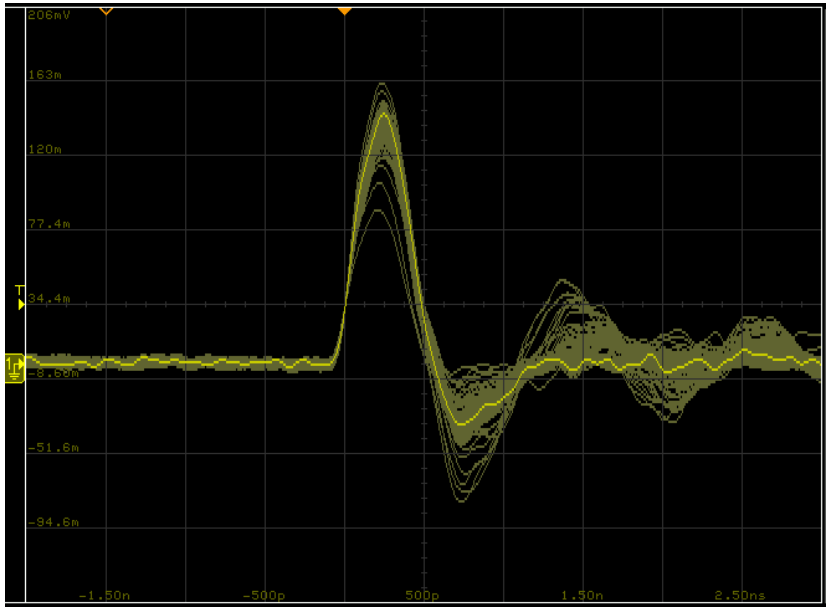
Repeatability of the LI-CCDM method versus the FICDM (JS-002) method

100 waveforms were captured using the 7.2pF calibration module at 100V

The repeatability of the LI-CCDM method compared to the JS-002 method can clearly been seen by simply comparing the waveforms shown below



LI-CCDM waveforms overlaid in EvaluWave
(Thermo Fishers' waveform analysis program)



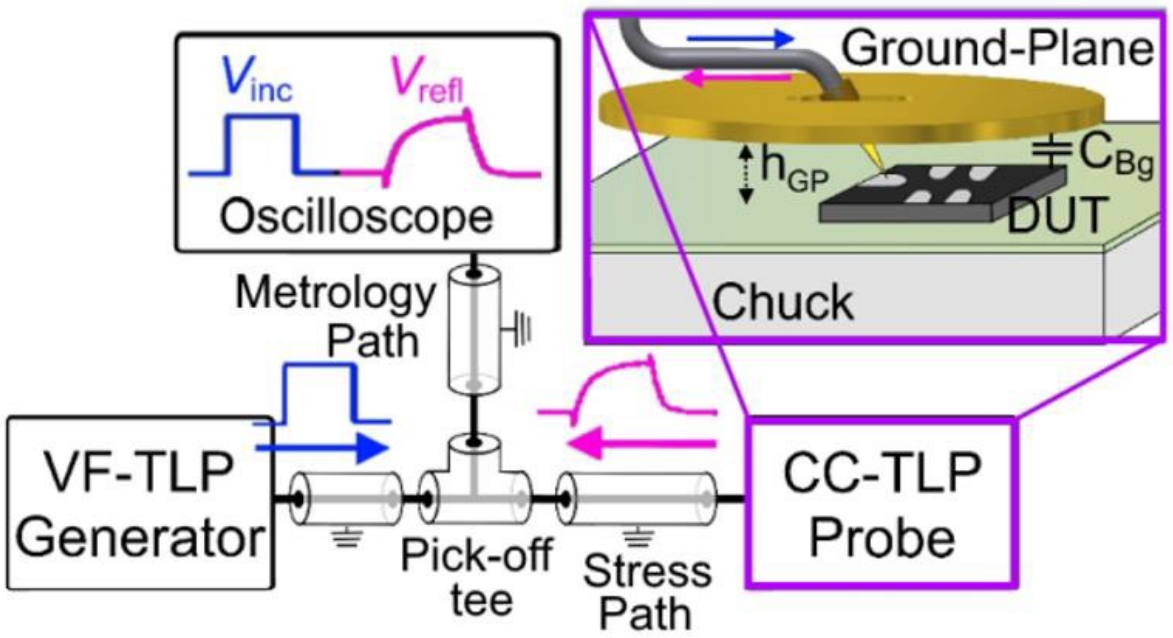
JS-002 waveforms captured using infinite persistence on the oscilloscope

Capacitively Coupled TLP (CC-TLP)

- CC-TLP uses a TLP pulse and transmission line to produce a CDM like waveform
- Because it is a contact method, it is extremely repeatable
- Has a very high bandwidth measurement capability and the ability to switch rise time

Advantages of the CC-TLP method

- Impervious to environmental conditions
- Since event does not happen in air, field strengths are the same and they do not depend on the needle geometry
- Very repeatable, even allowing evaluation of waveforms as a means of failure detection
- Better correlation from device to device and simulator to simulator
- Better resolution for single device pin performance
- Ability to test at bare die and wafer level



J. Weber et al., "Comparison of CDM and CC-TLP Robustness for an Ultra-High Speed Interface IC", EOS/ESD 2018

CDM Testing for the Future

Both the LI-CCDM and CC-TLP methods provide improved test repeatability and the ability to test at lower voltage levels over the Field Induced CDM test method

As it stands now, both documents are at a Standard Practice (SP) level, which means they both provide a “best known method” for performing the test, however they may not provide repeatable data

The next step is to perform “Round Robin” testing within the CDM committee to move them to the next level, which would be to “standard test method”

It should be noted, that both of these methods would specify a “current” value, rather than “voltage” level for the failure threshold information, which is different from voltage levels that the factory folks expect

The questions I mentioned earlier, regarding the testing of “micro bumps” will still need to be answered

- Is the protection of these components more of a factory control problem?
- If testing is required, what percentage of testing would be realistic?
  - How many bumps would have to be tested?

Device Level Testing – Latch-up Testing

Latch-Up is defined as -

"A low impedance path created within the device by triggering a parasitic SCR"
"Once triggered into conduction an SCR will remain in a conducting state until the current flowing through it falls below the holding value"

Typically, when the SCR is triggered, very high currents will flow through the device causing failure

Real world latch-up

JEDEC 78 is the most commonly used test method

- Testing is performed by powering the part, making a pre-IDD measurement and then injecting either a current or voltage pulse onto a signal pin or applying an overvoltage to the supply rail in an attempt to trigger a latch-up event. Once the stress is removed, a Post-IDD measurement is made to see if there has been an increase in the current draw

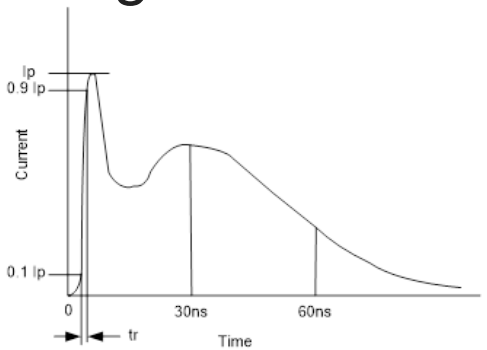
Device Level Testing – Latch-up Testing

JEDEC 78 is the most commonly used test method

- Although the JEDEC 78 test method has been in use for many years, there a number of “holes” in the document, regarding testing of analog devices, how to control devices during testing and a number of other device type specific issues
  - To help combat these issues, the JEDEC 78 working group rewrote the document and released version 78F in 2022
- In my experience, latch-up testing is possibly the hardest and most time-consuming test to perform because it requires detailed knowledge about the device and in many cases, knowledge that only the device designer will have
  - *Most of the application questions I receive, focus around setting up a latch-up test and reviewing the results of the tests!!*
- Some of today’s newer devices are adding another hurtle to testing, and that’s the requirement for high level power requirements, some exceeding the need for 500amps or more in order to power the device!!

System Level Testing at the Device Level

Device manufacturers are being asked by their customers to provide ESD threshold level data, using the waveform specified in the IEC-61000-4-2 System Level test



IEC 61000-4-2	Value	Unit
10 to 90% Pulse Rise time	0.7 to 1	ns
First peak current of the discharge	3.75 ± 15%	A / KV
Current at 30 ns from initial 10% point	2 ± 30%	A / KV
Current at 60 ns from initial 10% point	1 ± 30%	A / KV

The first request given to the ESDA was on how to perform testing of a single device using the IEC waveform, in a controlled manner

- The ESDA developed a Standard Practice SP5.6 Human Metal Model (HMM) which outlined how a system level like event could be delivered to a device to determine its susceptibility level against the IEC event
- Although this is not seen as a realistic test and the level determined on the stand-alone device will not match or corelate once it is mounted on a PCB in say a notebook PC

System Level Testing at the Device Level

Recently however, customer requirements have changed, and they are now asking for the results with the device mounted on the PCB within the notebook PC, requesting a pulse be delivered through a pin on an external port, connector pin

- Although the IEC 61000-4-2 document states, testing should not be done directly on connector pins, only on the shell, this is what is being asked of device manufacturers

To understand this requirement better and determine what is really required, the Industry Council produced a survey recently which was sent to industry

This requirement has been termed System Level Direct Pin ESD (SL-DPE)

- Feedback showed that some companies are performing this type of testing, however there were still a number of unknows as to the type of waveform being used or whether testing was being performed powered or unpowered
- The Council will be investigating this need further and if required, will work with the ESDA to develop a test method addressing this testing need

System Level Testing at the Device Level

Related to this type of testing, the ESDA's System Level ESD working group (WG14) had been developing a Cable Discharge Event (CDE) document

- However, due to several roadblocks the document has been stalled
- Issues like -
  - What types of cables are we trying to replicate?
    - Ethernet?
    - USB?
    - HDMI?
    - Would it be cable alone, or would there be a load at the end of the cable?
  - What type of waveform are we expecting to generate – is there enough 'real-world" cable discharge waveform data to determine this?
  - Could a TLP pulse be used to simulate an event?

Device Level Testing – Questions and Concerns

Designing to meet ESD requirements for today and tomorrow's devices and systems will continue to be an important part of a company's qualification process, to ensure electronics can withstand today's harsh environments!!

Testing methods continue to evolve, with new methods being introduced to meet new threats discovered as new technologies emerge

We all need to be vigilant in designing, handling and testing products to ensure we can meet the needs of our customers, which in some cases is us ☺

Visit the EOS/ESD Associations website for both Factory and Device Level standards and information related to EOS and ESD

Factory documents –

- ANSI/ESD S20.20 Control Plan Audit Checklist
- ANSI/ESD TR53 Compliance Verification of ESD Protective Equipment and Materials
- ANSI/ESD SP17.1 Process Assessment

Setting the Global Standards for Static Control

https://www.esda.org/

Questions?

Thank You

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CTS Product Offerings – Complete solutions for the ESD market

MK series

Human Body Model,
Machine Model
& Latch-Up

The MK series HBM, MM and Latch-up systems offer high speed, automated testing to industry standards and are an intricate part of today's device qualification practices.

The MK series ranges from 64 pin systems, up to today's highest pin count ESD test system, the MK.4 at 2304 pins

Orion3

Charged Device Model

The Orion3 CDM test system allows the user to perform device qualification testing. Testing can be performed using either the Field Induced method most widely used industry or new contact test methods, such as the Low-Impedance Contact CDM (LI-CCDM) method

Celestron

Transmission Line Pulse

The Celestron TLP/VF-TLP test system allows the user to characterize their devices ESD protection structures to help analyze new designs or the impact a new technology may have on older designs. Testing can be performed at both package and wafer level

Pegasus

2-Pin ESD
& Curve Trace

The Pegasus 2-pin HBM, MM and HMM system provides testing at both the device and wafer level, providing both engineering and device qualification support

Please visit www.thermofisher.com/esd for additional information