



## IEEE Orange County Solid-State Circuits Society (SSCS) Present: *Cryogenic CMOS for Future Scaled Quantum Computing Systems*

**By Dr. Daniel Friedman, Distinguished Research Scientist/Senior Manager, IBM Research**

<b>Day:</b>	Wednesday, February 12, 2025		
<b>Time:</b>	Registration & Networking	6:00 p.m. – 6:30 p.m.	
	Presentation	6:30 p.m. – 8:00 p.m.	
	Q&A and Networking	8:00 p.m. – 8:15 p.m.	
<b>Fee:</b>	Free for all the IEEE & SSCS members, students, engineers in transition, technologists, as well as those who are exploring to join IEEE & SSCS in the future.		
<b>Address:</b>	Custom Silicon Solutions (CSS), 18021 Cowan, Irvine, CA 92614, USA.		
<b>Parking:</b>	Free Parking available in the permitted & unmarked spaces.		

**Abstracts:** Quantum computing represents a new paradigm that has the potential to transform problems that are computationally intractable today into solvable problems in the future. Significant advances in the last decade have lent support to the idea that quantum computers can be implemented, and further that the goal of demonstrating true performance advantages over traditional computing techniques on one or more problems may be achieved in the not-so-distant future. Delivering on this promise is expected to require quantum error correction solutions, in turn demanding large qubit counts that pose significant challenges for quantum computer implementations, especially in the area of qubit interface electronics. An active area of research to address this challenge is the use of integrated cryogenic CMOS designs. In this presentation, we will present a superconducting qubit-based quantum computing system framework, opportunities for cryogenic CMOS introduction into future systems, example cryogenic CMOS implementations and results, and next challenges that must be met to enable cryogenic CMOS adoption.



**Biography:** Dr. Daniel Friedman is currently a Distinguished Research Scientist and Senior Manager of the Communication Circuits and Systems department, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA; he is also an IEEE Fellow. He received his doctorate from Harvard University and then subsequently completed post-doctoral work at Harvard and consulting work at MIT Lincoln Laboratory. At IBM, he initially developed field-powered RFID tags before turning to high data rate wireline and wireless communication. His current research interests include accelerator designs for AI, high-speed I/O design, and circuit/system approaches to enabling new computing paradigms, the latter including cryogenic electronics for use in quantum computing systems. He holds more than 90 patents and has authored or co-authored more than 85 publications. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 International Solid-State Circuits

Conference (ISSCC), the 2009 Journal of Solid-State Circuits (JSSC) Best Paper Award (given in 2011), the 2017 ISSCC Lewis Winner Outstanding Paper Award, and the 2017 JSSC Best Paper Award (given in 2019). He has served on the technical program committees of the Bipolar Circuits and Technology Meeting (2003-2008) and of the ISSCC (2008-2016); since 2016, he has served as the ISSCC Short Course chair. He served as a member-at-large of the IEEE Solid-State Circuits Society (SSCS) Adcom from 2018-20, as the SSCS Distinguished Lecture chair from 2020 to 2021, and as Associate Editor of the JSSC from 2019-2023. He is the current Vice President of the SSCS.

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**Send questions to Farhad Mafie, IEEE-OC SSCS Chairman: [FarhadMISC@Gmail.com](mailto:FarhadMISC@Gmail.com)**

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