Virtual Training Program on

VLSI SoC Design using Verilog HDL

by

IEEE CAS Society (CASS) SBC60981AG

Date: 08.01.25 to 08.02.25

Resource Person: **Mr.P.R.Sivakumar,**

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Title: "VLSI SoC Design using Verilog HDL "

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Students learned about VLSI (Very Large Scale Integration) SoC (System on Chip) design using Verilog HDL (Hardware Description Language)which is a crucial approach for creating compact, high-performance integrated circuits. Verilog HDL allows designers to model, simulate, and implement complex digital systems efficiently. In VLSI SoC design, multiple subsystems like

processors, memory, and I/O interfaces are integrated into a single chip. Verilog's ability to describe both the structural and behavioural aspects of a circuit makes it ideal for large-scale designs. It facilitates synthesis, timing analysis, and verification, ensuring that the chip meets desired specifications. The design process involves writing Verilog code, simulating the behaviour, and then synthesizing it into a physical layout. Challenges include managing power consumption, minimizing area, and ensuring signal integrity. However, Verilog's scalability and robust tool support make it indispensable in modern VLSI SoC design.

Students who completed this training were given certificates. We take this opportunity to thank our **CEO Sir, Principal Sir, and HOD-ECE** for their support and guidance towards the successful completion of this training Program.