IEEE MTT-S Distinguished Microwave Lecture

Power Without Pain: High Power MMIC PA Design, the Pitfalls and how to Avoid Them

Michael Roberg

Qorvo, Inc.

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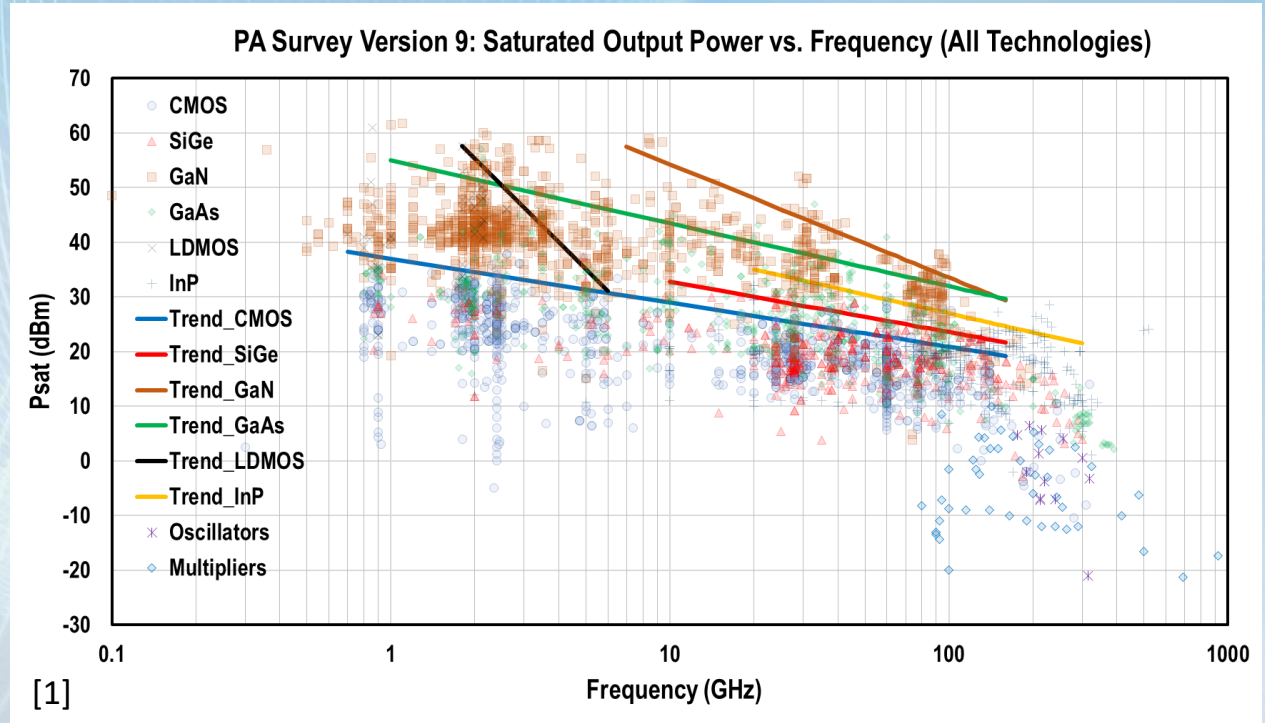
Background & Motivation



[1]

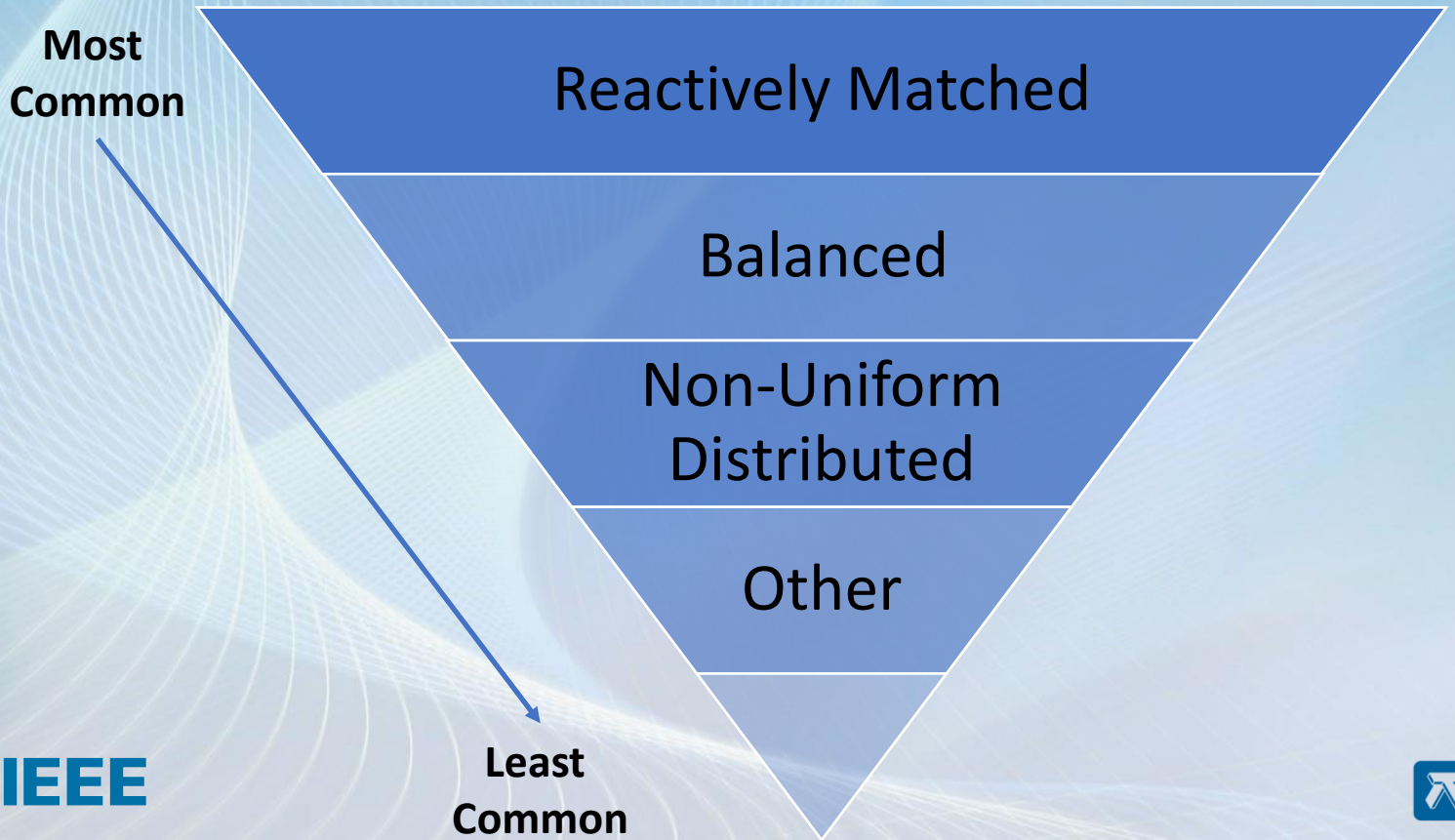
GaAs and GaN PAs Dominate Below 100 GHz

GaAs vs. GaN

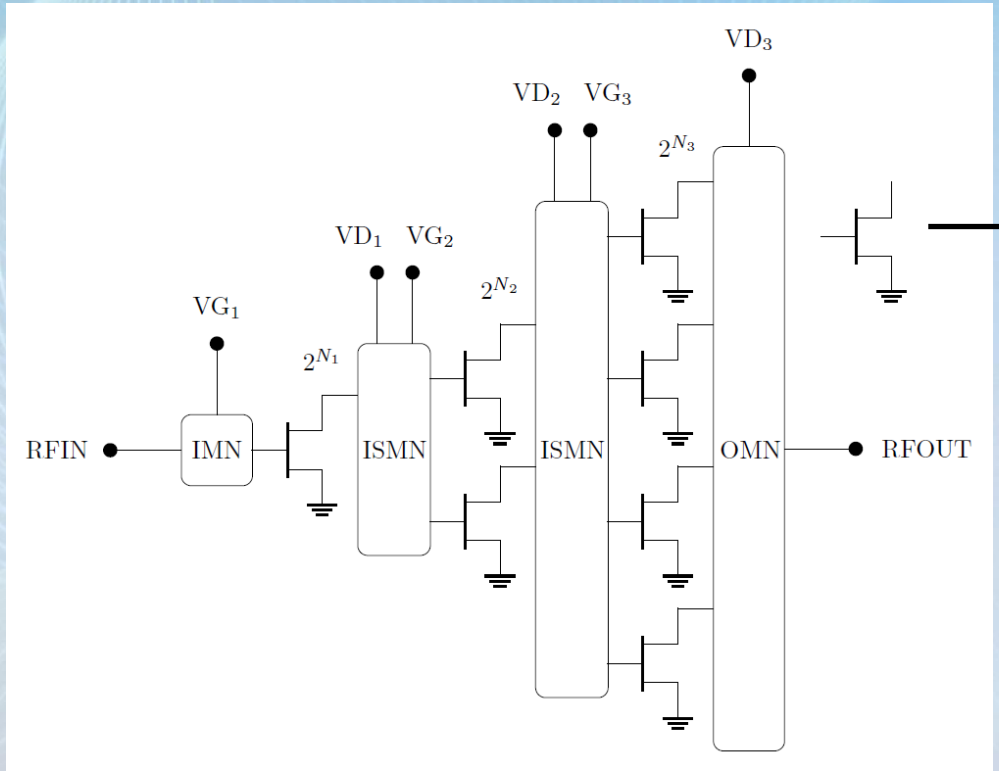
- **Power**: GaN has higher maximum power density (>10x) mainly due to drain voltage, resulting in higher power MMICs
- **Efficiency:** Efficiency is similar between the technologies
- **Linearity:** GaAs is typically a more linear technology. GaN linearity is still a work in progress although some foundries are doing quite well
- **Frequency:** Relatively similar. Strong research thrust to push GaN to D-band
- **Thermal:** GaN has can operate reliably at a higher channel temperature (typically 225°C) vs < 160°C typical in GaAs. GaN is typically grown on a SiC substrate, which has a higher thermal conductivity than GaAs
- **Matching:** GaAs is often easier to match (lower Rp x Cp product) due to lower drain voltage. Typical GaN has a knee voltage which is quite high precluding useful operation at a GaAs operating voltage (e.g. < 8V).
- **Cost:** GaN is more expensive than GaAs (~2X)
- **Schedule:** GaN typically takes longer than GaAs to process (~2X)

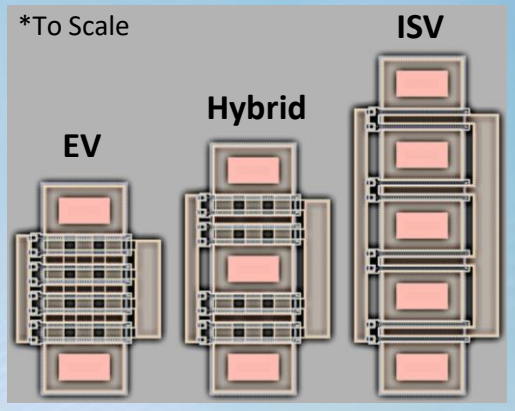
	GaAs	GaN
Power		✓
Efficiency	✓	✓
Linearity	✓	
Frequency	✓	✓
Thermal		✓
Matching	✓	
Cost	✓	
Schedule	✓	

GaN & GaAs MMIC PA Topologies



Reactively Matched PA Topology





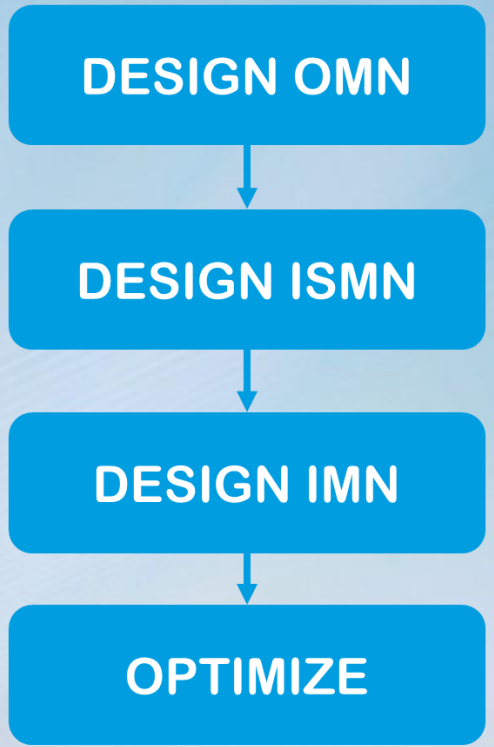
2-Finger FET Building Block

Why Reactive? Highest Power / PAE and Straightforward

Reactively Matched PA Design Procedure

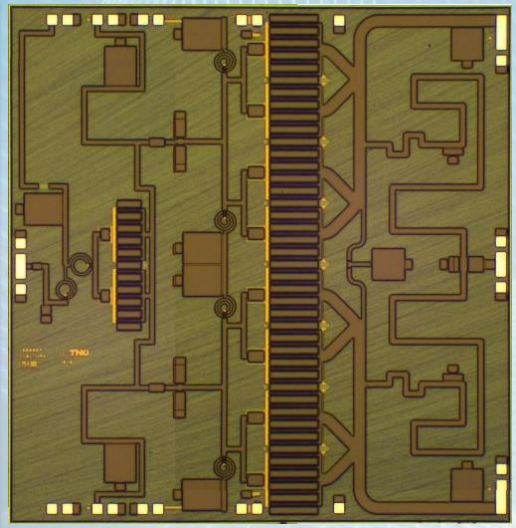
Attack The Problem Backwards

- Design the Output Matching Network first
  - Typically the designer has an idea of the optimal load for desired performance parameters (e.g. power, PAE, etc)
  - Ensure the load to each device is uniform and the match is low loss to maximize power combining efficiency
- Once the OMN is designed, design the Inter-Stage Matching Network
  - Apply same techniques used to design the OMN
  - Ensure adequate drive margin
  - Often the most difficult network to design
- Keep working backwards to the Input Matching Network
  - Typically the easiest network to design
- Optimize all networks to maximize performance



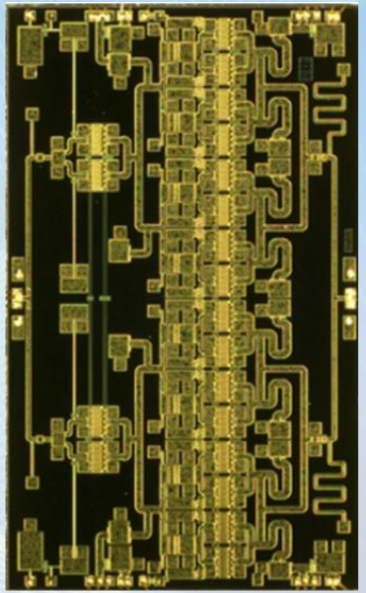
Reactively Matched MMIC PA Examples

[2] 400W S-Band



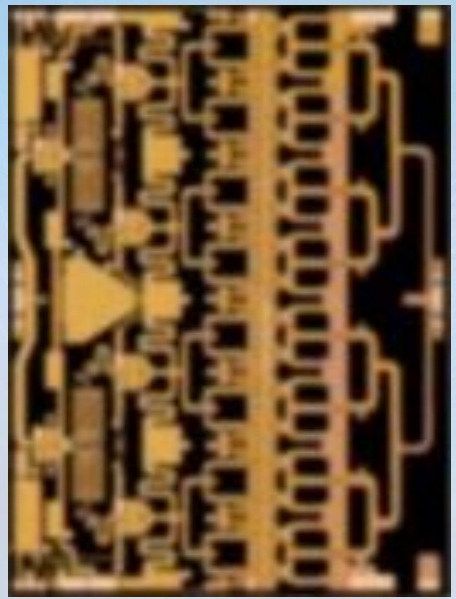
V_D = 55V, L_G = 450nm

[3] 100W X-Band



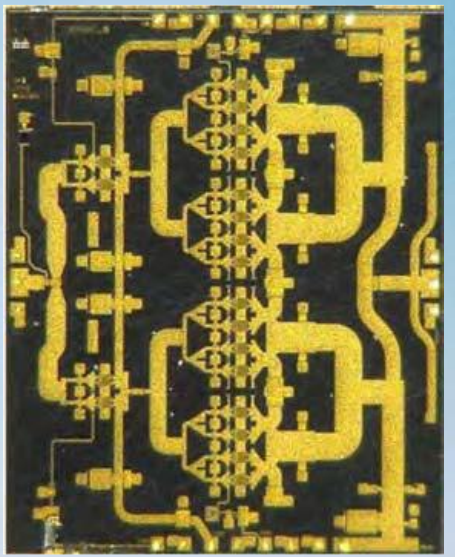
V_D = 40V, L_G = 250nm

[4] 50W Ku-Band



V_D = 28V, L_G = 150nm

[5] 40W Ka-Band

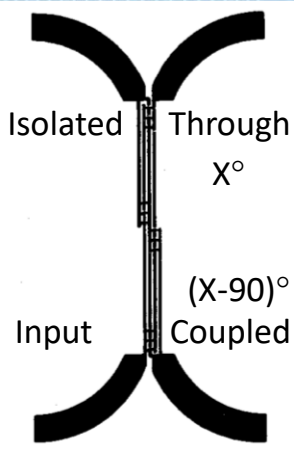


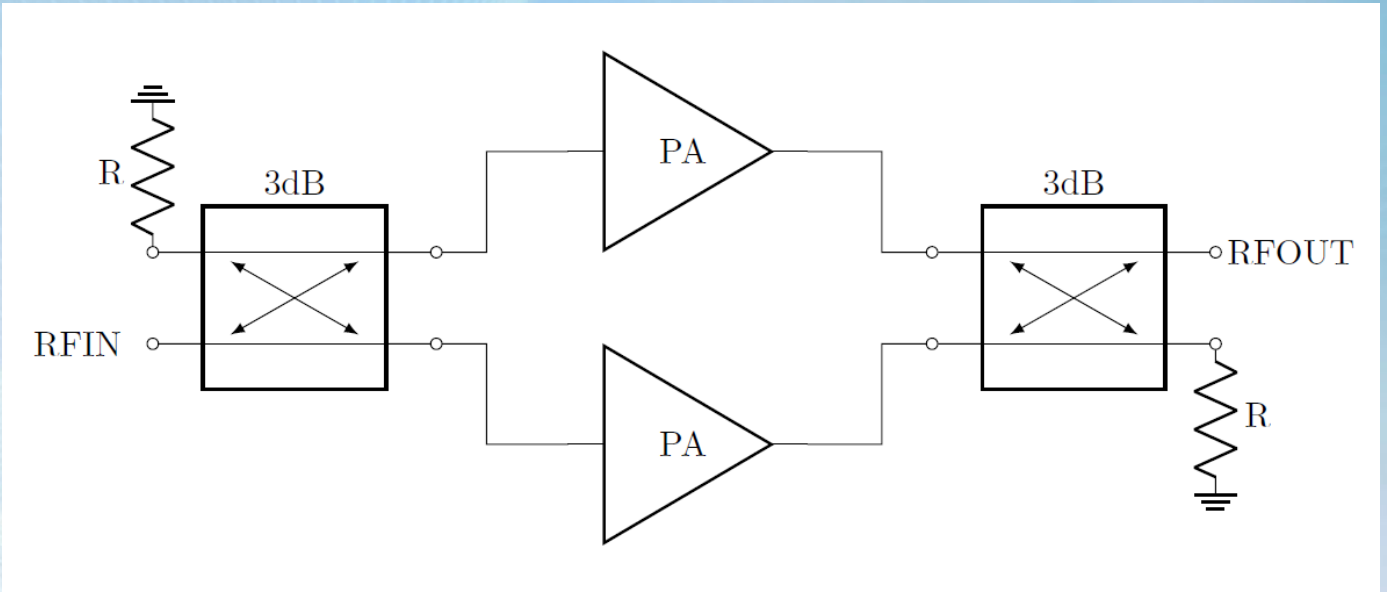
V_D = 28V, L_G = 200nm

*All die are not to scale

Balanced MMIC PA Topology

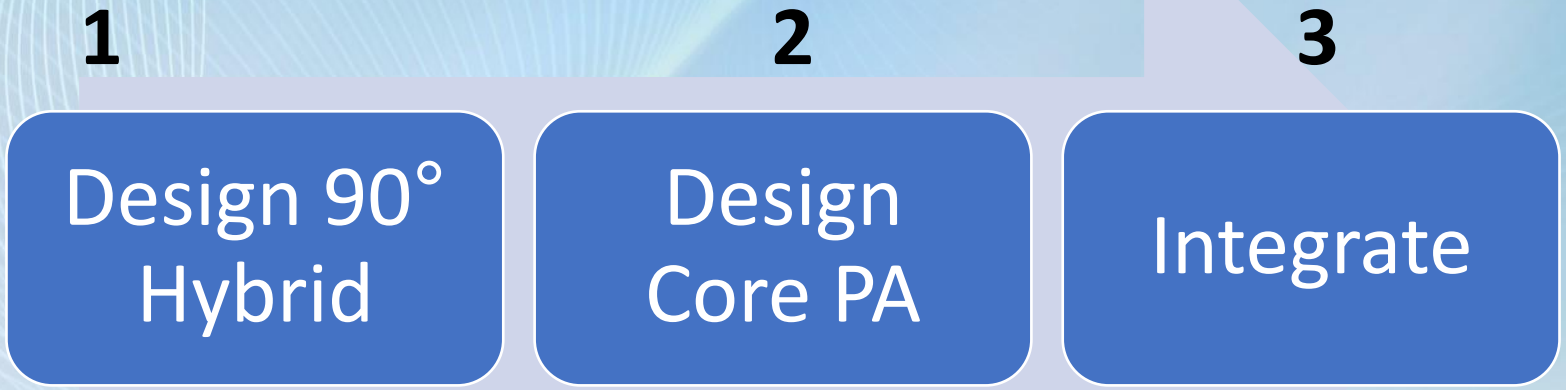
[6] Lange Coupler





Why Balanced? Good Return Loss, Load Mismatch Tolerance and 2-Way Combining

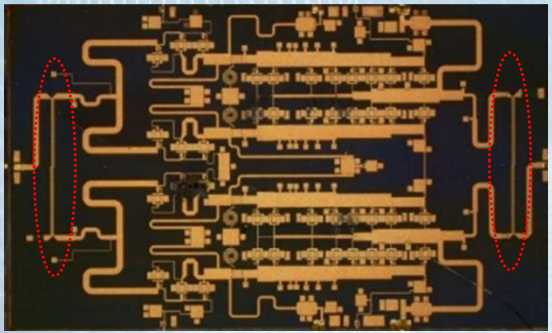
Balanced PA Design Procedure



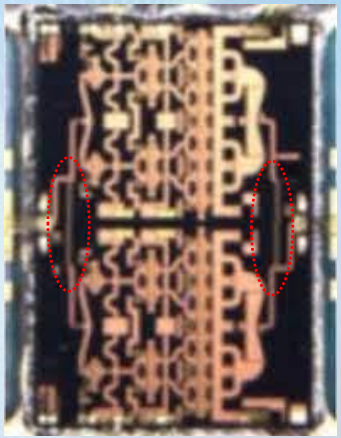
Hybrid is almost always a Lange Coupler

Balanced MMIC PA Examples

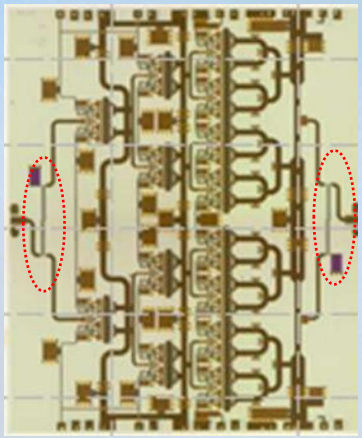
[7] 40W 4-18 GHz



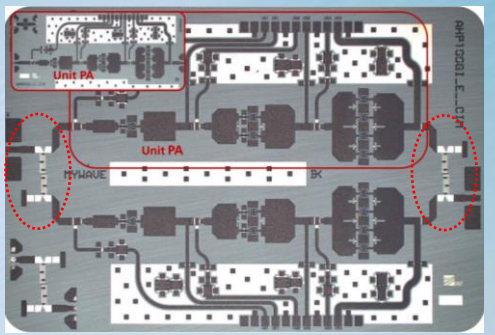
[8] 40W 27-31 GHz



[7] 25W 32-38 GHz

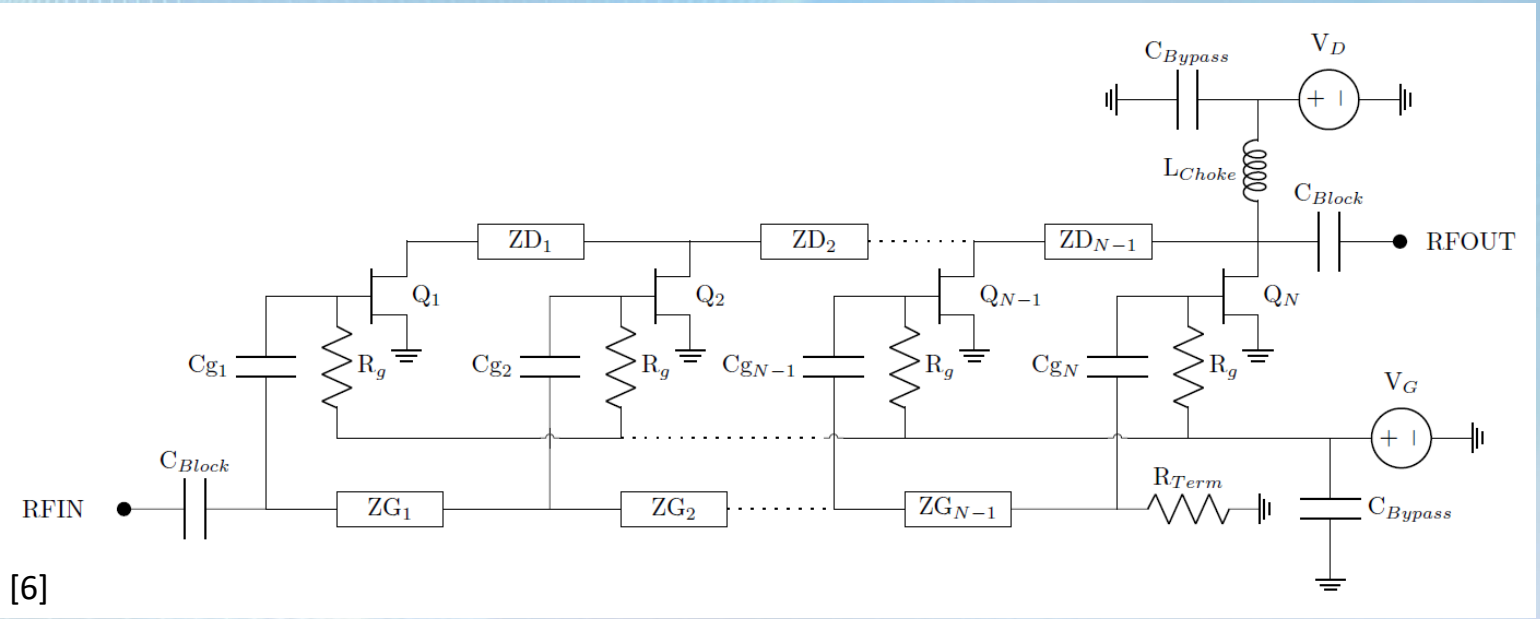


[9] 4W 74-80 GHz



= Lange Coupler

Nonuniform Distributed MMIC PA Topology

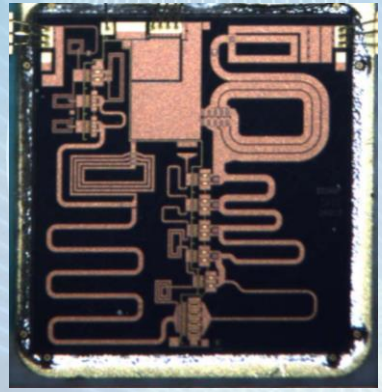


[6]

Why Distributed? Bandwidth and Load Tolerance

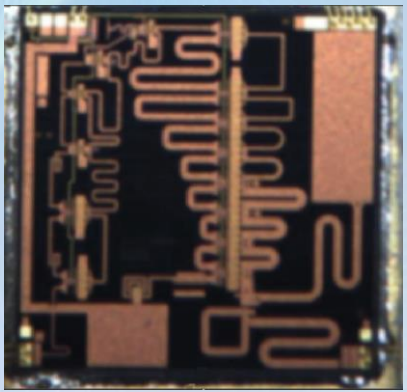
Nonuniform Distributed MMIC PA Examples

[10] 10W 1-8 GHz

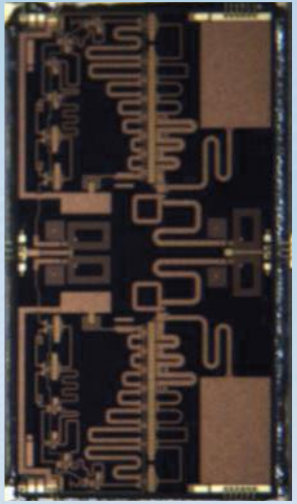


[11] 35W 4-18 GHz

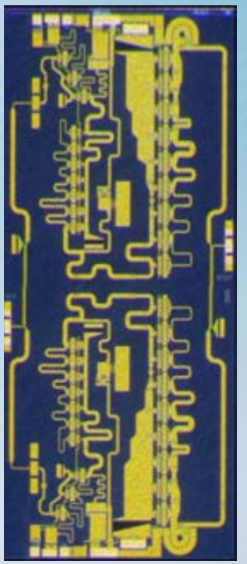
[12] 10W 2-20 GHz



[13] 20W 2-20 GHz



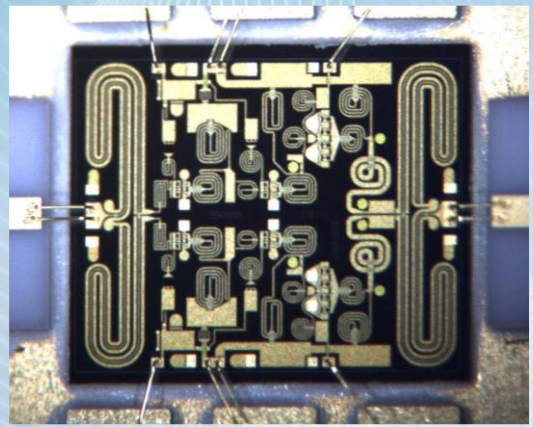
[14] 7-16W 16-40 GHz



*All die are not to scale

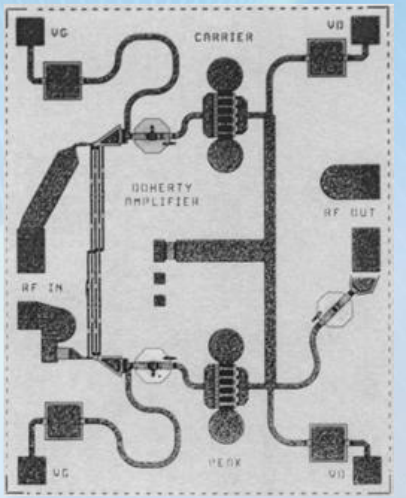
Other Topologies

Push Pull



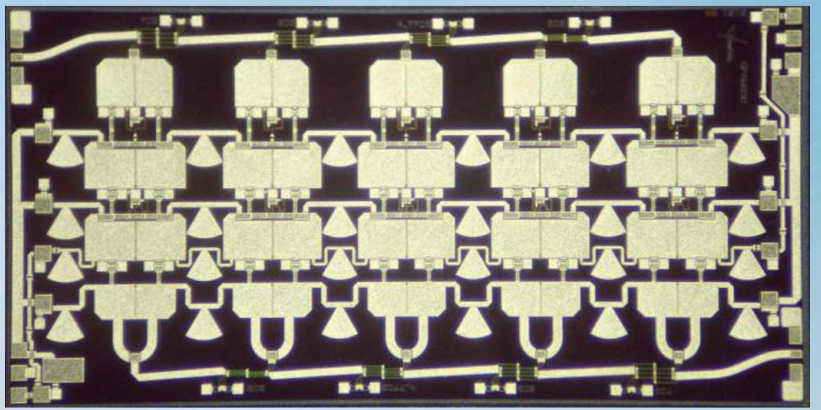
[15] 2W 6-12 GHz

Doherty



[16] 25dBm 17 GHz

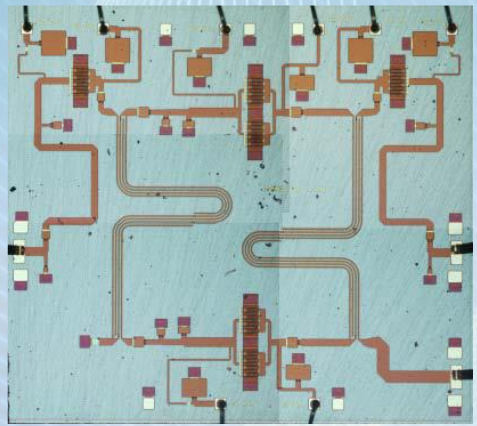
Serially Combined



[17] 2W 75-100 GHz

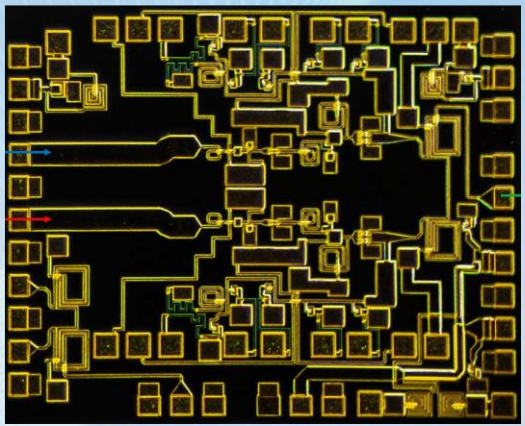
Other Topologies

Load Modulated Balanced Amplifier (LMBA)



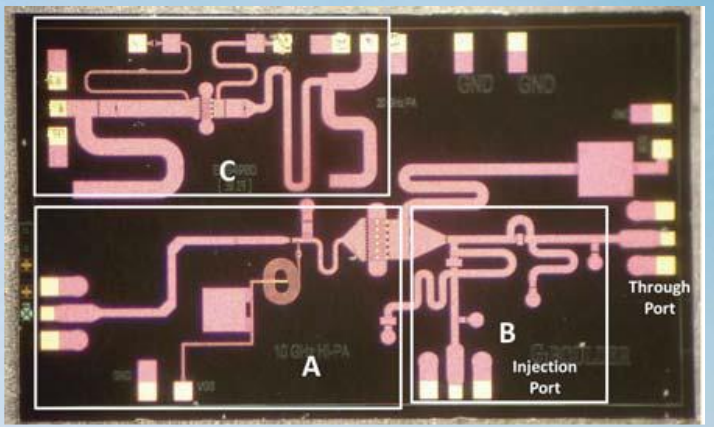
[18] 14W 8-9 GHz

Outphasing



[19] 0.2W 18-38 GHz

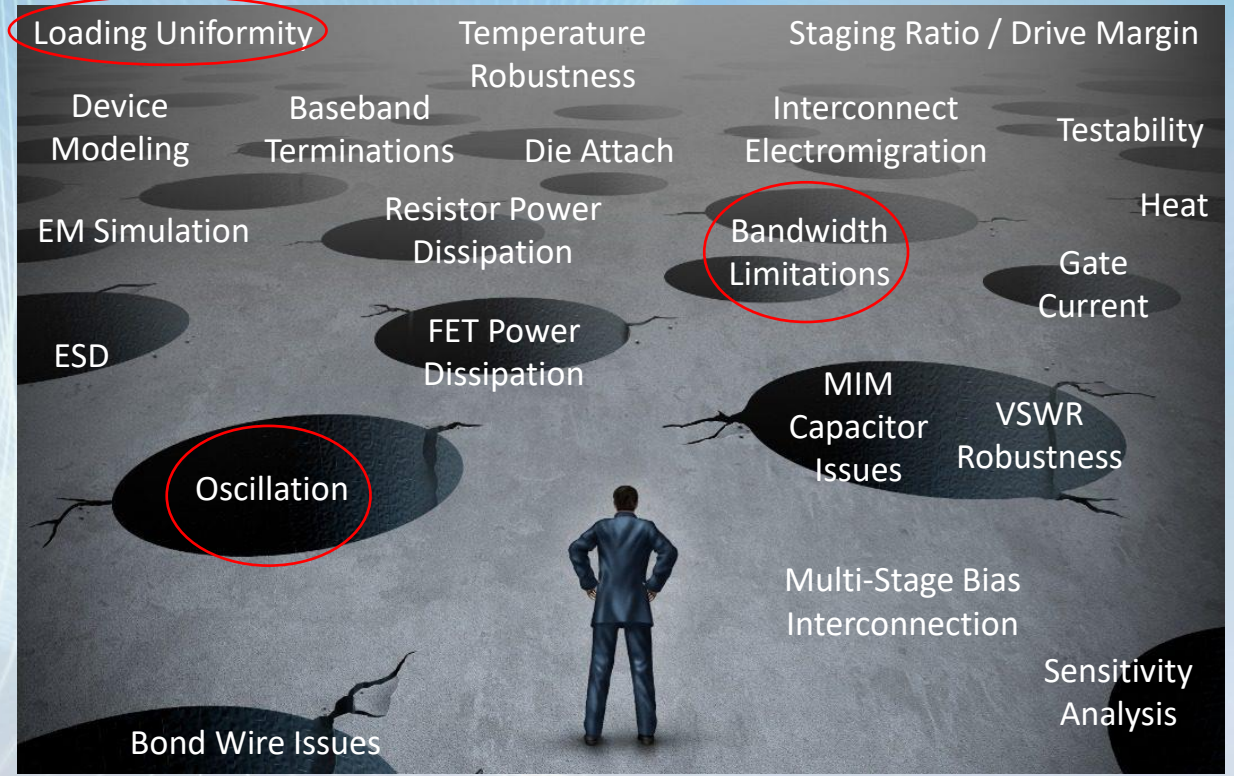
Harmonic Injection



[20] 4W 10 GHz

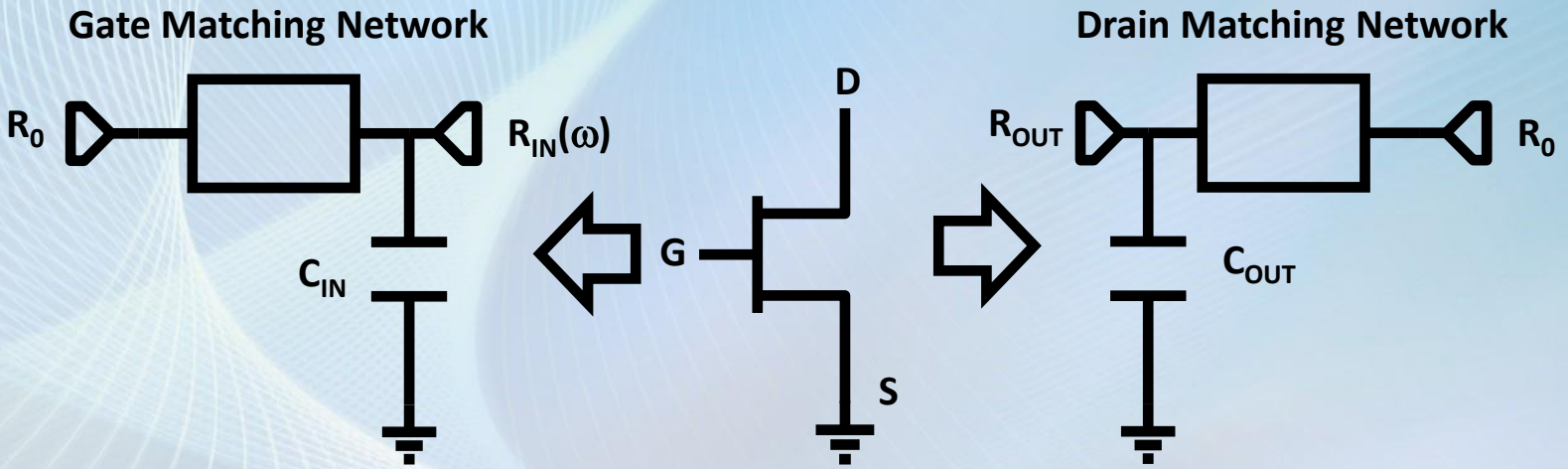
Not a complete list of topologies by any means!

Preventing Pain: Avoiding The Pitfalls



Understanding Bandwidth Limitations

- Input & output match targets are ~ R || C networks, specified in Ω·mm and pF/mm
- Output Example: **50 Ω·mm, 0.3 pF/mm (relatively constant vs. frequency)**



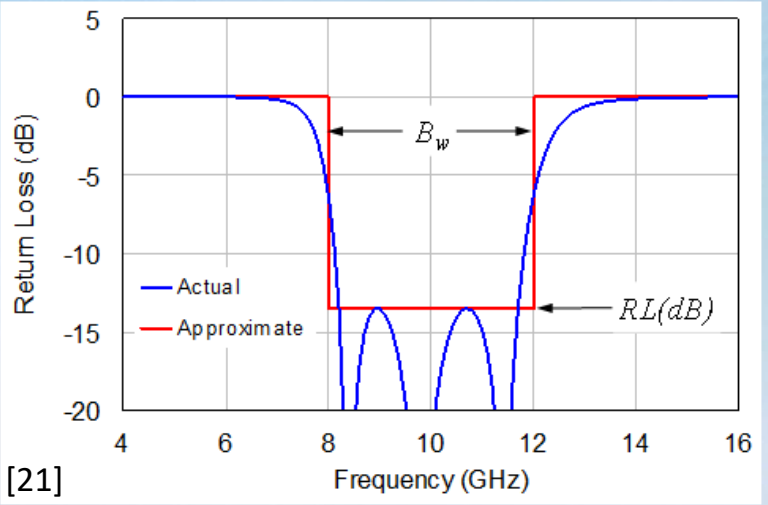
How does output matching target impact the matching bandwidth?

Bode Fano Limitation

- Bode-Fano limit for matching to a R || C network

$$\int_0^{\infty} \ln\left|1/\Gamma(\omega)\right| d\omega \le \frac{\pi}{R_p C_p}$$

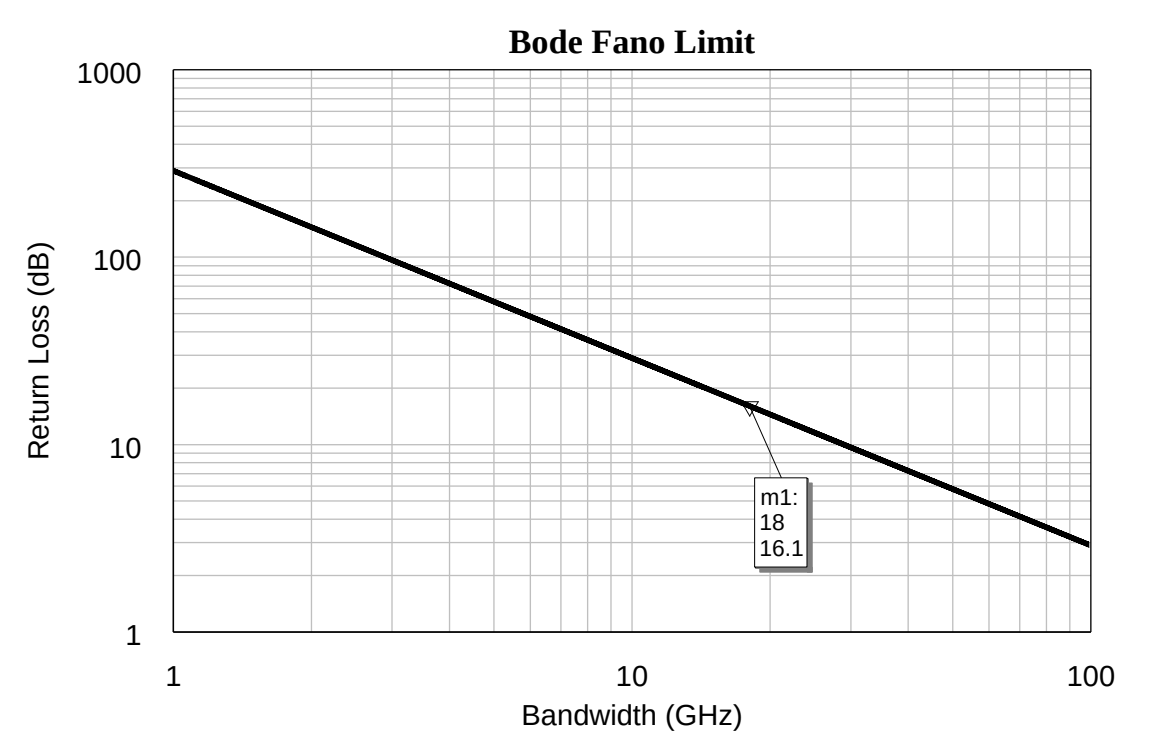
$$B_w < \frac{4.343}{R_p C_p RL(dB)}$$



[21]

Let's investigate a 2-20 GHz design

Best Case Return Loss vs. Bandwidth



Output Example: **50 Ω·mm, 0.3 pF/mm**

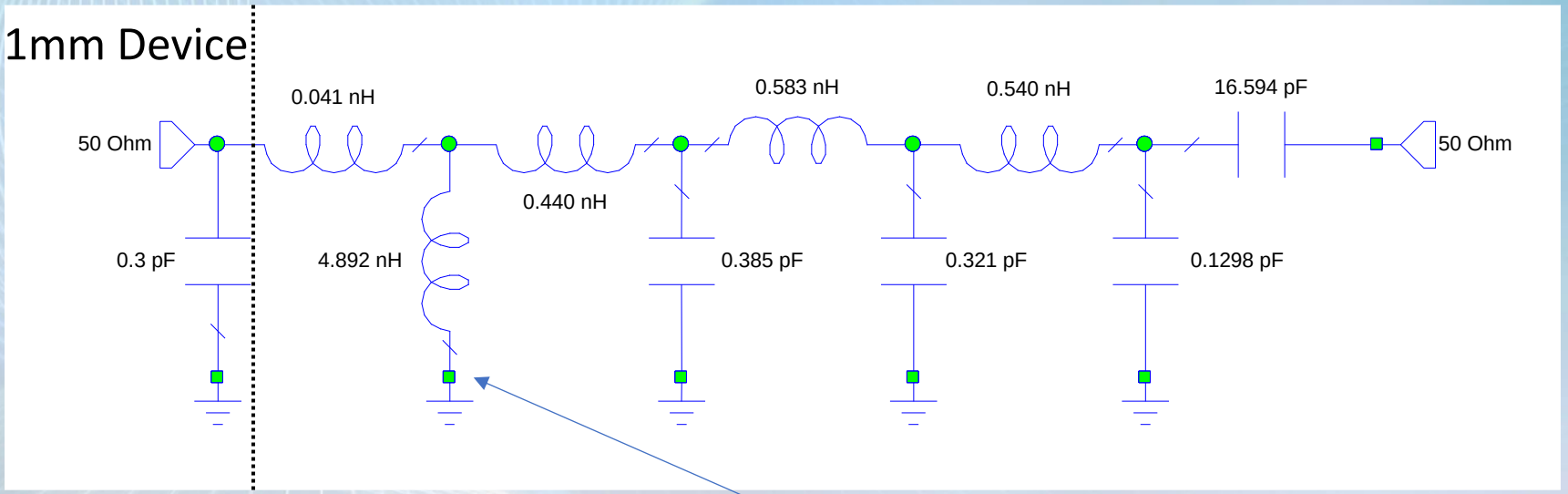
Bode Fano Caveat

- Over a given bandwidth, I should be able to get the same match for any amount of FET periphery, right?

"One must keep in mind, however, that the network will, in general, involve an ideal transformer, since both the terminations are assumed to be one ohm. The turns ratio of the transformer can be determined easily from the zero frequency behavior of the network." [22]

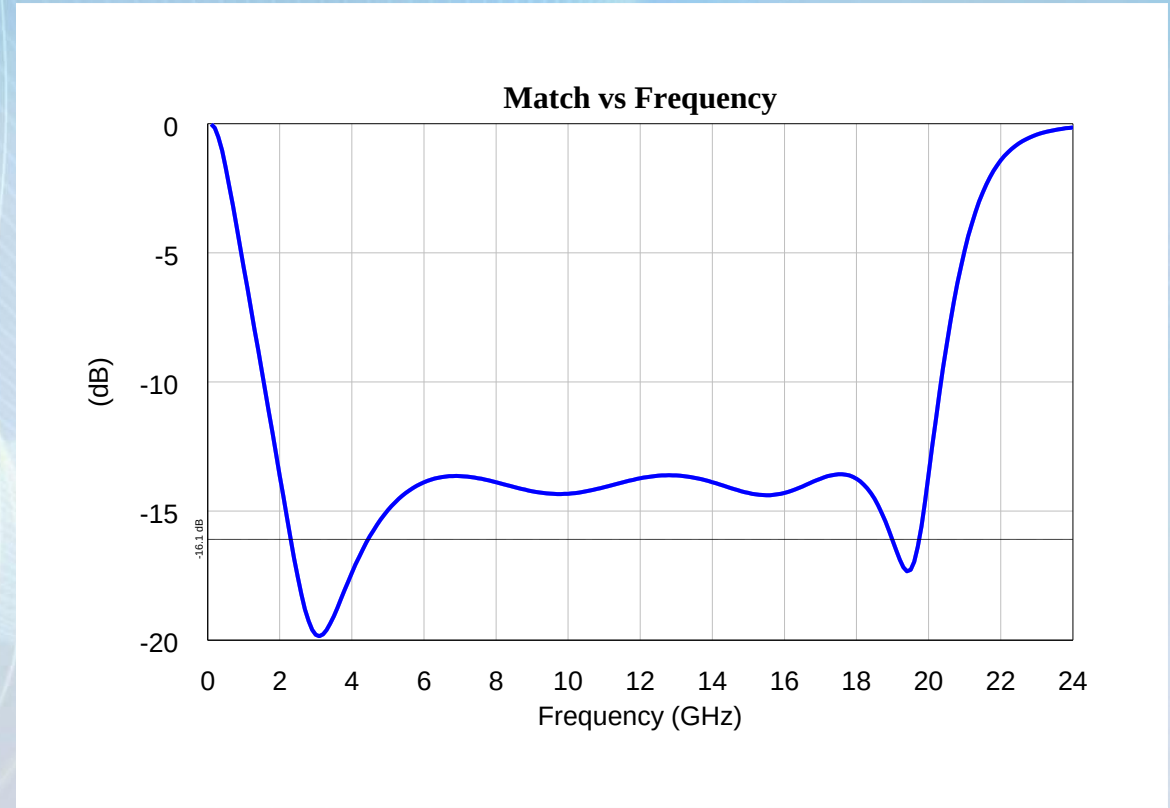
Example Reactive Matching Network

- Example, network design, 2-20 GHz, 1mm of periphery



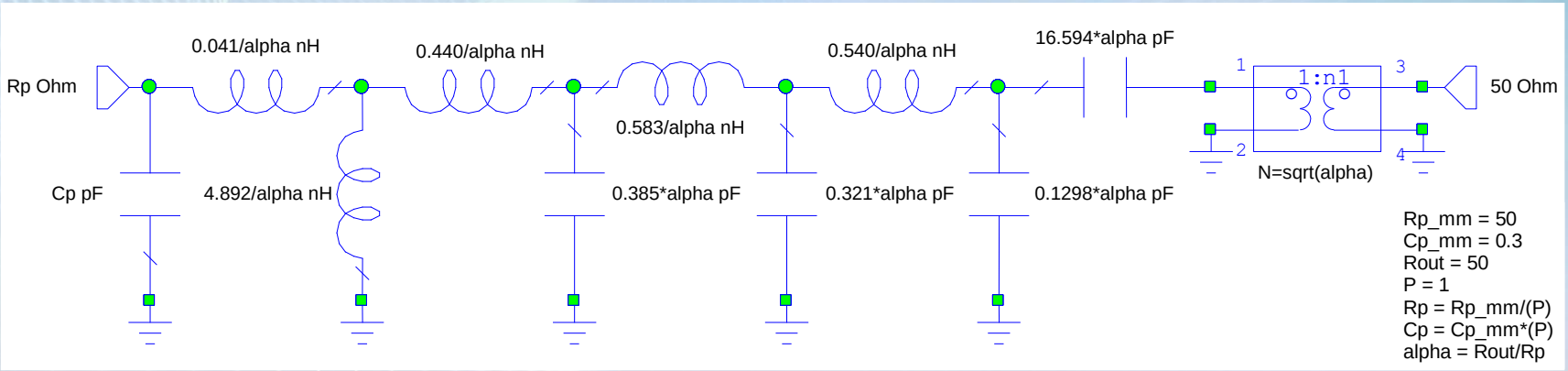
In practice, ground here is replaced with large bypass capacitor to apply drain voltage

Example Matching vs Frequency



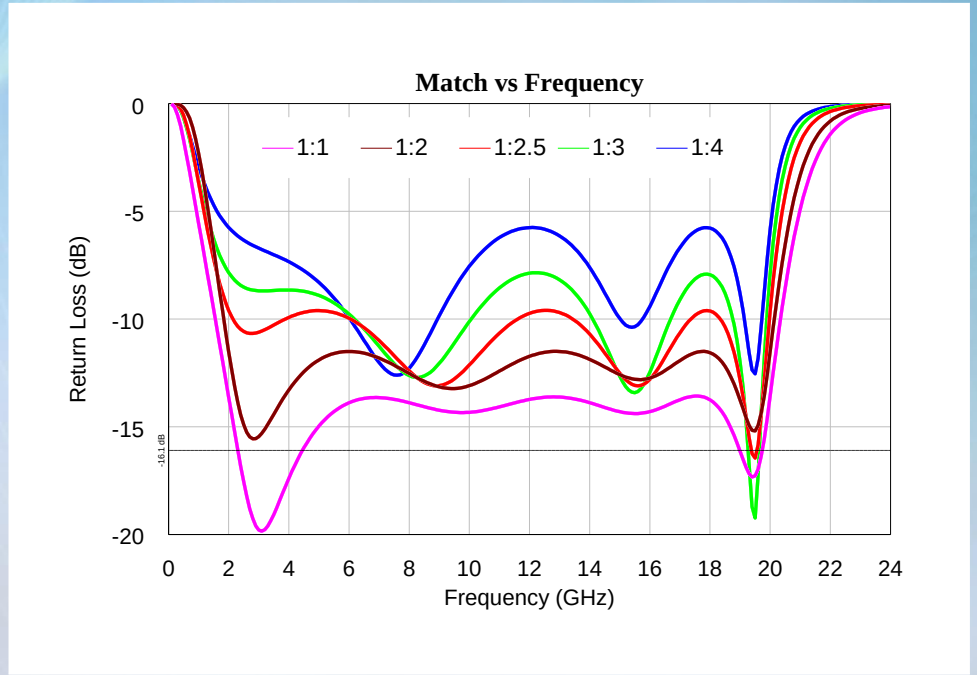
Network Scaling by Device Periphery

- Network design with scaling and transformer, works for any amount of periphery (presuming you can realize the values and transformer)
- As periphery increases, inductors divide, capacitors multiply, and a transformer is required to match resistance

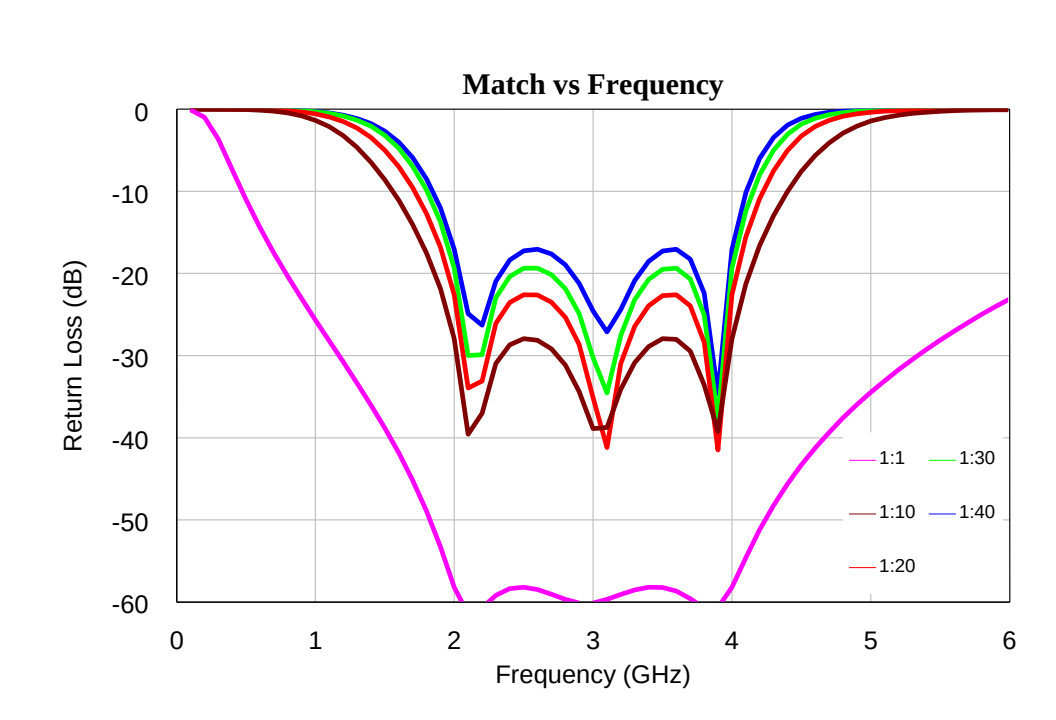


Practical Pitfall: No Transformer

- What happens if I don't use (have) a transformer?
- Network must be modified to do as "well as you can"
- Bandwidth degrades as Rp deviates from the output load
- But this doesn't affect my narrowband design… Not so fast!

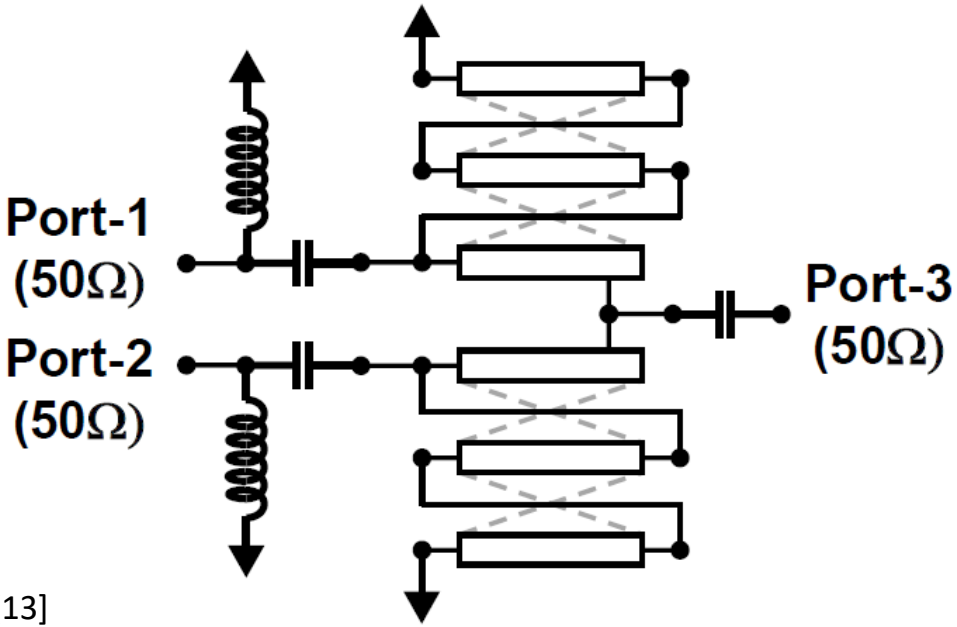


Narrowband Example Performance

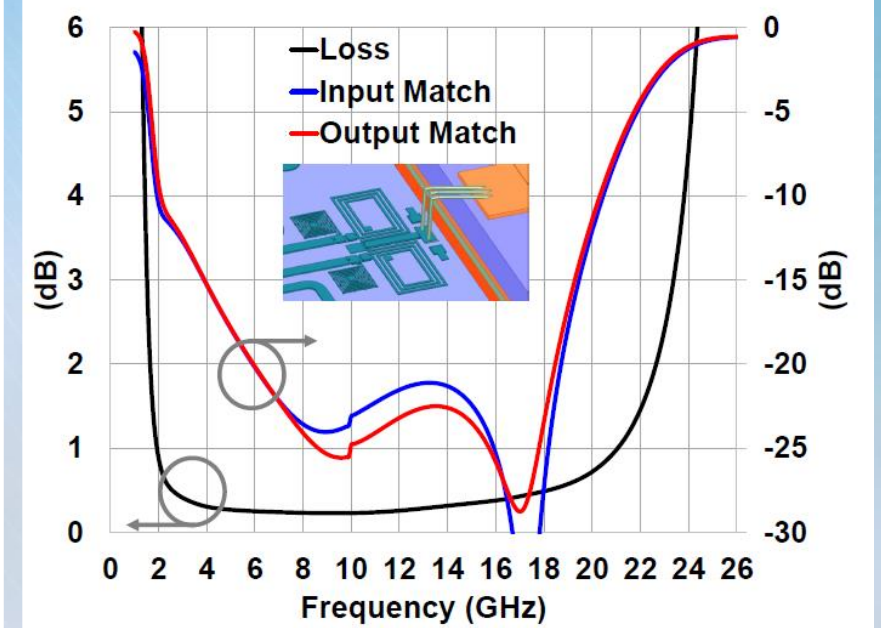


2-4 GHz Example, 1mm to 40mm Periphery

Trifilar Transformer Example (~1:2)



[13]

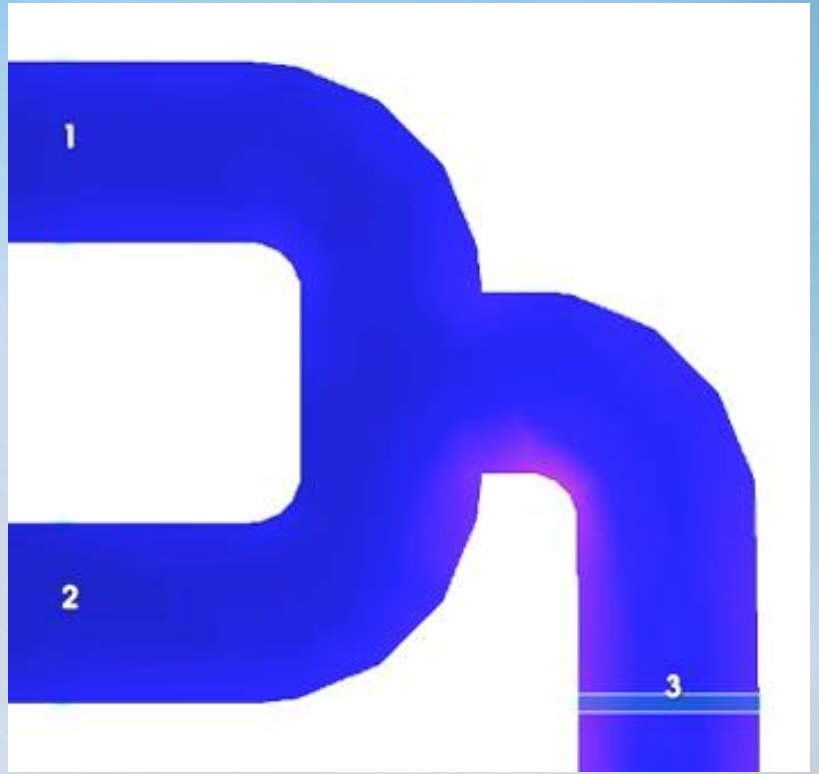


Summary

- Understand design limitations based on the chosen technology
- Transformers will enable you to come closer to the Bode-Fano limit
- Common broadband transformers include Ruthroff and Trifilar
- Narrowband transformers (e.g. quarter wave) often integrated into the matching network

Loading Asymmetry

- Port-1 and Port-2 are driven in-phase with equal power, Port-3 is terminated
- Current crowds around the bend, causing a difference in the loading at Port-1 vs. Port-2
- This would not show up with lumped element models of the bends and lines, EM Simulation is a must!



Efficient Power Combining

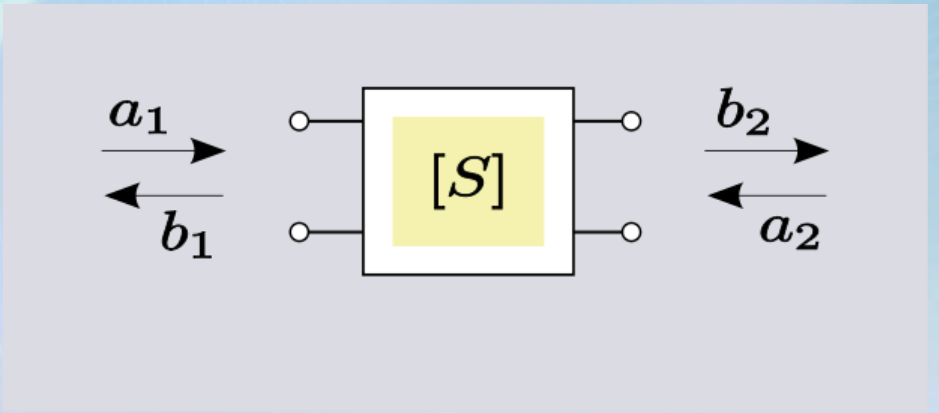
- Remember this from your microwave engineering class?

$$b = Sa$$

$$b = \begin{bmatrix} b_1 \\ \vdots \\ b_N \end{bmatrix} \quad a = \begin{bmatrix} a_1 \\ \vdots \\ a_N \end{bmatrix}$$

$$S = \begin{bmatrix} s_{11} & \cdots & s_{1N} \\ \vdots & \ddots & \vdots \\ s_{N1} & \cdots & s_{NN} \end{bmatrix}$$

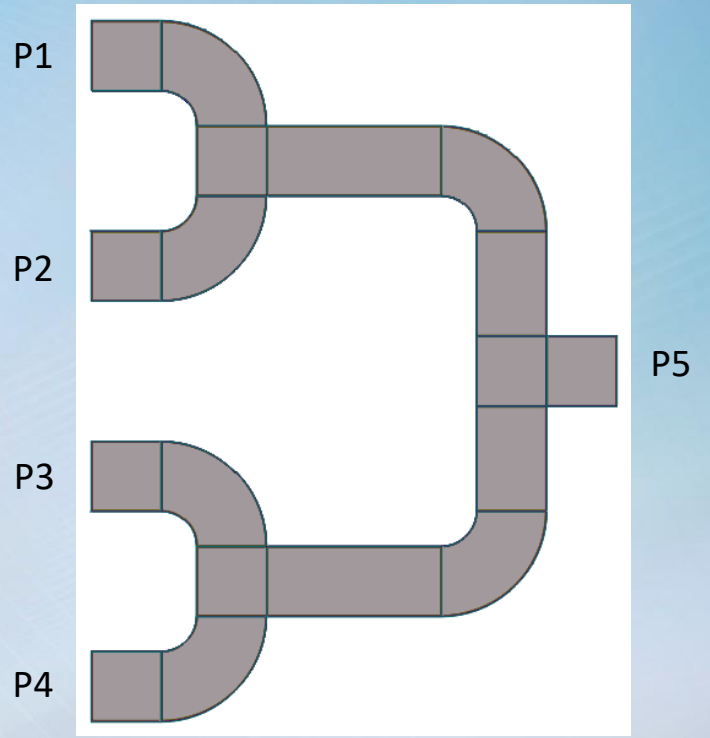
Two Port Network Example



a_i = incident power wave at port-*i*
b_i = reflected power wave at port-*i*
S = Scattering Parameter Matrix

Efficient Power Combining

- A greatly simplified 4-way combiner is shown on the right
  - Ports 1-4 are the input ports and port 5 is the output port
- To efficiently power combine, the input impedances at ports 1-4 to need be as uniform as possible
- What are the input impedances of this network at ports 1-4?
  - Hint: It's a function of the terminations and signals at all the ports



Efficient Power Combining

- Assume all incident power waves are equal (which implies driven port impedances are equivalent)

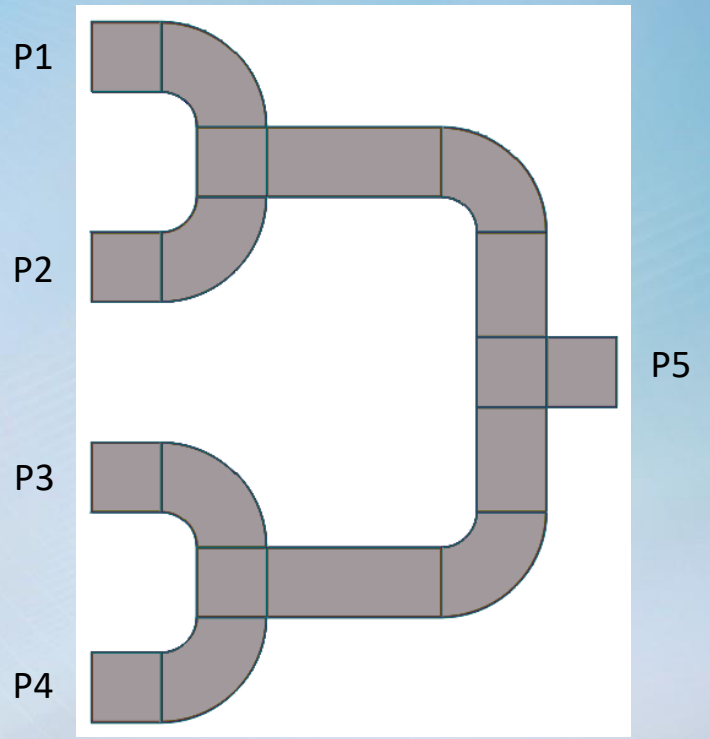
$$a_1 = a_2 = a_3 = a_4 = a_{inc}$$

- Assume no incident wave at the output port

$$a_5 = 0$$

- The equations simplify substantially

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \end{bmatrix} = \begin{bmatrix} s_{11} + s_{12} + s_{13} + s_{14} \\ s_{21} + s_{22} + s_{23} + s_{24} \\ s_{31} + s_{32} + s_{33} + s_{34} \\ s_{41} + s_{42} + s_{43} + s_{44} \\ s_{51} + s_{52} + s_{53} + s_{54} \end{bmatrix} a_{inc}$$



Efficient Power Combining

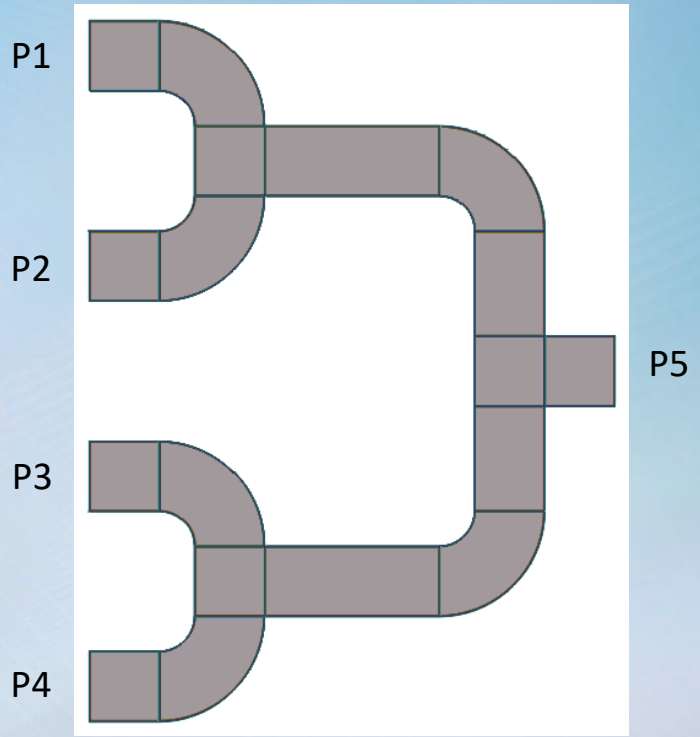
- The effective reflection coefficients at ports 1-4 are evaluated by dividing by the incident wave a_{inc}

$$\begin{bmatrix}\Gamma_1\\ \Gamma_2\\ \Gamma_3\\ \Gamma_4\end{bmatrix} = \begin{bmatrix}b_1/a_{inc}\\ b_2/a_{inc}\\ b_3/a_{inc}\\ b_4/a_{inc}\end{bmatrix} = \begin{bmatrix}s_{11}+s_{12}+s_{13}+s_{14}\\ s_{21}+s_{22}+s_{23}+s_{24}\\ s_{31}+s_{32}+s_{33}+s_{34}\\ s_{41}+s_{42}+s_{43}+s_{44}\end{bmatrix}$$

- The input impedances are then easily evaluated

$$Z_i = \frac{Z_0^* + Z_0\Gamma_i}{1-\Gamma_i} \qquad Z_0 = \text{Port Impedance}$$

- This equation is valid for complex port impedances



Efficient Power Combining

- Now we have a direct relationship between the S-parameters of the network and the load input impedance at the driven ports
- This impedance can be evaluated quickly in modern microwave circuit simulators
- A simple technique for evaluating power as a function of load is the Cripps Technique [24]

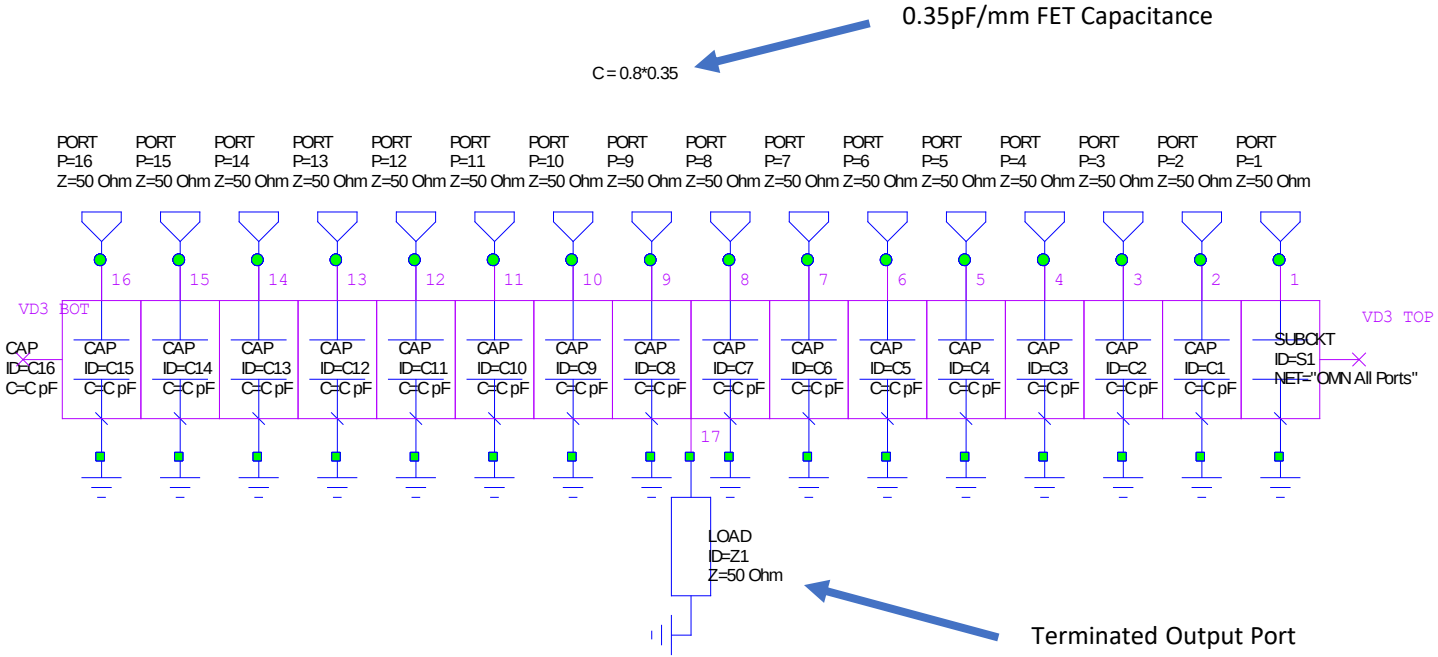
P_{max}	= Maximum Power
R_{opt}	= Optimal Load (Resistive)
V_{max}	= Maximum Voltage
I_{max}	= Maximum Current
Z_L	= Load Impedance
Y_L	= Load Admittance
*	= Complex Conjugate

- In this technique the device has an optimum intrinsic load and maximum output power
- The device voltage or current limits when not optimally loaded, degrading the power
- This power estimate can now be calculated for each loaded FET and the balance can be optimized

$$V_{\max} = \sqrt{2P_{\max}R_{opt}} \qquad I_{\max} = \sqrt{\frac{2P_{\max}}{R_{opt}}}$$

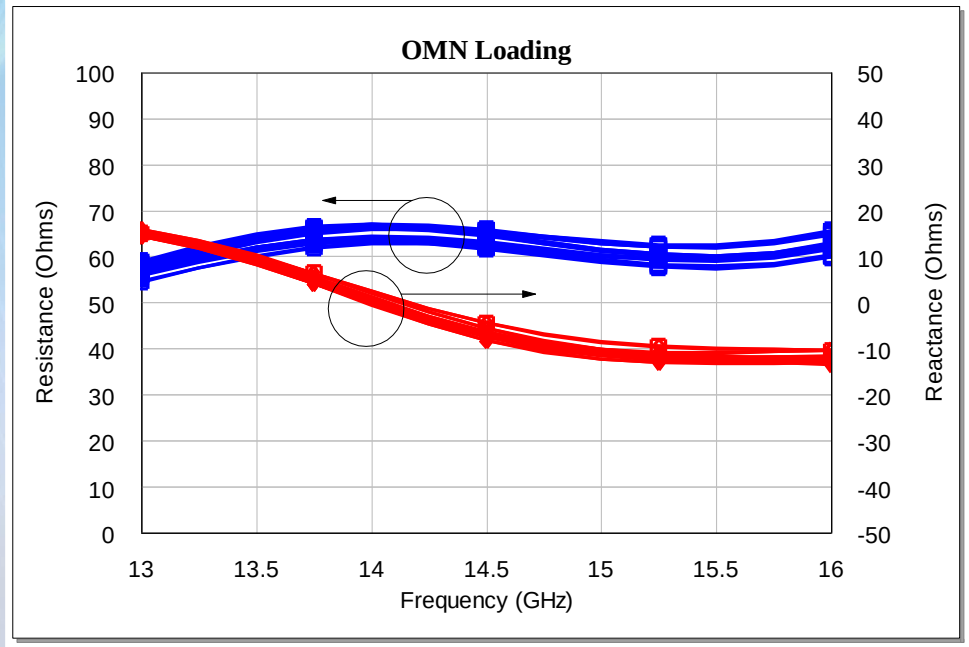
$$P_{out} = \frac{1}{2}\min\left\{\mathrm{Re}\left(I_{\max}^2 Z_L\right), \mathrm{Re}\left(V_{\max}^2 Y_L^*\right)\right\}$$

Example Schematic For Analysis



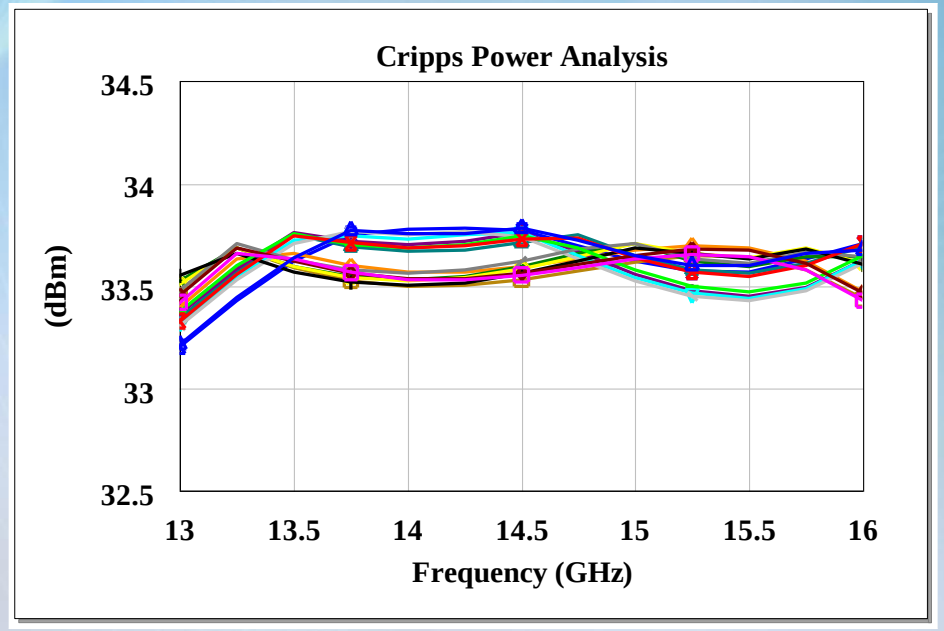
Intrinsic Loading

- Impedance for all ports shows small variation
  - Resistance and reactance variation ~ +/- 2.5Ω
- Variation is minimized by using physical layout asymmetries to improve electrical symmetry



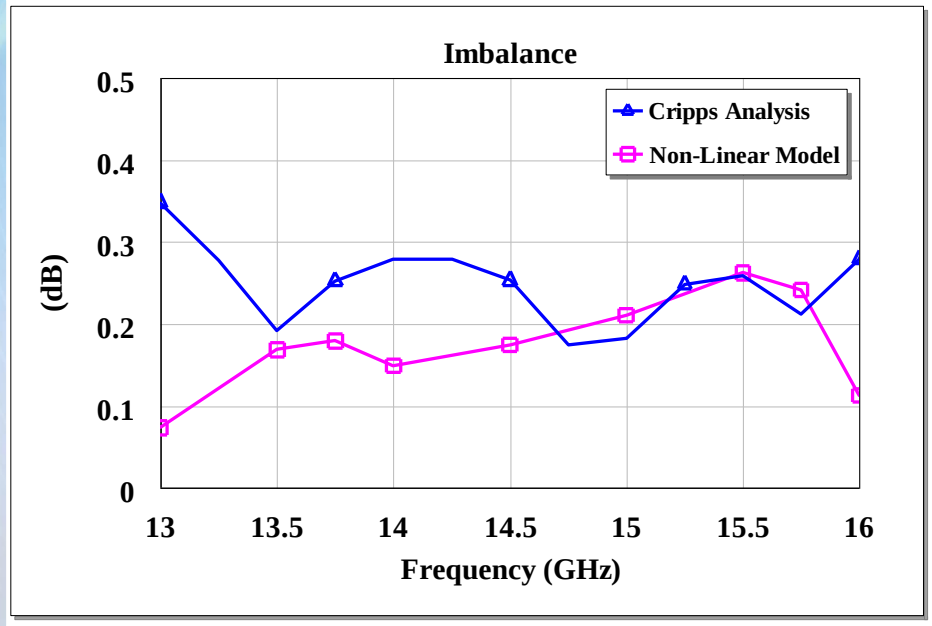
Intrinsic Loading Impact on Cripps Power

- Analysis assumes maximum power of 33.8dBm / FET (3W/mm)
- Linear analysis of power balance shows less than 0.3dB variation in FET output power (in-band)
- In my experience, power balance is usually as good or better when analyzed with a non-linear model



Comparison with non-linear model analysis

- Analysis with non-linear model shows similar power balance
- So why use the linear analysis?
- Non-linear analysis takes ~2 minutes to converge (16 points)
- Linear analysis takes less than 1 second to converge
- Note: Apply same techniques to other amplifier stages, not just output stage



Summary

- Minimize load variation to maximize power combining efficiency
- Load variation and impact on output power can be analyzed with linear techniques
- Use physical asymmetry to enforce electrical symmetry

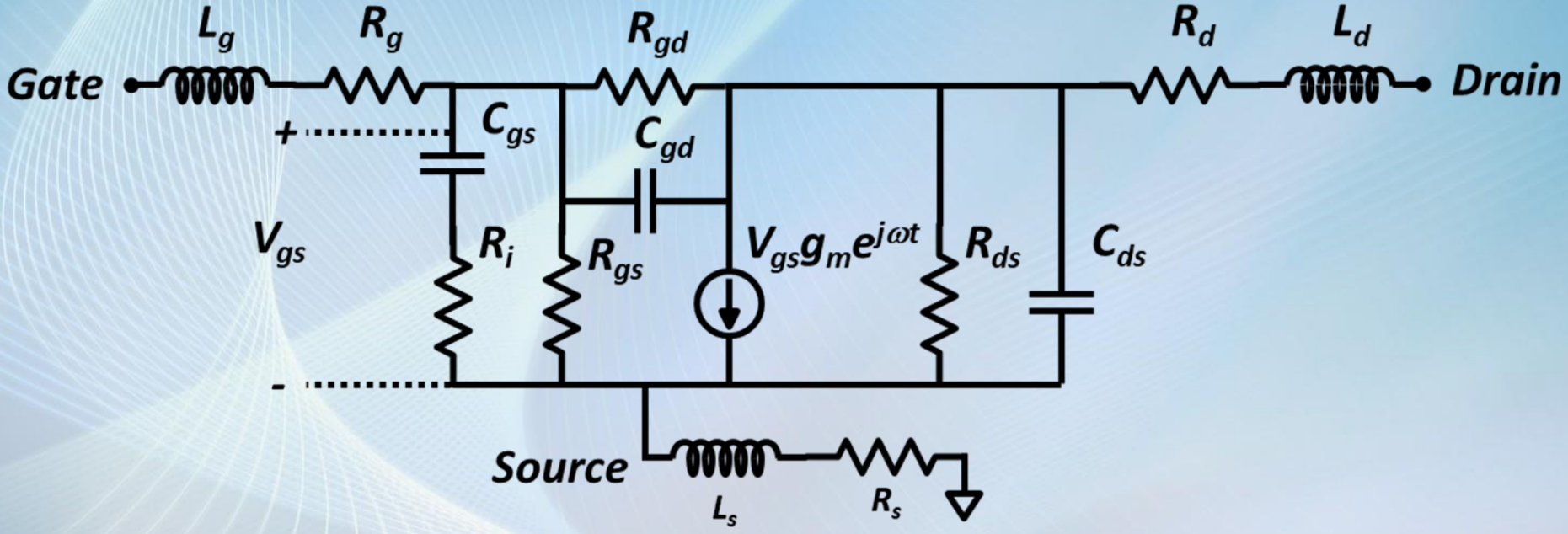
Preventing Oscillations

- Amplifier designers need stability analysis techniques during the design synthesis phase
- Rapid stability analysis techniques are highly desirable, which is why use of K-factor and mu-factor is so prevalent
- However, K-factor and mu-factor fail to reveal instabilities in multi-stage or parallel combined amplifiers

Preventing Oscillations

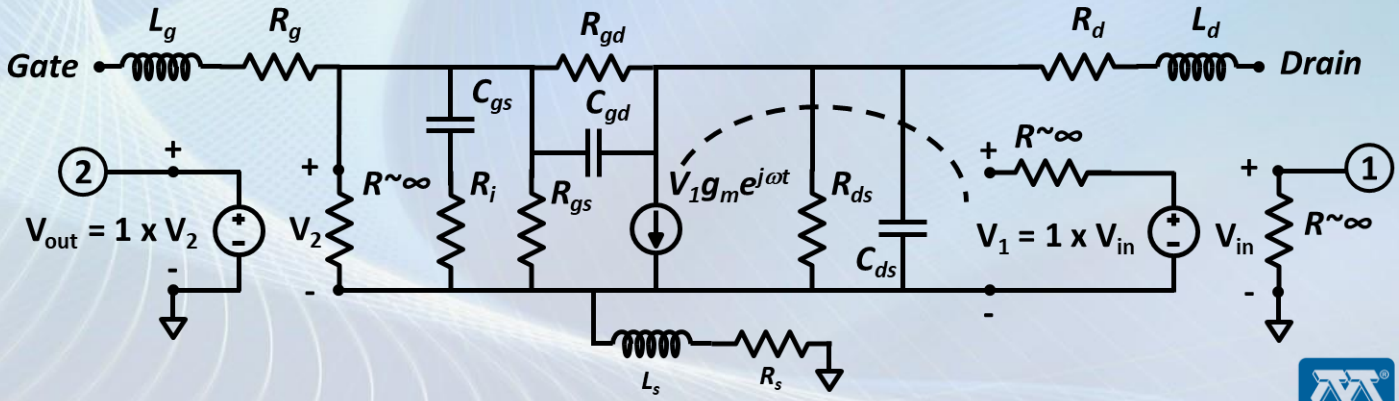
- Loop gain and Normalized determinant function (NDF) overcome the limitations of K-factor and mu-factor
- NDF and Stability Envelope fail to provide an indication of stability margin
- Loop gain provides an indication of stability margin, but requires additional odd mode loop analysis
- Both loop gain and NDF are slow analysis techniques which are not useful for design synthesis.

Standard Linear FET Model



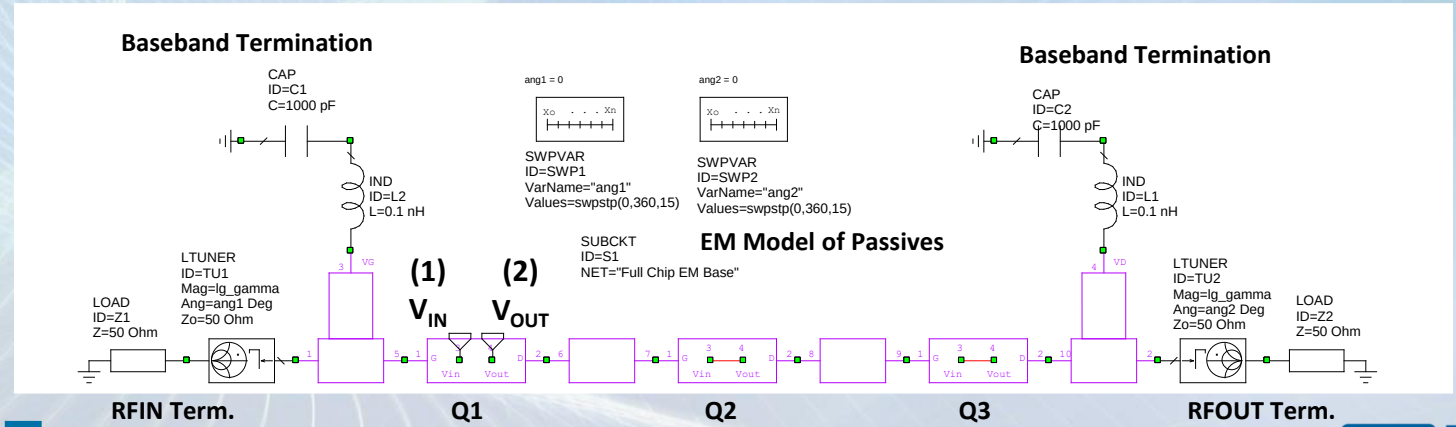
Loop Gain Stability Analysis Review

- Linear FET model typically used for loop gain evaluation
- Voltage gain from port-1 to port-2 is loop gain $G_{loop} = V_2 / V_1$
  - V_1 is injected at the device current source and resulting V_2 is measured at the intrinsic input to the device (V_{gs})
- Impedances at Gate and Drain impact G_{loop}
- Shorting port 1 to port 2 causes the model to degenerate to the standard linear FET model



Loop Gain Stability Analysis Review

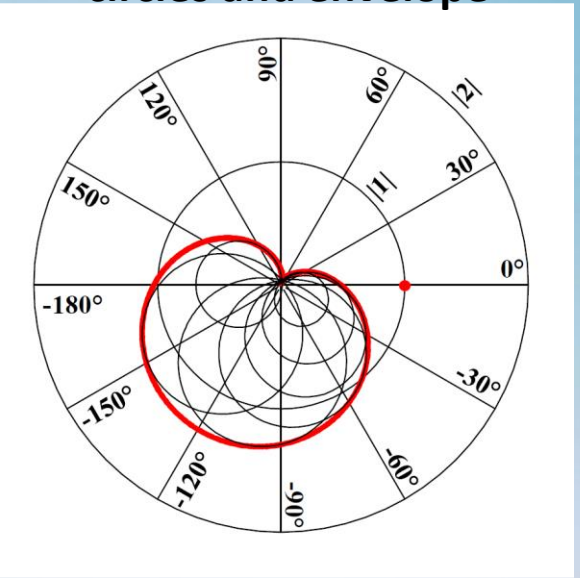
- Loop gain FET model is embedded in full PA
- RFIN and RFOUT terminations are swept, G_{Loop} is evaluated for each combination at each frequency
- Devices not under test have V_{in} and V_{out} shorted together
- Source not shown on device models below (grounded inside the subckt)



Loop Gain Stability Analysis Review

- At a specific frequency, for a fixed RFIN termination and varying RFOUT termination phase, the loop gain traces a circle in the complex plane
- Evaluating for a different fixed RFIN termination results in a different circle
- The collection of circles shows the loop gain behavior as a function of RFIN and RFOUT termination

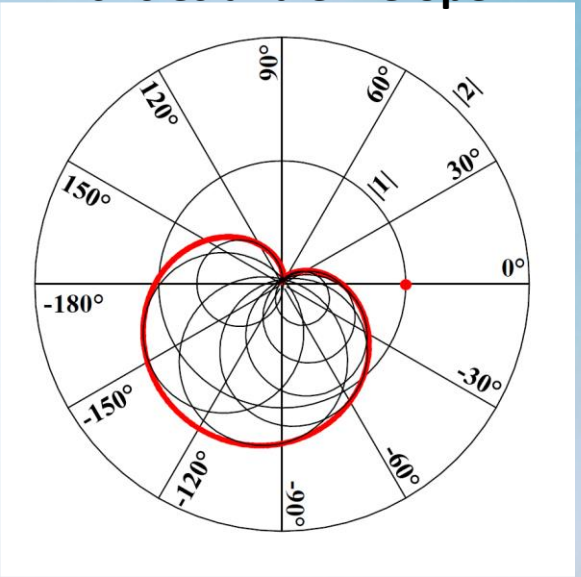
Example loop gain circles and envelope



Motivation for Envelope Technique

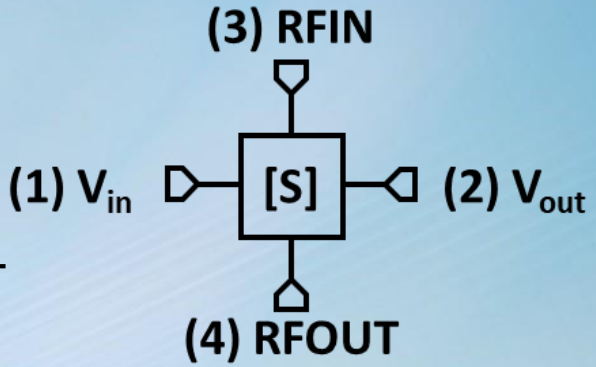
- Designers don't particularly care about the circles themselves
- They care about the envelope of the circles, because that defines the phase margin
- Phase Margin: Minimum Phase where $|G_{loop}| >= 1$
- Phase margin provides an indication of stability margin based on control theory, often 30° is acceptable
- Direct evaluation of the envelope would be highly desirable

Example loop gain circles and envelope



Loop Gain Envelope Derivation

- Consider the loop gain FET embedded in a MMIC amplifier, with simplified schematic shown to the right



- The loop gain ports (V_{in}, V_{out}), RFIN and RFOUT ports are interconnected by a 4-port network

- The 4-port S-parameters [S] are reduced to 2-port S-parameters by applying the RFIN termination (Γ_S) and the RFOUT termination (Γ_L) mathematically

Loop Gain Envelope Equations [23]

- The loop gain is a function of the reduced 2-port S-parameter network

$$G_{Loop} = \frac{\bar{s}_{21}}{2}$$

- Lots of math allows the loop gain to be expressed as

$$G_{Loop} = \frac{c_1\bar{\Gamma}_S + c_2\bar{\Gamma}_L + c_3\bar{\Gamma}_S\bar{\Gamma}_L + c_4}{d_1\bar{\Gamma}_S + d_2\bar{\Gamma}_L + d_3\bar{\Gamma}_S\bar{\Gamma}_L + d_4}$$

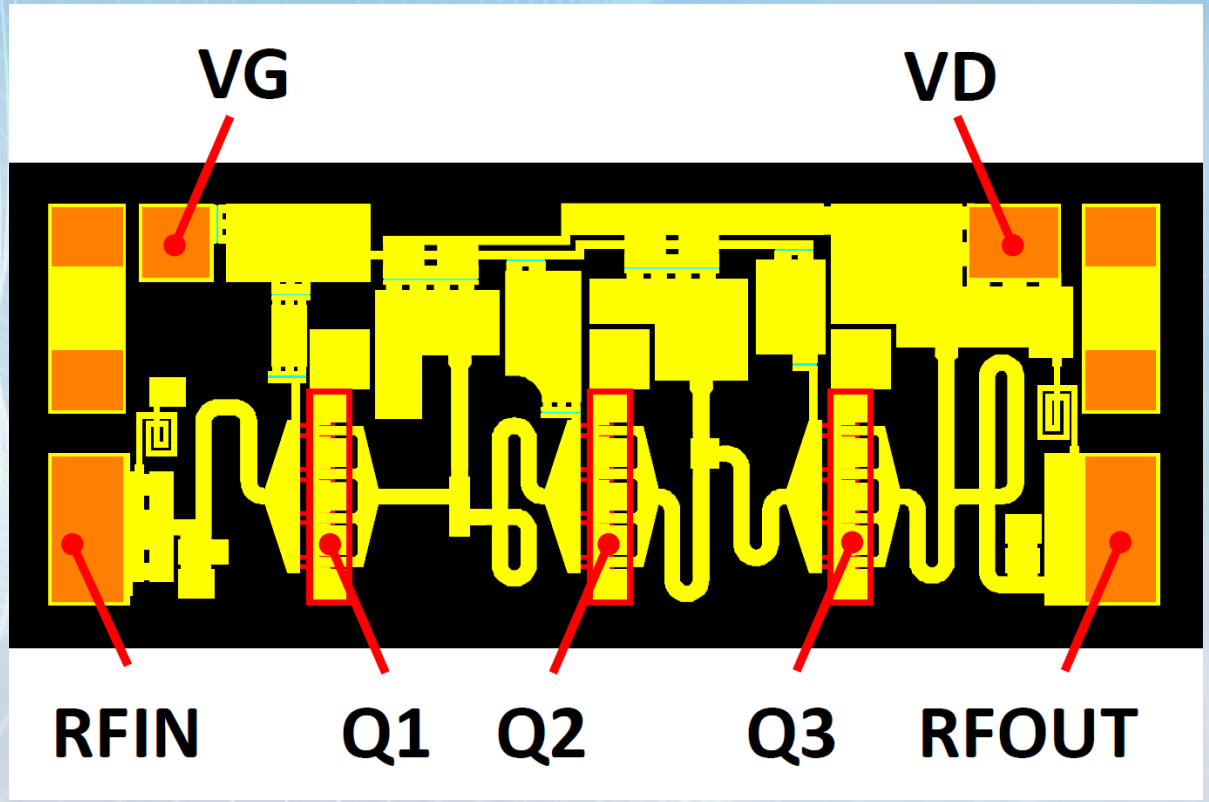
Derivation

- The key takeaway is this mathematical form is identical to the NDF form, therefore the solution to the NDF stability envelope can be applied to loop gain to calculate the loop gain envelope

- Therefore, the loop gain envelope at a particular frequency is solved mathematically by evaluating the phase of Γ_L for each phase of Γ_S that results in a point on the envelope of all possible loop gains

- Furthermore, this is all now automated in Microwave Office!

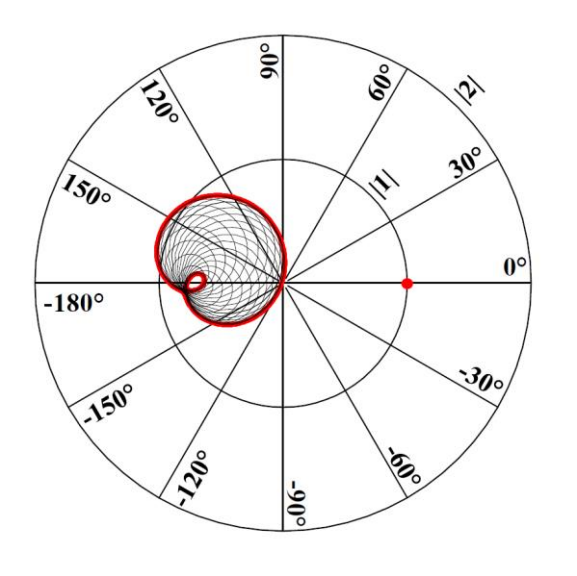
Multi-stage MMIC PA Example



Multi-stage MMIC PA Example

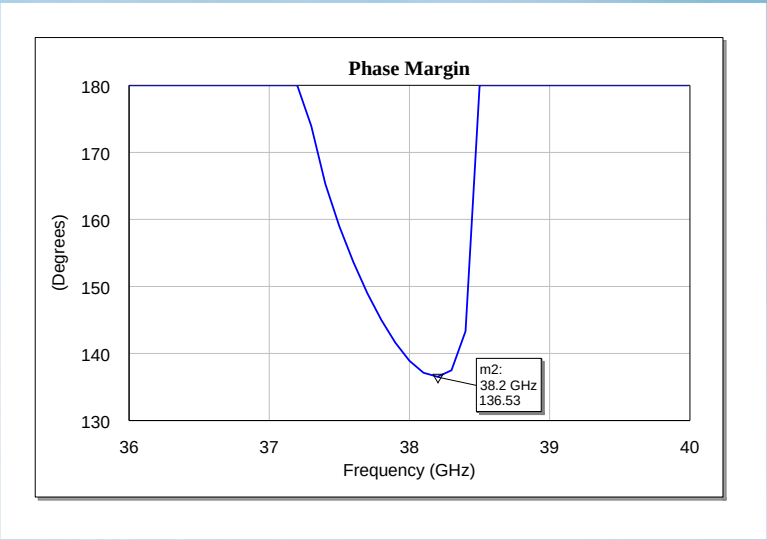
- Loop gain circles shown in black, loop gain envelope shown in red
- Phase margin is minimum phase at which $|G_{Loop}| = 1$
- Phase margin ~136°

38 GHz Loop Gain (Q1)



Phase Margin Evaluation

- Phase Margin can be easily evaluated in software from the loop gain envelope
- For a given frequency, find the minimum phase where $|G_{Loop}| >= 1$. That is the phase margin.
- An example for Q1 vs. frequency is shown to the right
- AWR also has a gain margin measurement



Analysis Speed Comparison

- 0.1 – 50 GHz, 0.1 GHz steps, 100 phase points, single device
- Traditional Loop Gain: 207.39 seconds
- AWR Loop Gain Envelope: 0.7 seconds
- 1000 phase points only increased LGE analysis time to 1.28 seconds
- Analyzing all three devices with 1000 phase points only increased loop gain envelope analysis time to 3.11 seconds! The traditional method would have taken well over 600 seconds for only 100 phase points!

Summary

- Stability is critical, oscillation ruins your MMIC!
- Many techniques are available, Loop Gain Envelope is one useful for both synthesis and analysis of designs
- No matter which technique you use, make sure you understand the assumptions and limitations

Final Summary

- Compared GaAs vs. GaN, to assist technology selection
- Presented several common MMIC PA topologies
- Discussed bandwidth limitations, loading uniformity and stability analysis
- Go design a MMIC, it's a lot of fun! Always be looking to learn!

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