Interns

Hands-on tra

Conducted by IEEE SSCS K

Day	Topics
Day 1	Orientation + FPGA Basics
Day 2	FPGA Architecture (Spartan-6, Artix-7)
Day 3	HDL Basics
Day 4	Combinational Logic Design
Day 5	Sequential Logic Design
Day 6	FSM Concepts and Design
Day 7	
Day 8	Design Flow in ISE
Day 9	Pin Constraints & Timing
Day 10	Mini System Design
Day 11	Memory Blocks
Day 12	FPGA Board Setup
Day 13	GPIO Interfacing
Day 14	Display Interface
Day 15	Project
Day 16	Project Presentation
Day 16	Project Presentation

ship on Digital System Design Using FPGA

ining with Xilinx ISE, Spartan-6 & Artix-7 boards

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Hands-on Activities			Mode
Introduction, digital systems overview, FPGA vs microcontroller vs ASIC			Offline
Study of CLBs, LUTs, Flip-Flops, slices, IO blocks			Offline
Verilog/VHDL syntax, modules, behavioral vs structural modeling Design: 4-bit adder, mux, demux – simulate using ISE			Offline
Design: D, T, JK FF, counters, shift registers – simulate and test			Offline
Mealy/Moore FSMs, state diagrams			Offline
Implement: Traffic light controller, sequence detector Project creation, HDL entry, synthesis, implementation Create .ucf files for Spartan-6/Artix-7, setup pin mapping			Online
Stopwatch or ALU – simulate and generate bitstream			Online
Configure Spartan-6 / Artix-7 board, download bitstream			Online
Blink LEDs, read switches – debouncing			Online
7-segment control, binary to BCD conversion			Online
Implement ROM, dual-port RAM using case and array methods			Online
UART Tx/Rx design, simulation, interfacing on board			Online
Choose: Calculator, Timer, FSM-based lock, UART terminal			Online
RTL design, testbench, functional sim Fit design for Spartan-6 / Artix-7, verify in ISE Debug with LEDs/7-segment/UART			Online
Final Project			Offline
Final presentation, report submission Set 1			Offline
Final presentation, report submission Set 2			Offline