IEEE Solid-State Circuits Society Distinguished Lecturer Talk

The SSCS DL Program provides experts in the Society's areas of interest to speak at chapter meetings and regional seminars. Lecturers, who serve for overlapping two-year terms, are deeply knowledgeable and excellent communicators. Their range of topics focuses on current IC activities, such as technology direction; novel devices, memories, and radio technology; high-speed and precision data converters; wireline and on-chip communication; low-noise clocking, and low power design. SSCS chapters are encouraged to benefit from DLs' expertise. The Columbus IEEE Joint Chapter of SSC &CAS Societies, SSC37/CAS04 is happy to host Prof. Shreyas Sen from Purdue University for the first of this year's DL talks.

Recent Circuit Advances for Resilience to Side-Channel Attacks

Date & Time: Thursday, October 2, 2025 • 6:00 – 8:00 PM EST
Location (In-person):
1275 Kinnear Rd
Columbus, OH 43228
Register Here: https://events.vtools.ieee.org/m/503548
Virtual Option (Google Meet):
Video call link: https://meet.google.com/vsa-xxwj-jva
Or dial: +1 470-485-9116 PIN: 920 754 535#
More phone numbers: https://tel.meet/vsa-xxwj-jva?pin=2286164210666

Abstract: Computationally secure cryptographic algorithms, when implemented on physical hardware, leak correlated physical signatures (e.g. power supply current, electromagnetic radiation, acoustic, thermal) which could be utilized to break the crypto engine. Physical-layer countermeasures, guided by understanding of the physical leakage, including circuit-level and layout-level countermeasures promise strong resilience by reducing the physical leakage at the source of the leakage itself. The past decade has seen significant advancements in circuit-level countermeasures, advancing resilience to side-channel attacks. In this talk, we will cover the fundamentals of the leakages and how each countermeasure increases resilience, by diving into the working mechanism of each and comparing the pros and cons of these techniques. The talk concludes by highlighting the open problems and future needs of this field.

Biography: Shreyas Sen is an Elmore Associate Professor of ECE & BME, Purdue University. His current research interests span mixed-signal circuits/systems and electromagnetics for the Internet of Bodies (IoB) and Hardware Security. He has authored/co-authored 3 book chapters, over 200 journal and conference papers and has 25 patents granted/pending. Dr. Sen serves as the Director of the Center for Internet of Bodies (C-IoB) at Purdue. Dr. Sen is the inventor of the Electro-Quasistatic Human Body Communication (EQS-HBC), or Body as a Wire technology, for which, he is the recipient of the MIT Technology Review top-10 Indian Inventor Worldwide under 35 (MIT TR35 India) Award in 2018 and Georgia Tech 40 Under 40 Award in 2022. To commercialize this invention Dr. Sen founded Ixana and serves as the Chairman and CTO and led Ixana to awards such as 2x CES Innovation Award 2024, EE Times Silicon 100, Indiana Startup of the Year Mira Award 2023, among others. His work has been covered by 250+ news releases worldwide, invited appearance on TEDx Indianapolis, NASDAQ live Trade Talks at CES 2023, Indian National Television CNBC TV18 Young Turks Program, NPR subsidiary Lakeshore Public Radio and the CyberWire podcast. Dr. Sen is a recipient of the NSF CAREER Award 2020, AFOSR Young Investigator Award 2016, NSF CISE CRII Award 2017, Intel Outstanding Researcher Award 2020, Google Faculty Research Award 2017, Purdue CoE Early Career Research Award 2021, Intel Labs Quality Award 2012 for industrywide impact on USB-C type, Intel Ph.D. Fellowship 2010, IEEE Microwave Fellowship 2008, GSRC Margarida Jacome Best Research Award 2007, and nine best paper awards including IEEE CICC 2019, 2021 and in IEEE HOST 2017-2020, for four consecutive years. Dr. Sen's work was chosen as one of the top-10 papers in the Hardware Security field (TopPicks 2019). He serves/has served as an Associate Editor for IEEE Solid-State Circuits Letters (SSC-L), Nature Scientific Reports, Frontiers in Electronics, IEEE Design & Test, Executive Committee member of IEEE Central Indiana Section and Technical Program Committee member of TPC member of ISSCC, CICC, DAC, CCS, IMS, DATE, ISLPED, ICCAD, ITC, and VLSI Design. Dr. Sen is a Senior Member of IEEE.

Agenda:

6:00 PM - 6:15 PM - Food and arrival

6:15-6:45 - Career journey, impact as an innovator in hardware security, and high-level introduction to Side-Channel Attacks

6:45 PM - 7:45 PM - DL talk + Q&A

7:45 PM - 8:15 PM - Networking

Learn more about Prof. Sen's work:

- TEDx Talk
- SPARC Lab homepage
- Google scholar
- LinkedIN