## *IEEE Solid-State Circuits Society Distinguished Lecturer Talk*

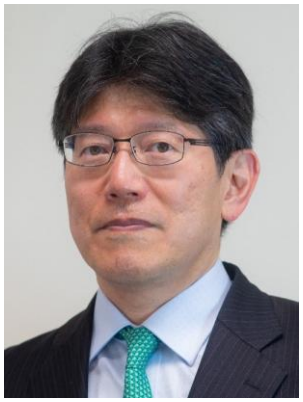
The SSCS DL Program provides experts in the Society's areas of interest to speak at chapter meetings and regional seminars. Lecturers, who serve for overlapping two-year terms, are deeply knowledgeable and excellent communicators. Their range of topics focuses on current IC activities, such as technology direction, novel devices, memories and radio technology, high-speed and precision data converters, wireline and on-chip communication, low-noise clocking, and low power design. The Columbus IEEE Joint Chapter of SSC &CAS Societies, SSC37/CAS04 is happy to host Prof. Makoto Ikeda from the University of Tokyo for our 2025 series of Distinguished Lecturer talks.

### First DL Talk: Basics of Asynchronous circuits design
### &
### Second DL Talk: Acceleration of Encryption Algorithms, Elliptic Curve, Pairing, Post Quantum Cryptoalgorithm (PQC), and Fully Homomorphic Encryption (FHE)

**Date & Time: Monday, November 10, 2025 • 9:00 – 11:00 AM EST**
Location (In-person):
2015 Neil Ave
Columbus, Ohio
United States 43210
Building: Dreese Labs, Room Number: 260
Register Here: https://events.vtools.ieee.org/m/507434
Virtual Option (Google Meet):
Video call link: https://meet.google.com/uud-qwao-wvz
Or dial: (US) +1 252-573-3244 PIN: 475 204 007#
More phone numbers: https://tel.meet/uud-qwao-wvz?pin=4135848920384

**1st Abstract:** This lecture will overlook basics and variety of asynchronous controlling, from the view point of advantages for low-voltage & variation rich conditions. This lecture takes two extreme example of complete completion detection type asynchronous designs as examples and demonstrate details of operation and performance. In addition, this talk will cover recent trial on design flow of random logic by the self-synchronous circuits.

**2nd Abstract:** This lecture will cover basics of public-key encryption, and example design optimization of elliptic-curve based encryption algorithm, including pairing operations, and its security measures. Then extend design optimization on lattice-based encryption algorithms including post quantum crypto-algorithm, CRISTALS-Kyber/Dilithium, isogeny based encryption argorithms, and fully homomorphic encryption algorithm.



**Biography:** Makoto Ikeda received the BE, ME, and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1991, 1993 and 1996, respectively. He joined the University of Tokyo as a research associate, in 1996, and now professor and director of Systems Design Lab(d.lab), the University of Tokyo. At the same time he has been involving the activities of VDEC(VLSI Design and Education Center, the University of Tokyo), to promote VLSI design educations and researches in Japanese academia. He worked for hardware security, asynchronous circuits design, smart image sensor for 3-D range finding, and time-domain signal processing. He has been serving various positions of various international conferences, including ISSCC ITPC Chair(ISSCC 2021), IMMD sub-committee chair (ISSCC 2015-2018), A-SSCC 2015 TPC Chair, VLSI Circuits Symposium PC Chair(2017)&Symposium Chair(2019). He is a senior member of IEEE, IEICE Japan, and a member of IPSJ and ACM.

**Agenda:**

8:30 AM - 9:00 AM – Networking, coffee and donuts

9:00 AM - 9:45 AM – Basics of Asynchronous circuits design

9:45 AM -10:00 AM – Break

10:00 AM - 10:45 AM - Acceleration of Post Quantum Encryption Algorithms