ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Mixed-signal technologies for ultra-wide band signal processing systems

GABRIELE MANGANARO

Agenda

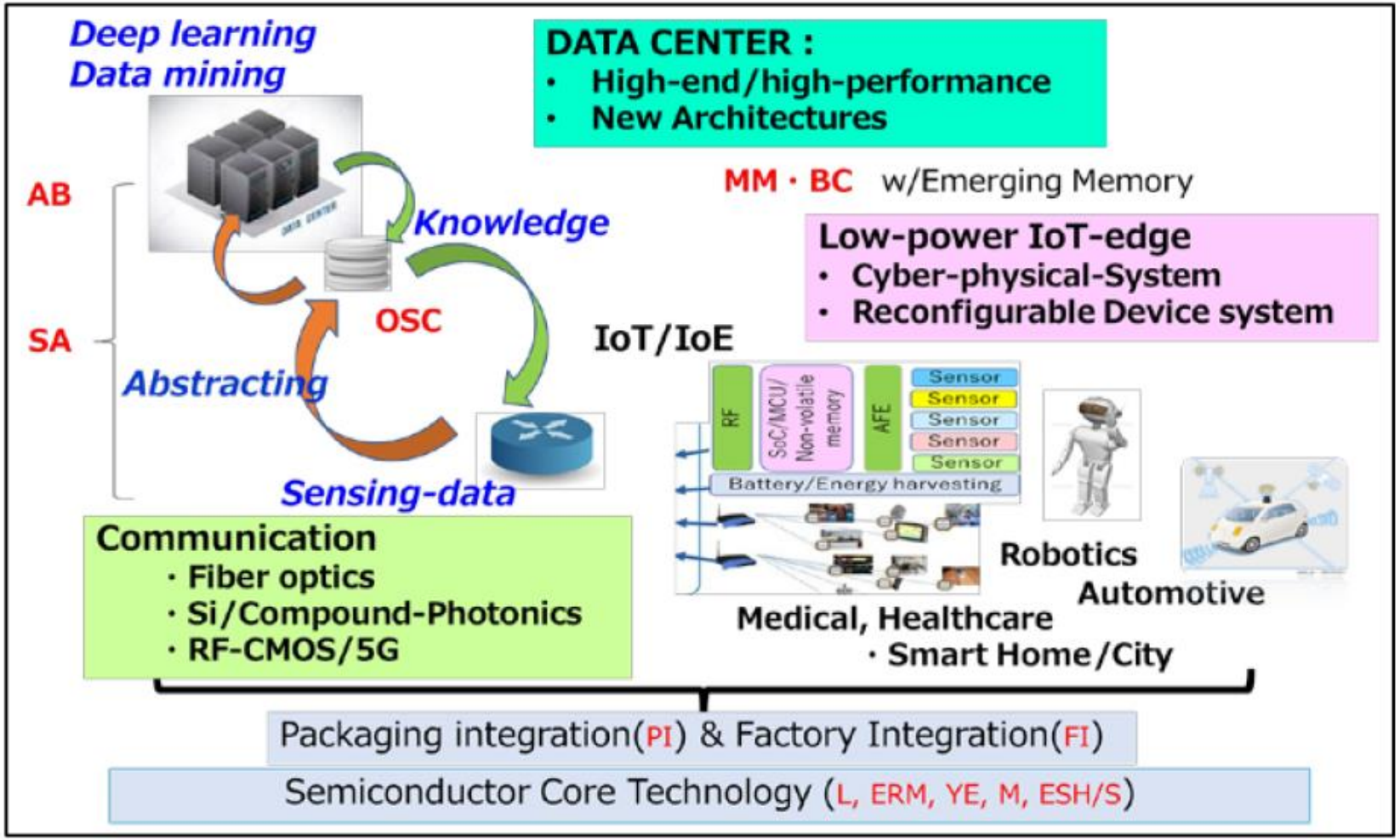
- Motivation / Applications
- Process Technology
- ADC architectures
- Integration
- Signal Chain Linearization
- Conclusion

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Motivation / Applications

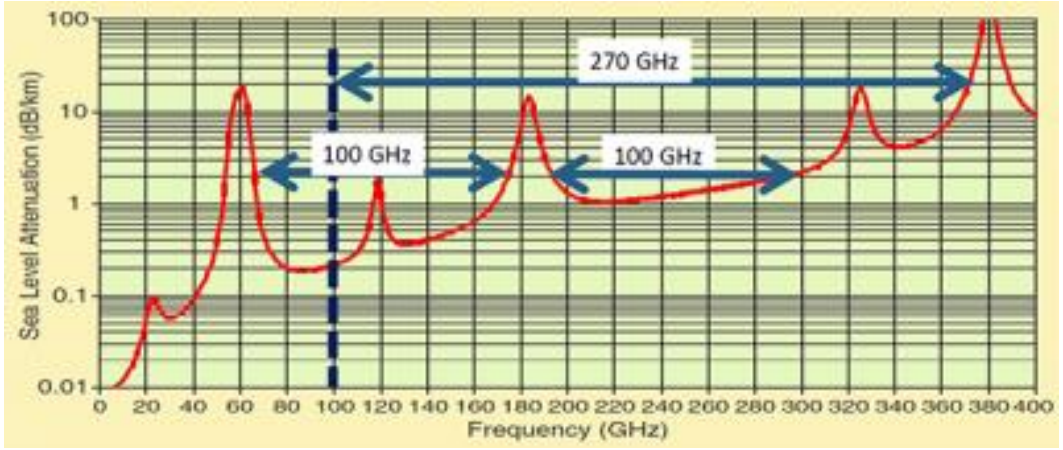
Application pull / Technology Push



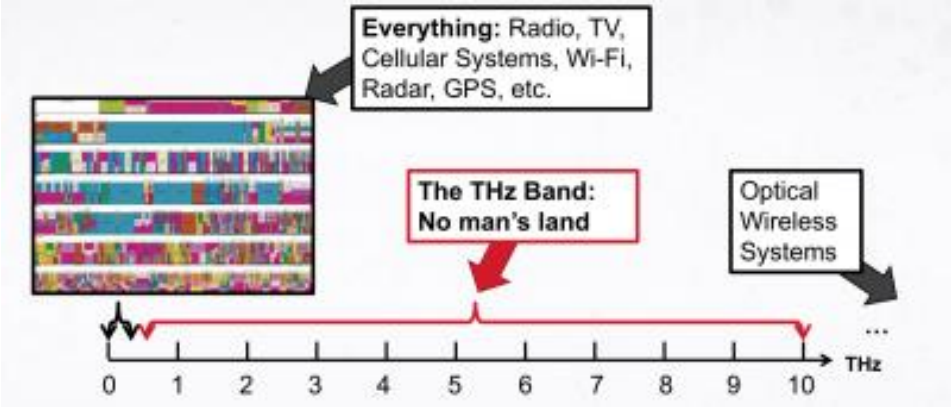
AB: Applications Benchmark
SA: Systems & Architecture
OSC: Outside System Connectivity
MM: Moore Moore
BC: Beyond CMOS
PI: Packaging Integration
FI: Factory Integration
L: Lithography
M: Metrology
ERM: Emerging Research Materials
YE: Yield Enhancement
ESH/S: Environment, Safety & Health and Sustainability

International Roadmap for Devices and Systems (IRDS) – 2018 Edition.

Higher frequency in search for more BANDWIDTH



T. Rappaport et al., “Wireless Communications and Applications Above 100 GHz: Opportunities and Challenges for 6G and Beyond”, IEEE Access, June 2019

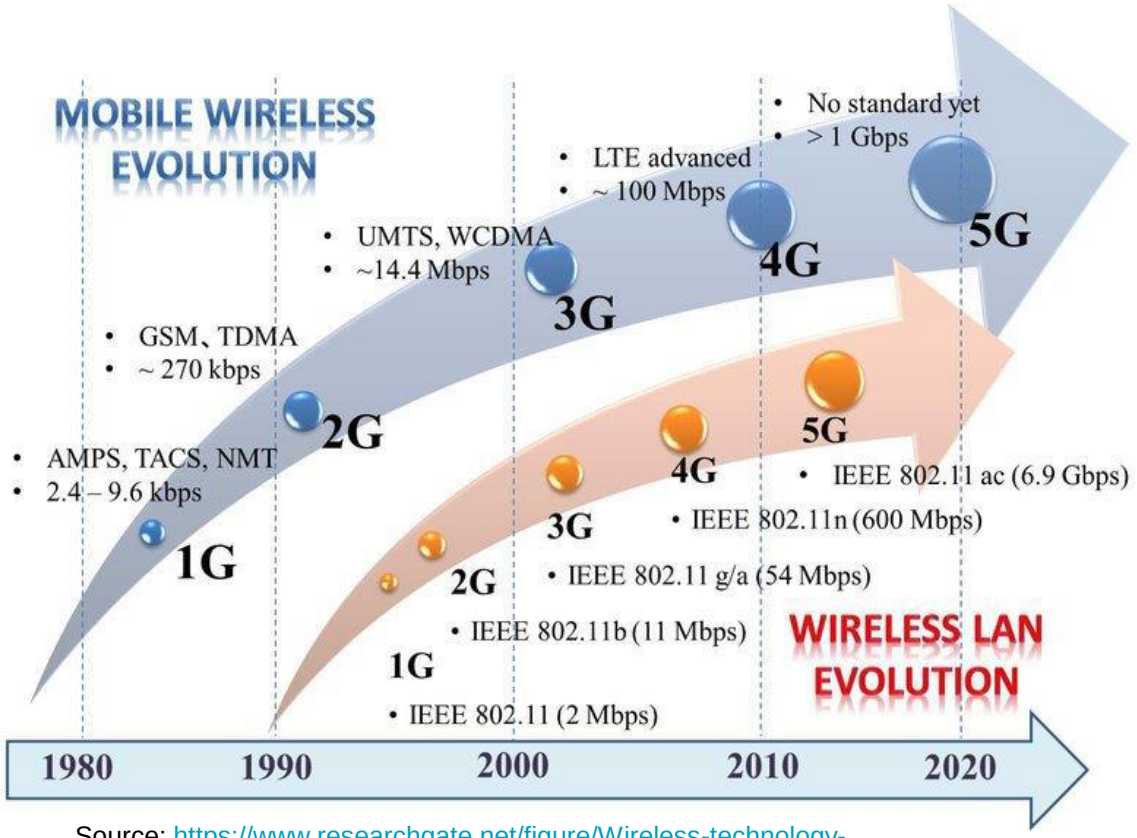


J. M. Jornet, “Terahertz Communications: The Quest for Spectrum”, IEEE ComSoc News, 22 Nov 2019

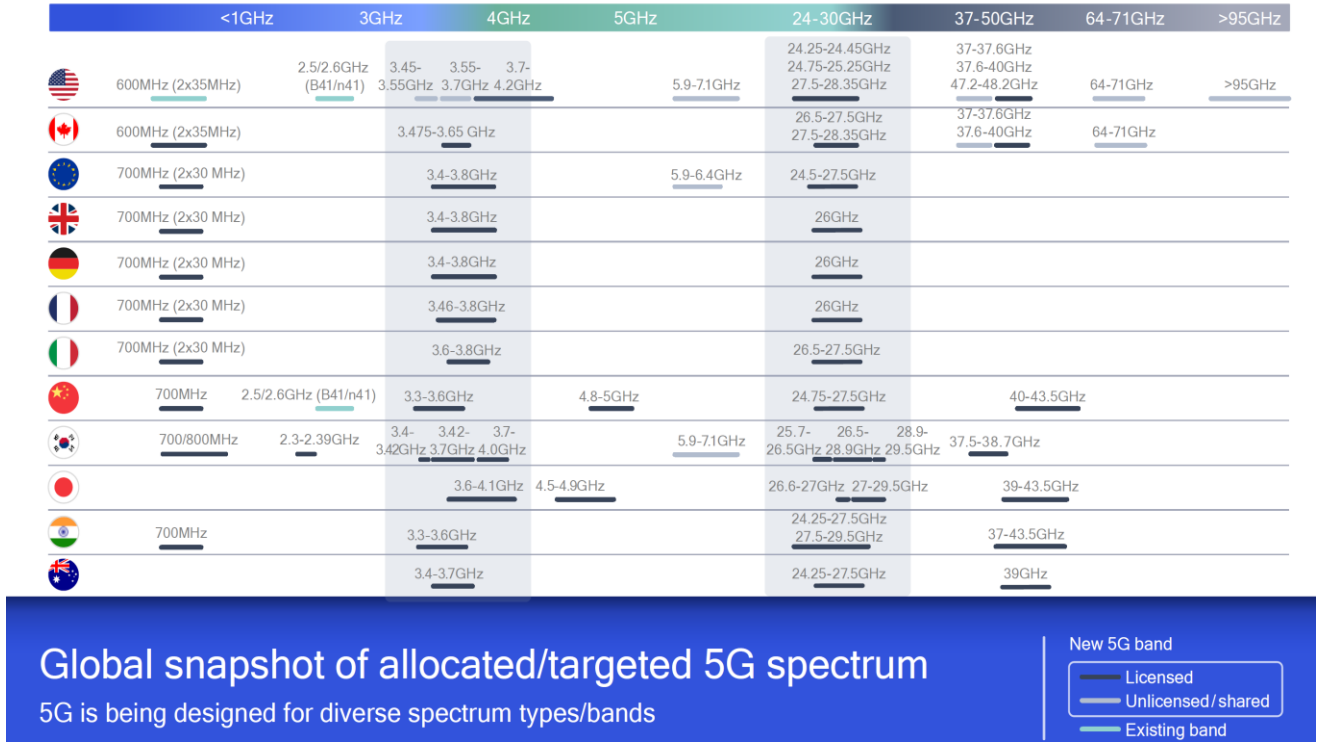
Some application drivers:

- 6G wireless / “Future Networks”
- Data centers / Comm Backhaul
- Immersive virtual reality / remote medicine
- Broadband sensing for cyber-physical systems
- Beamformers / wideband radars

Mobile phone's generations



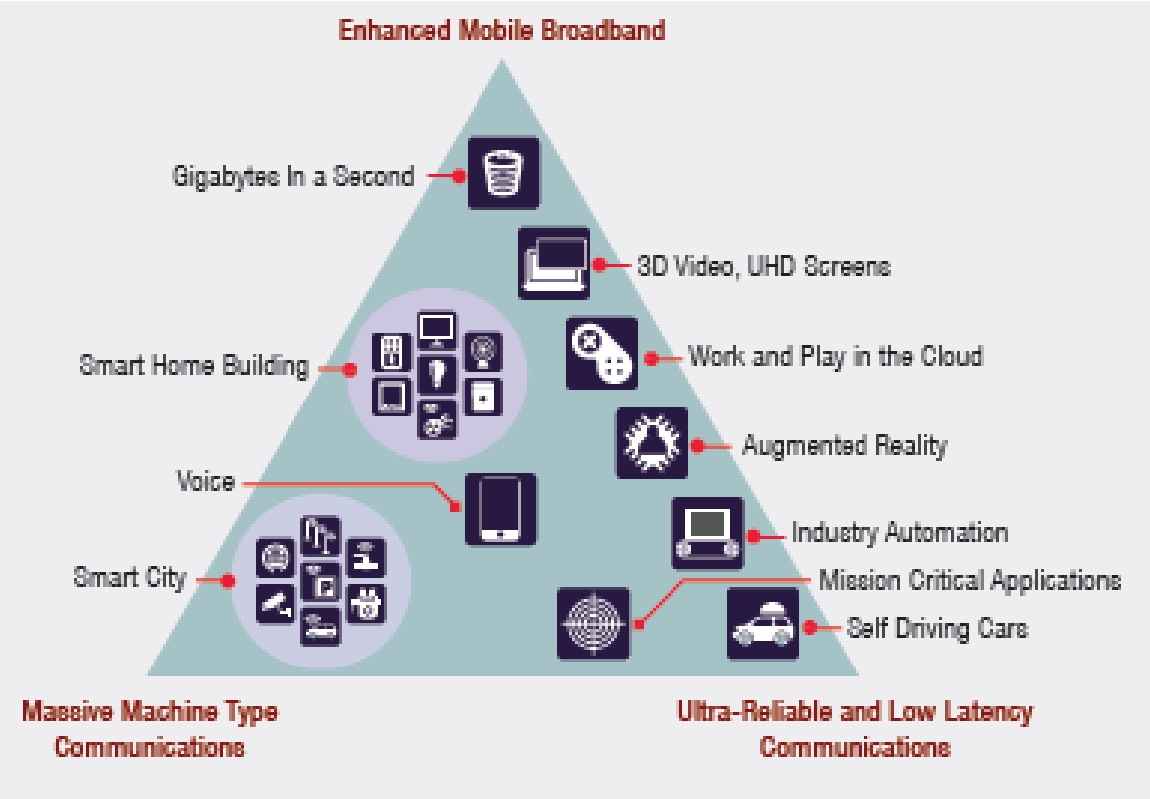
Source: https://www.researchgate.net/figure/Wireless-technology-evolution_fig1_322584266

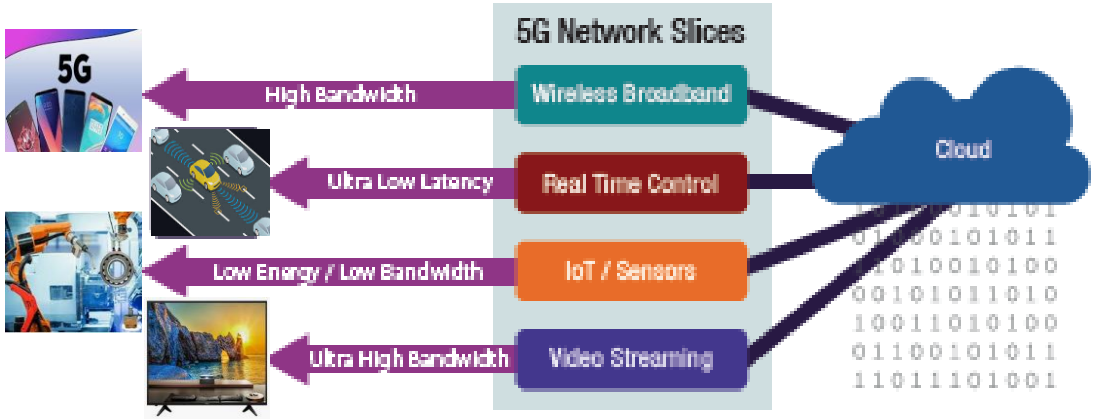


Qualcomm – Global update on spectrum for 4G & 5G, April 2020

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

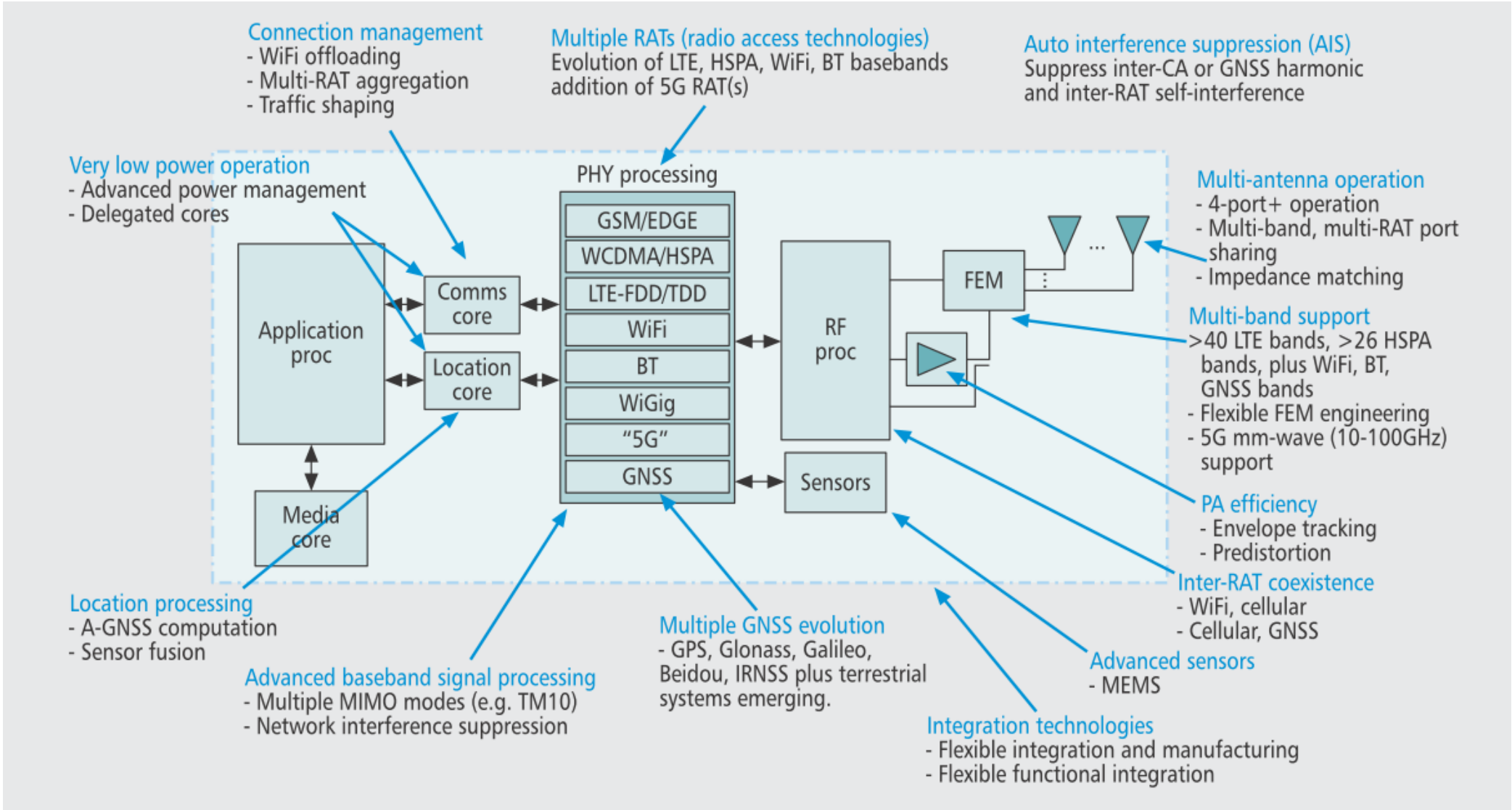
Wireless communication: 5G



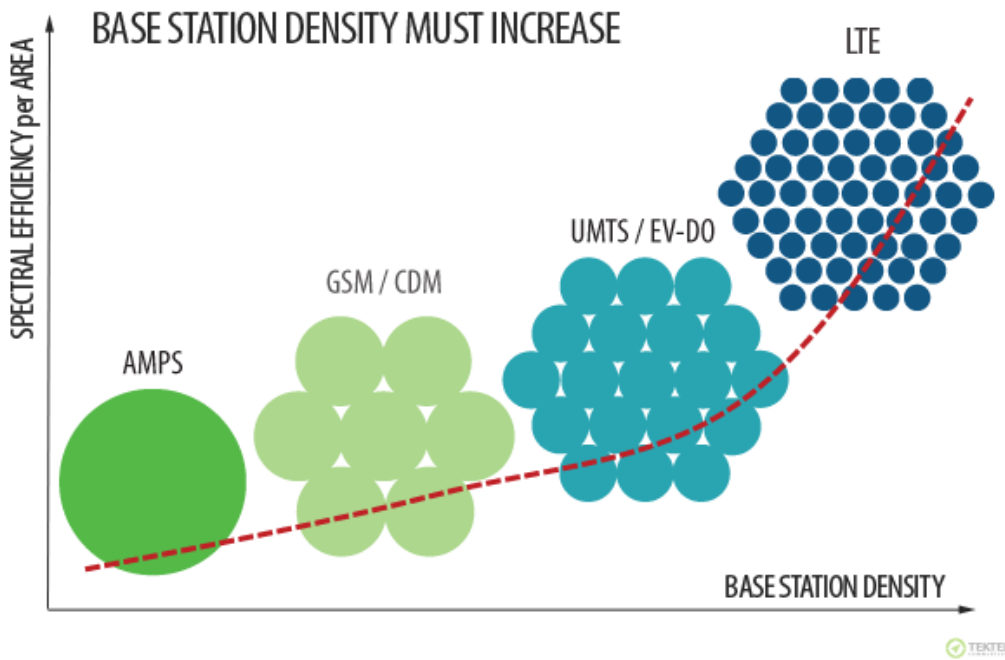


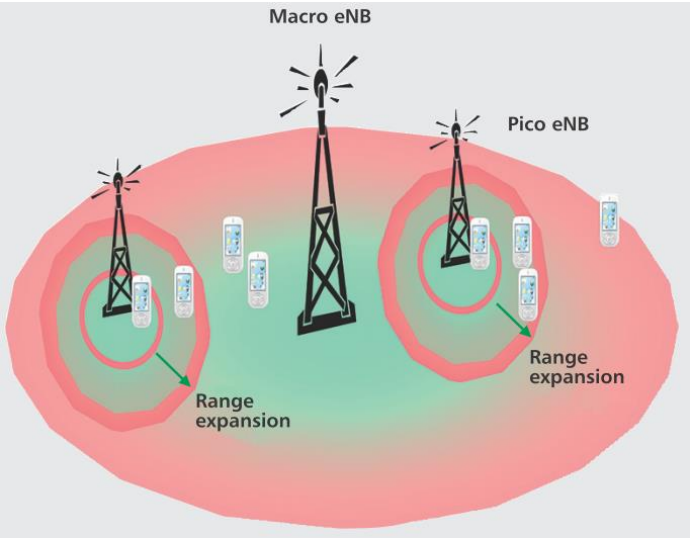
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

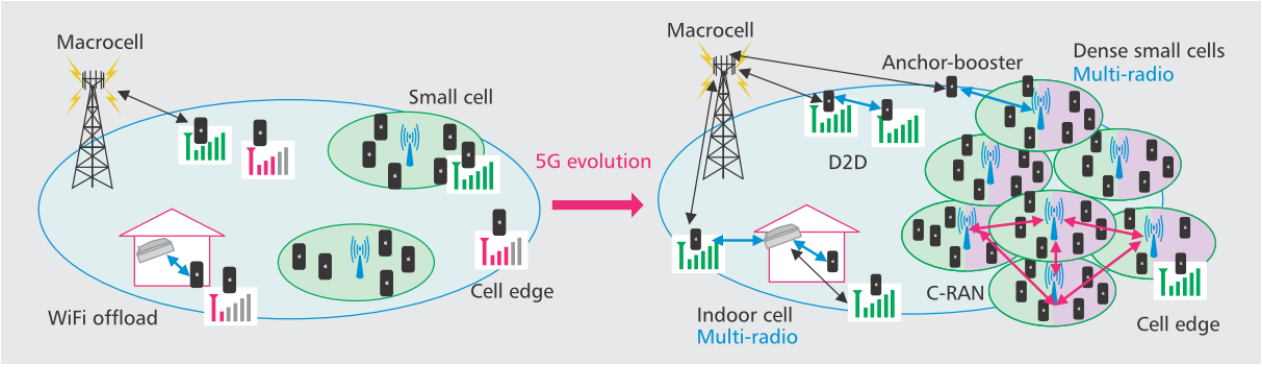
Wireless communication: 5G



Densification/Range Extension



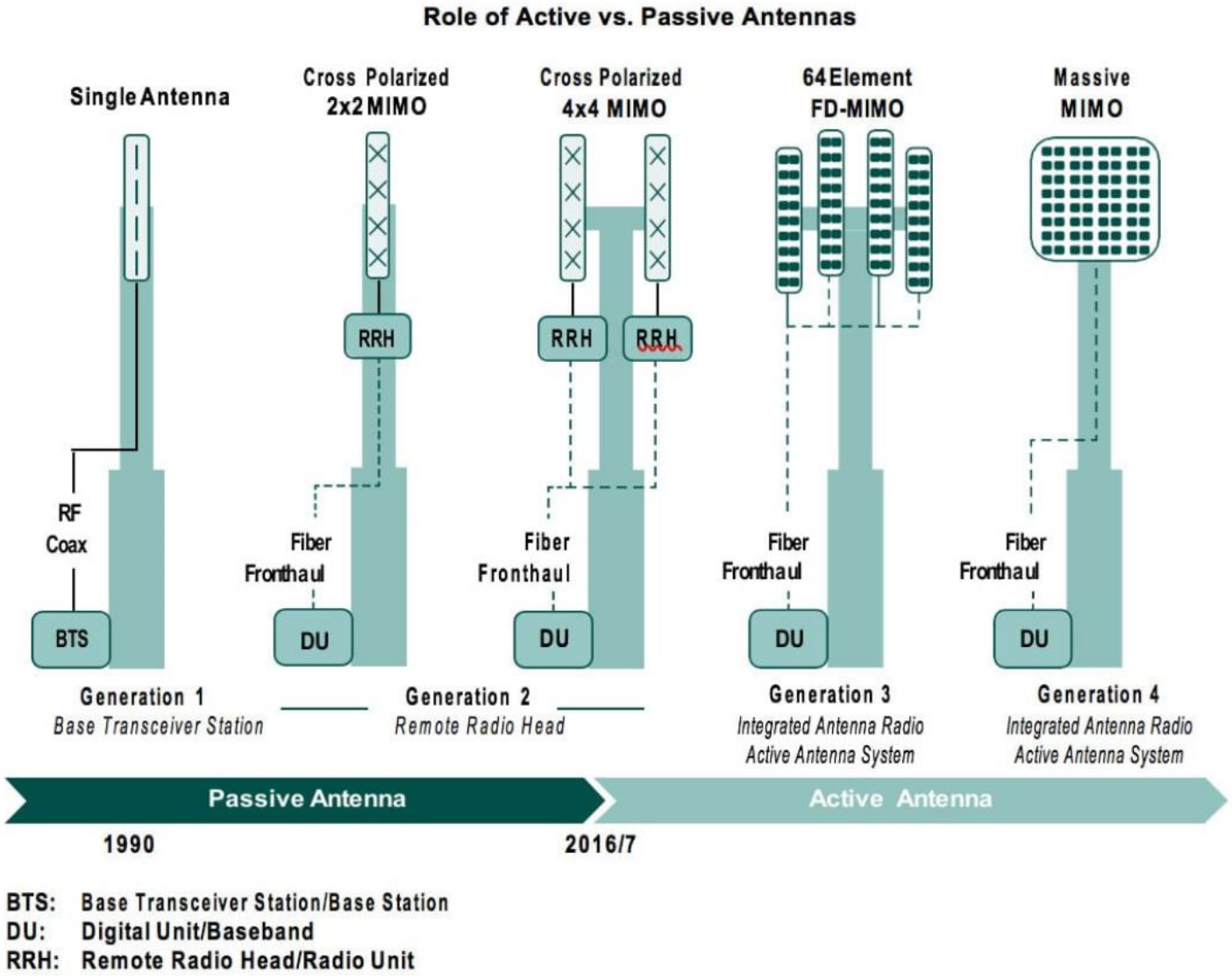




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Cellular Base Stations (BTSs)

- Three complementary initiatives:
  - Proactive cell shaping
  - Vector sectorization
  - MIMO Antennas
- An active antenna is one that has active electronic components (i.e., transistors).
- Examples of active antennas:
  - Smart antennas
  - Remote radio head antennas
  - Beamforming antennas.



ABI Research - Analyst angle: The rise and outlook of antennas in 5G, June 2018

Antenna arrays

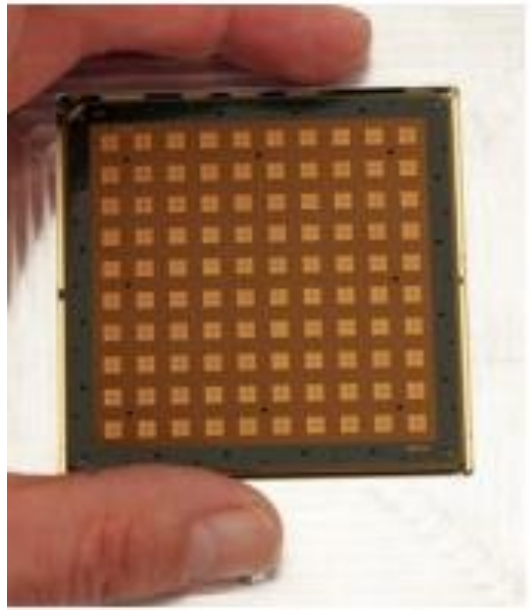
$$G = \frac{4\pi A_{phys}\eta}{\lambda^2}$$

A_{phys}: Physical aperture area
η: Aperture efficiency
λ: Wavelength

UHF Phased Array Radar

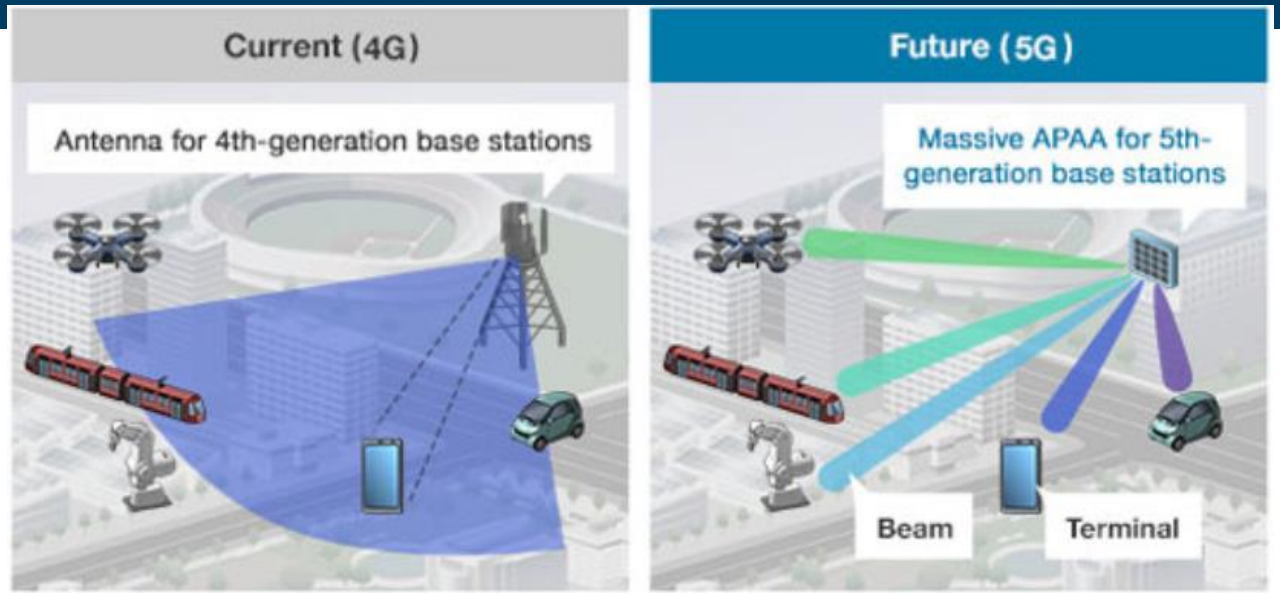
Source: https://www.bcpowersys.com/military-programs/uhf-phased-array-radar/

mmW Phased Array Antenna

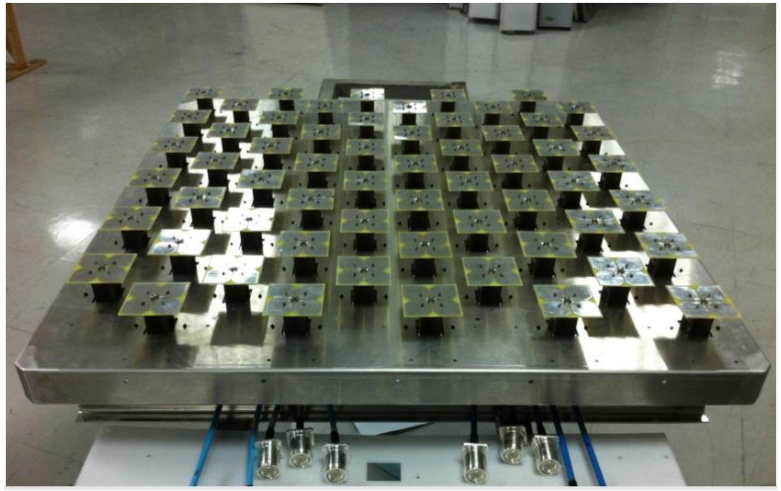


Source: https://www.sciencedirect.com/topics/engineering/antenna-arrays

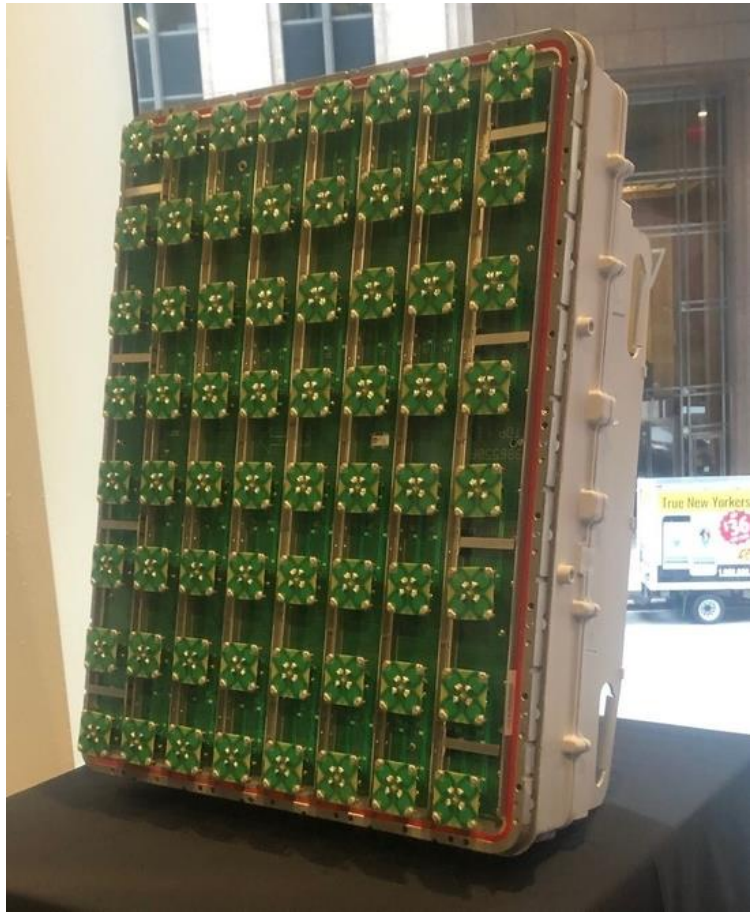
5G Antenna Arrays



Source: https://www.mitsubishielectric.com/en/about/rd/research/highlights/communications/5g.page



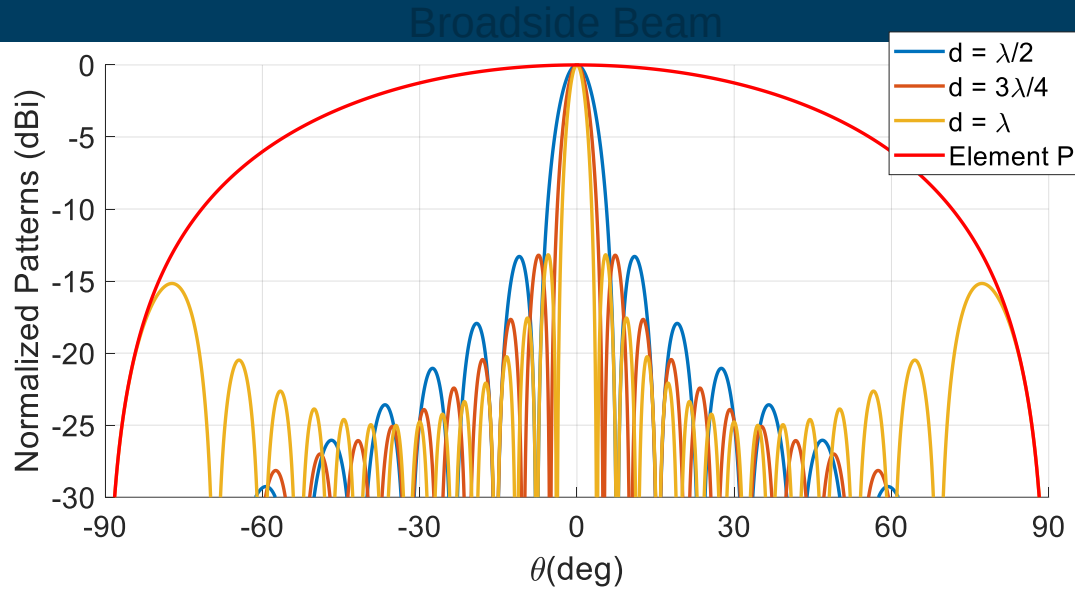
Source: https://www.engineersaustralia.org.au/sites/default/files/resource-files/2017-01/Div_Syd_techPres_advanced_cellular_base_station_antennas.pdf

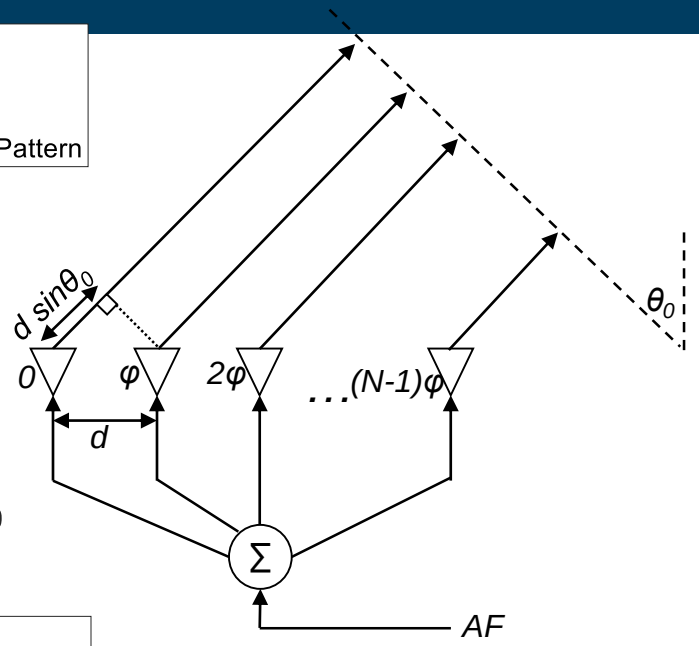


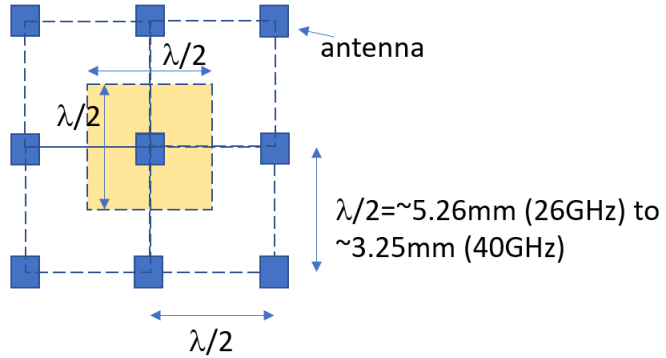
Source: *Sprint's massive-MIMO/Bevin Fletcher, FierceWireless* https://www.fiercewireless.com/5g/sba-says-sprint-only-carrier-it-sees-deploying-massive-mimo

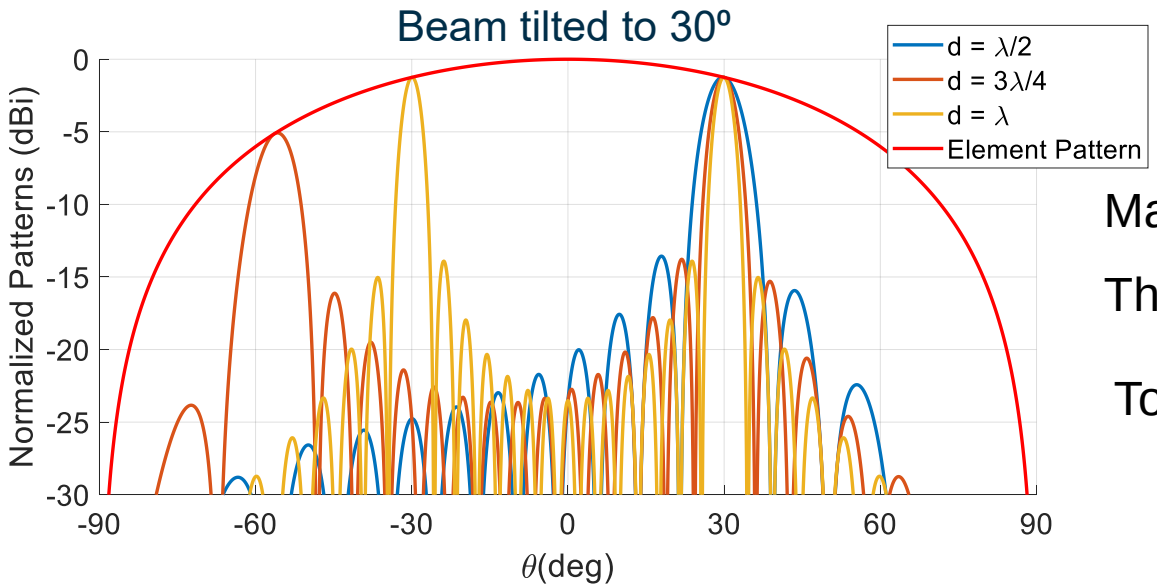
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

What determines the spacing between the antenna elements?









$$AF = 1 + e^{j\varphi} + e^{j2\varphi} + \cdots + e^{jN\varphi},\ \varphi = kdsin\theta_0$$

Maximum beams occur at $\varphi = \pm n\pi \quad \rightarrow \quad sin\theta_0 = \pm n\pi/kd$

These beams are in real space when $-1 < sin\theta_0 < 1$

To avoid grating lobes:

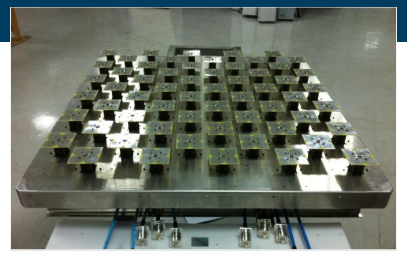
$$d < \frac{\lambda}{1 + |sind(\theta_0)|},$$

θ_0 is the beam angle

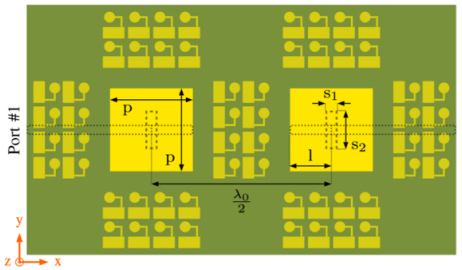
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Phased arrays / Beamforming

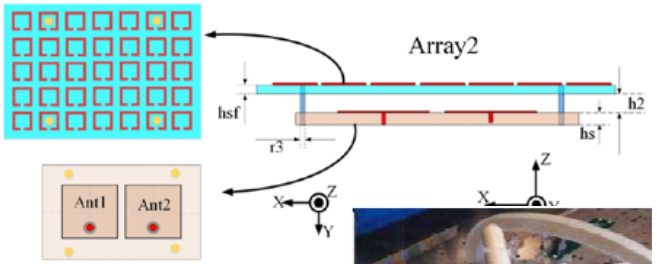
- Ultra-wideband base station antennas
- High dense antenna arrays
- Phased array calibration
- Beamforming and beam management



Source: https://www.engineersaustralia.org.au/sites/default/files/resource-files/2017-01/Div_Syd_techPres_advanced_cellular_base_station_antennas.pdf



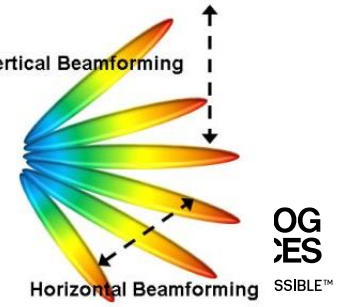
A. Stark, “Buried EBG Structures for Antenna Array Applications,” Proceedings of the 40th European Microwave Conference, 2010



Z. Wang et al, “A meta-surface antenna array decoupling (MAAD) method for mutual coupling reduction in a MIMO antenna system,” Scientific Report, Feb. 2018

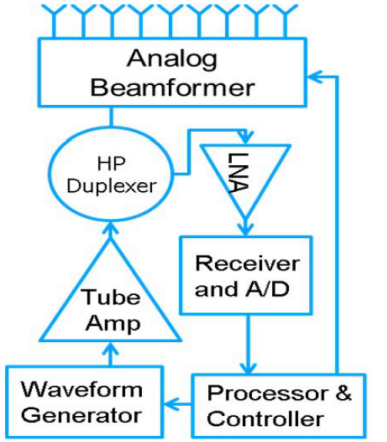
Roy Butler et al, “Broadband multiband phased array antennas for cellular communications,” ISAP, 2016

Source: https://amphenol-antennas.com/news-2/10020-2-4/



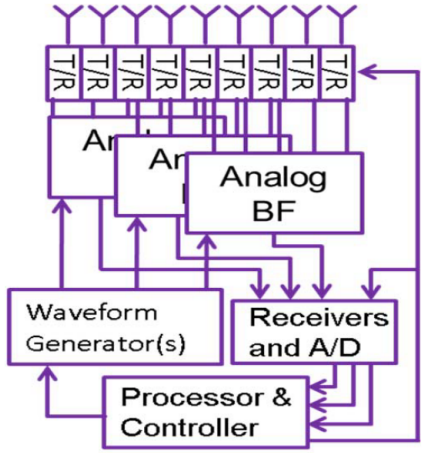
Phased array system evolution

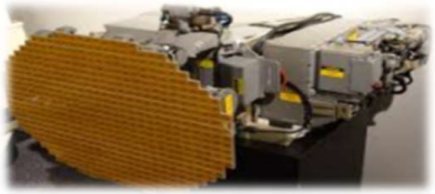
Classical



- All Analog Beamforming
- Centralized Receivers & Exciters
  - Low electronics content:

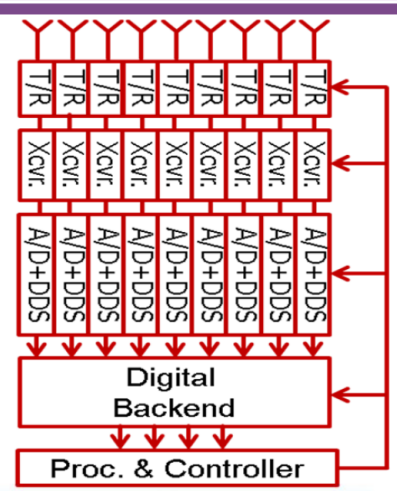
Hybrid Solution





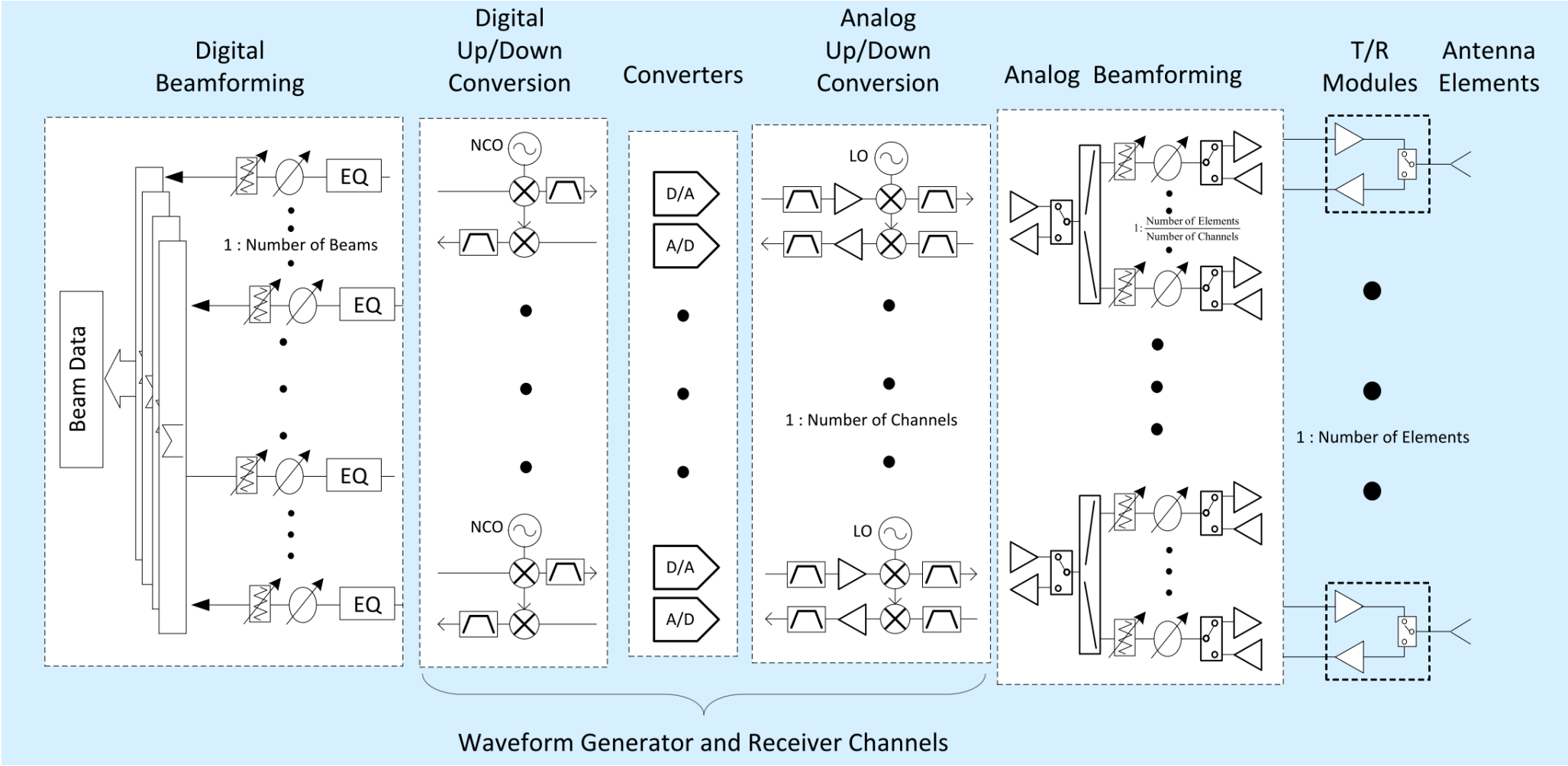
- Sub-array Architecture
  - Analog/Digital Beamforming
- Distributed Receivers & Exciters
  - At Subarray Level

All Digital

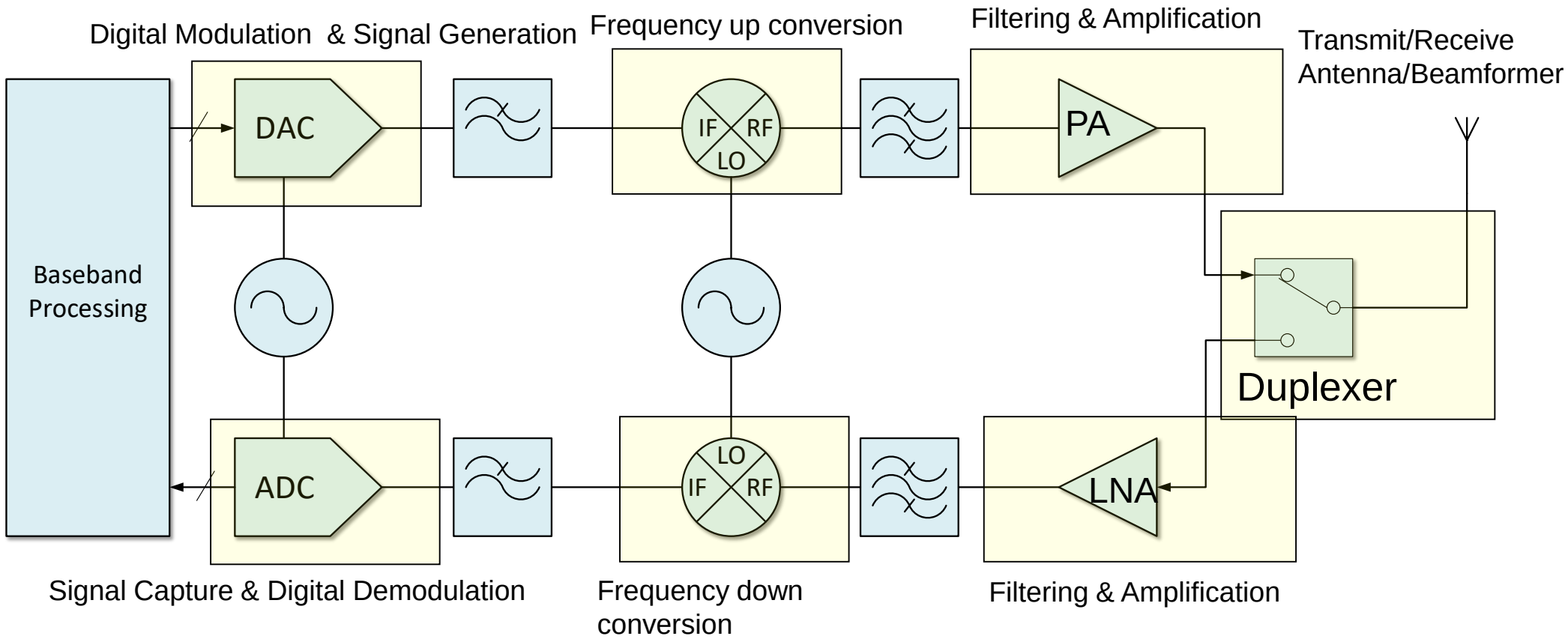


- Every Element Digital Beamforming
  - No Analog Beamforming
- Distributed Receivers & Exciters
  - At a per element level

Generic beamforming phased array system signal chain

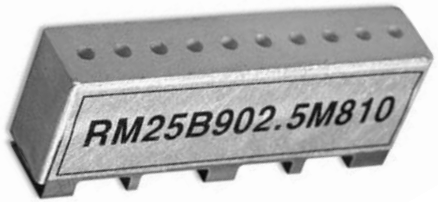


T/R signal chain (simplified)



The $$ stuff that does not want to scale: duplexer & other filters

SAW
(photo lithography)



Ceramic Monoblock
(mechanical)

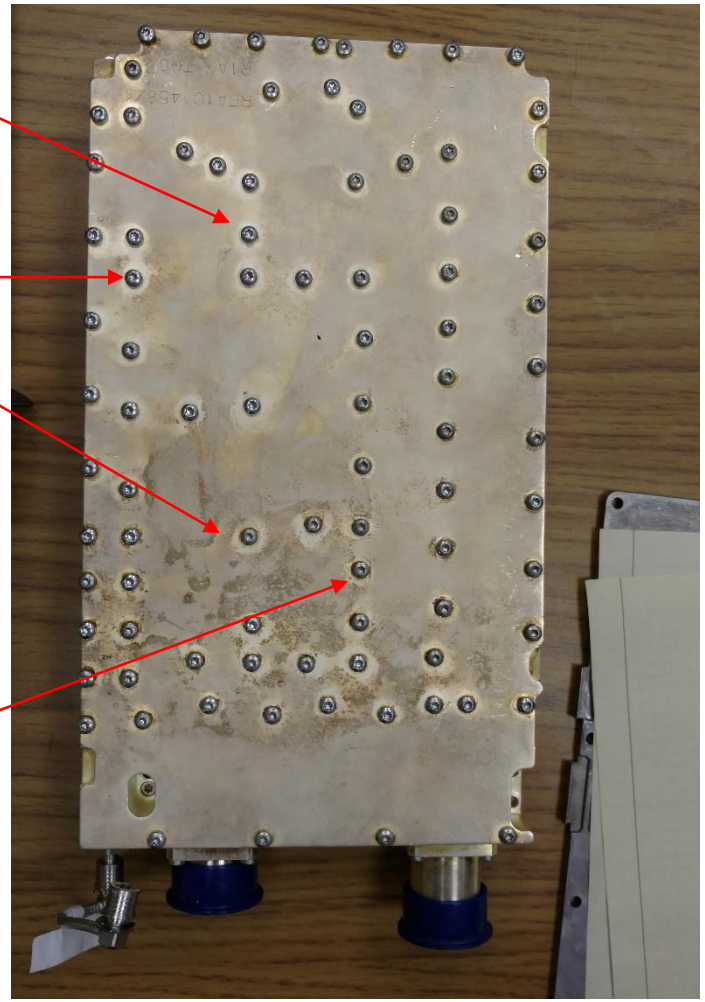
Cavity (GHz)
(manual assembly)

$$size \propto performance \qquad size \propto \frac{1}{frequency}$$

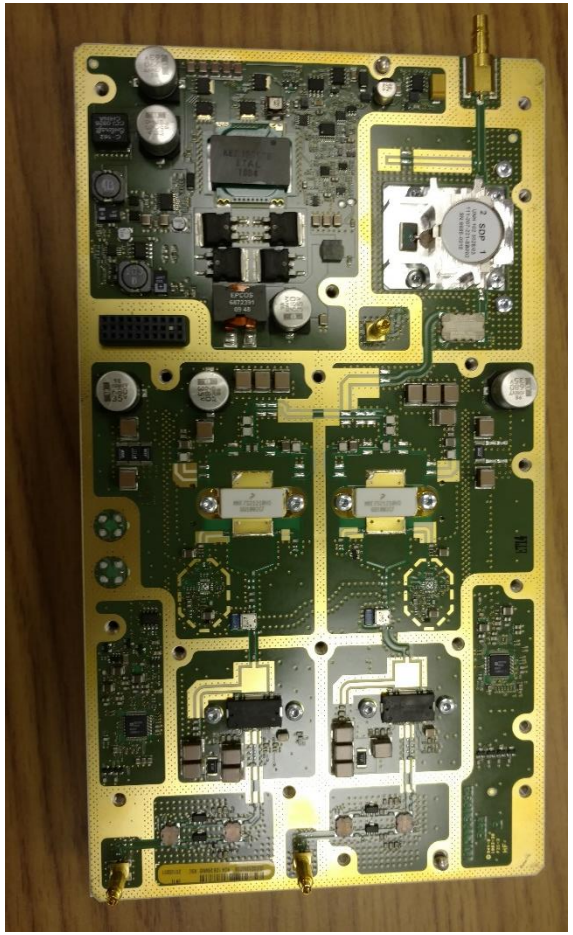
$$cost \propto size$$

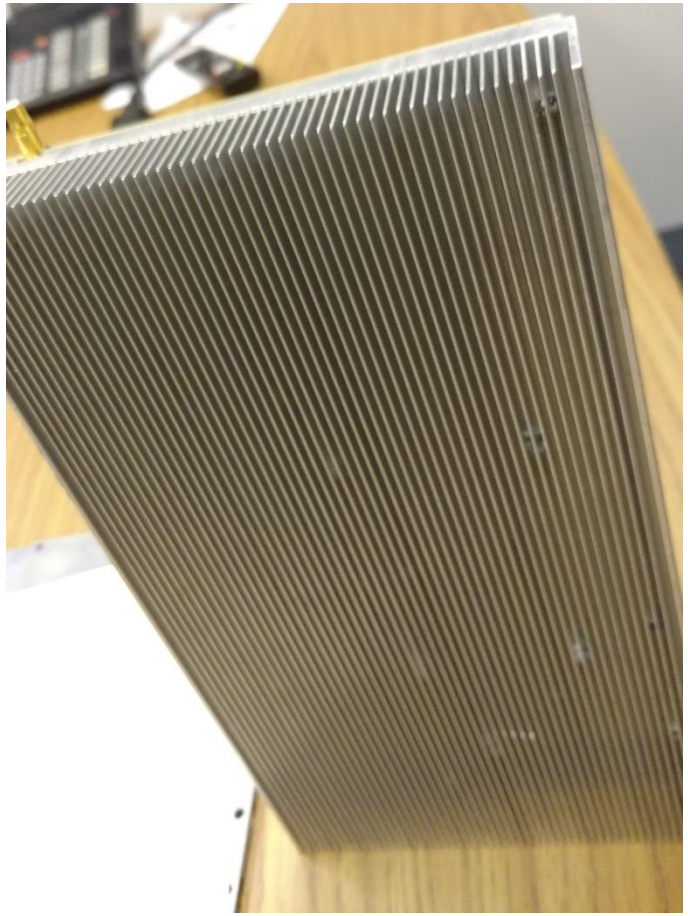
An actual BTS's duplexer

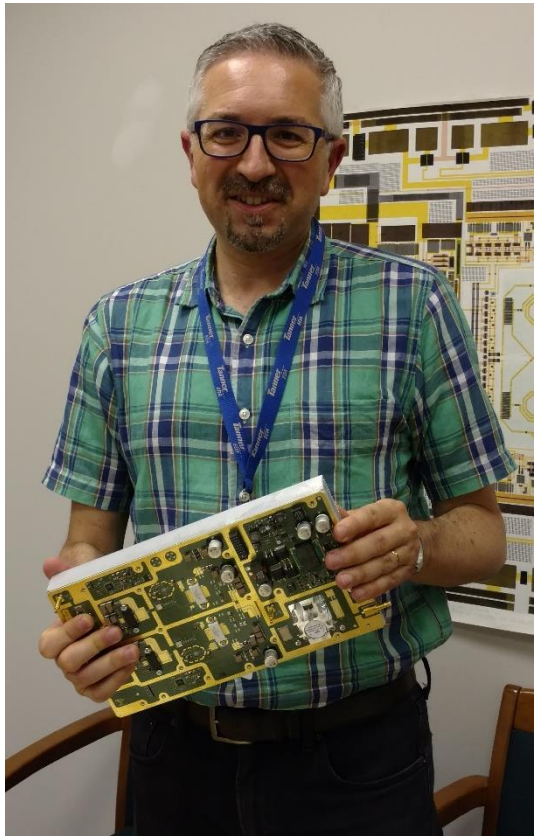
Tuning screws!!!



An actual power amplifier





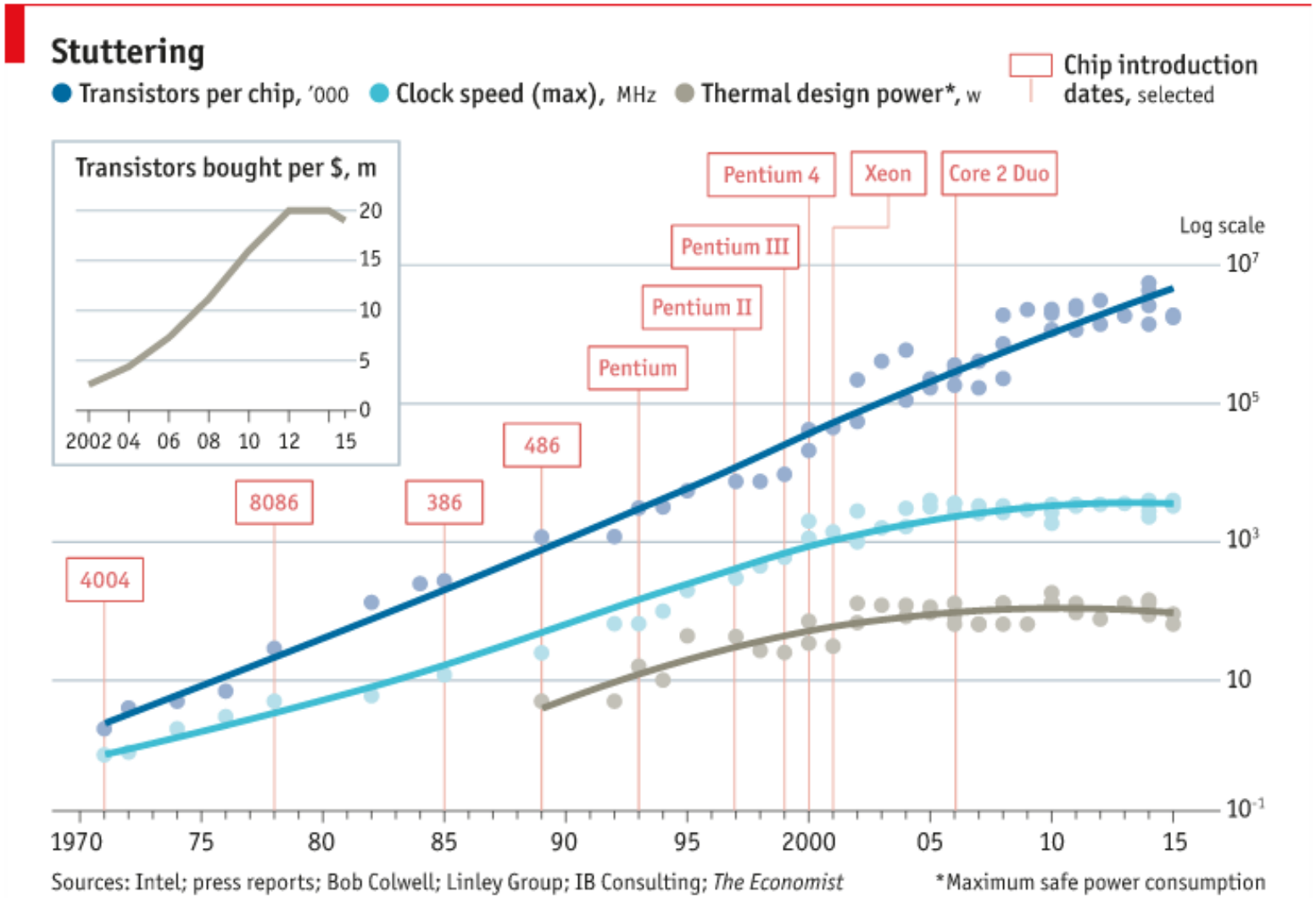


ANALOG DEVICES

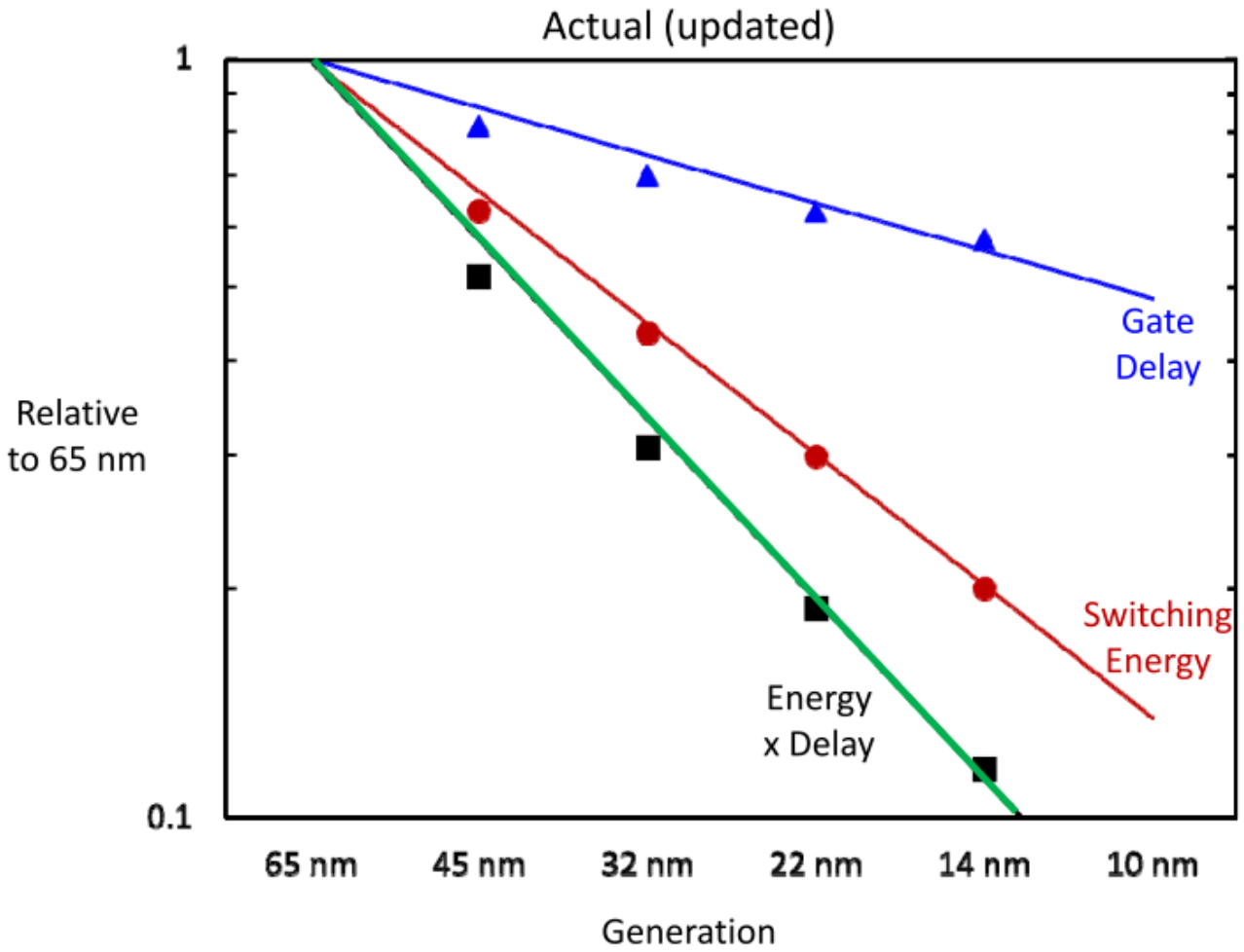
AHEAD OF WHAT'S POSSIBLE™

Process Technology

Moore’s law

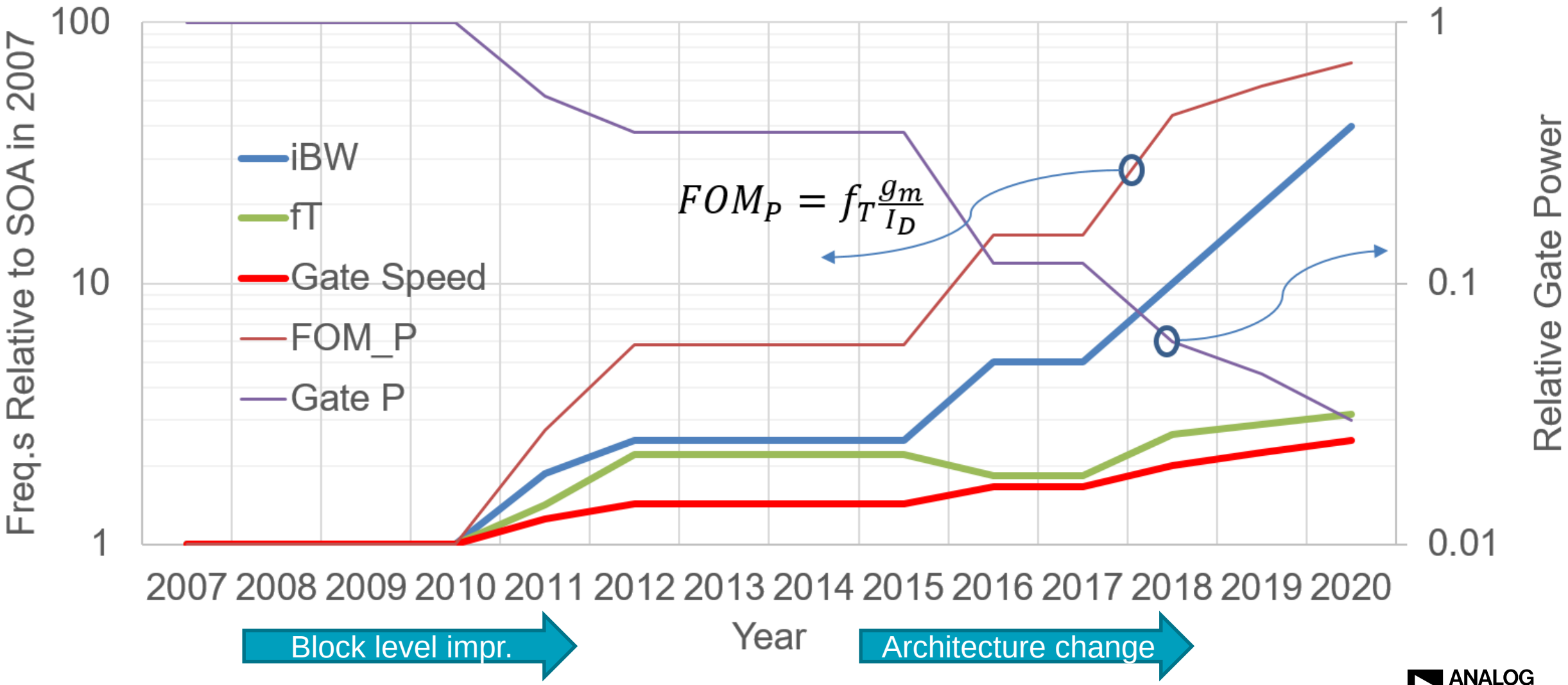


Higher digital power efficiency, but not (much) higher device speed!



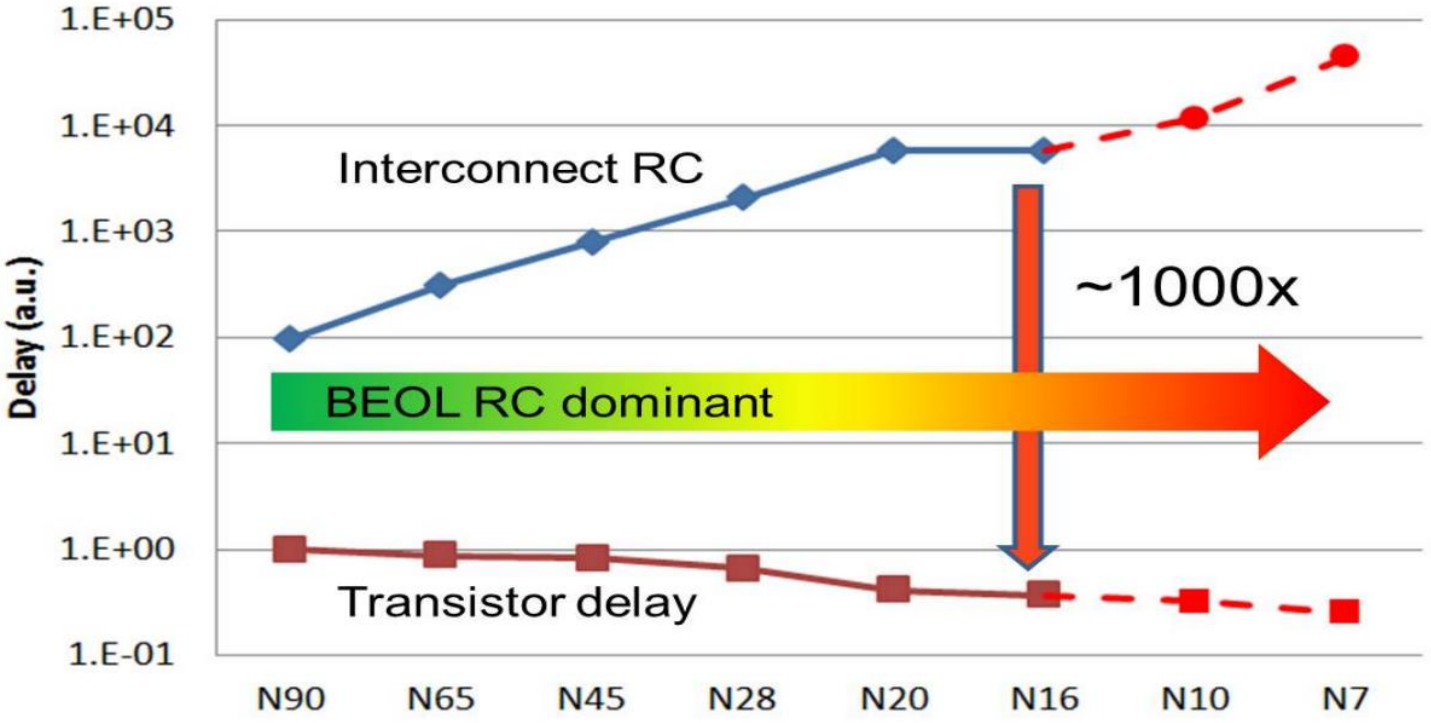
Source: W.M.Holt, "Moore's Law: A path going forward", ISSCC 2016

Application pull: Wireless Infrastructure (BTS) bandwidth demand versus MS CMOS capability

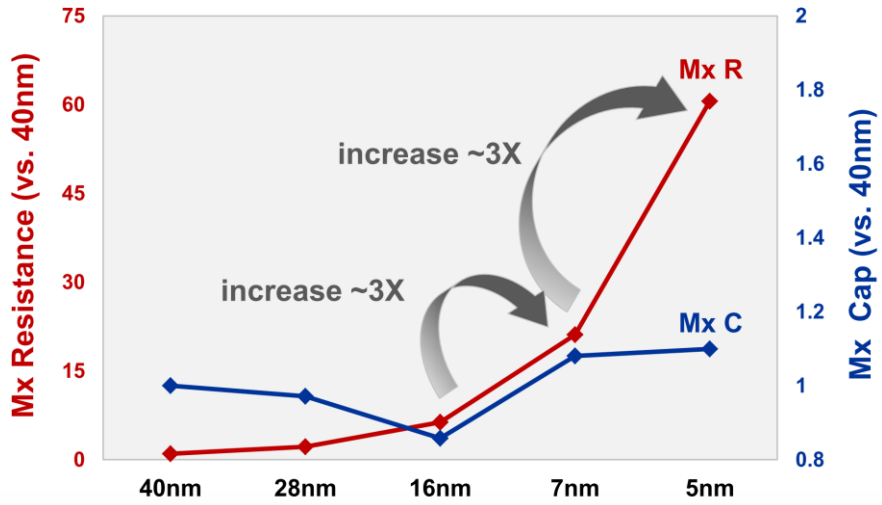


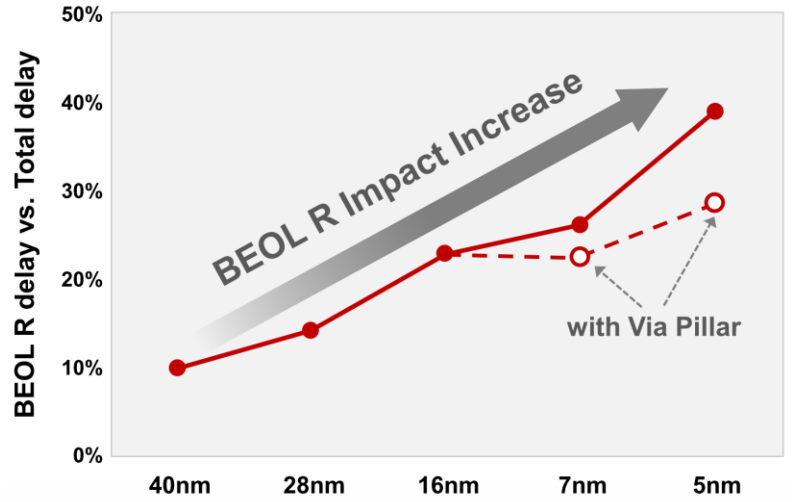
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Die interconnects are the biggest bottleneck



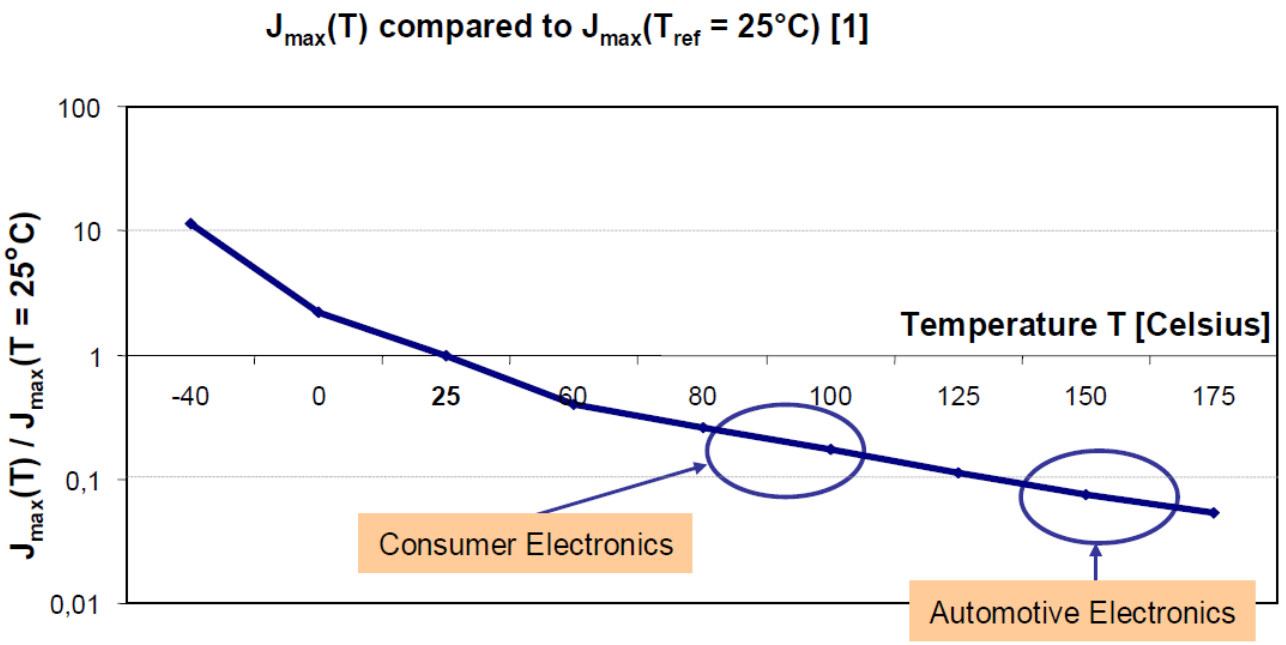
Source: G. Yeap (Qualcomm), IEEE Electron Devices Meeting (IEDM), 2013

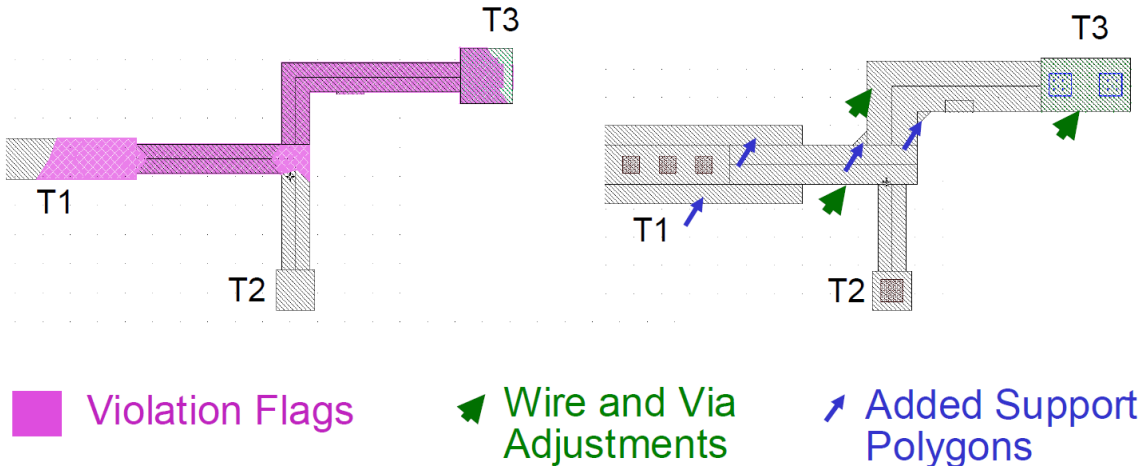




C. Hou (TSMC), ISSCC 2017 & L. Lu (TSMC), ISPD 2017

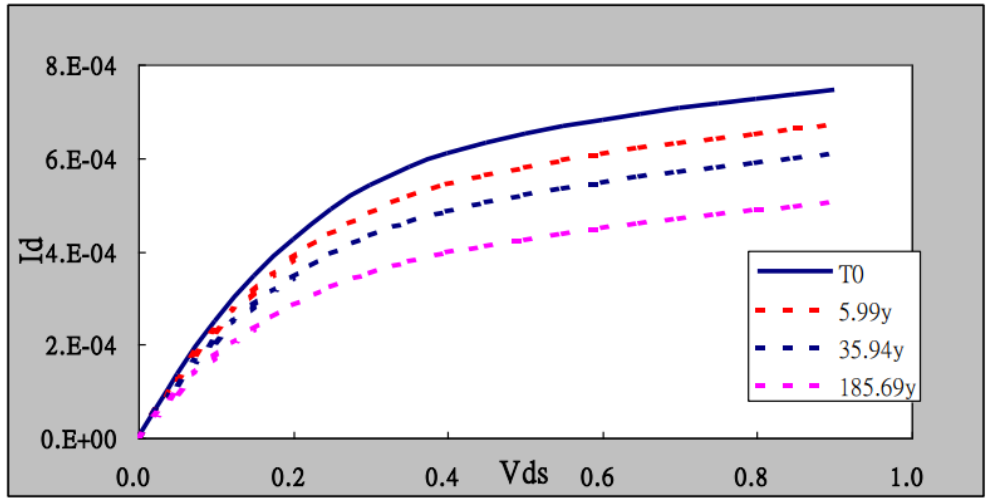
Electromigration

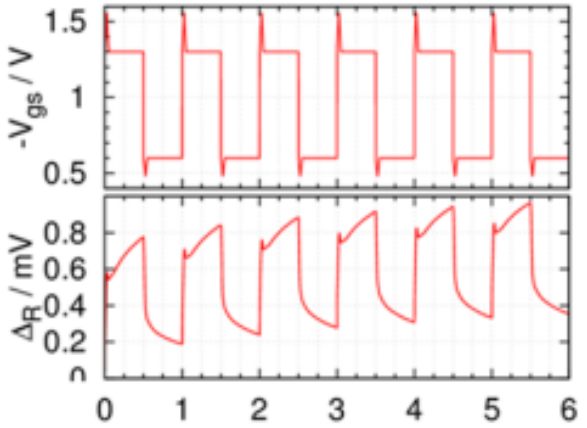




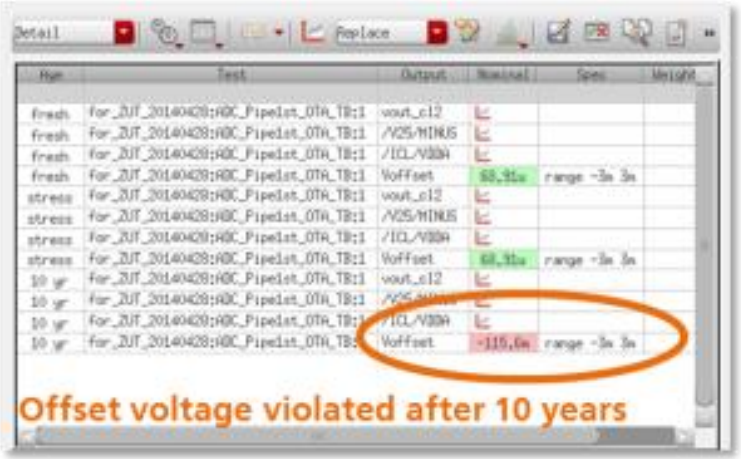
The maximum permissible current density of an aluminum metallization, calculated at e.g. 25°C, is reduced significantly when the temperature of the interconnect rises

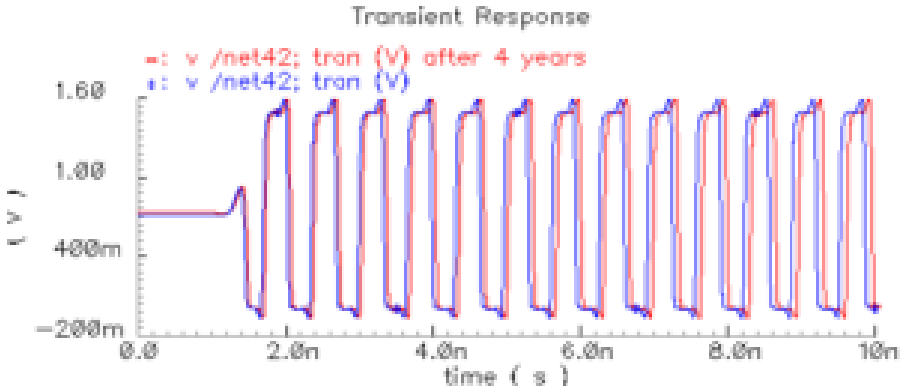
Device Aging





Vt shift due to NBTI degradation

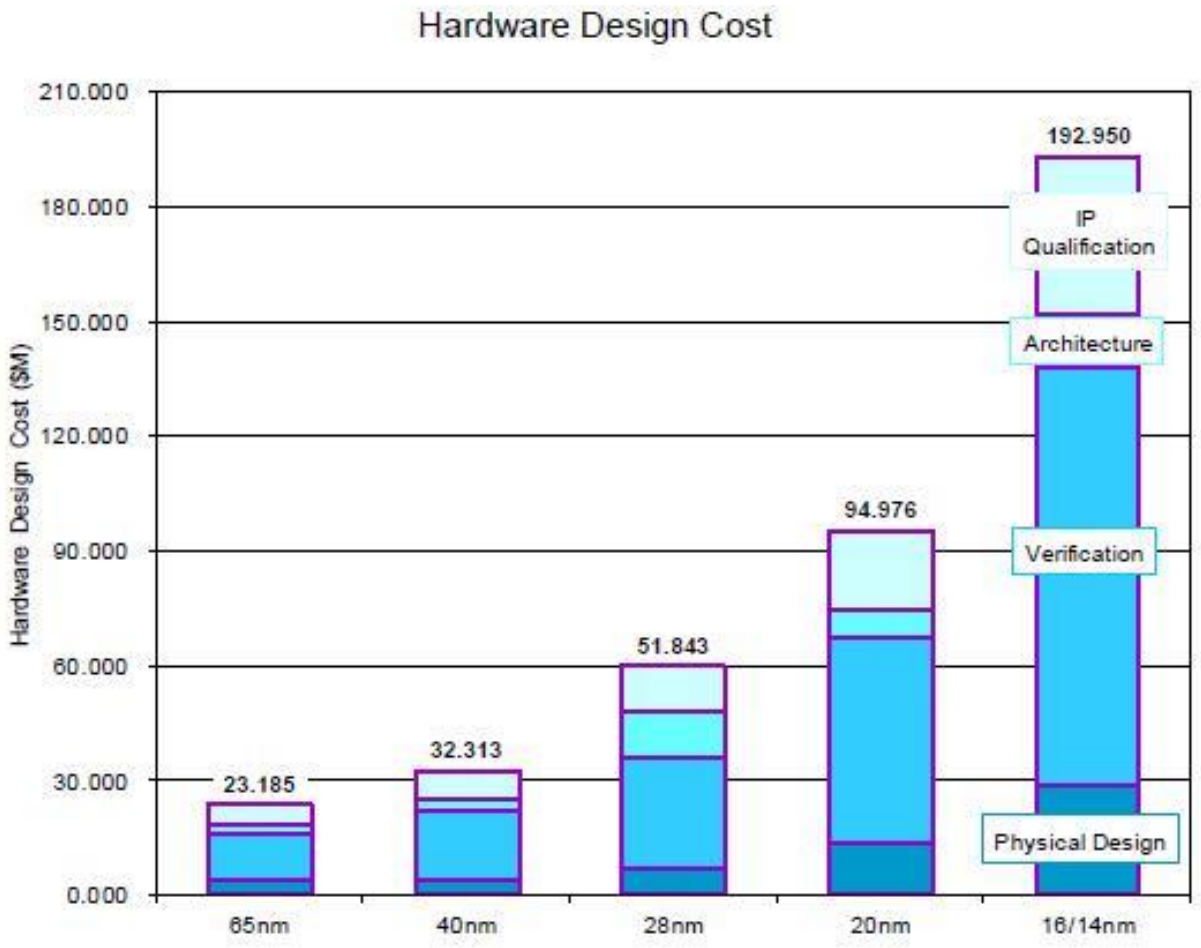




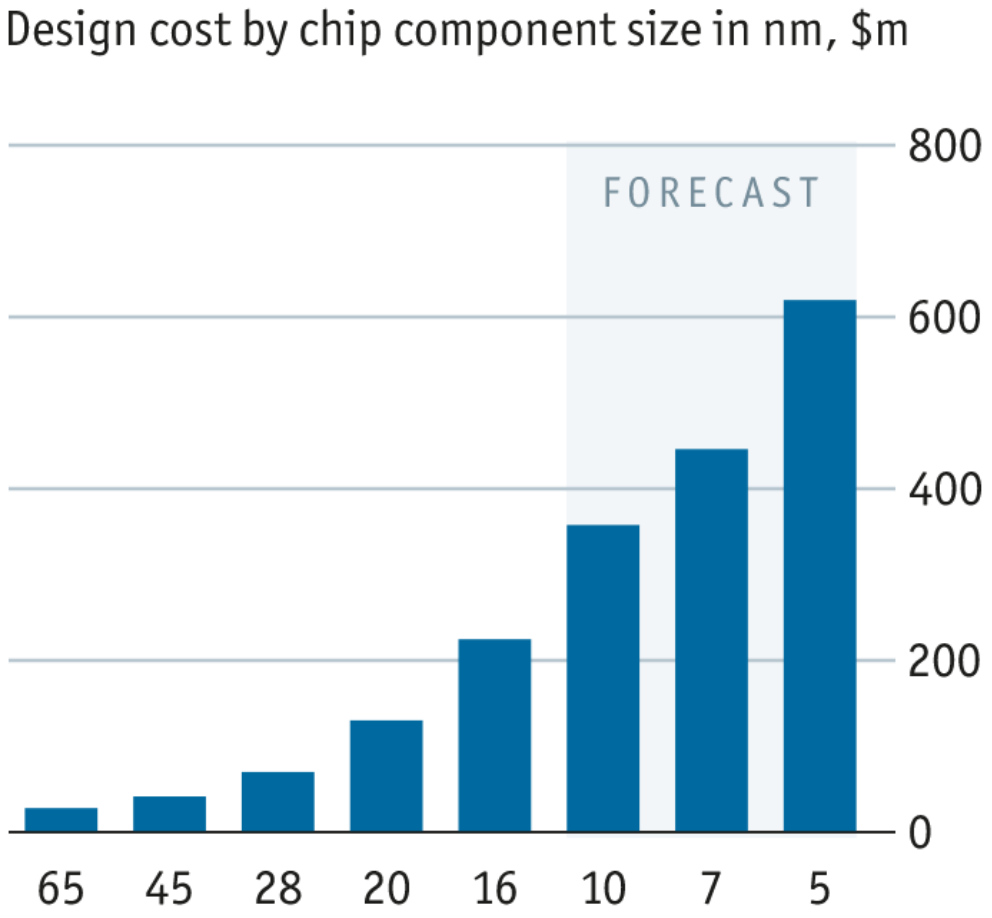
Frequency shift after 4 years of op.

Source: Fraunhofer Institute for Integrated Circuits

Complexity drives development cost



Source: International Business Strategies, Inc 2013 report



Source: IB Consulting

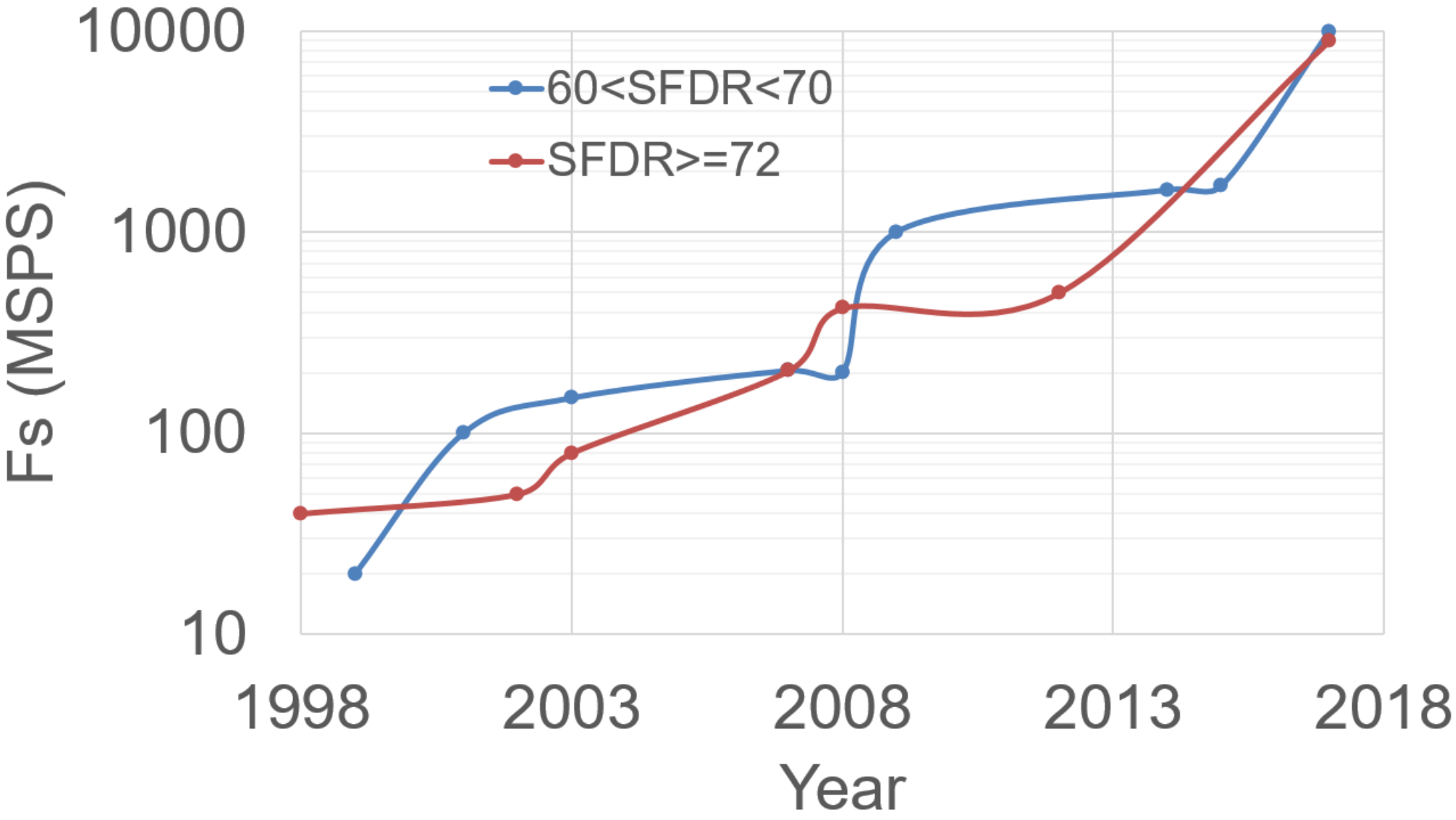
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

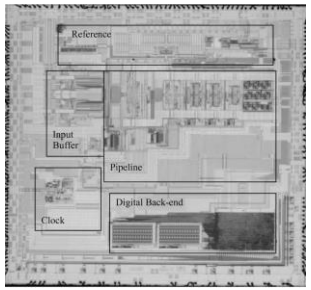
ADC architectures

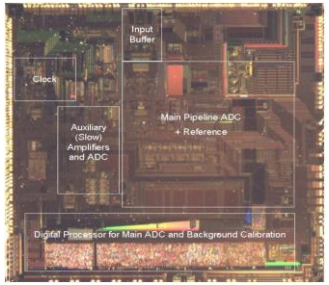
Technology progression: 12b/14b High Speed (HS) ADC progression

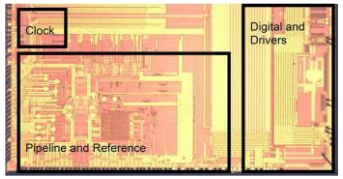


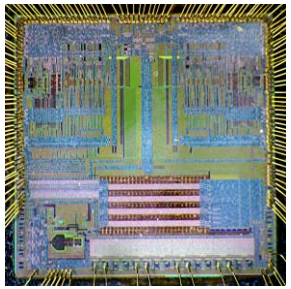
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

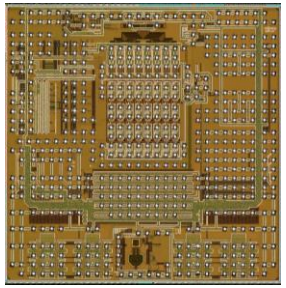
Evolution of high-speed A/Ds at ADI (see ISSCC papers)

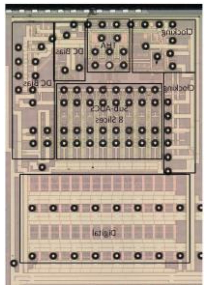










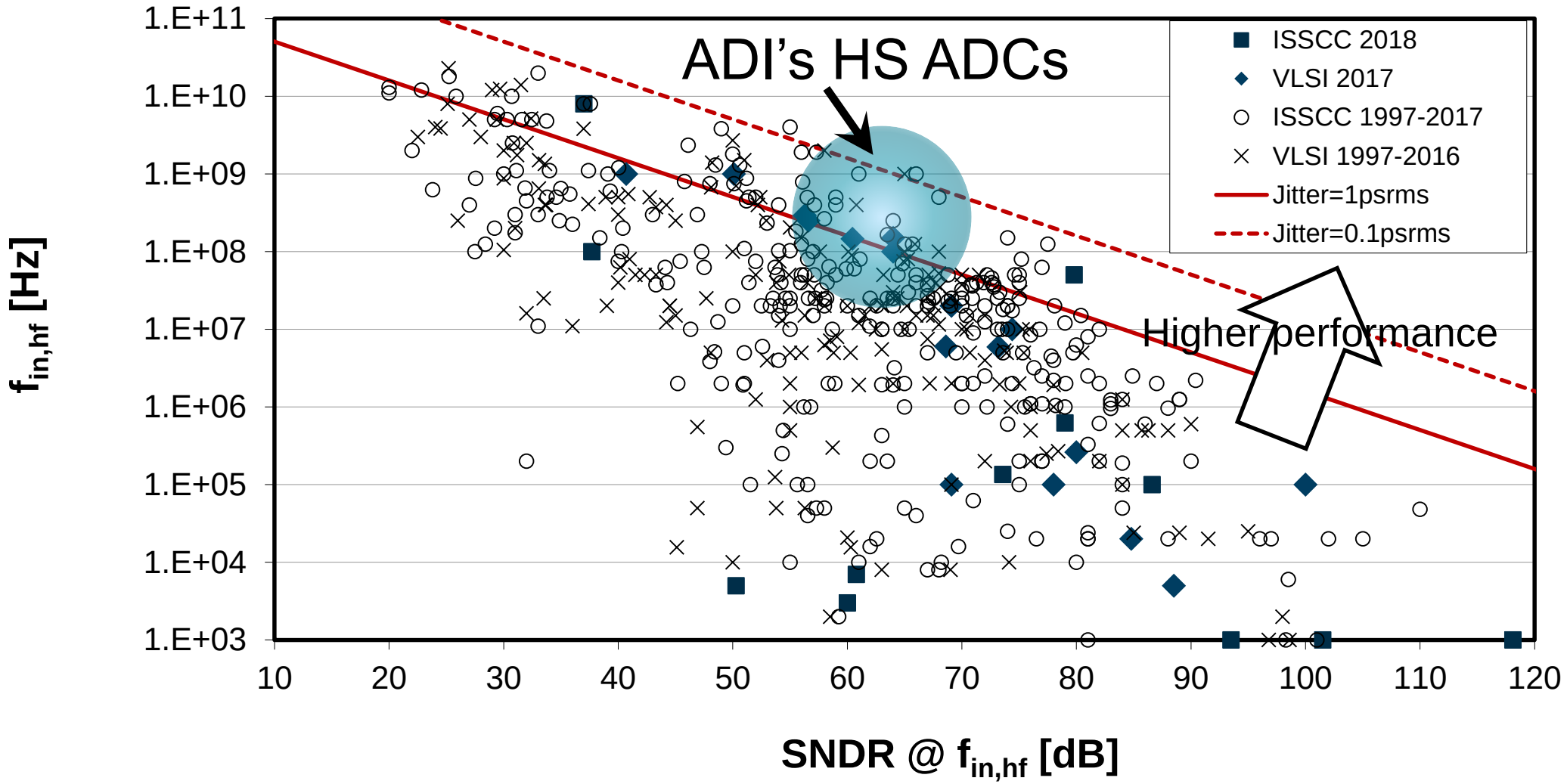


2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020

14b/125MSPS	16b/250MSPS	14b/1.25GSPS	14b/3GSPS	12b/10GSPS	12b/18GSPS
0.35u BiCMOS	0.18u BiCMOS	65nm CMOS	28nm CMOS	28nm CMOS	16nm FinFET
85%A/15%D	80%A/20%D	75%A/25%D	70%A/30%D	60%A/40%D	40%A/60%D

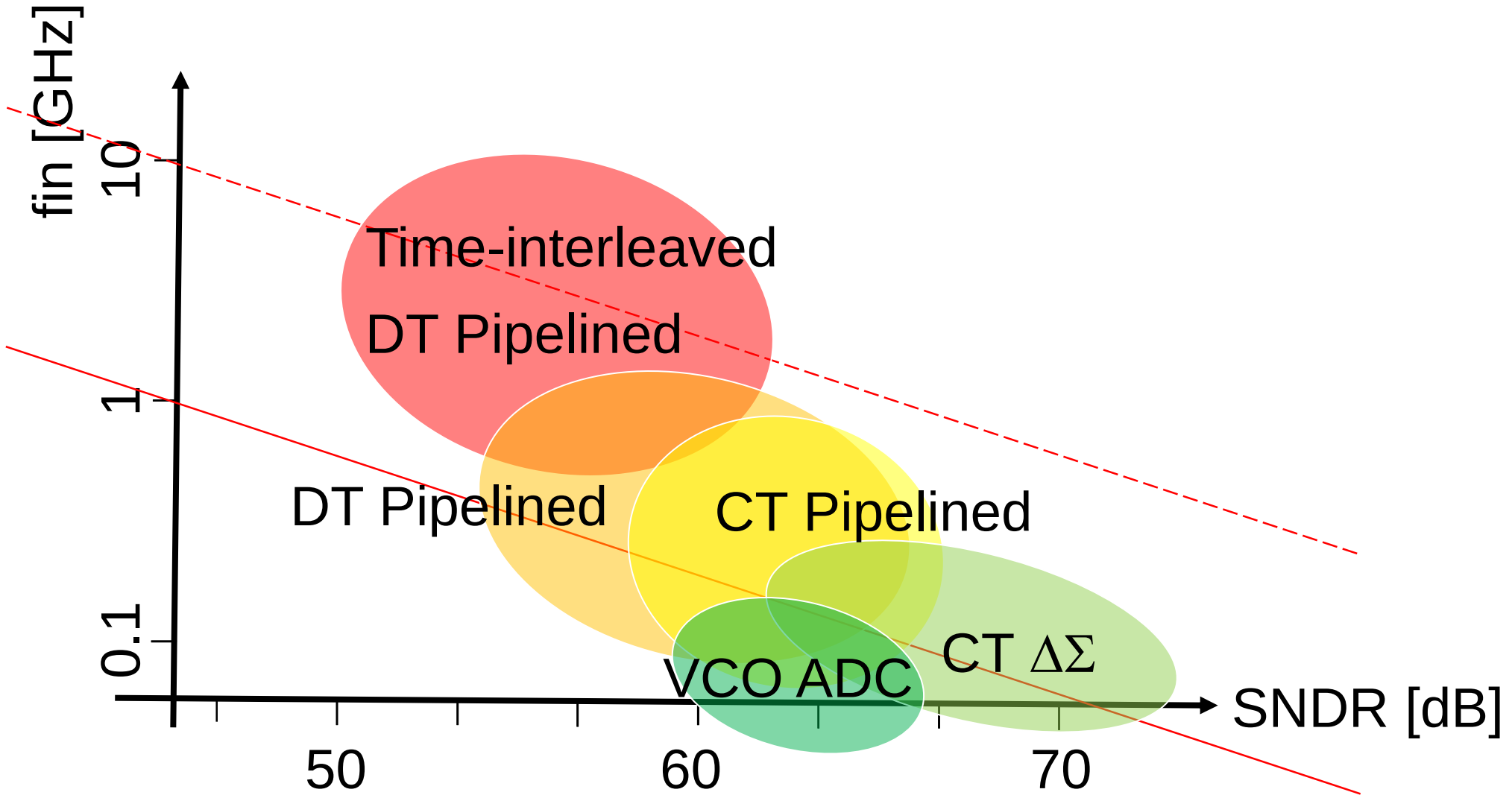
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Architectures (no one fits all): ADC “Aperture plot” (i.e. Bandwidth vs. Dyn Range or sample rate vs. resolution)



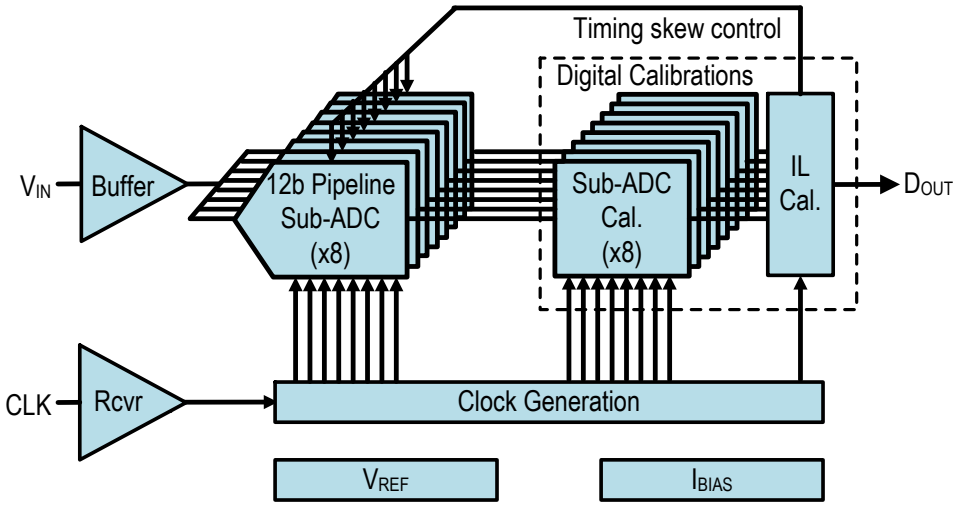
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

ADI's ADC architectures: one cannot fit all

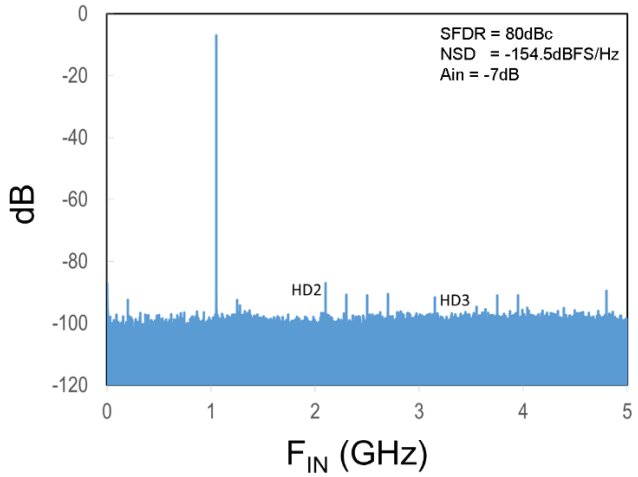


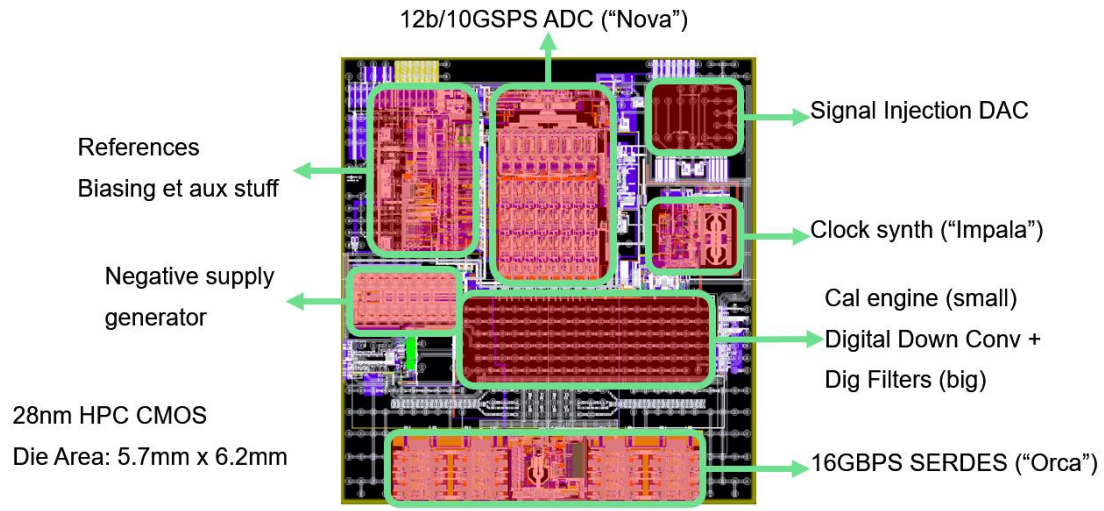
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

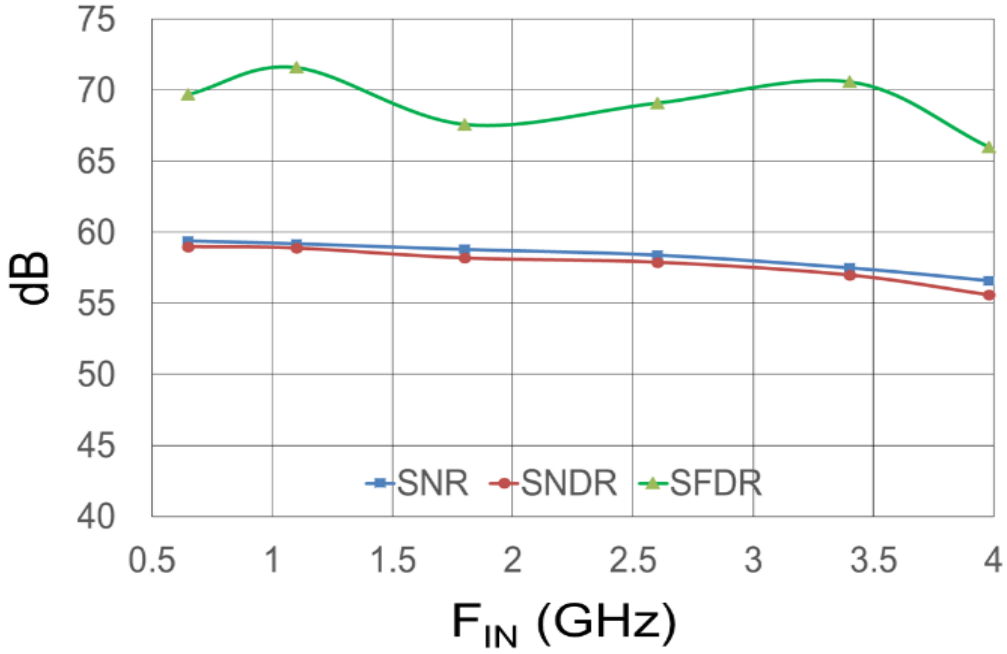
12b/10GSPS ADC: 8x interleaved Analog to Digital converter



Resolution	12b
F_{SAMPLE}	10GS/s
SNR	56dB
SNDR	55dB
SFDR	66dB
Input fin	4GHz
Power	2.9W
FOMS_HF	147dB
BW	7.4GHz
DR	60dB
$NSD_{small-signal}$	-157dBFS/Hz
Technology	28nm

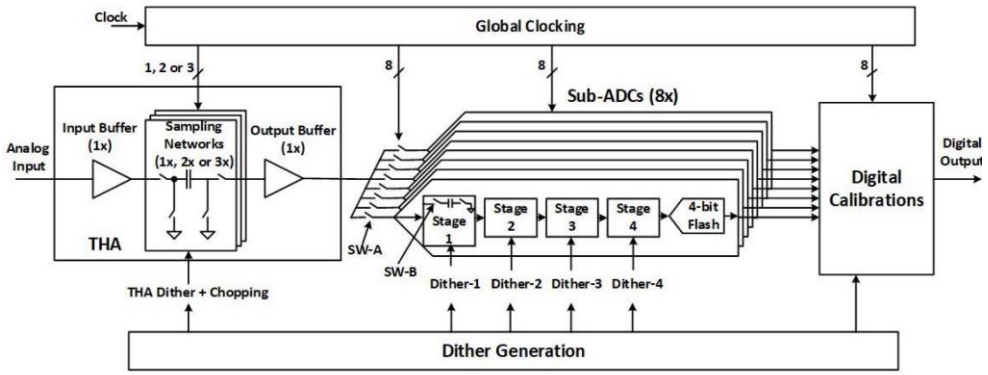




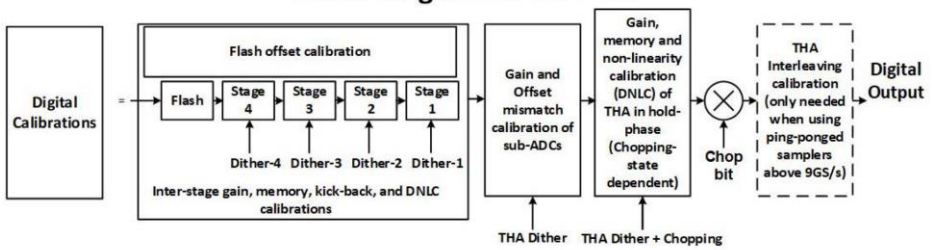


ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

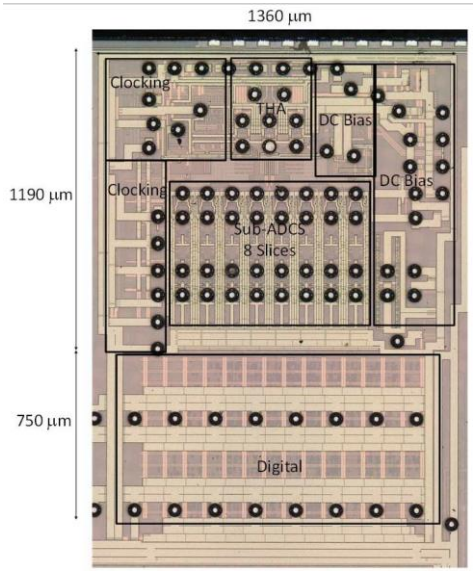
12b/18GSPS ADC: 8x interleaved Analog to Digital converter



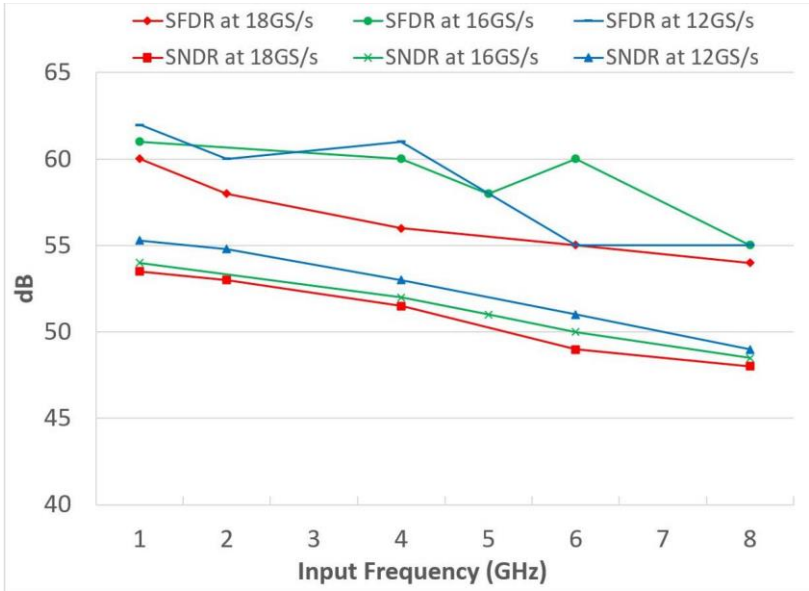
Block Diagram of the ADC



Block Diagram of the Digital Calibrations

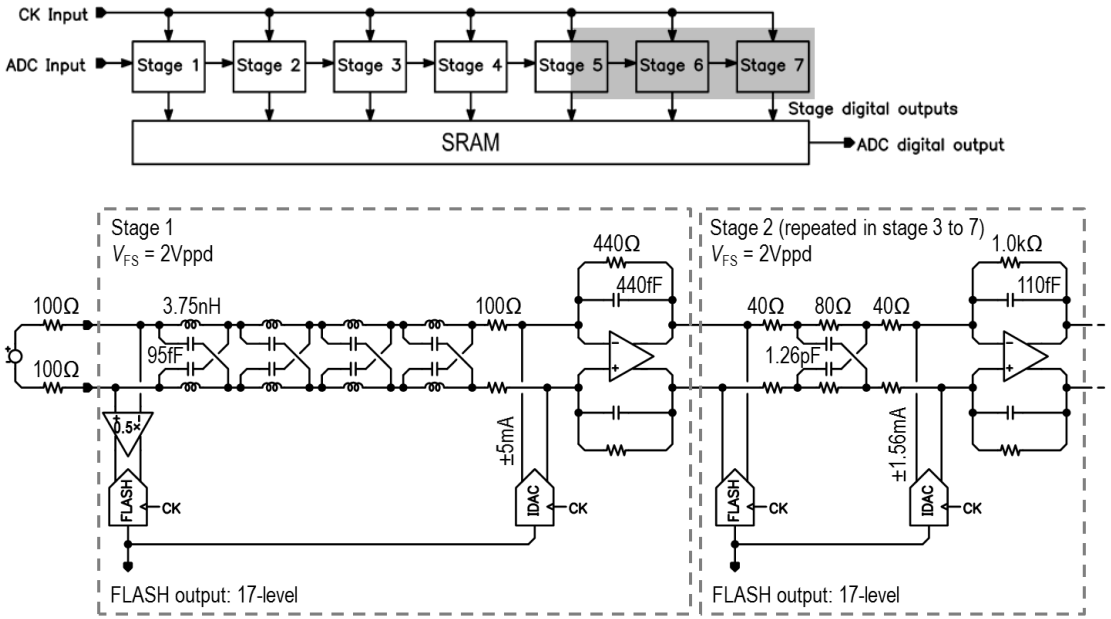


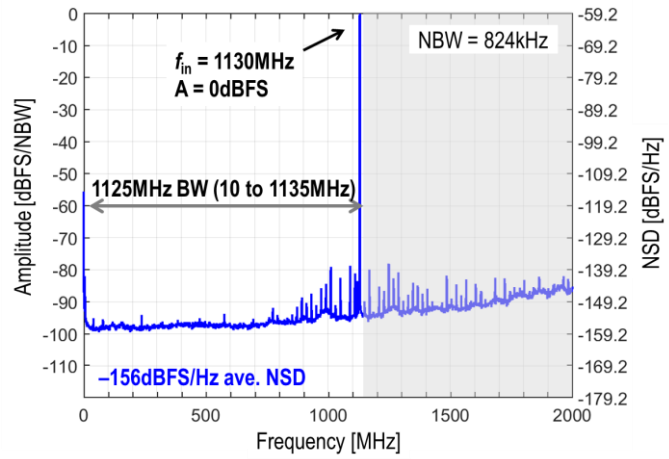
	This Work			
Sampling Rate (Fs)	18 GS/s		12 GS/s	
Resolution (bits)	12		12	
Input BW (GHz)	18		18	
Power (W)	1.3		0.85	
Noise Floor (dBFS/Hz)	-157		-157	
Fin (GHz)	4	8	2.5	4
SNDR at Fin (dB)	52	48	54.5	53
SFDR at Fin (dB)	56	54	60	61
Schreier FOM (dB): FOMS_HF=SNDR+10log(Fs/(2*Power))	150.4	146.4	153	151.5
Walden FOM (fJ/step): FOMW_HF=Power/(Fs*10$^{(SNDR-1.76)/20}$)	222	351.9	163.3	194.1
THA or input buffer	THA		THA	
Sampling time and BW mismatch	2-way or optional randomized (2+1)		2-way or optional randomized (2+1)	
Sub-ADC	Pipeline		Pipeline	
Area	2.6		2.6	
Process Technology	16nm FinFET		16nm FinFET	

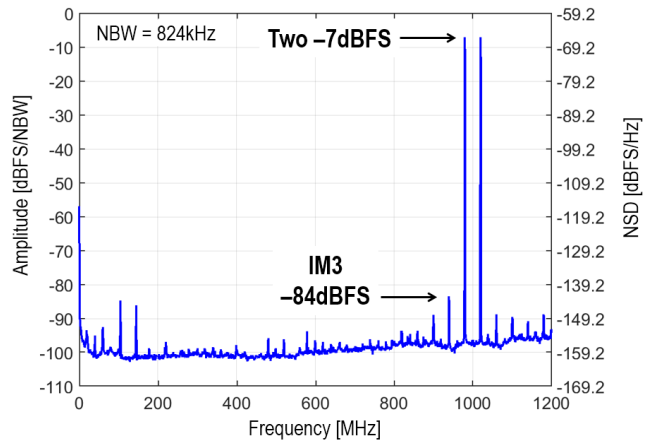


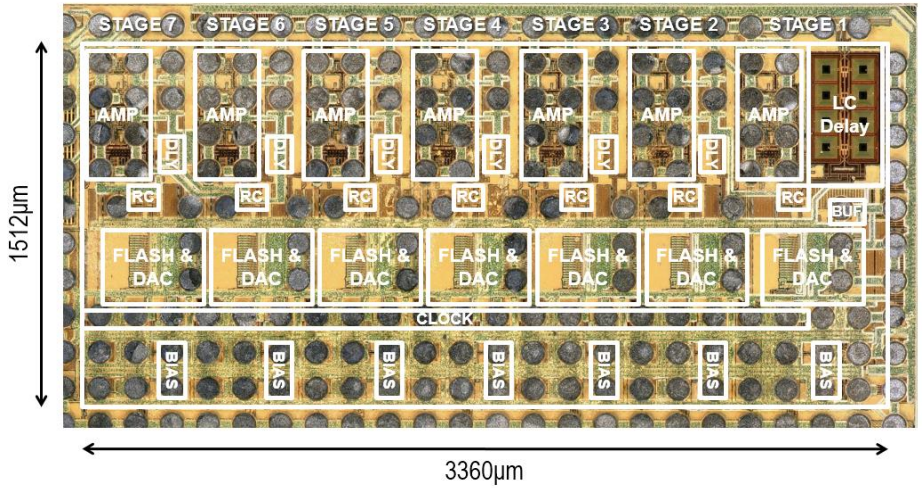
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

CT pipelined ADC Gen 1

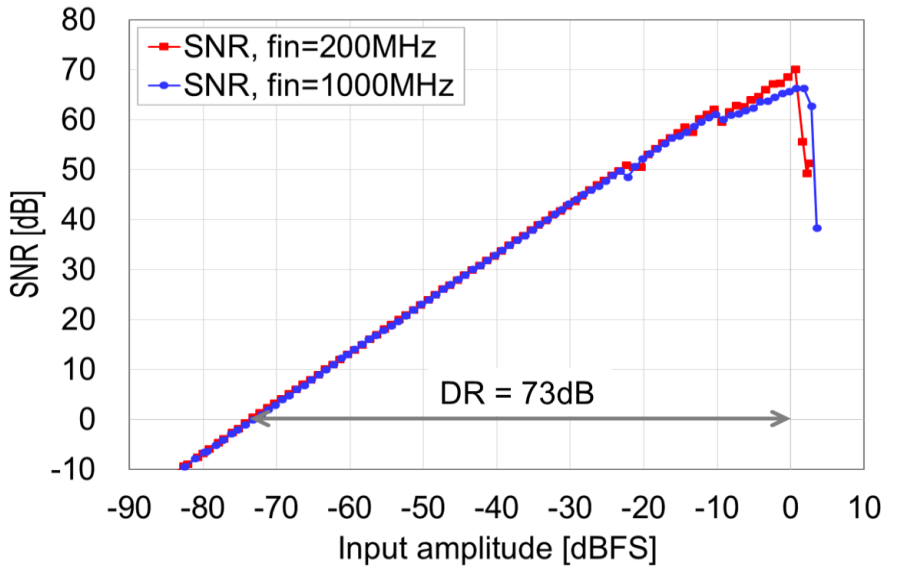








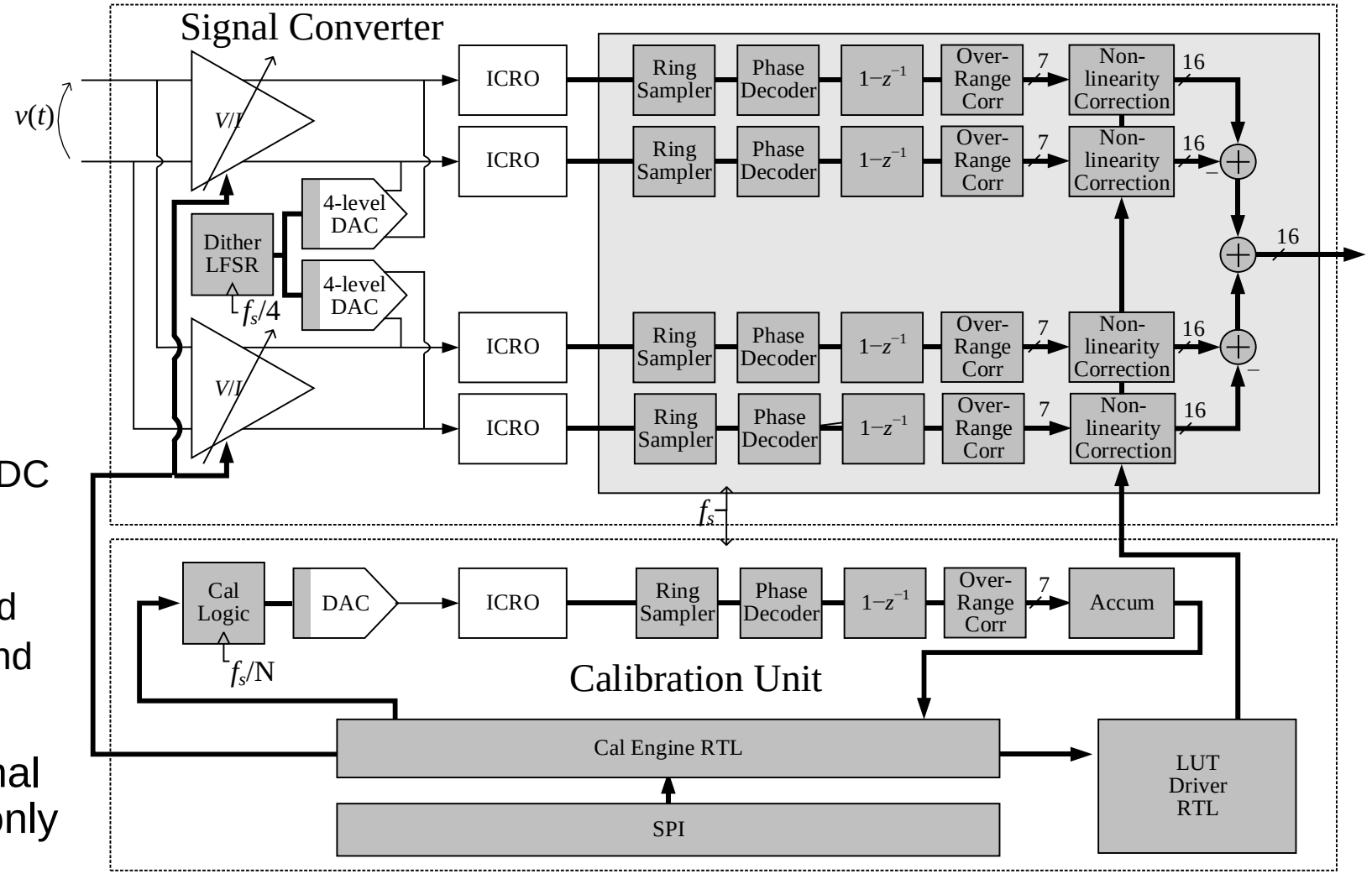
	This work
Architecture	CT pipeline
Inherent Anti-aliasing	Yes
Process Technology	28nm CMOS
f_S [GHz]	9
Raw BW = f_S / (2 OSR) [MHz]	1125
App BW = f_S / (2 App OSR) [MHz]	1125
App OSR	4.0
Small-signal NSD = DR + 10 log10(BW) [dBFS/Hz]	–164
Large-signal NSD (low f) = SNR + 10 log10(BW) [dBFS/Hz]	–160
Large-signal NSD (high f) = SNR + 10 log10(BW) [dBFS/Hz]	–156
IM3 [dBFS]	–84
HD2 [dBFS]	–79
HD3 [dBFS]	–86
SFDR [dB]	73
Area [mm²]	5.1
Power [mW]	2330
FOM_S = DR+10log$_{10}$(BW/P) [dB]	160



ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

VCOADC

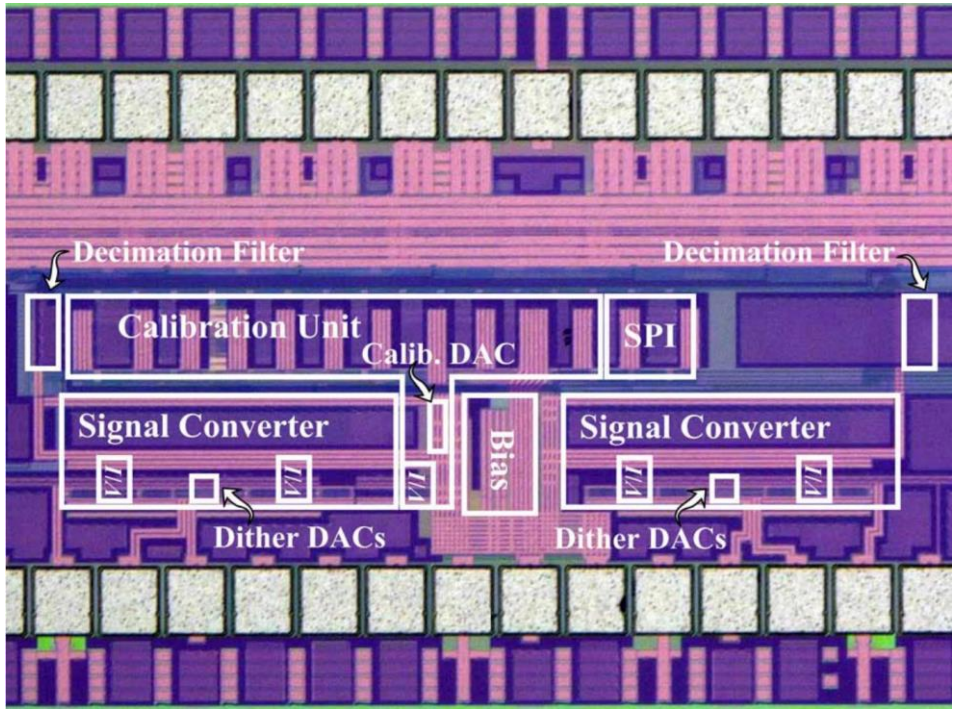
- Variable gain V/I
- Reconfigurable
  - f_s =1.1-2.2Gsps
  - BW=10-20-50MHz
  - NSD=-147 to -154dBFS
  - Power=7-30mW/adc
- SFDR > 85dBc
- Calibration:
  - Background calibration of replica ADC signal path.
  - All calibration engine logic included with ADC IP, no uController required
  - Continuous calibration or on-demand
  - Calibration period=15-30uS
- Manual layout for high-speed signal path, P&R for calibration engine only



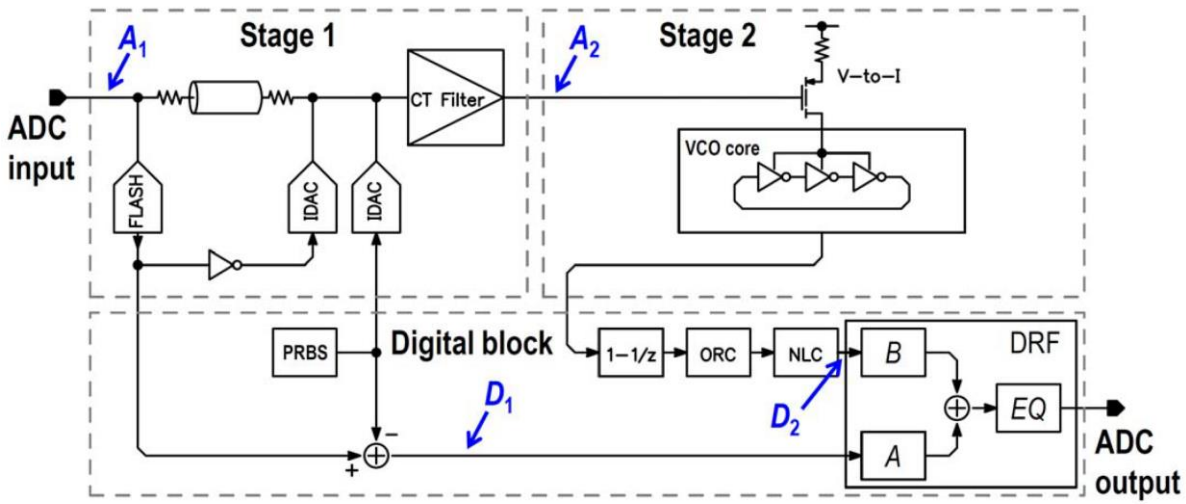
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

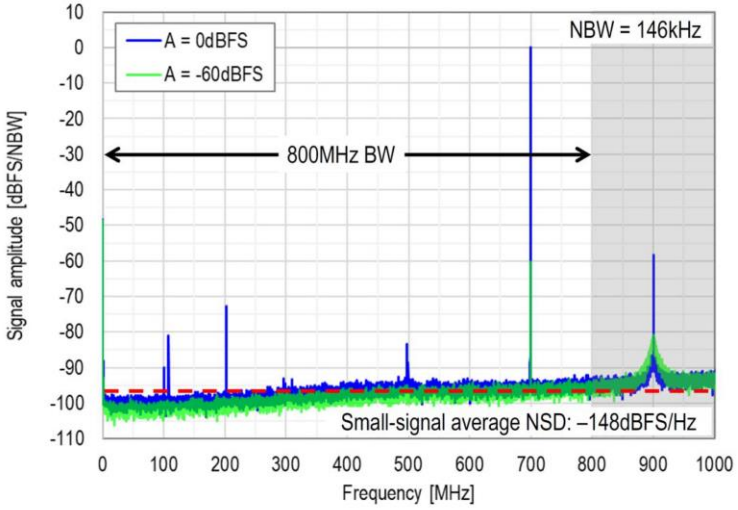
Why VCOADC?

- Area is 5-10x smaller than other ADCs with similar specs
- CT front end-> drive-able
- Mostly digital->Scalable

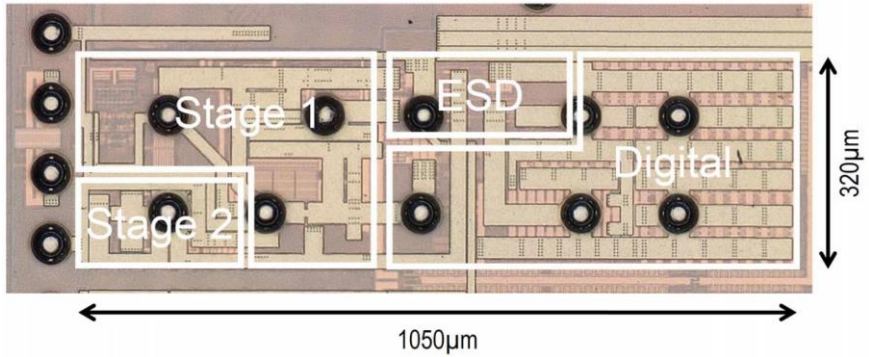


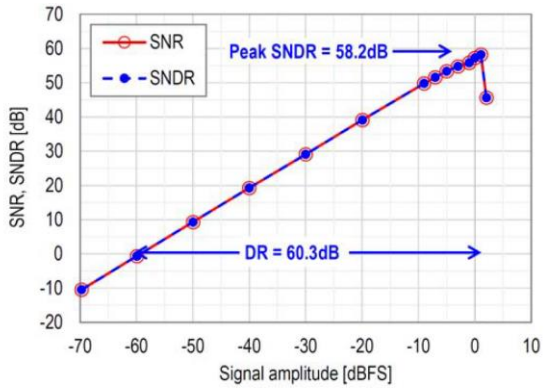
CT pipelined ADC Gen 2

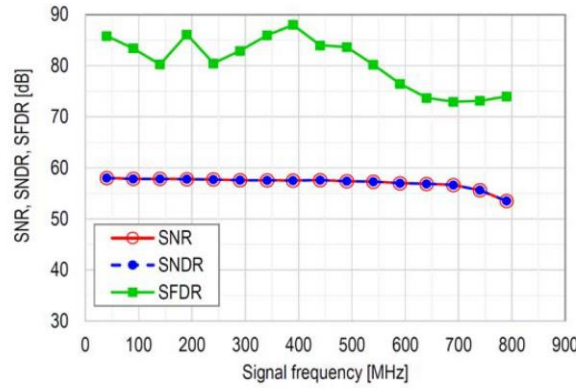


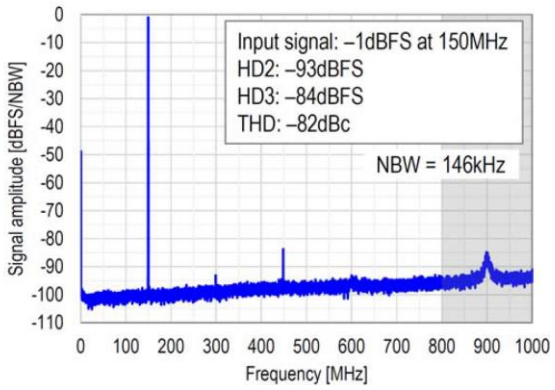


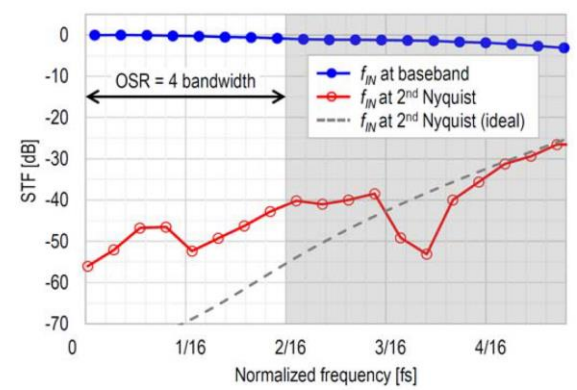
	This work	JSSC 2017 [1]
Architecture	VCO-based CT pipeline	CT pipeline
Inherent anti-aliasing [dB]	41	68
Process Technology	16nm FinFET	28nm CMOS
f_S [GHz]	6.4	9.0
Raw BW = f_S / (2 OSR) [MHz]	800	1125
App BW = f_S / (2 OSR) [MHz] (OSR ≥ 4 for all ADCs)	800 (OSR = 4.0)	1125 (OSR = 4.0)
Power [mW]	280	2330 **
Dynamic range [dB]	60	73
Peak SNDR [dB]	58	66
HD2 [dBFS]	–93	–79
HD3 [dBFS]	–84	–86
SFDR [dB]	73	73
Area [mm^2]	0.34	5.1 **
FOM_S = SNDR + 10 $\log_{10}$(BW / P) [dB]	153	153 **









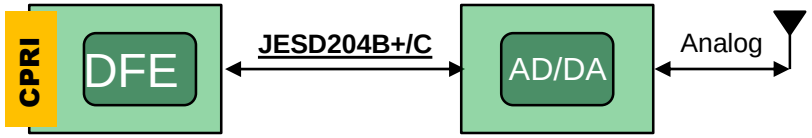


ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

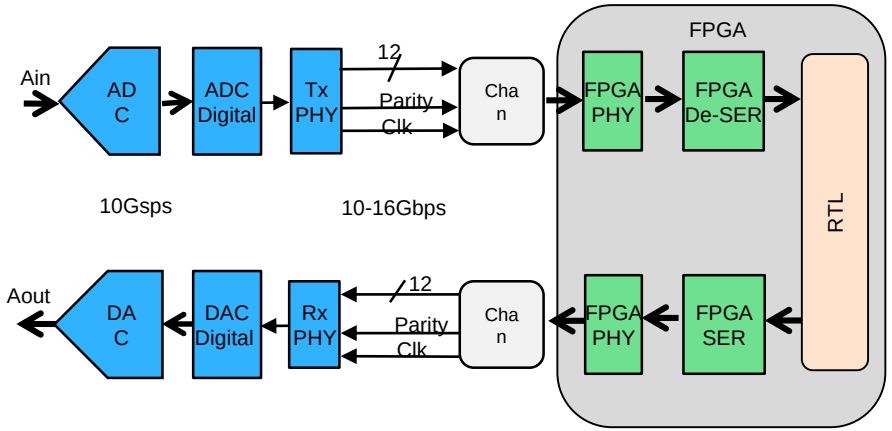
Integrated Systems: SoCs/SiPs with Mixed-Signal + Embedded DSP Capability

Interfaces: JESD204B/C, High Speed Parallel and Ultra Short Reach



Optimised for 20cm on PCB

USR/ASIC target integration in 70mm x 70mm laminate



JESD204B/C

- **Core1 – 16.2Gbps, 8 pJ/b**
- **Core 2 – 25Gbps, 9.4 pJ/b**

USR - Ultra Short Reach Interface (2pJ/b)

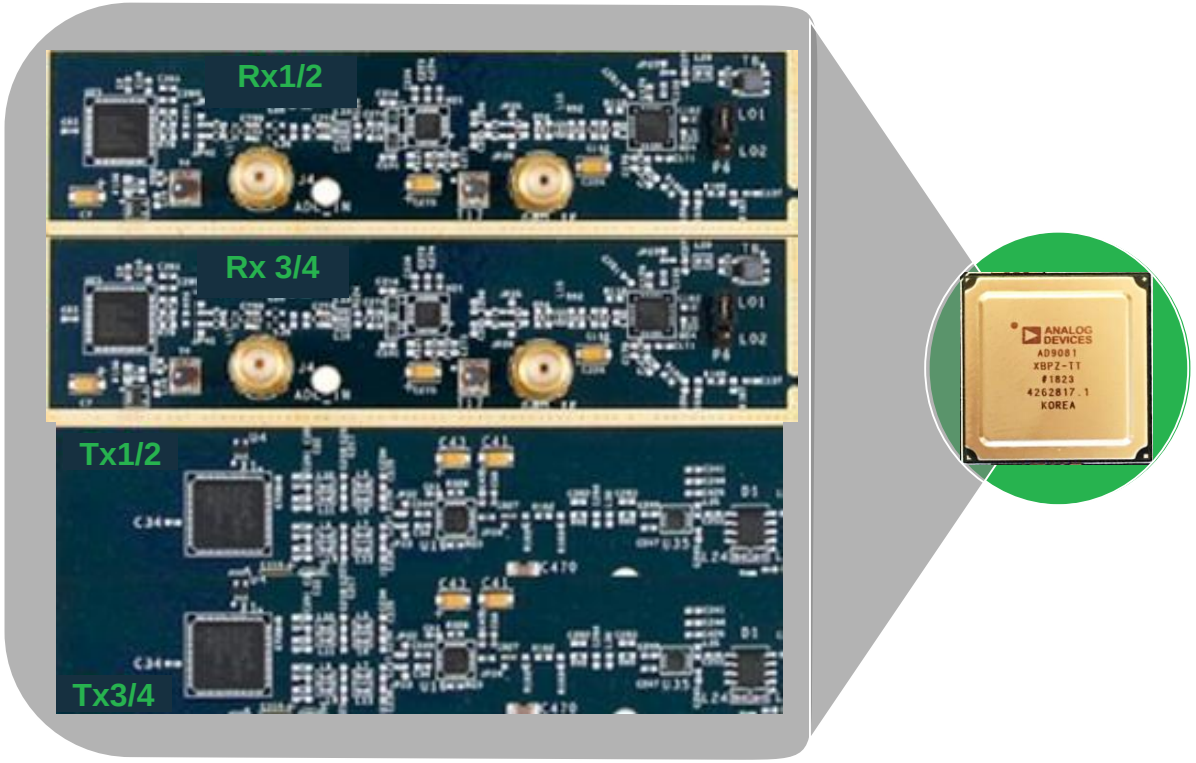
- **Goal - Scalable, Power Efficient (2 to 4pJ/b) Interface for SIP and near-Package connect**
  - Spans OIFCEI 28G USR and VSR channels
- Lane Rates – 10-28Gbps

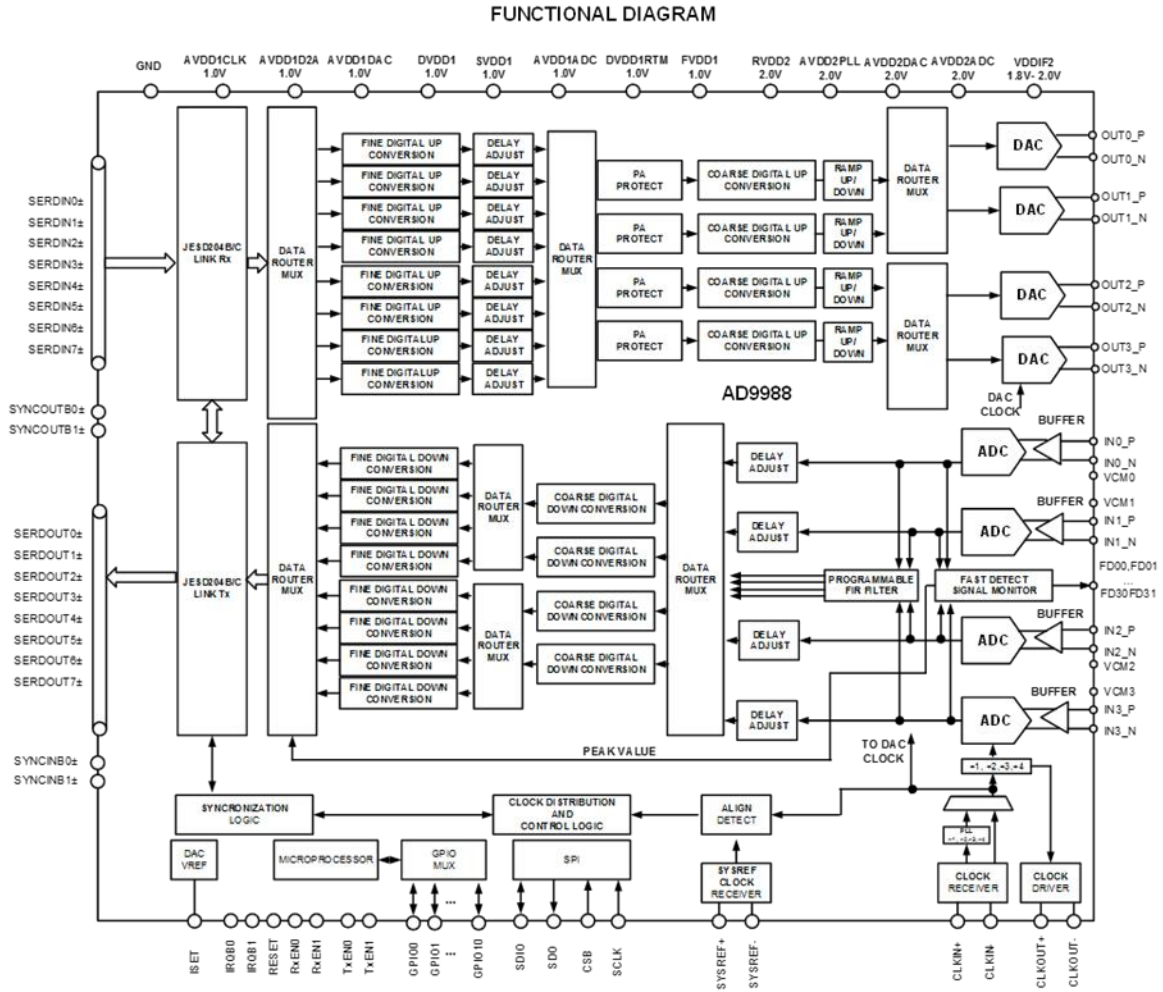
HSP – High Speed Parallel Interface (8pJ/b)

- **Goal – Enable Ain to Aout Latency < 100ns**
- **Clock Forwarded Architecture**
  - No CDR, Limited FIFOs, may not need PLL
- **Benefits**
  - Signal Path Latency <100ns
  - 30% FPGA Power Reduction vs. JESD

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

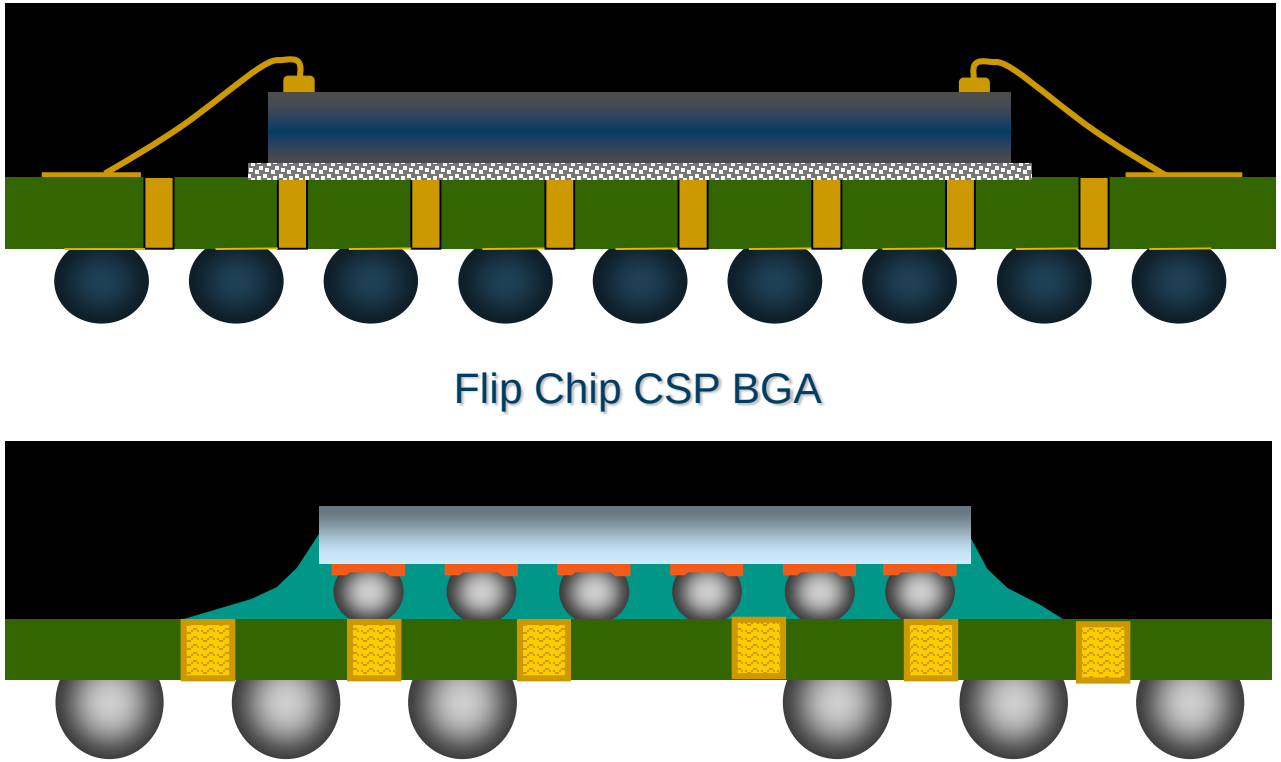
quad Tx / quad-dual Rx fully integrated wideband MxFE





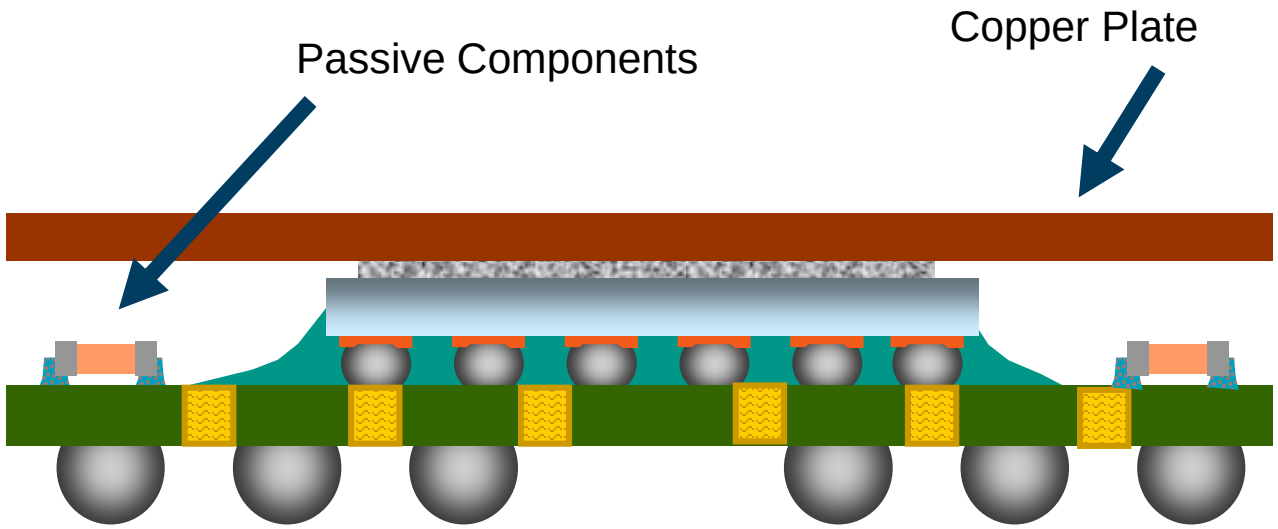
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Flip Chip Chip Scale Package BGA

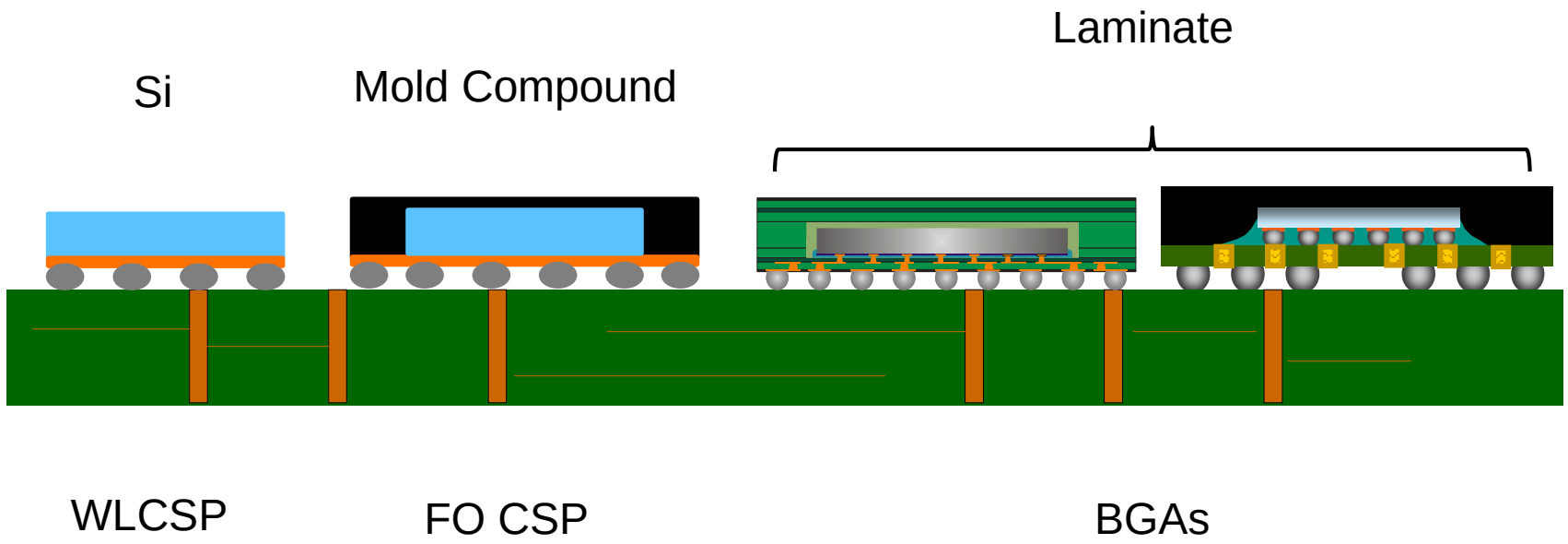


Flip Chip CSP BGA

Flip Chip – Thermally Enhanced BGA

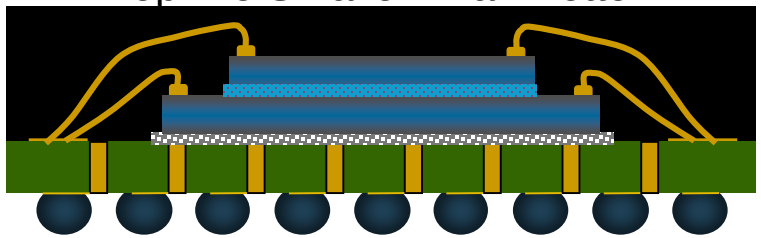


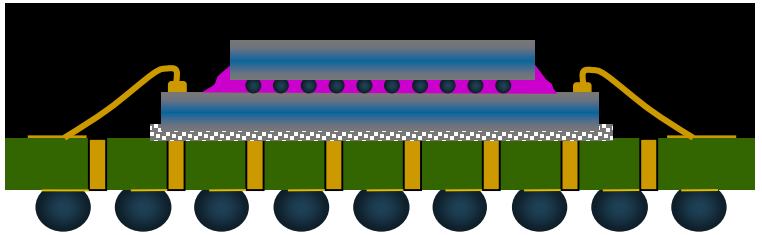
Higher frequency performance



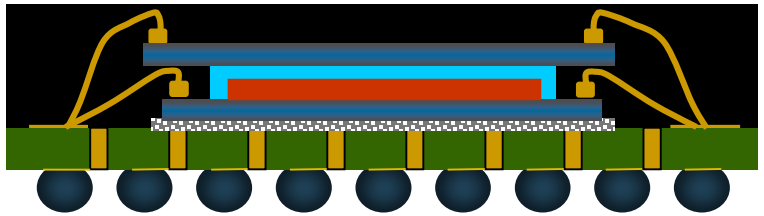
3D Packaging

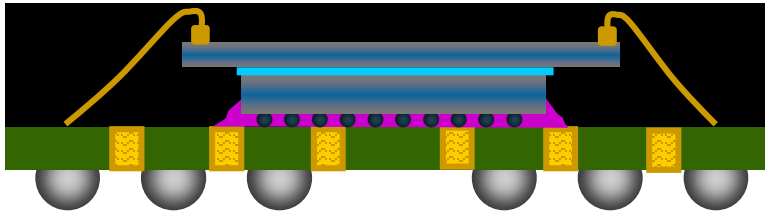
“Pyramid”
Top Die Smaller Than Bottom





Top Die Same Size or Larger
Than Bottom

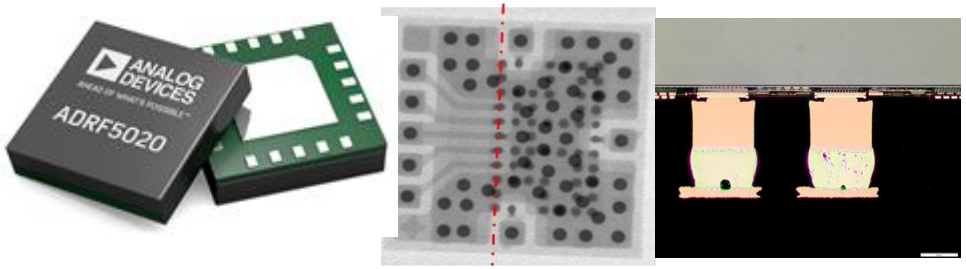




Wirebond Versions

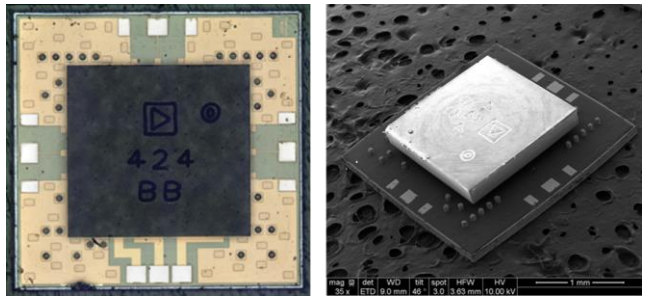
Bumped Die Flip Chip Versions

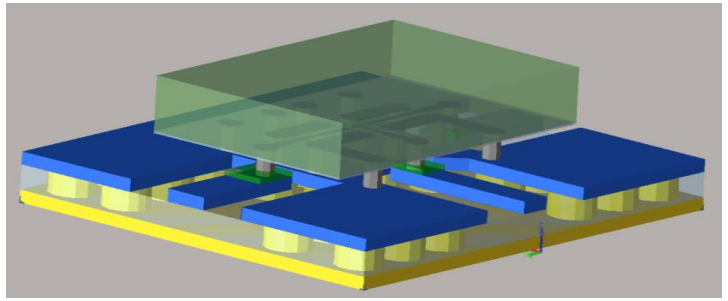
mmWave front-end modules



FlipChip on Laminate (LGA)

Die-On-Carrier (DOC)
“Die-like” RF Product

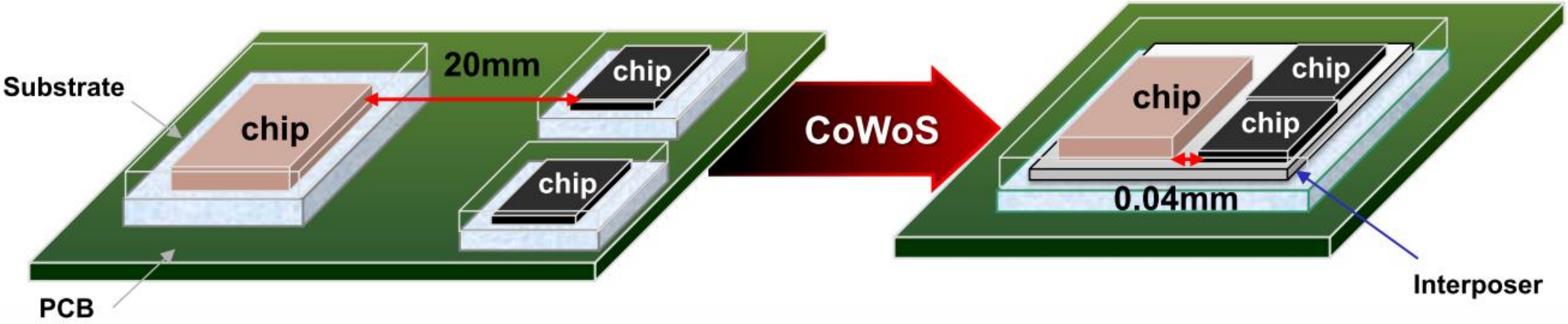


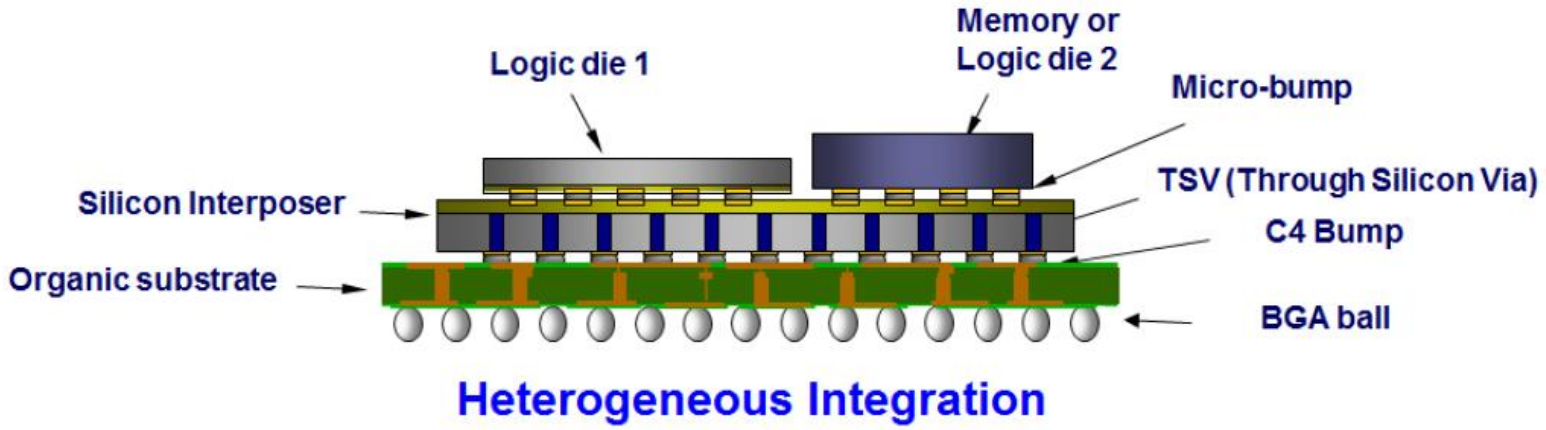


Bumped Flip Chip (SMT Assembly)

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Interposer Systems in a Package



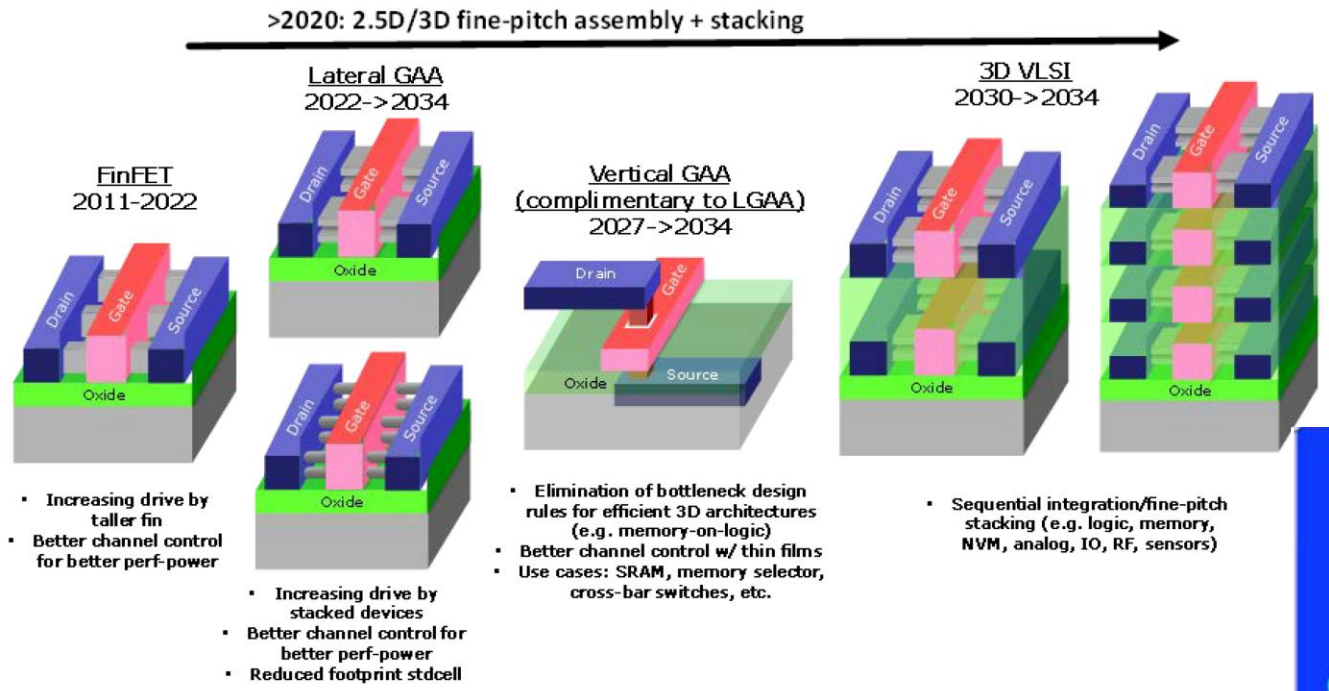


Heterogeneous Integration

TSMC's CoWoS® (Chip-on-Wafer-on-Substrate) Services, https://www.tsmc.com/english/dedicatedFoundry/services/cowos.htm

P. Gupta and S. S. Iyer, "Goodbye, Motherboard. Hello, Silicon-Interconnect Fabric", IEEE Spectrum, Sept 2019

Evolution of VLSI into 3D: density!



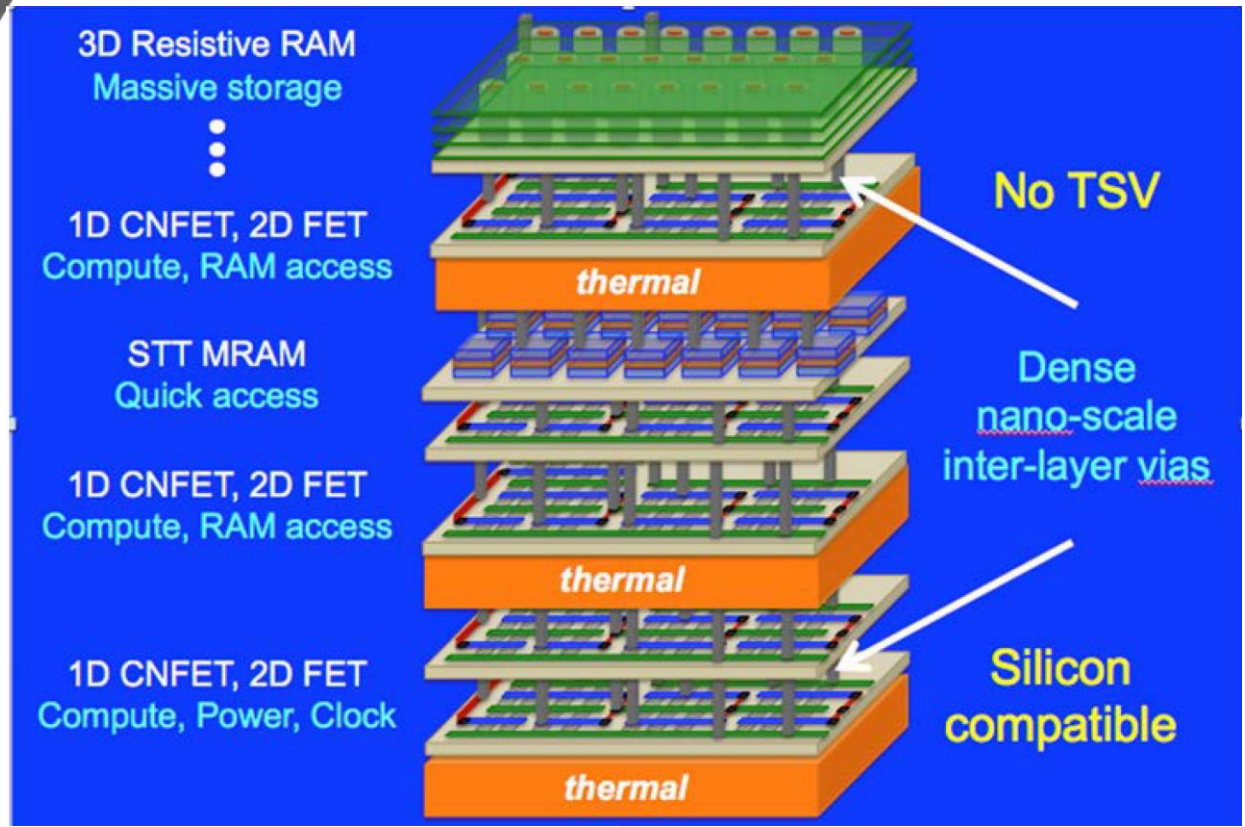
International Roadmap for Devices and Systems (IRDS) – 2018 Edition.

Main advantages:

- Density
- Power efficiency
- Mitigation of local interconnect issues

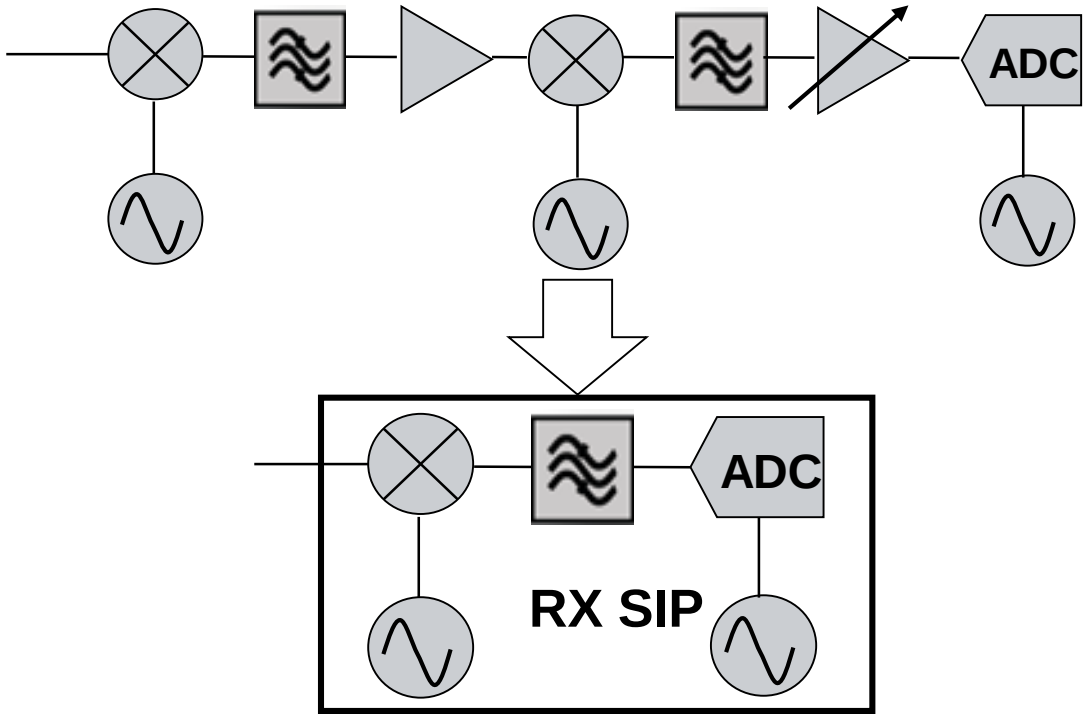
Main challenges:

- Cost
- Heat management

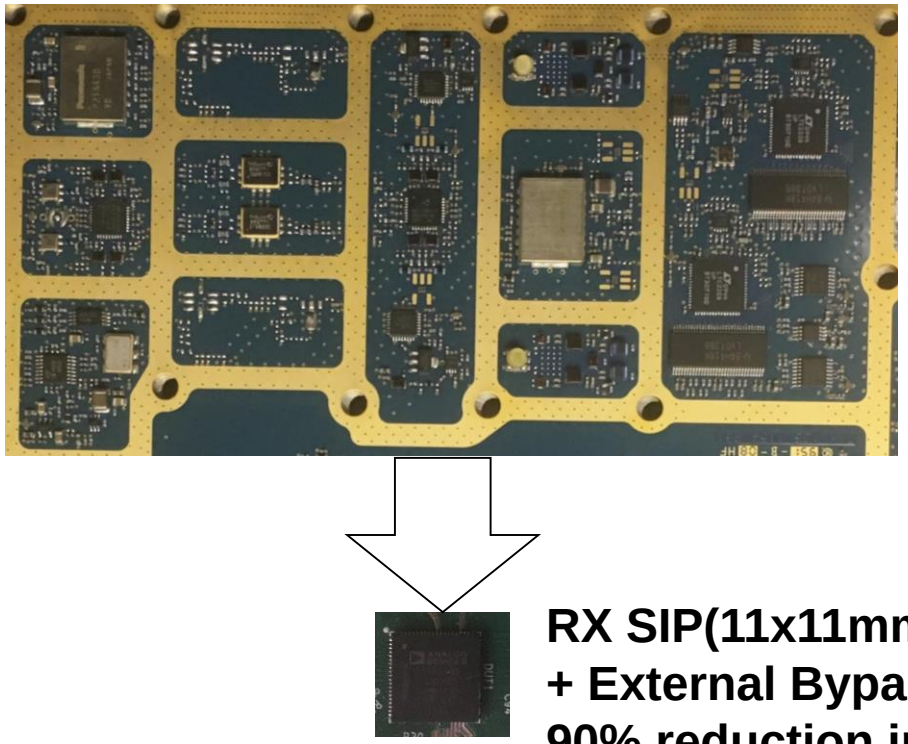


Why do a SiP?

Traditional Receiver Architecture

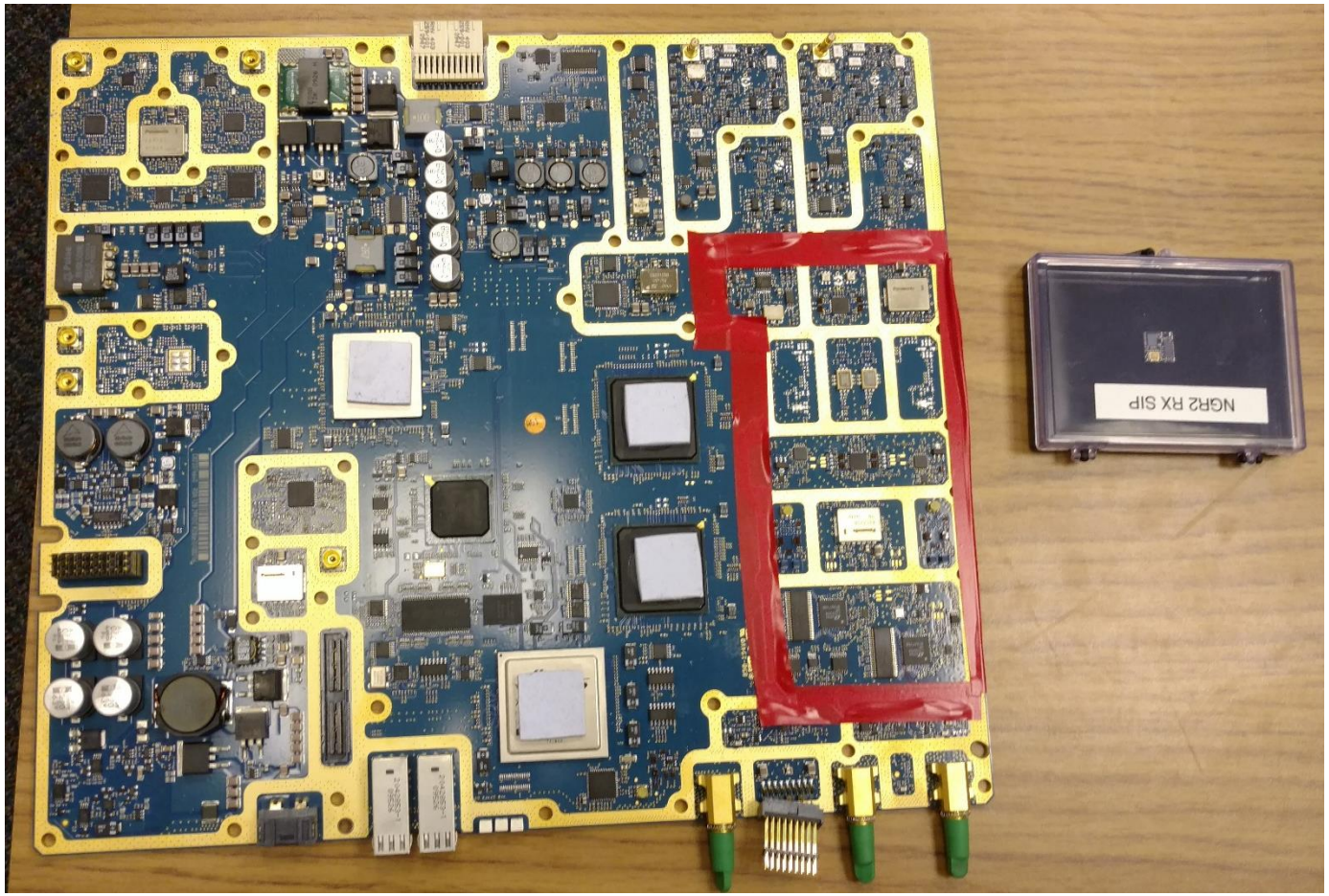


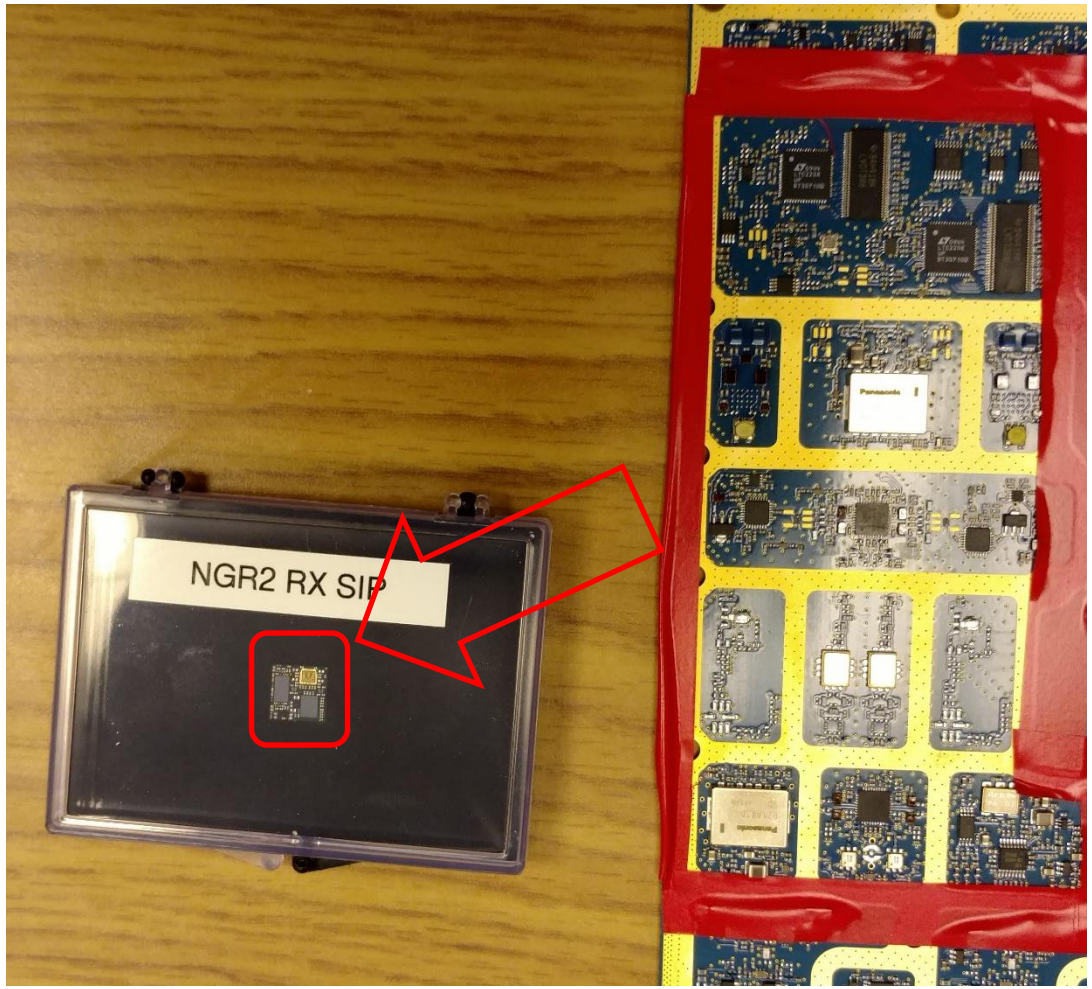
Traditional Base Station Board



RX SIP(11x11mm)
+ External Bypass
90% reduction in Board Area

Real BTS's TRx board

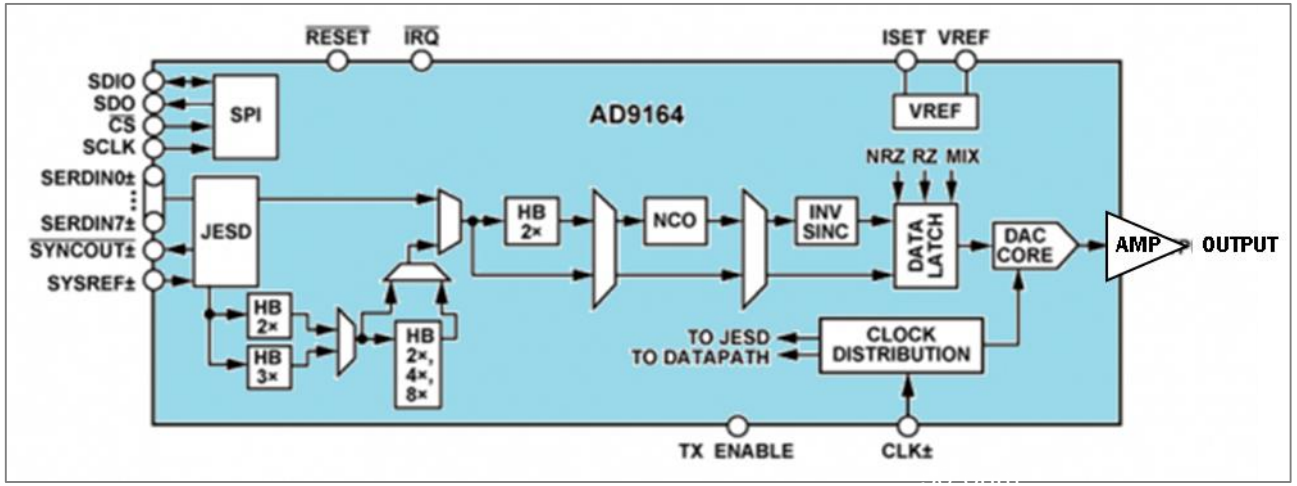




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

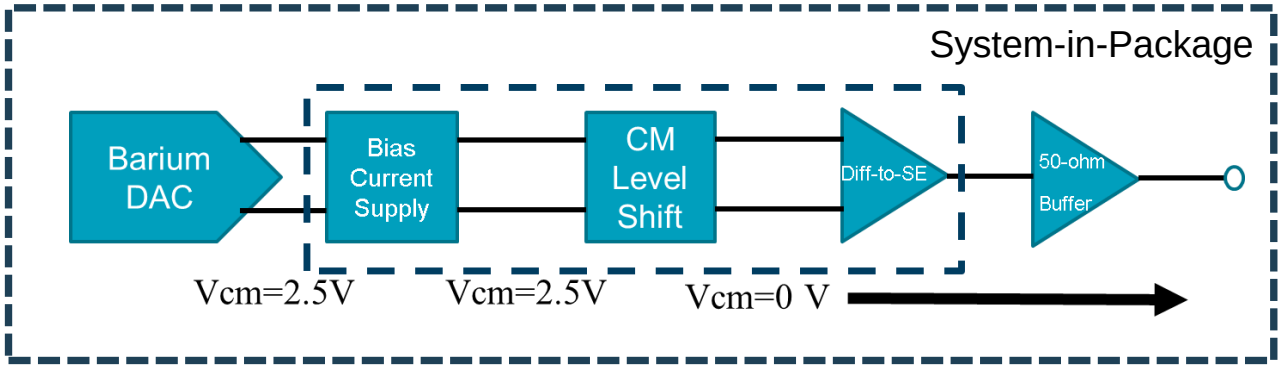
16-bit 12.0 GSPS RF DAC with Integrated Buffer

- Direct-to-RF synthesis up to 5GHz with 2.5 GHz maximum signal bandwidth
- Integrated amplifier reduces the overall cost of the system simplifies the design, and extends the overall broadband performance
- High-Dynamic range, ultra wideband and flexible frequency planning
- Enables software configurable radio transmitter with configurable data path signal processing functions



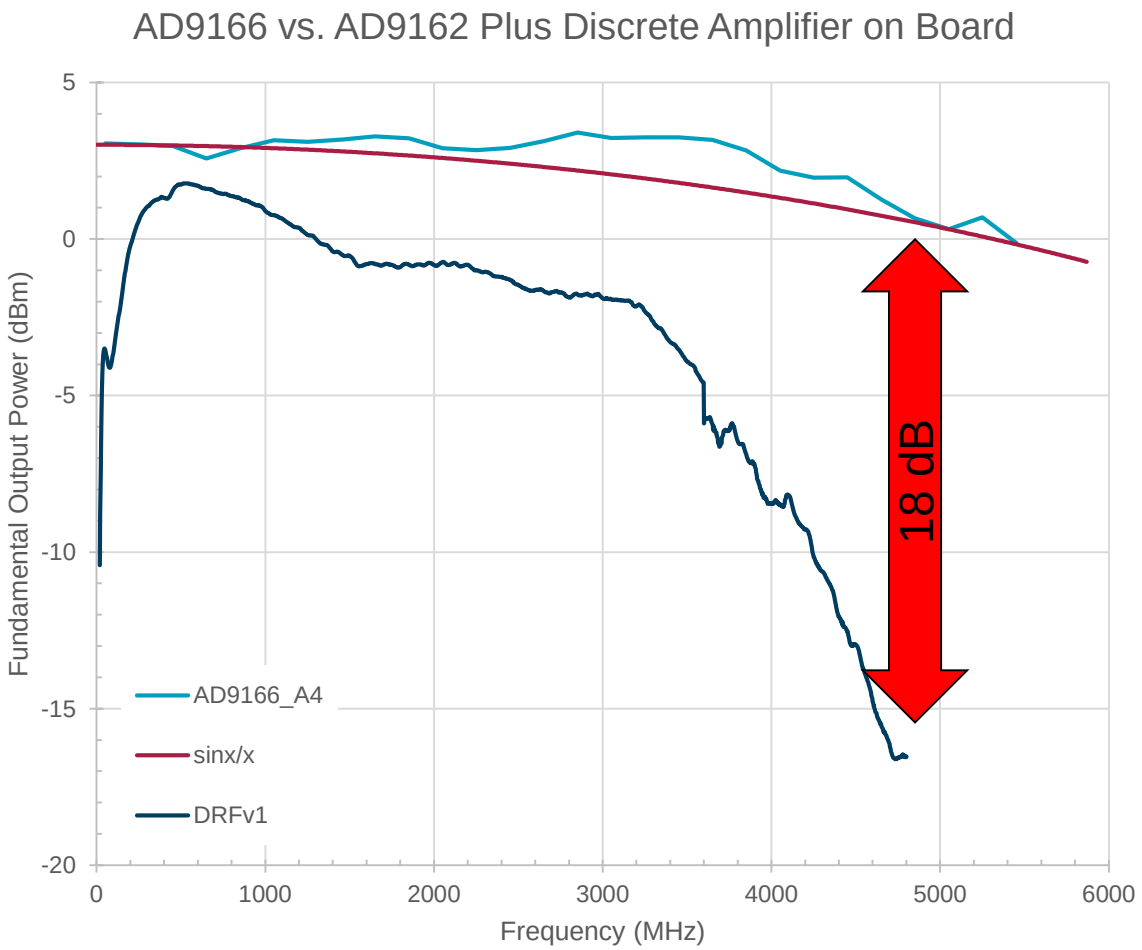
Key Benefits

- Flexible frequency planning with multiple DAC rates and interpolation modes available for synthesizing the same RF frequency
- Common hardware platform for flexible and reliable RF design
- Absorbs analog RF functions into configurable digital domain and eliminates IF low pass filters and analog up-conversion imperfections
- Eliminates IF-to-RF up-conversion stage and LO generation lowering overall system power consumption
- Integrated amplifier extends operation to DC and provides bandwidth flatness out to 5GHz.

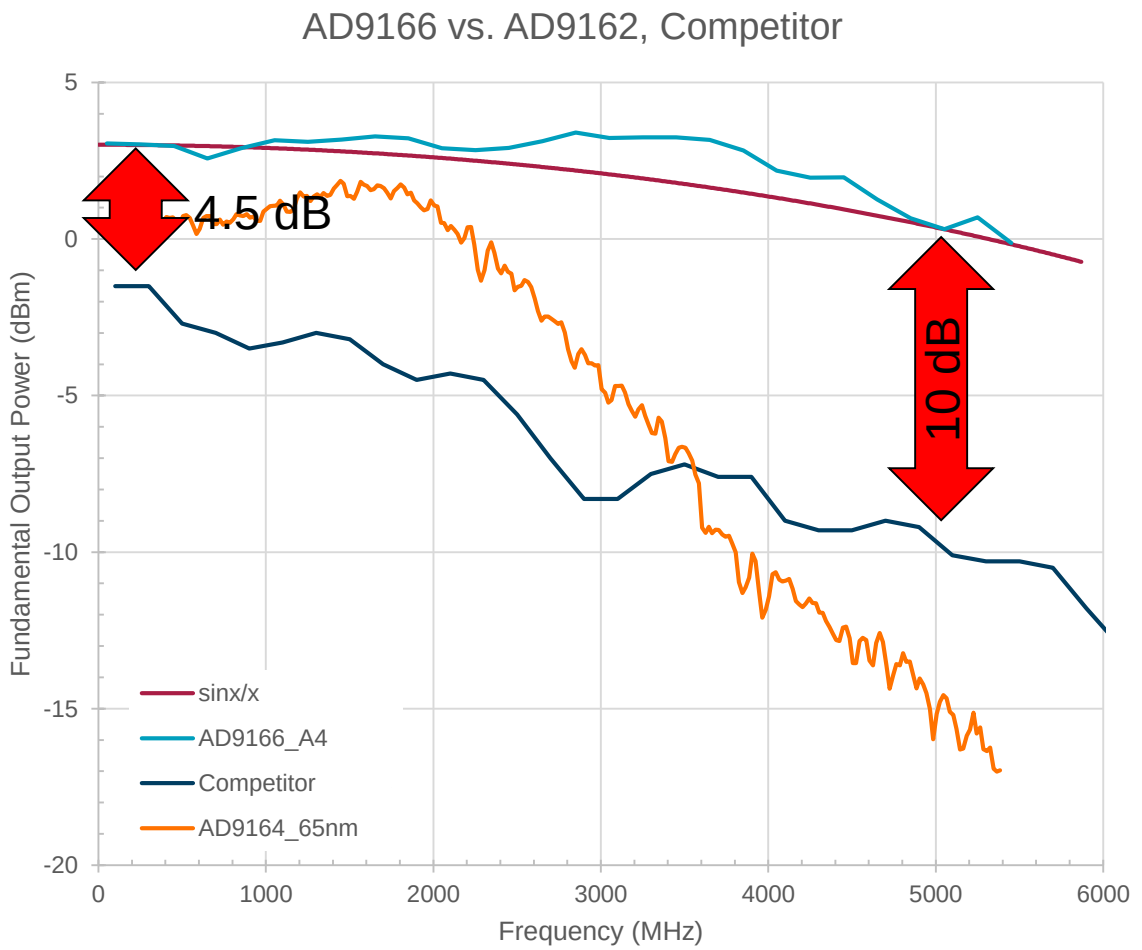


Frequency Response

- AD9166



- AD9166 vs. Competitor



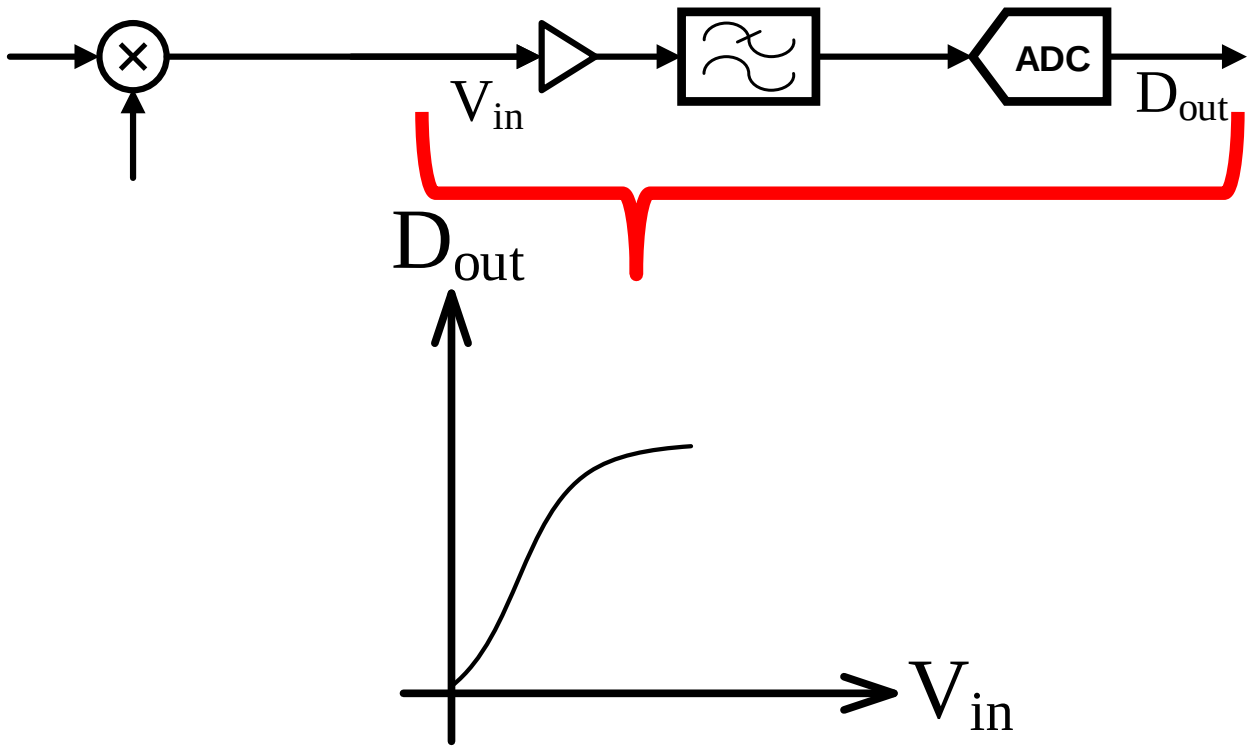
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

ANALOG DEVICES

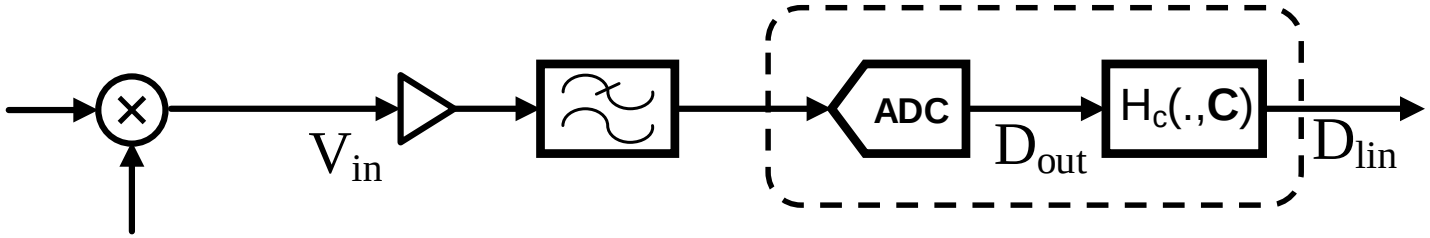
AHEAD OF WHAT'S POSSIBLE™

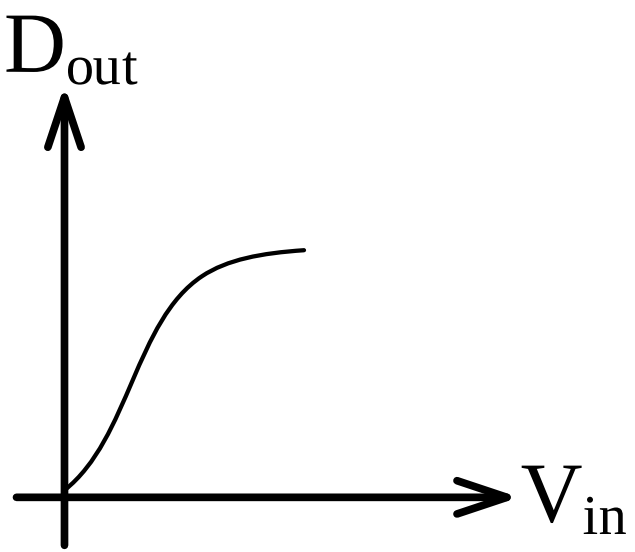
Algorithmic Capability: System-level Linearization

Non-linear Correction for Rx Signal Chain



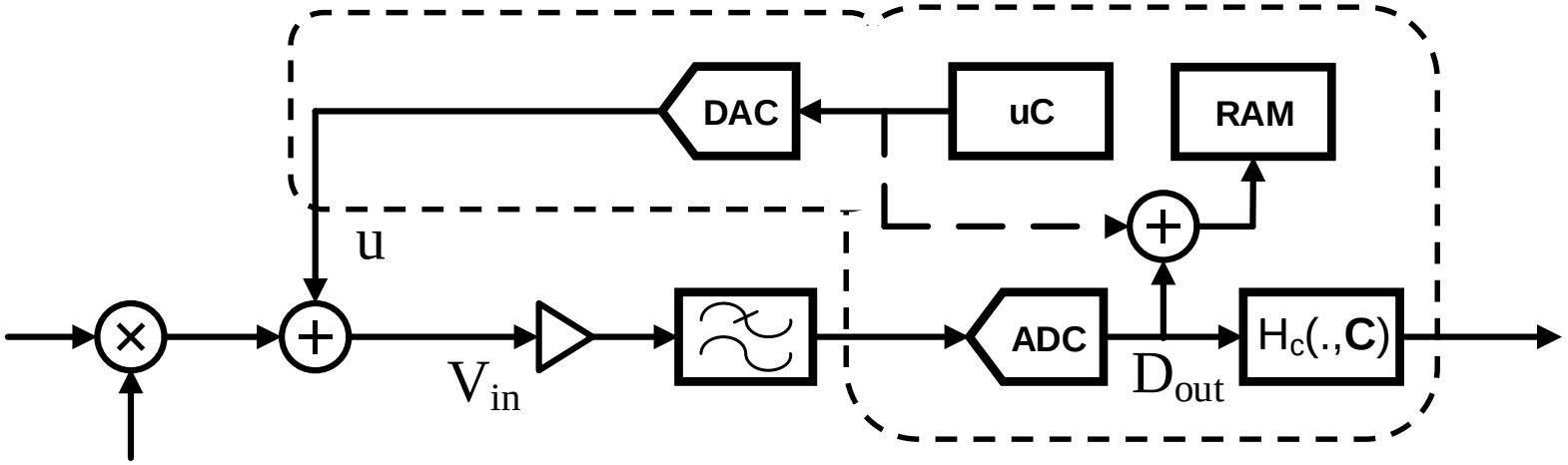
Non-linear Correction for Rx Signal Chain

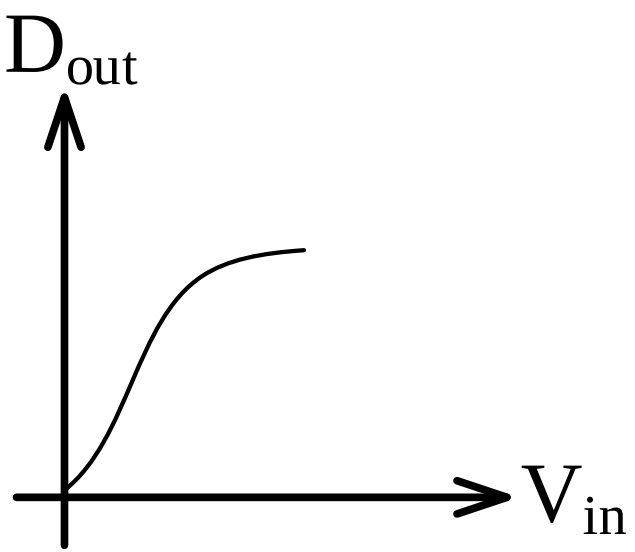




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

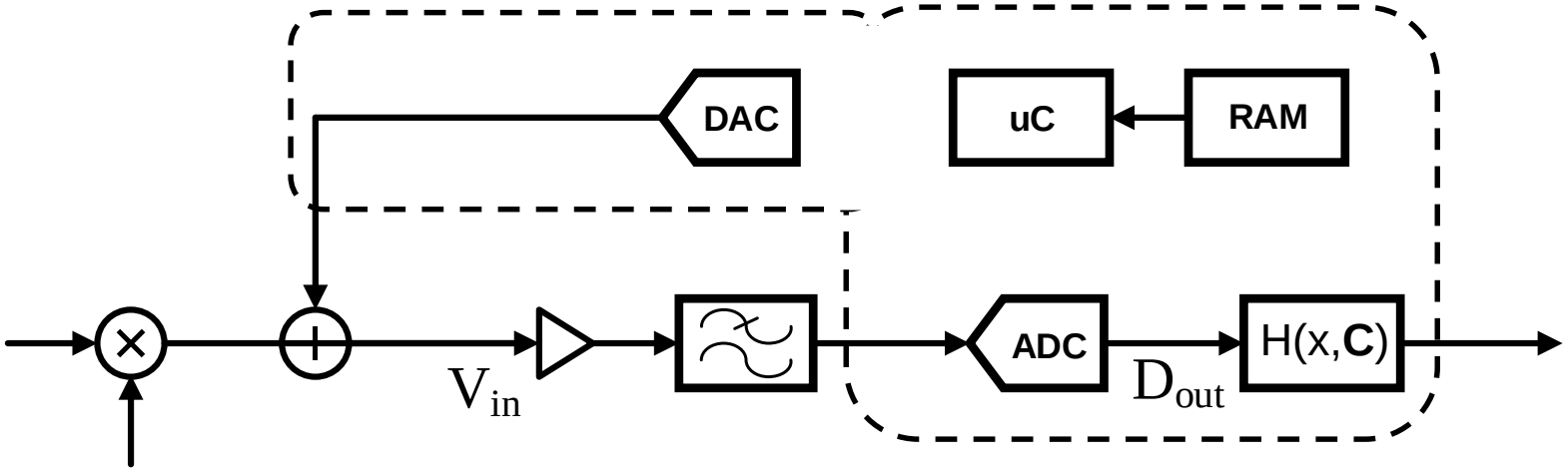
Non-linear Correction for Rx Signal Chain

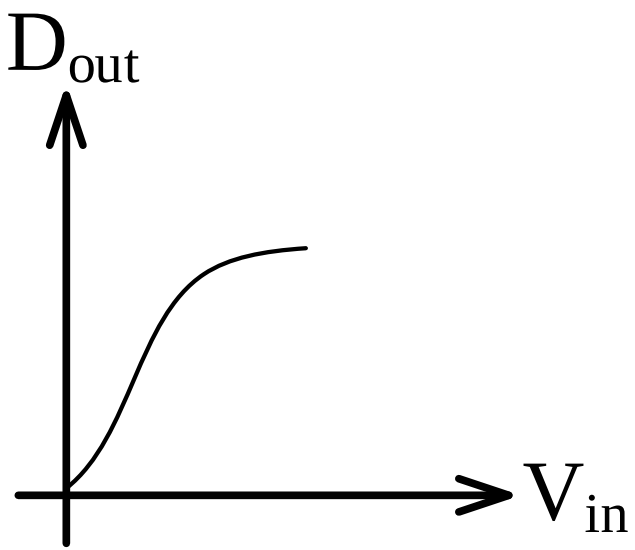




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

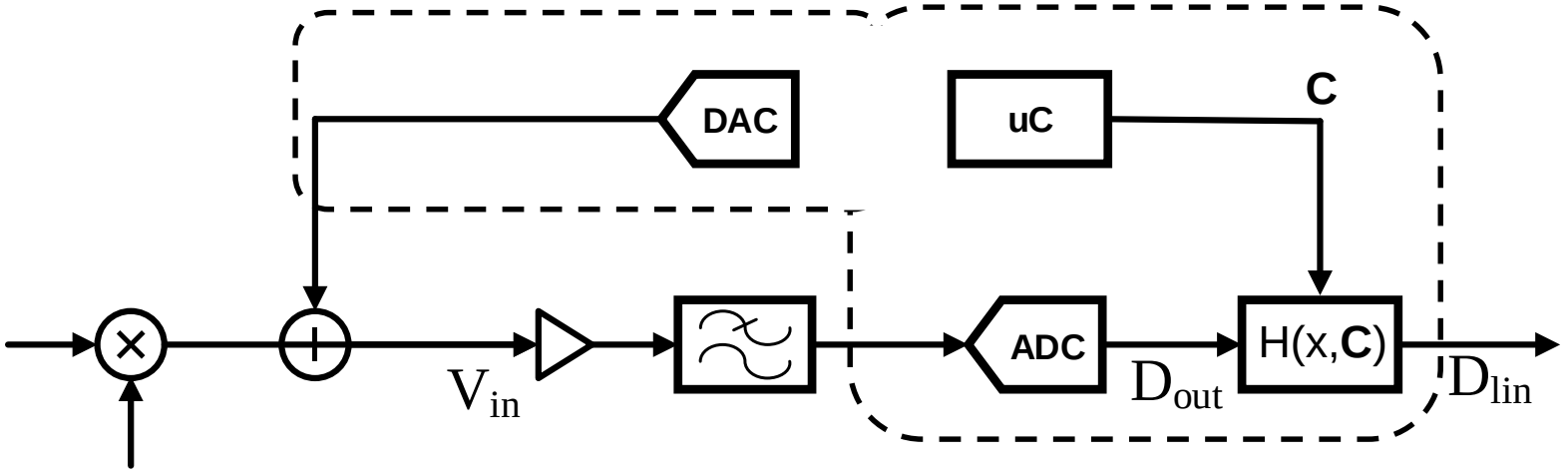
Non-linear Correction for Rx Signal Chain

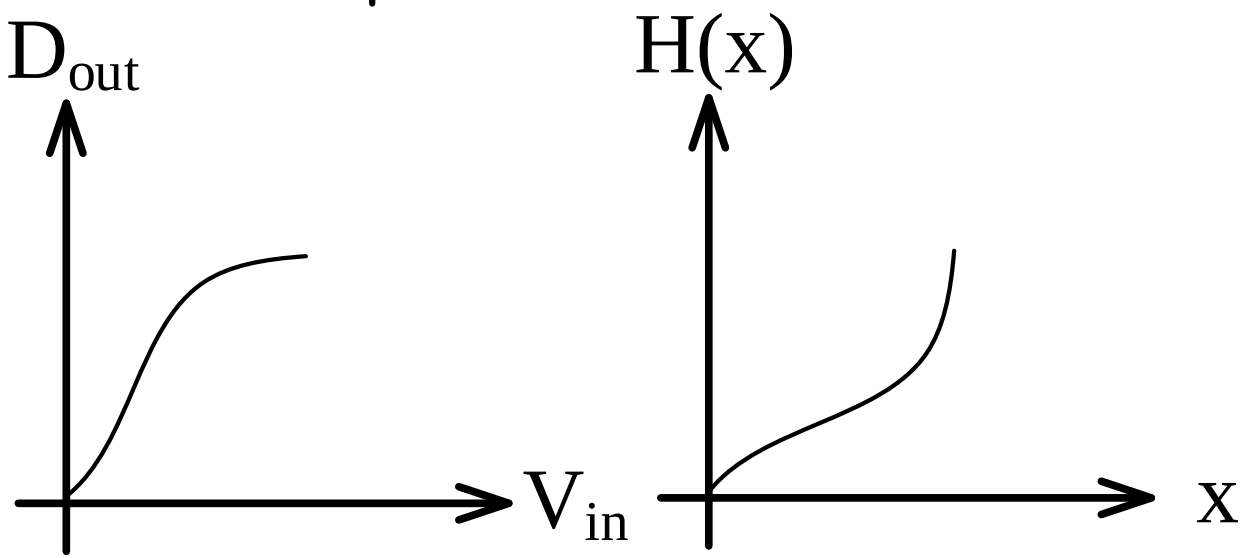




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

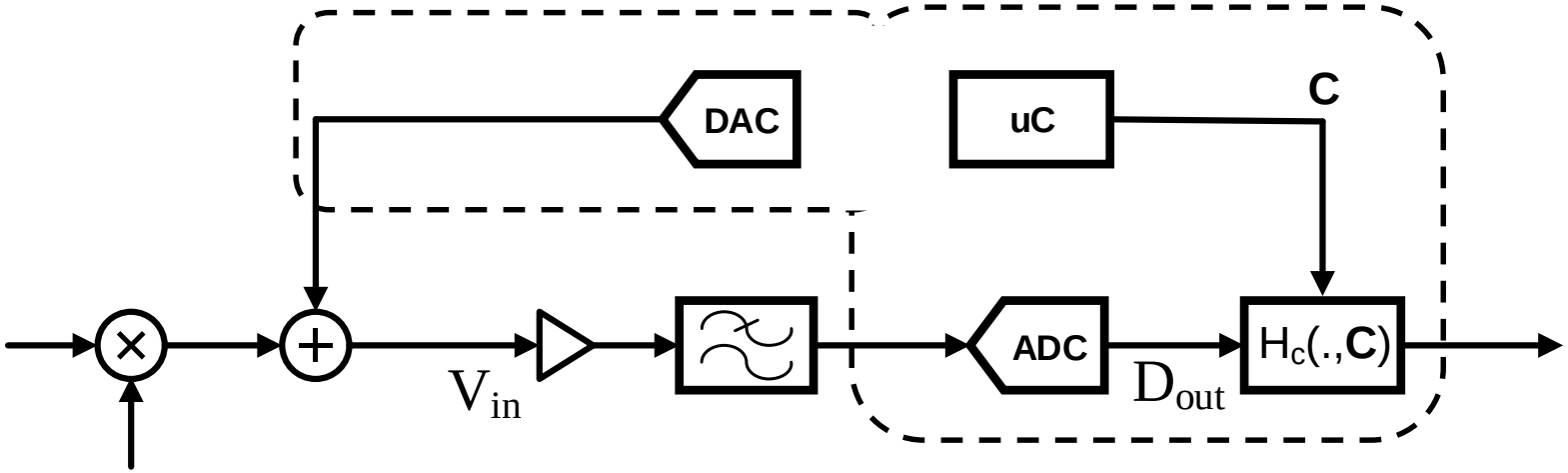
Non-linear Correction for Rx Signal Chain



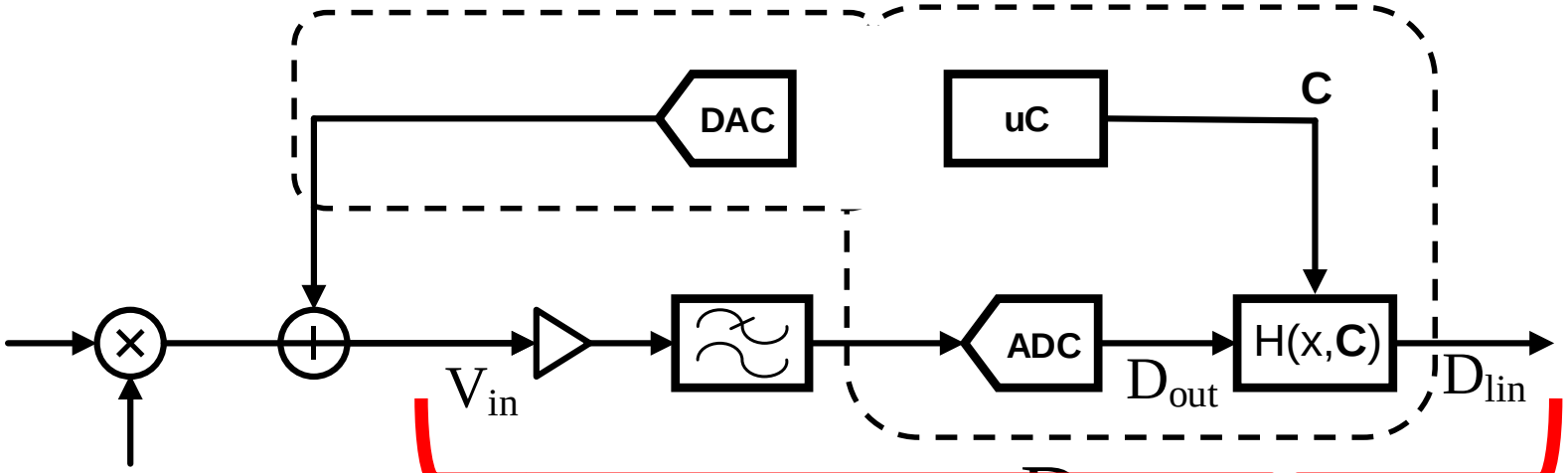


ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

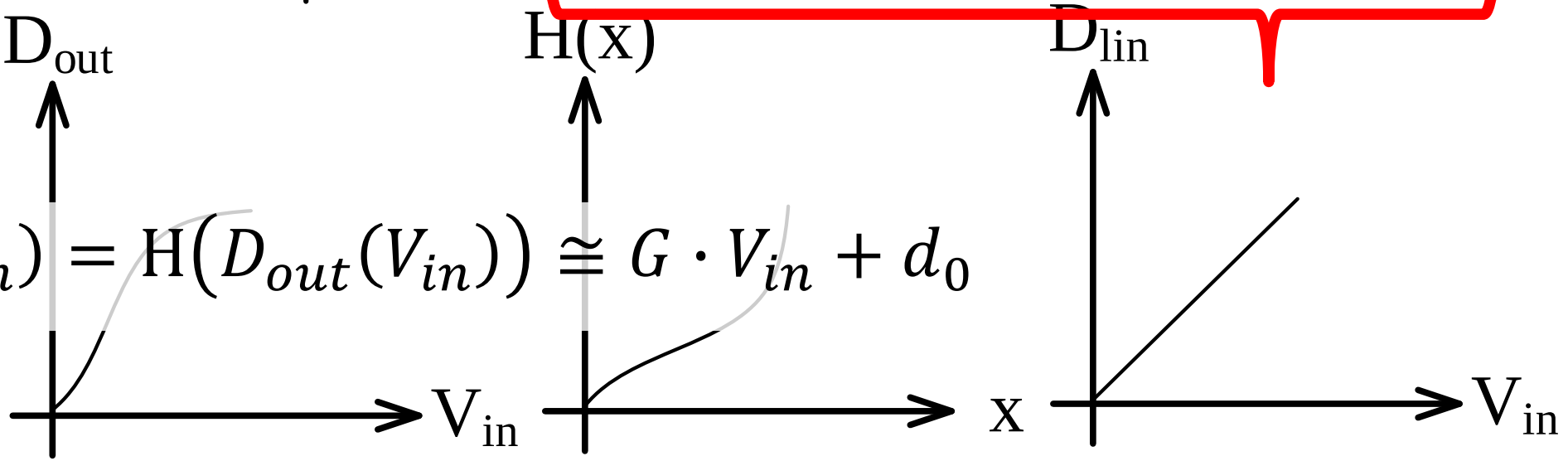
Non-linear Correction for Rx Signal Chain



Non-linear Correction for Rx Signal Chain

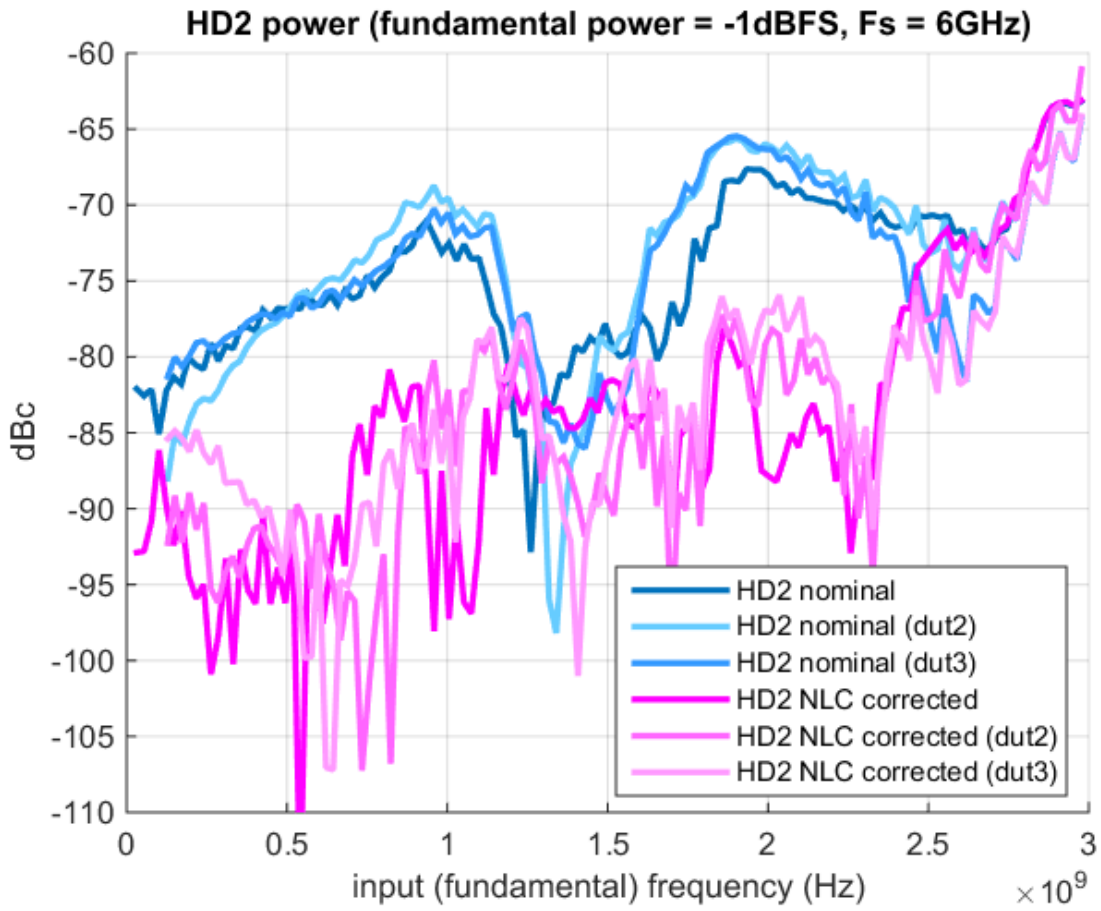


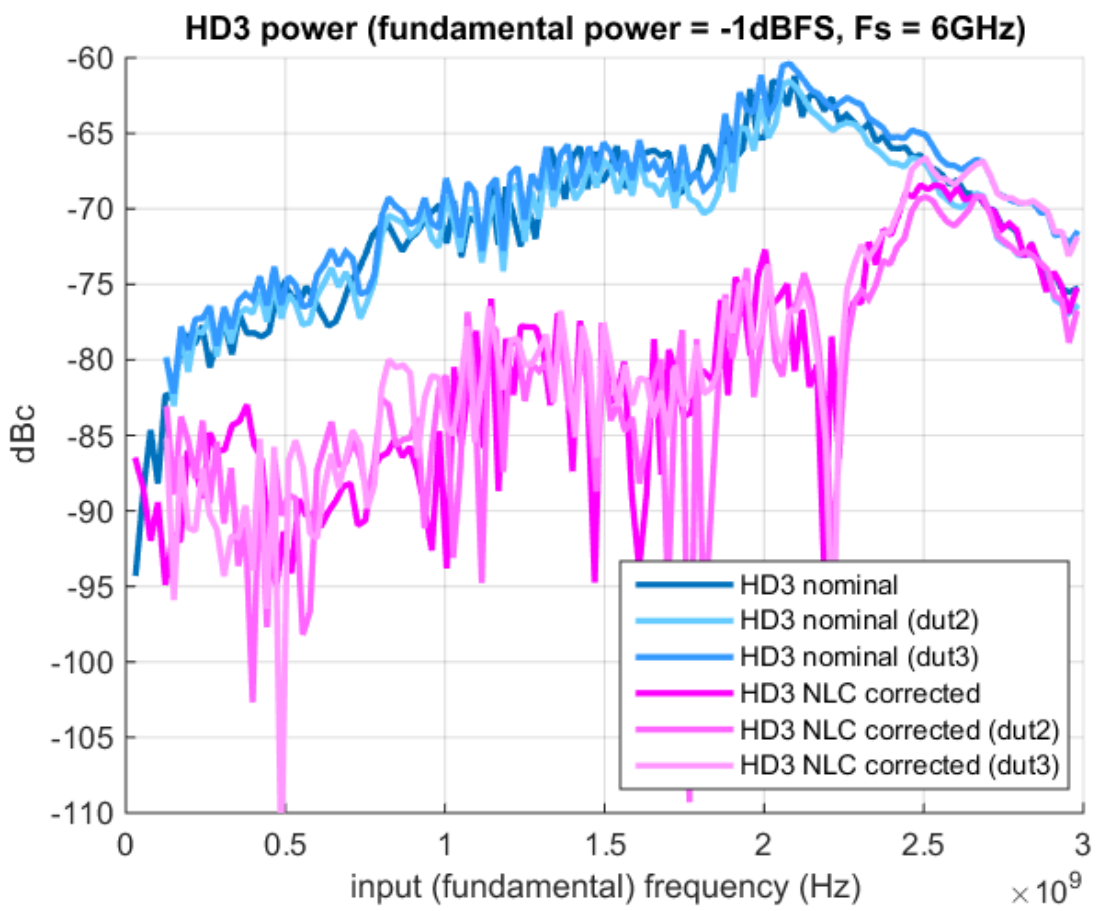
$$D_{lin}(V_{in}) = \mathrm{H}\big(D_{out}(V_{in})\big) \cong G \cdot V_{in} + d_0$$



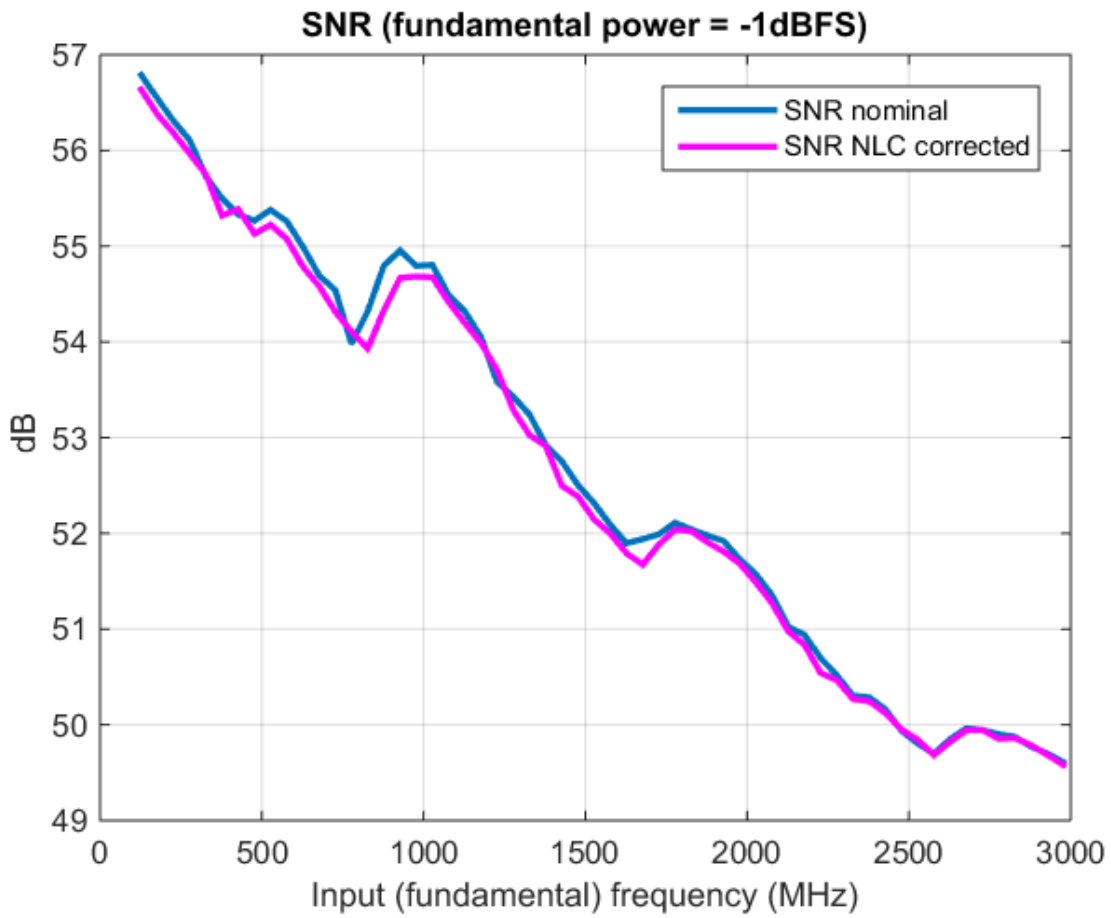
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

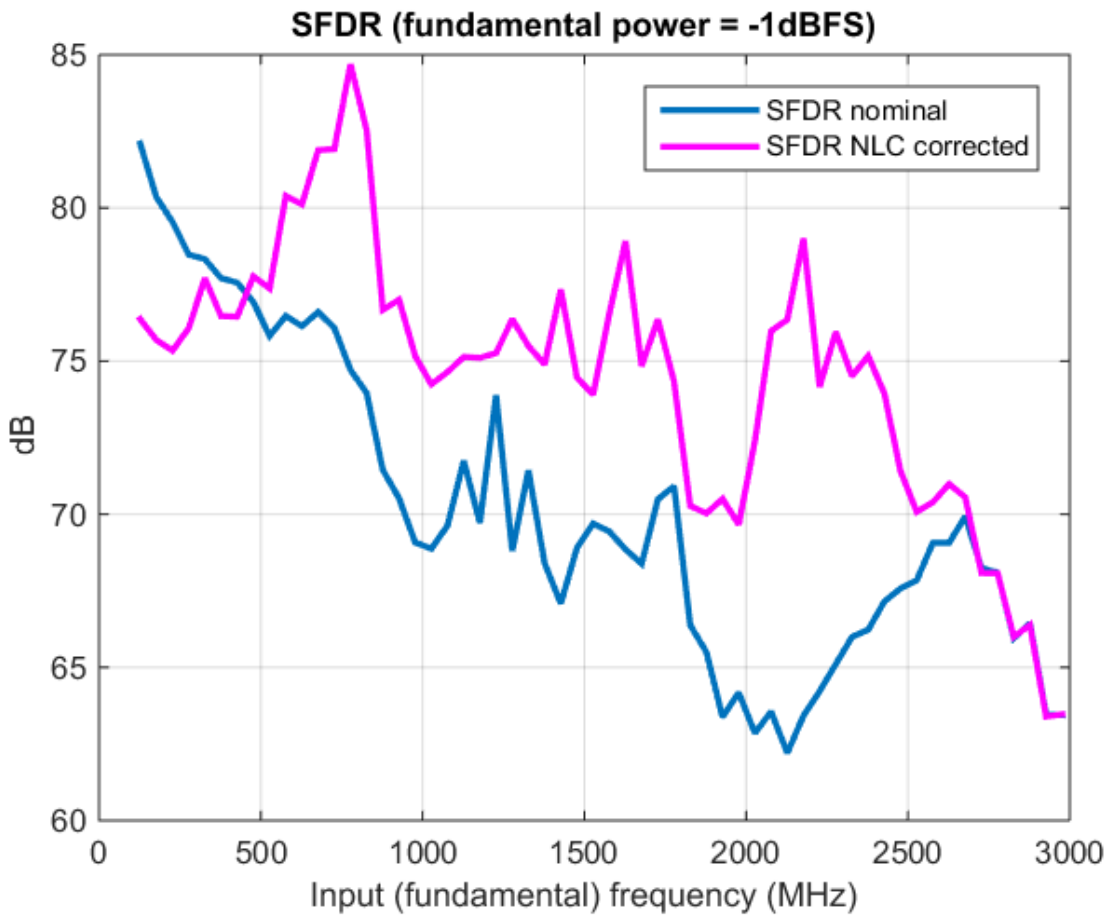
Fs=6GSPS Lab Data: HD2 & HD3 correction





Fs=6GSPS Lab Data: SNR and SFDR

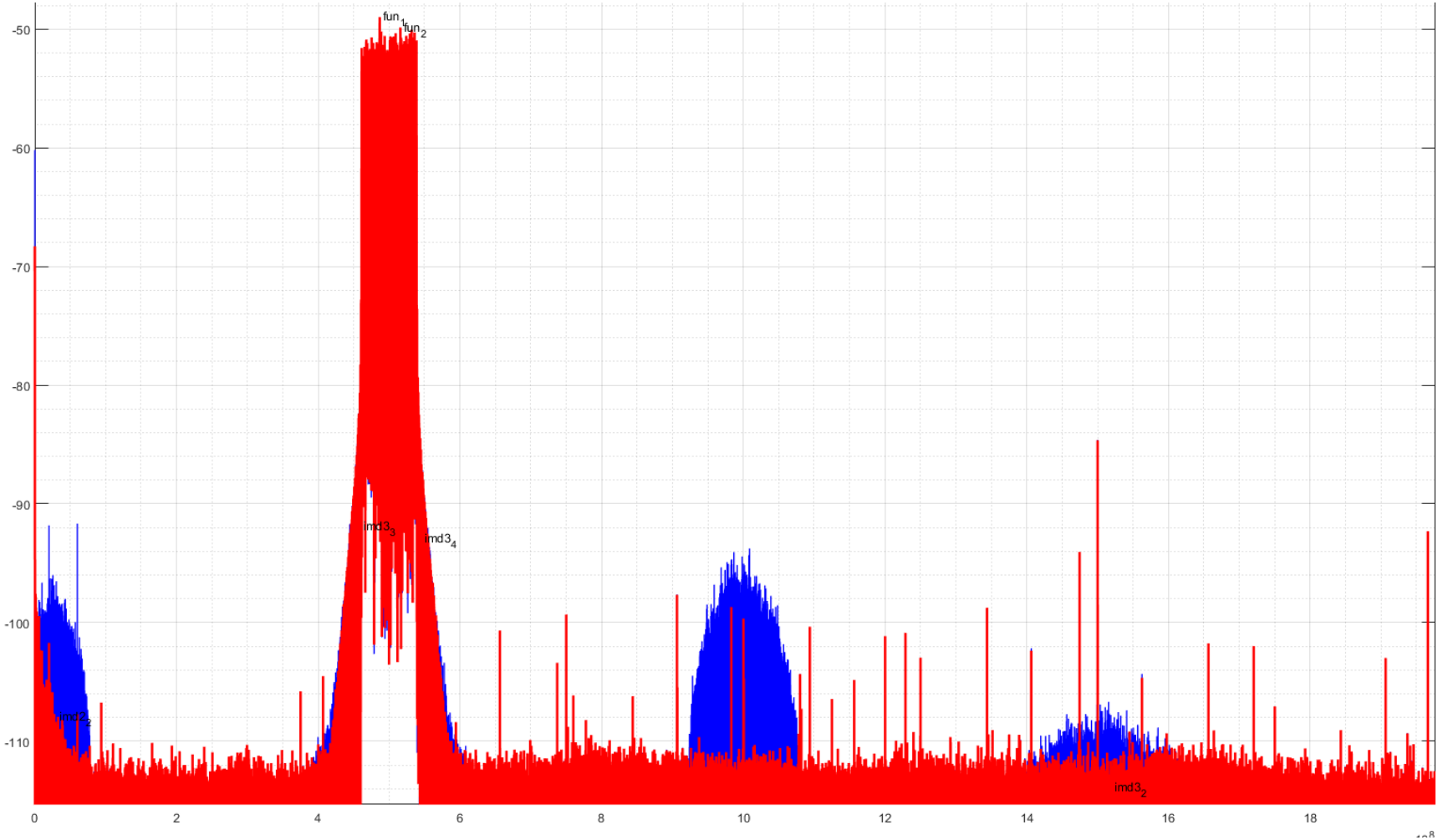




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Wi-Fi 6 (802.11AX) Test Signal (500M)

- Test signal shown at right
- Before LinearX™ correction in blue
- After LinearX™ correction in red (tonal spurs are common to both)
- Training was done using a different wideband training signal spanning 400 – 600M



ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Conclusion

Summary

Challenges	Possible avenues to solutions
Heat management/Power efficiency	Power efficient Devices, Circuits and Systems
	New materials
	New architectures
Phase noise in sampling clocks	New materials (photonics?)
	Hybrid continuous-discrete sampling systems
Packaging/Interconnect strays	System partitioning
	Heterogeneous Integration
	3D integration
MOS scaling	Greater digital-analog co-design
	Parallel analog processing architectures
Higher frequency electronics	New devices/III-V
	Photonics/CMOS integration

Conclusion

A comprehensive approach is required to address the multiple important design constraints:

- Heat removal
- Devices' reliability and aging
- Process technology
- Packaging
- Data interfaces
- Performance/band/power consumption
- Area/costs

QUESTIONS!?