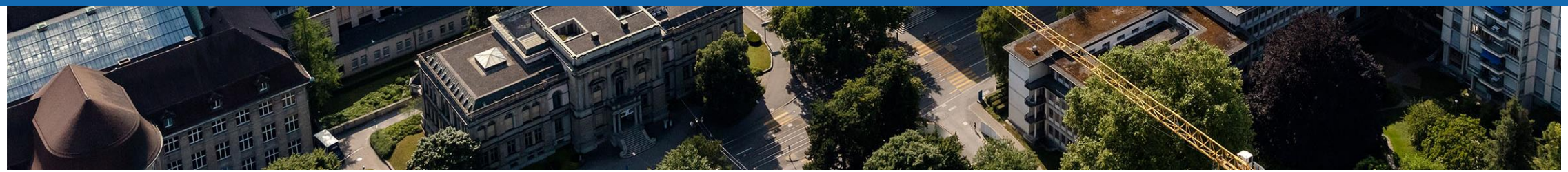
ETH zürich

Integrated Systems Laboratory
Energy Efficient Circuits and IoT Systems

A 8.7ppm/°C, 694nW, One-Point Calibrated RC Oscillator Using a Nonlinearity-aware Dual Phase-Locked Loop and DSM-controlled Frequency-Locked Loops

Giorgio Cristiano*, Jiawei Liao*,
Alessandro Novello, Gabriele Atzeni and Taekwang Jang
ETH Zürich
***contributed equally to this work**



Outline

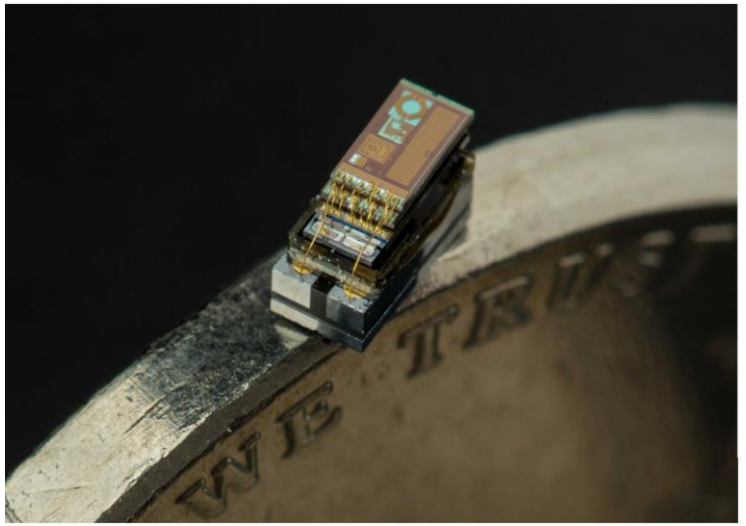
1. Background and Motivation
2. Proposed Timer
    1. One-point calibration with a nonlinearity-aware dual PLL structure
    2. DSM-Controlled FLL
    3. Digital Loop Filter with non-linearity cancellation
    4. Example of Operation
3. Measurement Results
4. Conclusions

IoT Devices

- **IoT sensor node applications**

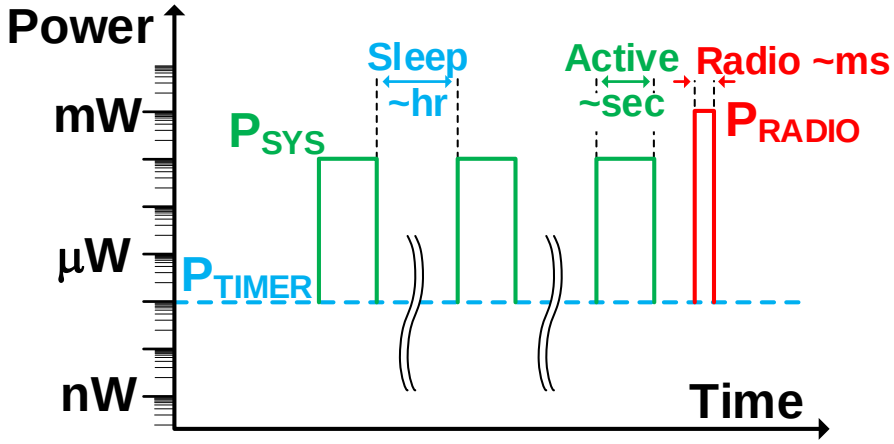
P. Mayer et al. SUSCOM 2020

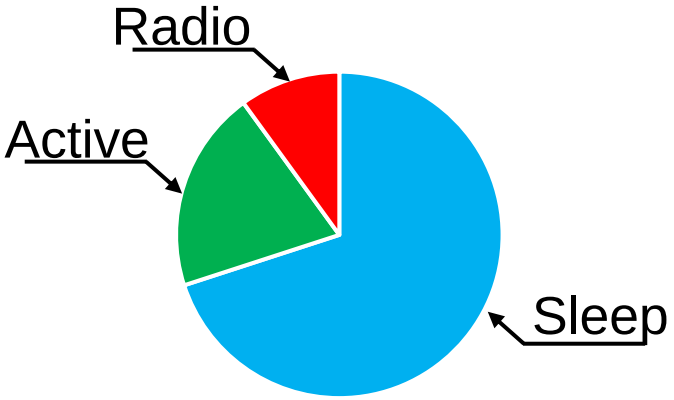
T. Jang et al. TCAS1 2017



S. Oh et al. JSSC 2015

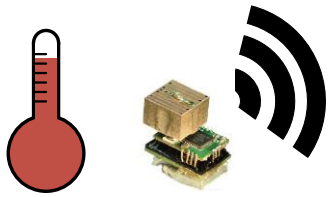
Challenges in Timer Circuits

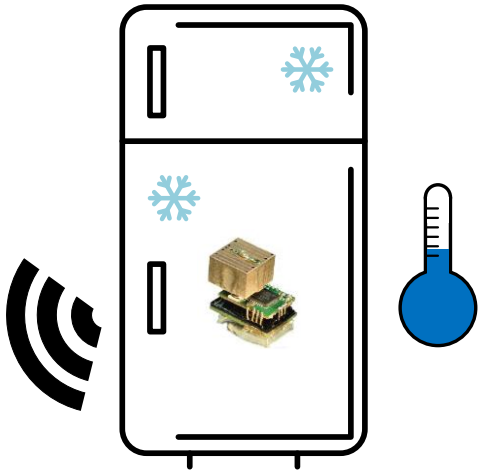


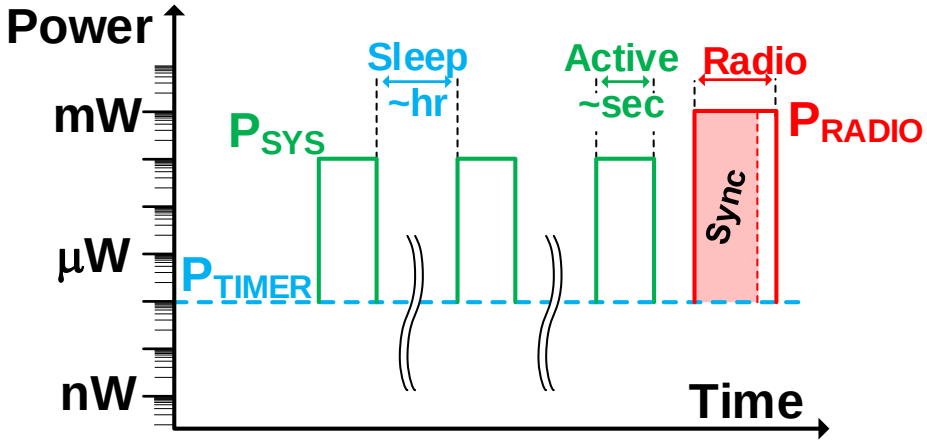


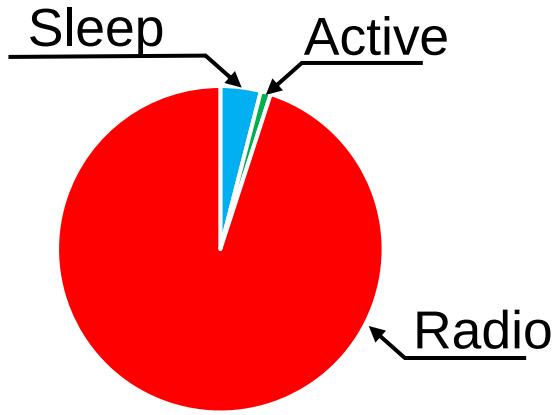
Power Consumption

Challenges in Timer Circuits







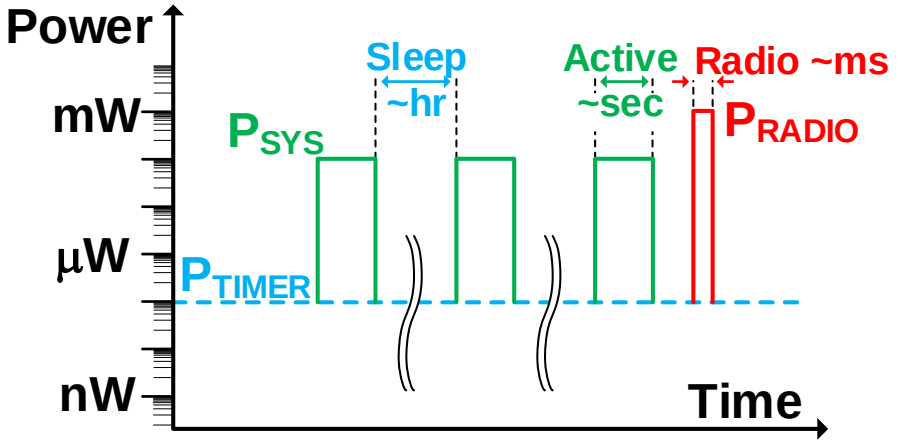


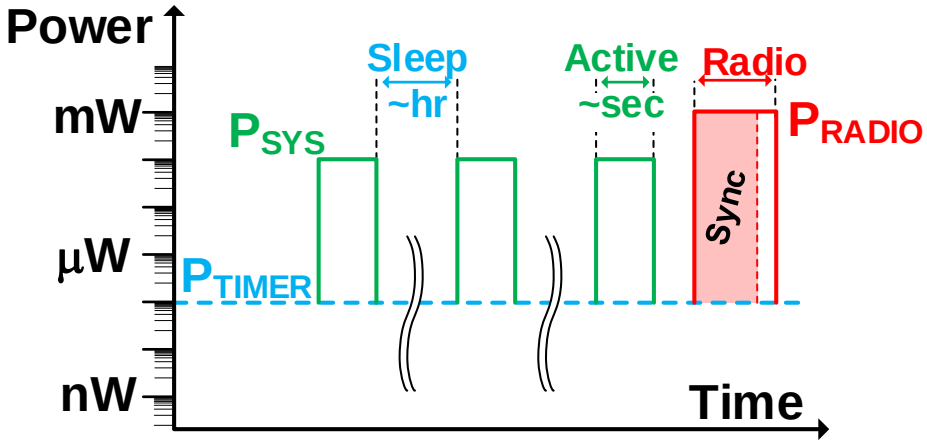
Power Consumption

Challenges in Timer Circuits

IoT node timers must have:

- Ultra-low power consumption
- High frequency accuracy
  - Insensitivity to process, voltage, temperature (PVT) variations
  - Long-term frequency stability (Low Allan deviation)

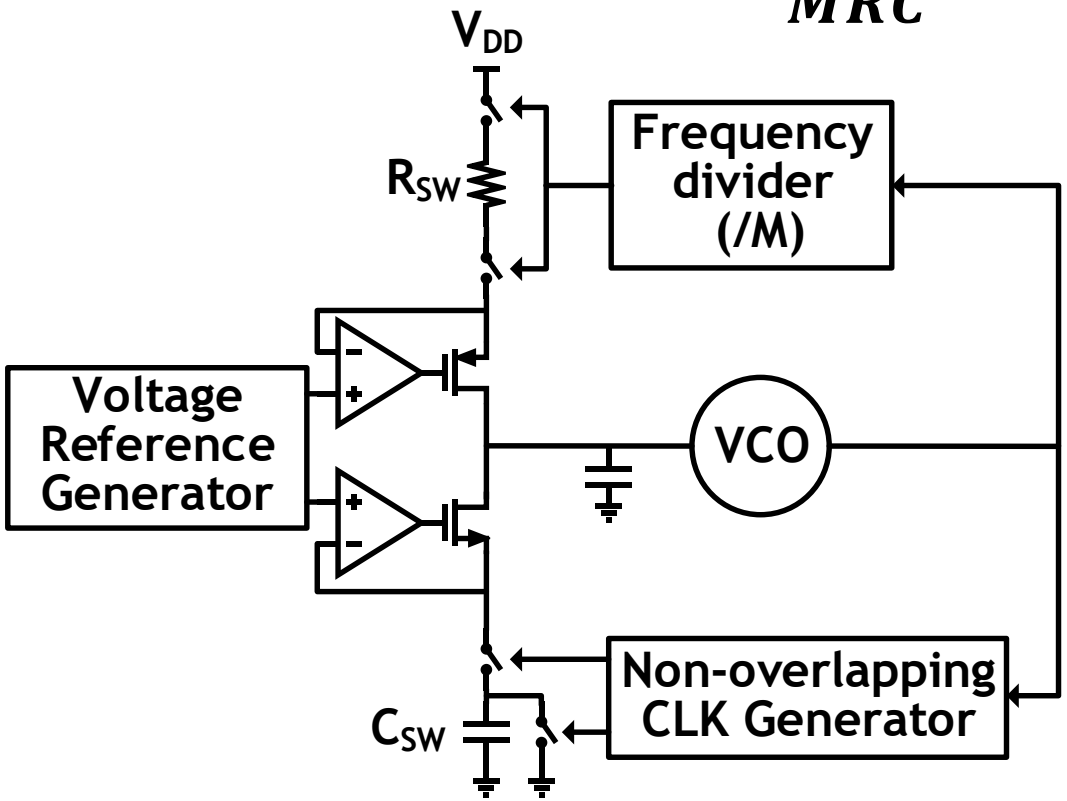




Conventional on-chip Timers

- **FLL based timer**

$$F_{osc} = \frac{1}{MRC}$$



T. Jang et al. ISSCC 2016

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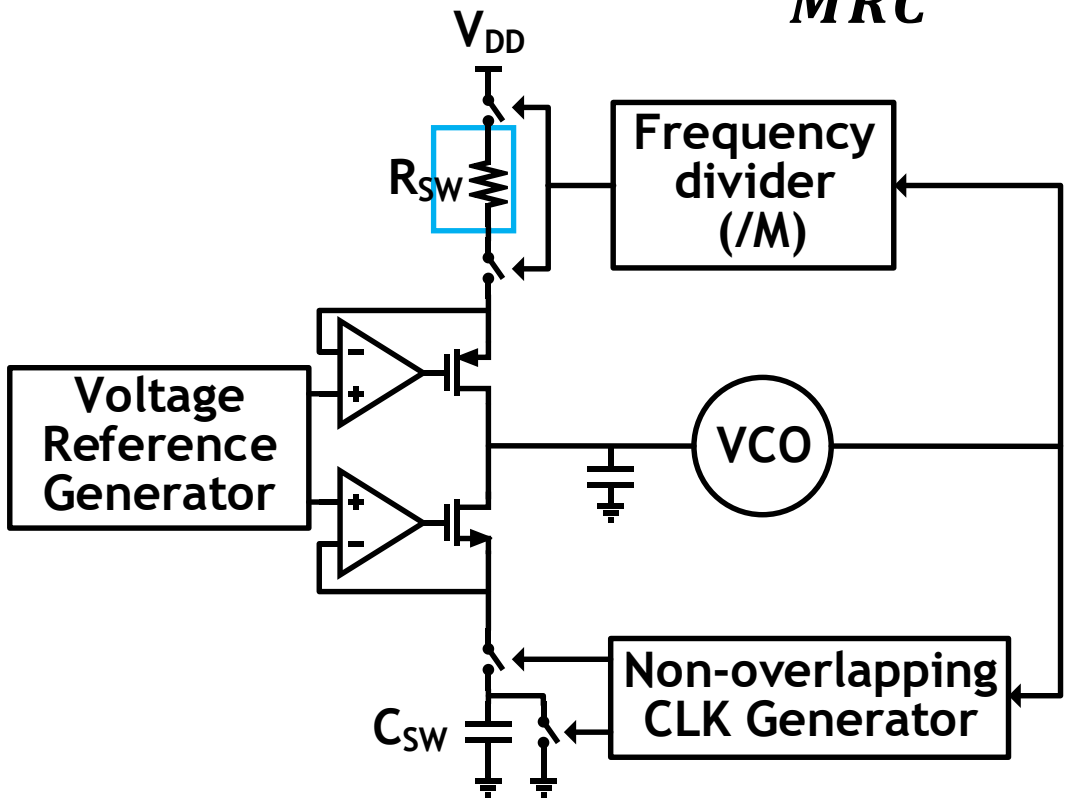
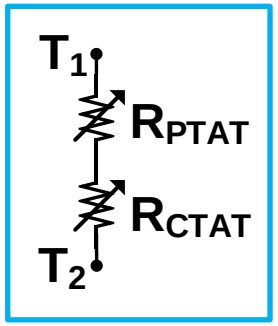


T. Jang et al. ISSCC 2016



Issues

- Necessary resistor trimming
- 2-point calibration to cancel out R variation

$$R = R_P(1 + \alpha_P \Delta T) + R_C(1 + \alpha_C \Delta T) =$$
$$= (R_P + R_C) + (R_P \alpha_P + R_C \alpha_C)\Delta \mathrm{T}$$

Must measure at least at 2 temperatures to cancel this contribution

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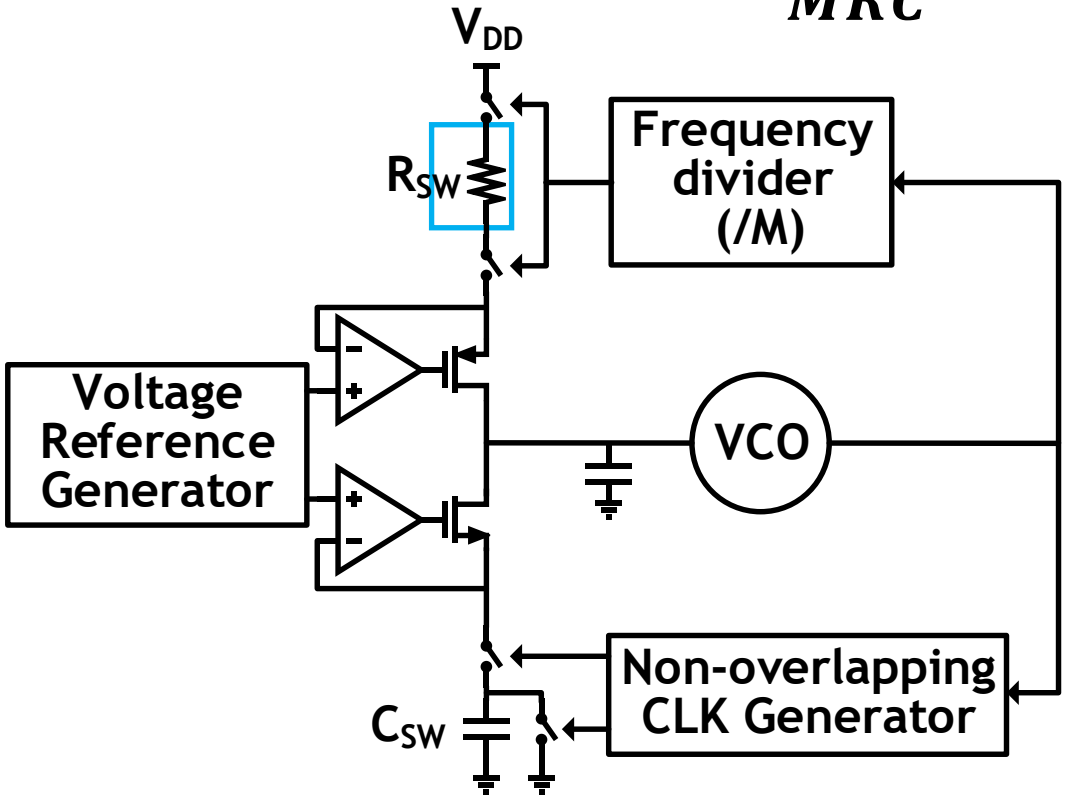
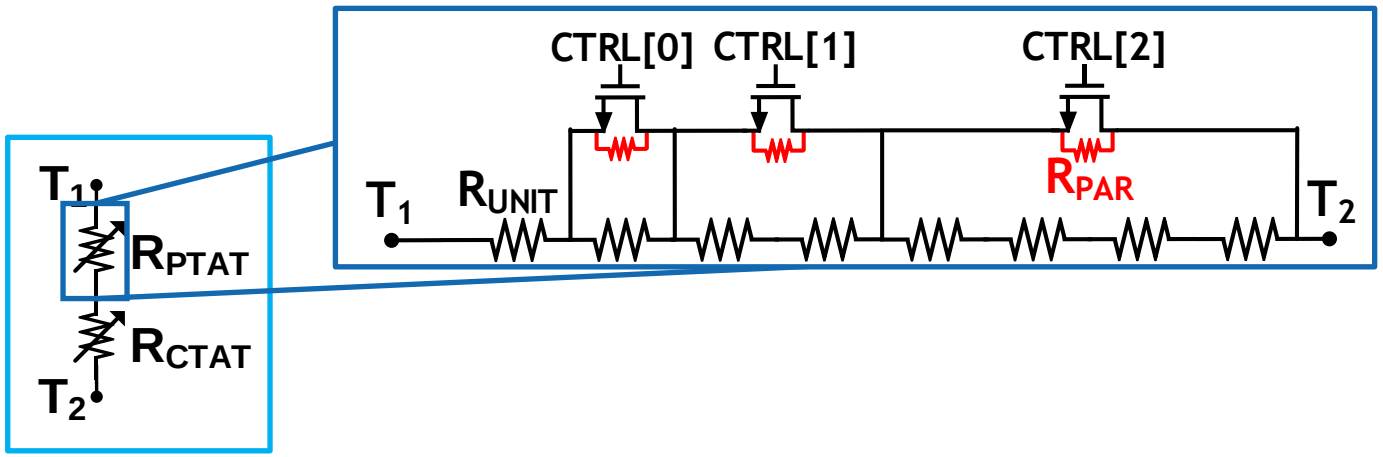


T. Jang et al. ISSCC 2016

Issues

- Necessary resistor trimming
- 2-point calibration to cancel out R variation
- Additional temperature-dependent parasitic due to trimming



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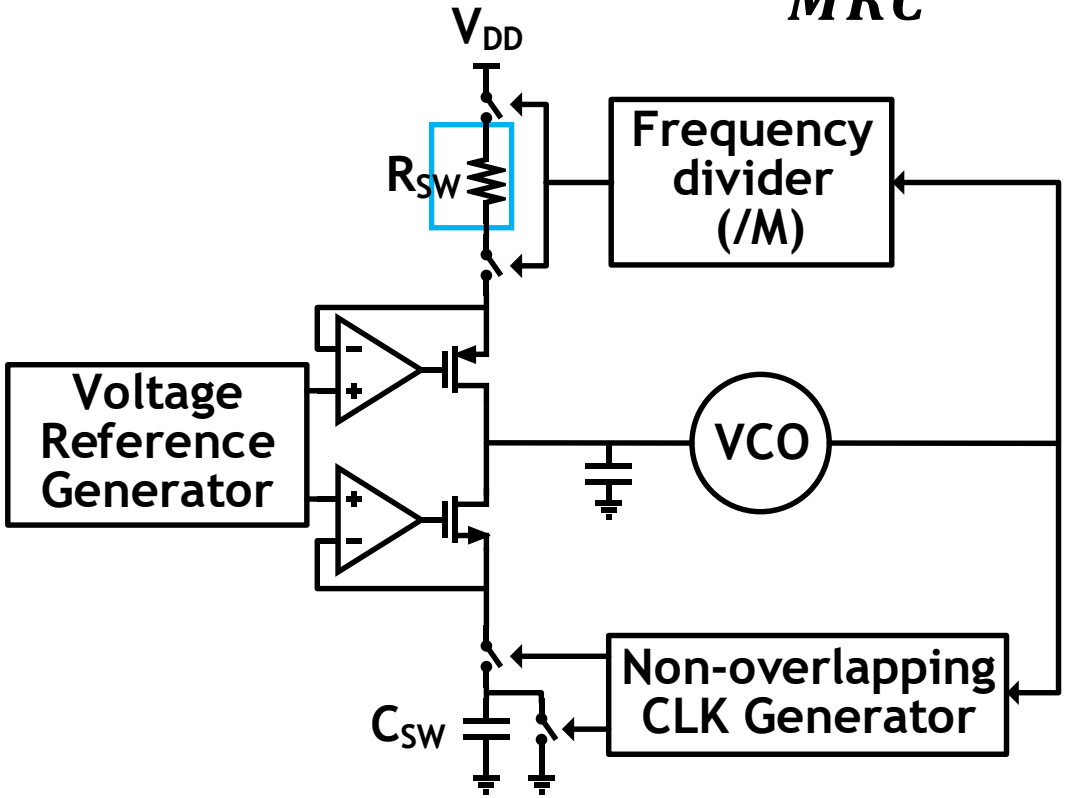

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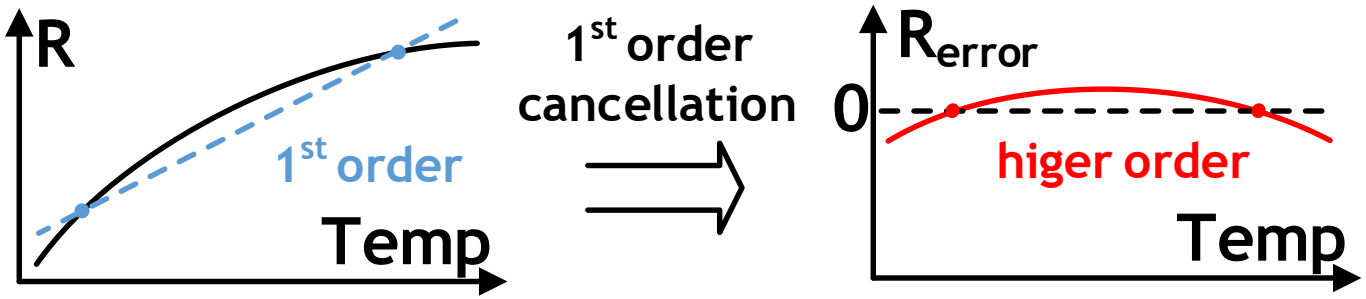
- 2-point calibration to cancel out R variation
- Additional parasitic due to trimming
- Accuracy limited by higher-order variations



T. Jang et al. ISSCC 2016

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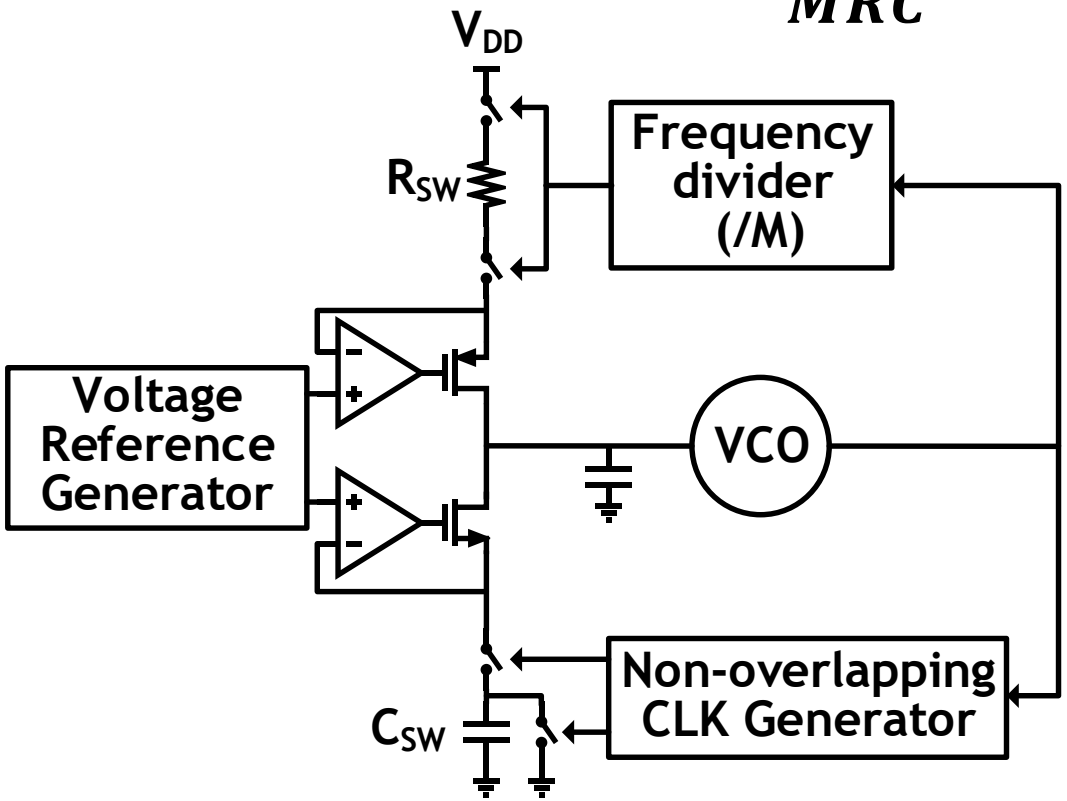

T. Jang et al. ISSCC 2016

Issues

- Necessary resistor trimming
- 2-point calibration to cancel out R variation
- Additional parasitics due to trimming
- Accuracy limited by higher-order variations

Possible improvements

- Avoid resistor trimming
- Use 1-point calibration
- Cancel out higher-order variations

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Proposed FLL Architecture

- **Conventional**

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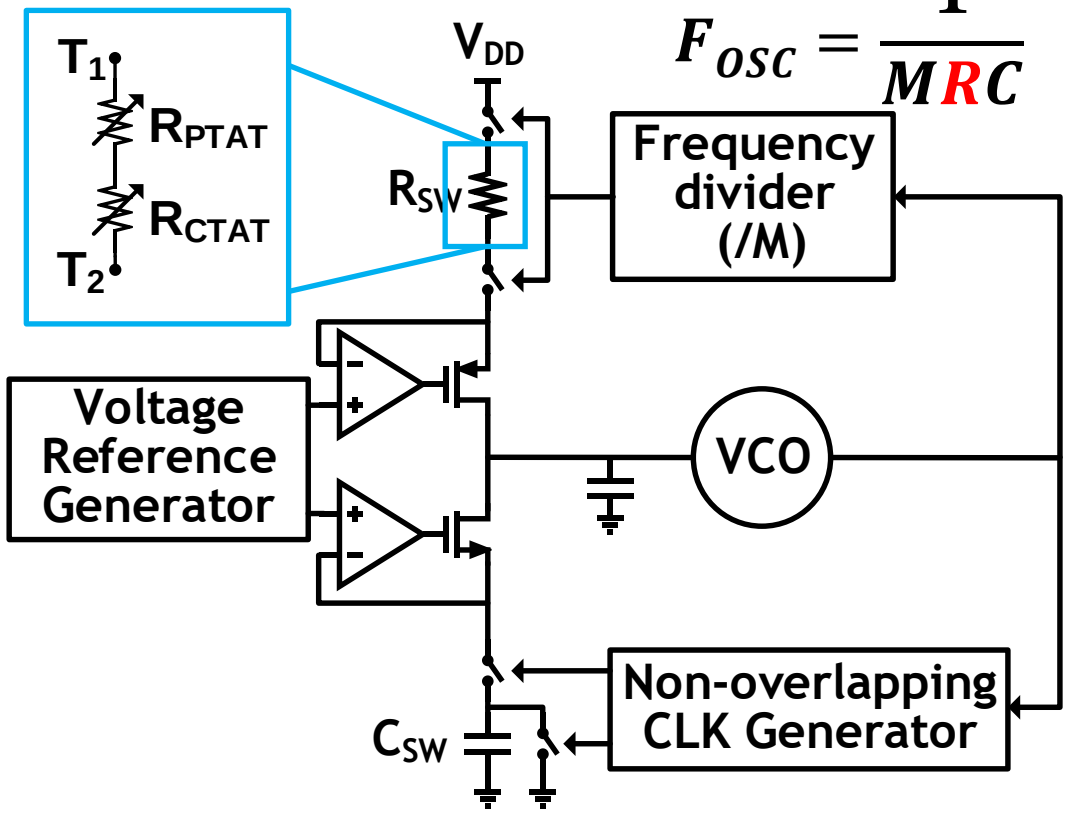
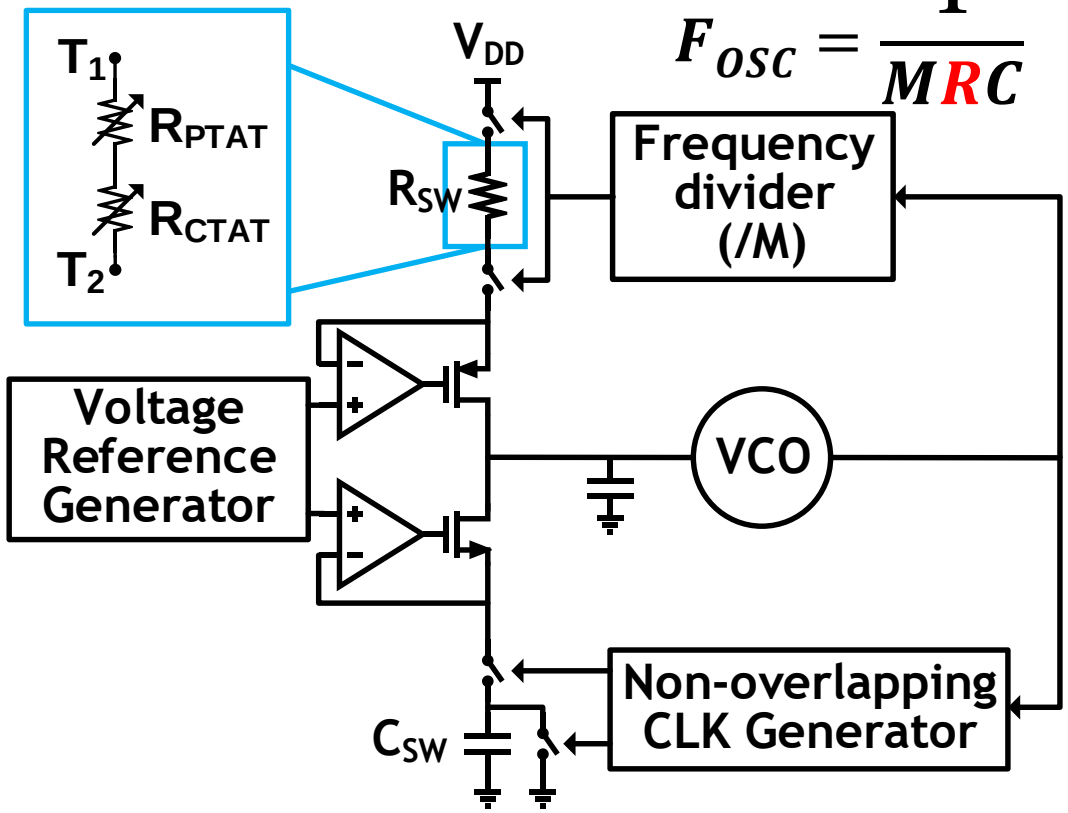


- Trimming and temperature insensitivity through R
- Current reuse scheme

Proposed FLL Architecture

- **Conventional**

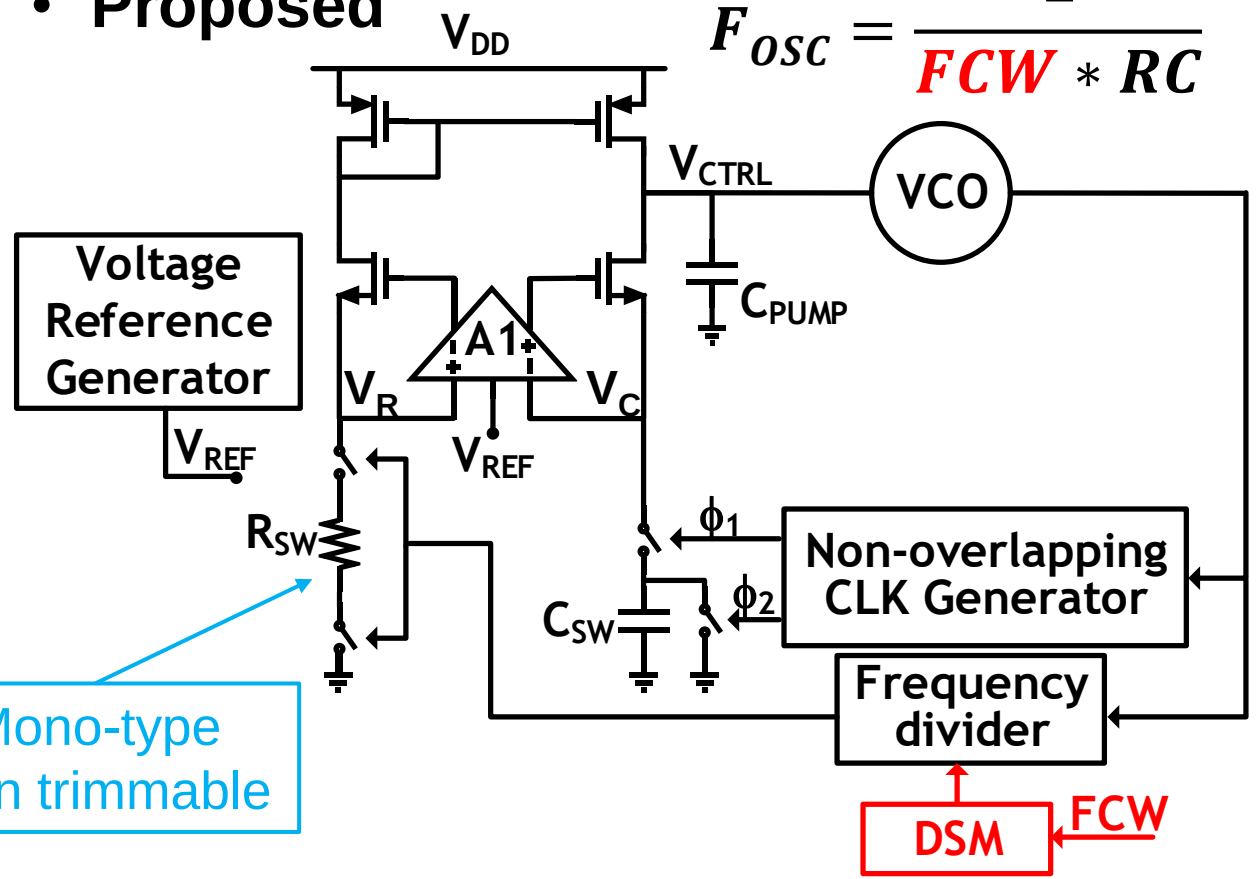
$$F_{osc} = \frac{1}{MRC}$$



- Trimming and temperature insensitivity through R
- Current reuse scheme

- **Proposed**

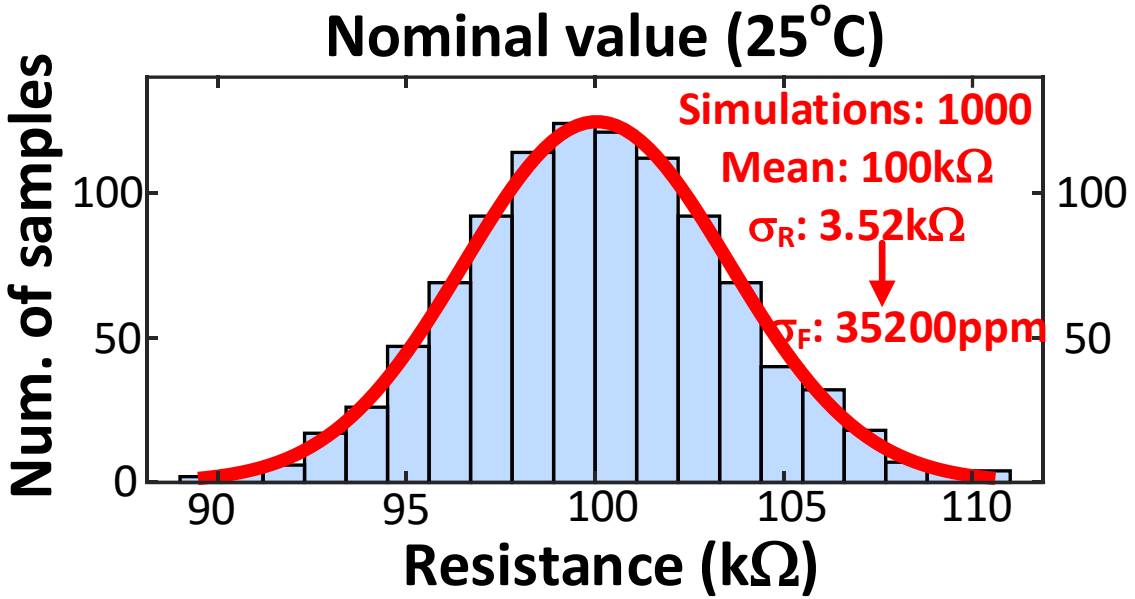
$$F_{osc} = \frac{1}{FCW * RC}$$



- Trimming and temperature insensitivity through Frequency Control Word (FCW)
- Differential branches scheme

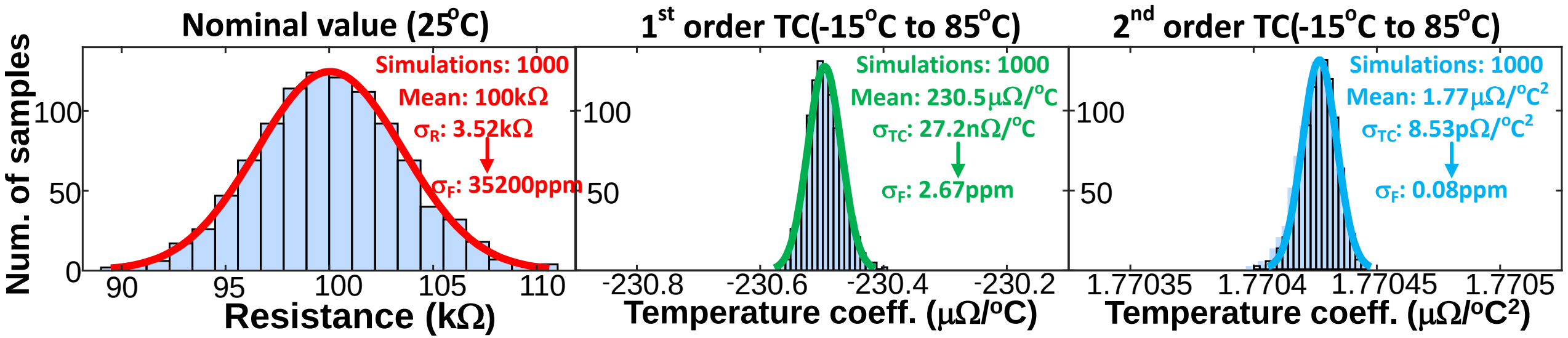
Resistor Variation

$$R = R_0(1 + \alpha\Delta T + \beta\Delta T^2) \qquad F_{osc} = \frac{1}{FCW * RC}$$



Resistor Variation

$$R = R_0(1 + \alpha\Delta T + \beta\Delta T^2)$$



J. Lee et al. JSSC 2012
A. Jain et al. ISCAS 2019

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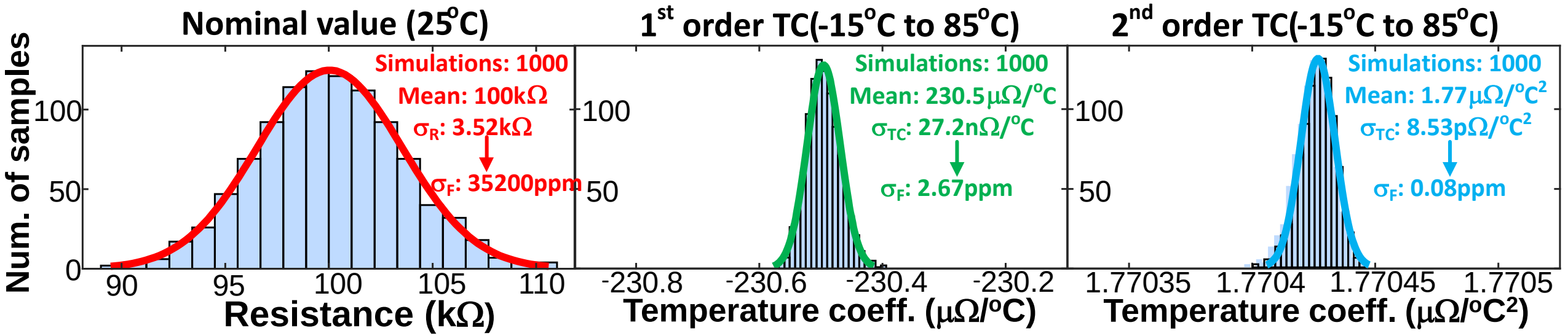

$$FCW(\Delta T)R_0(1 + \alpha\Delta T) = FCW_{nom}R_0 \longrightarrow FCW(\Delta T) = FCW_{nom}\frac{1}{(1 + \alpha\Delta T)}$$

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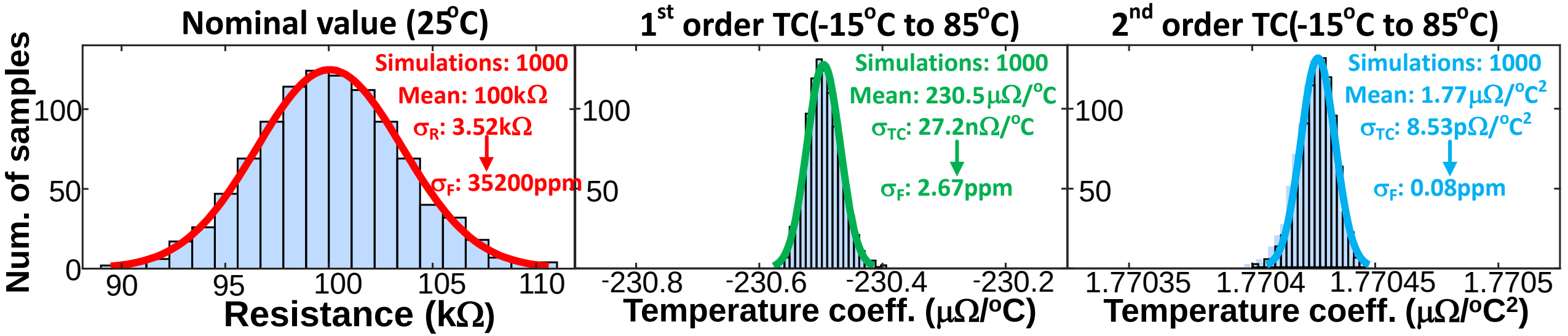
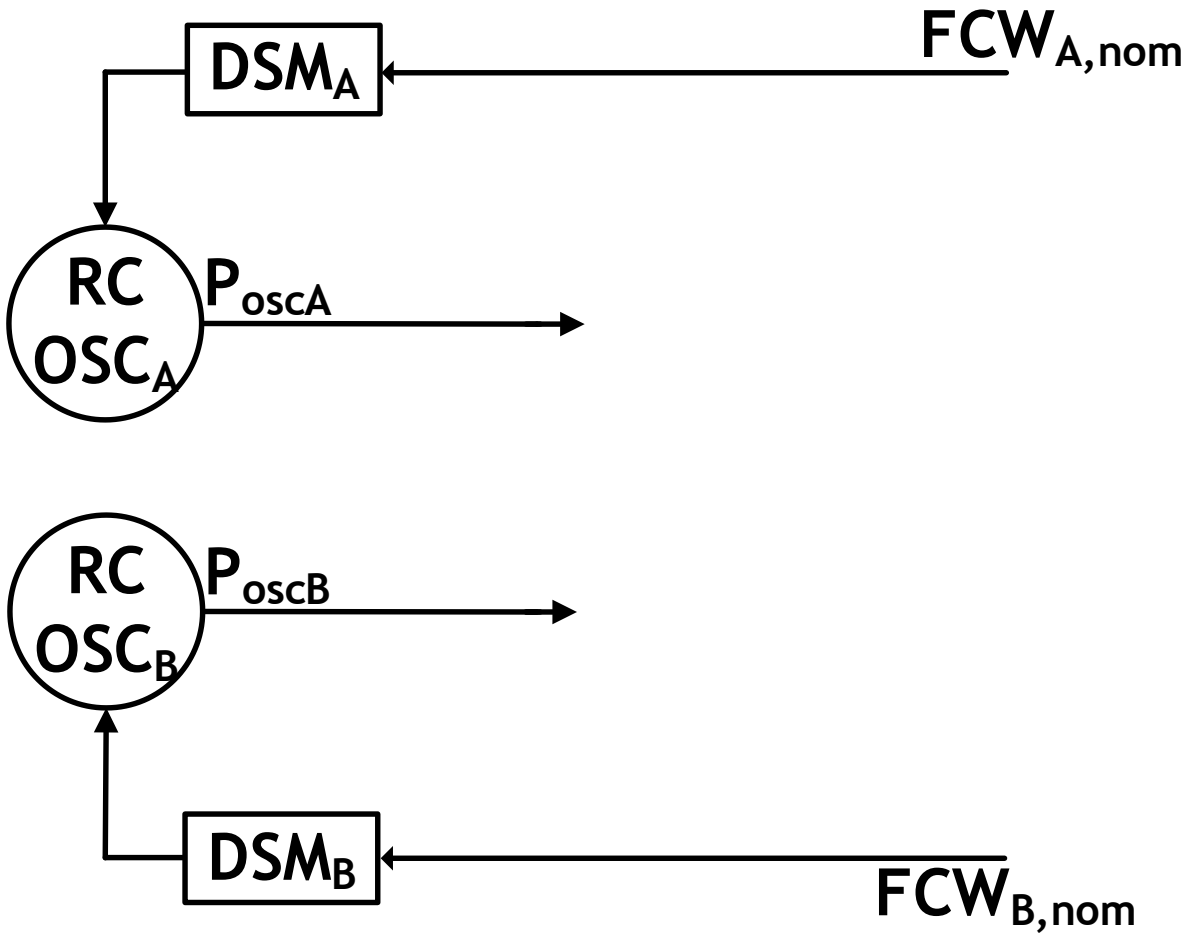


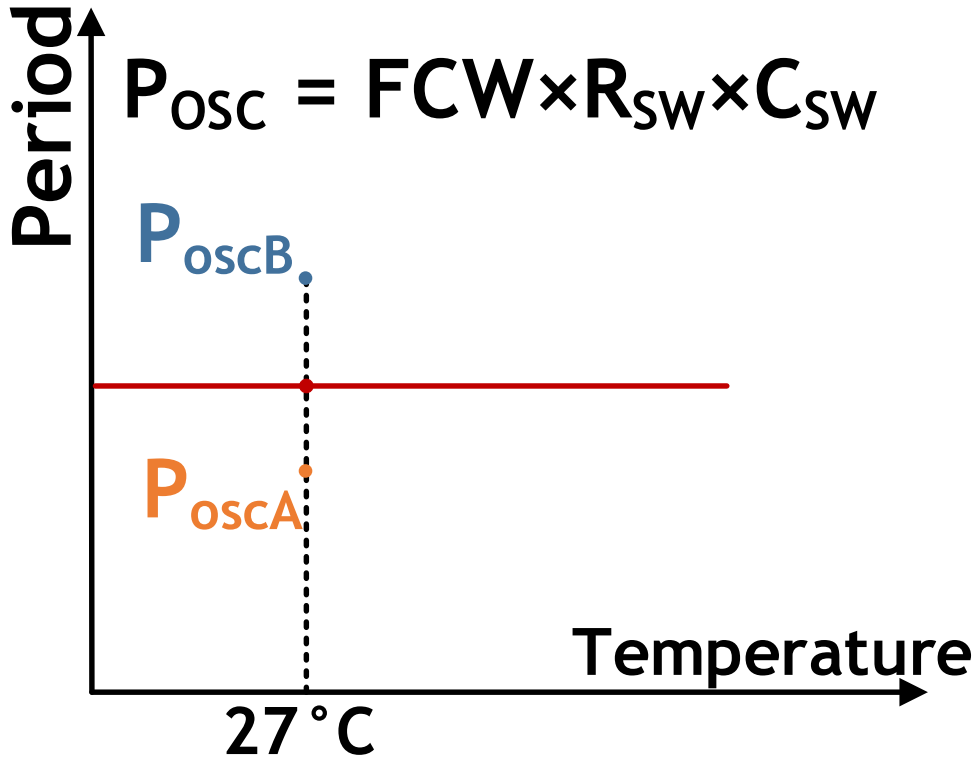
$$FCW(\Delta T)R_0(1 + \alpha\Delta T) = FCW_{nom}R_0 \longrightarrow FCW(\Delta T) = FCW_{nom}\frac{1}{(1 + \alpha\Delta T)}$$

Temperature insensitivity can be achieved with a 1-point measurement only

Proposed Timer Architecture

$$R_A = R_{0,A}(1 + \alpha_A \Delta T)$$





$$R_B = R_{0,B}(1 + \alpha_B \Delta T)$$

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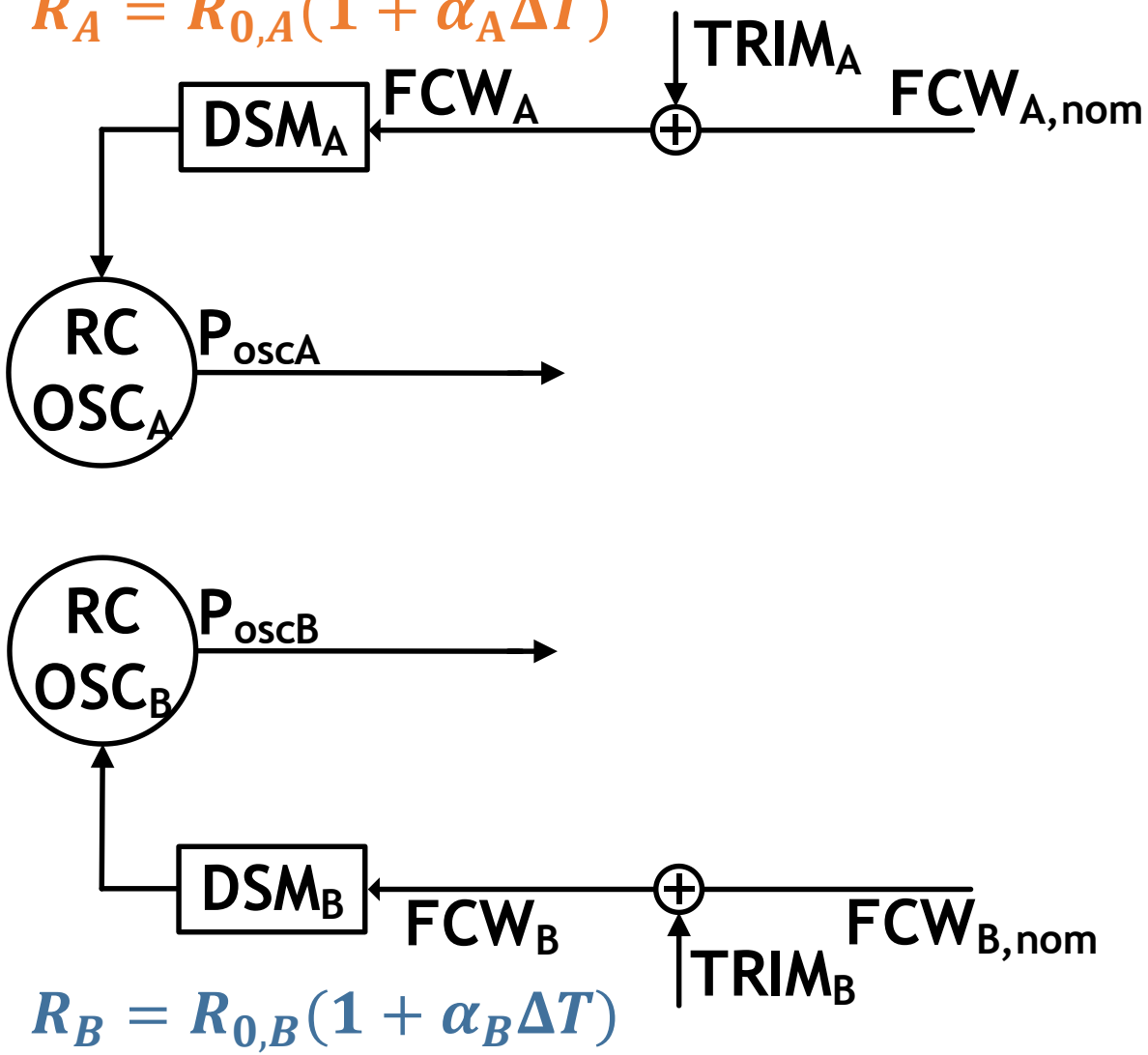

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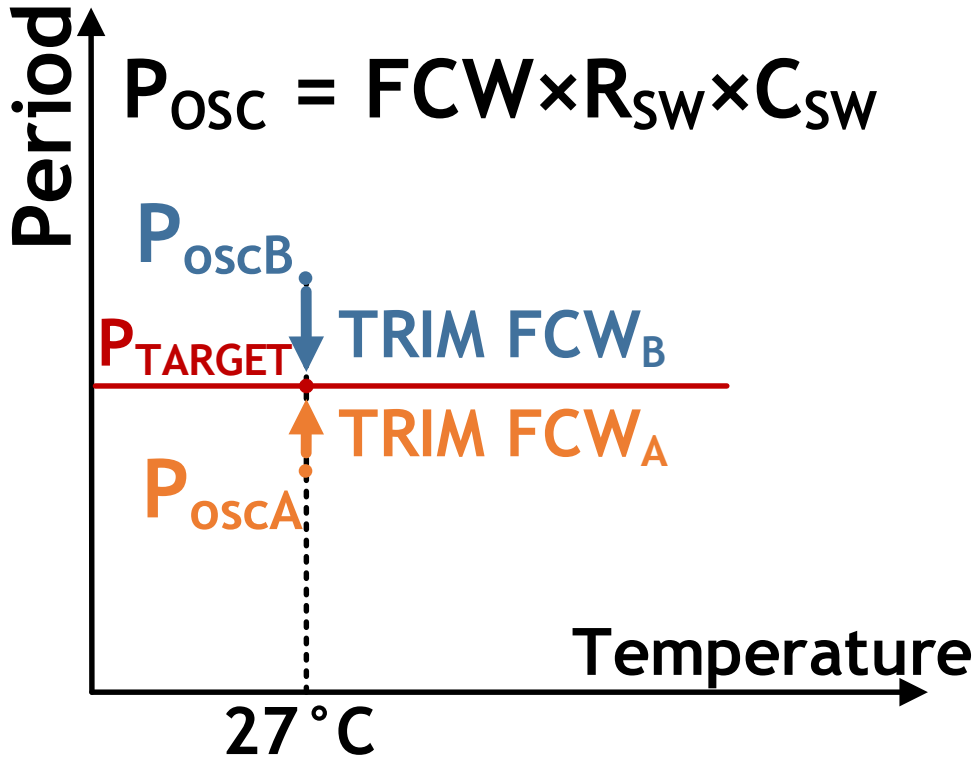

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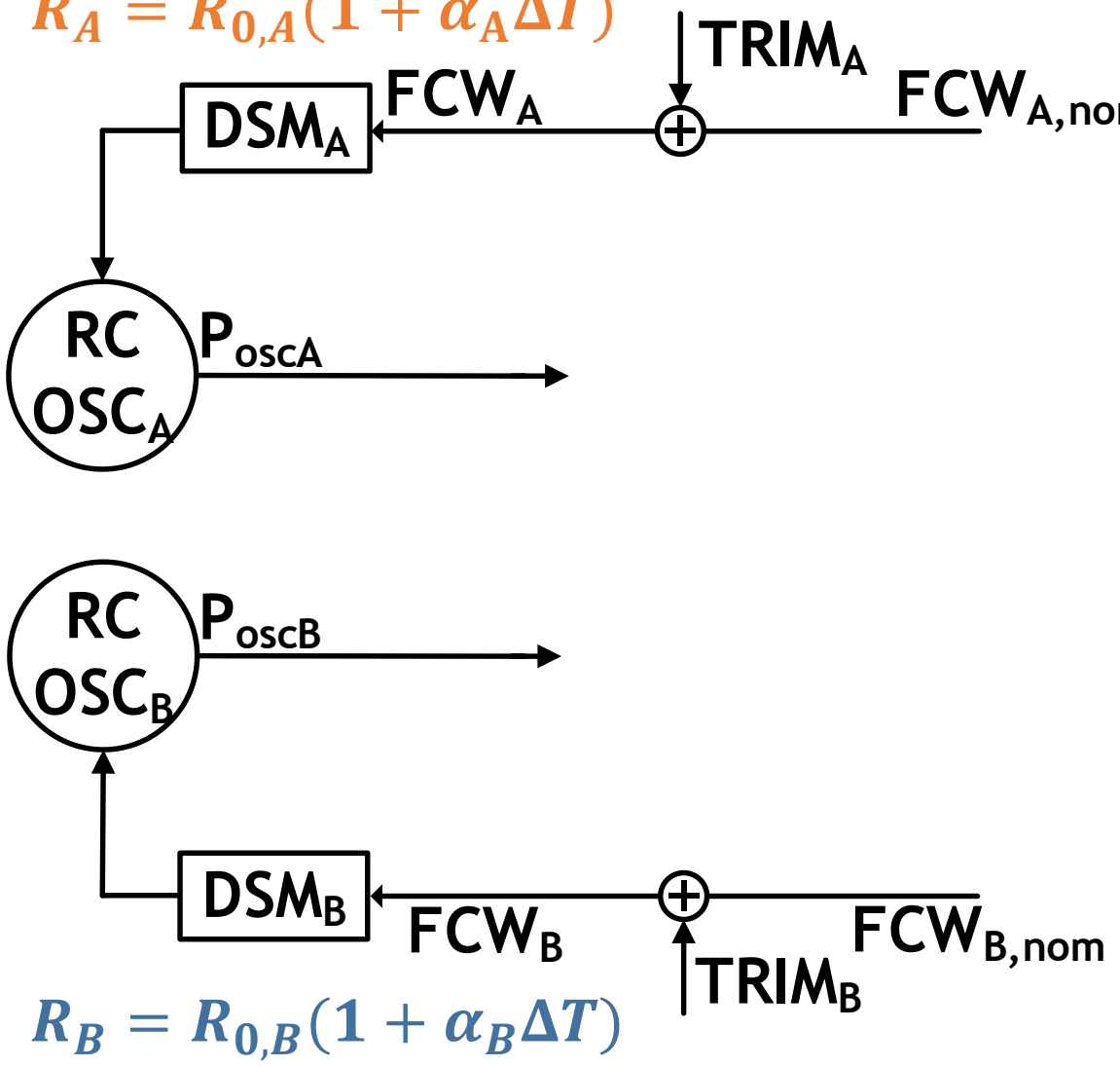

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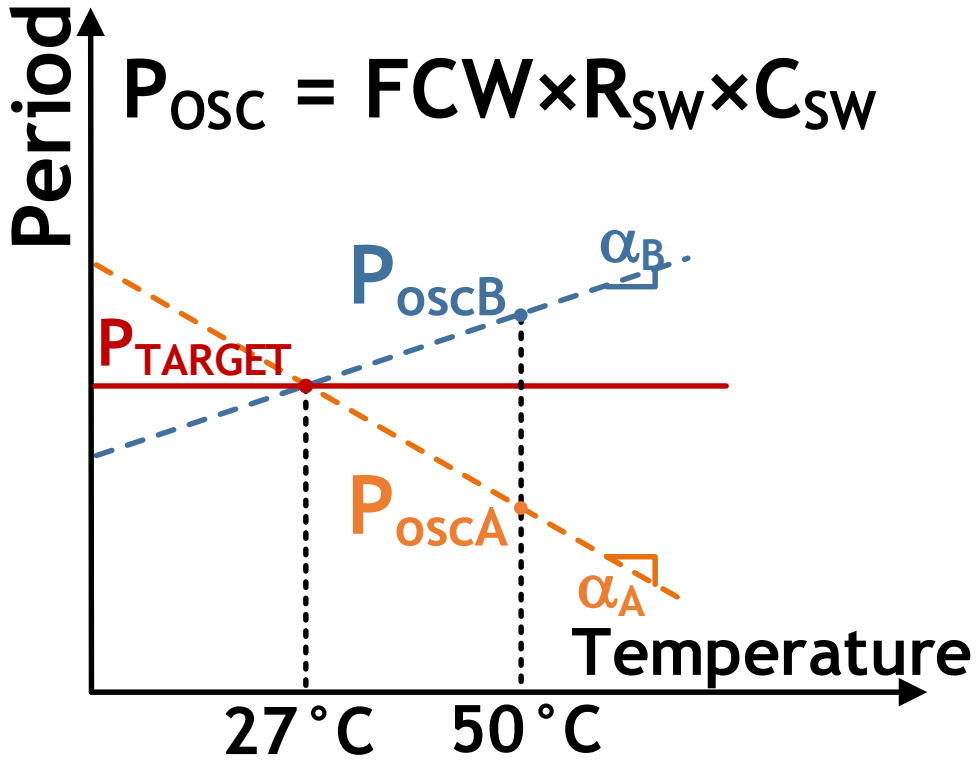

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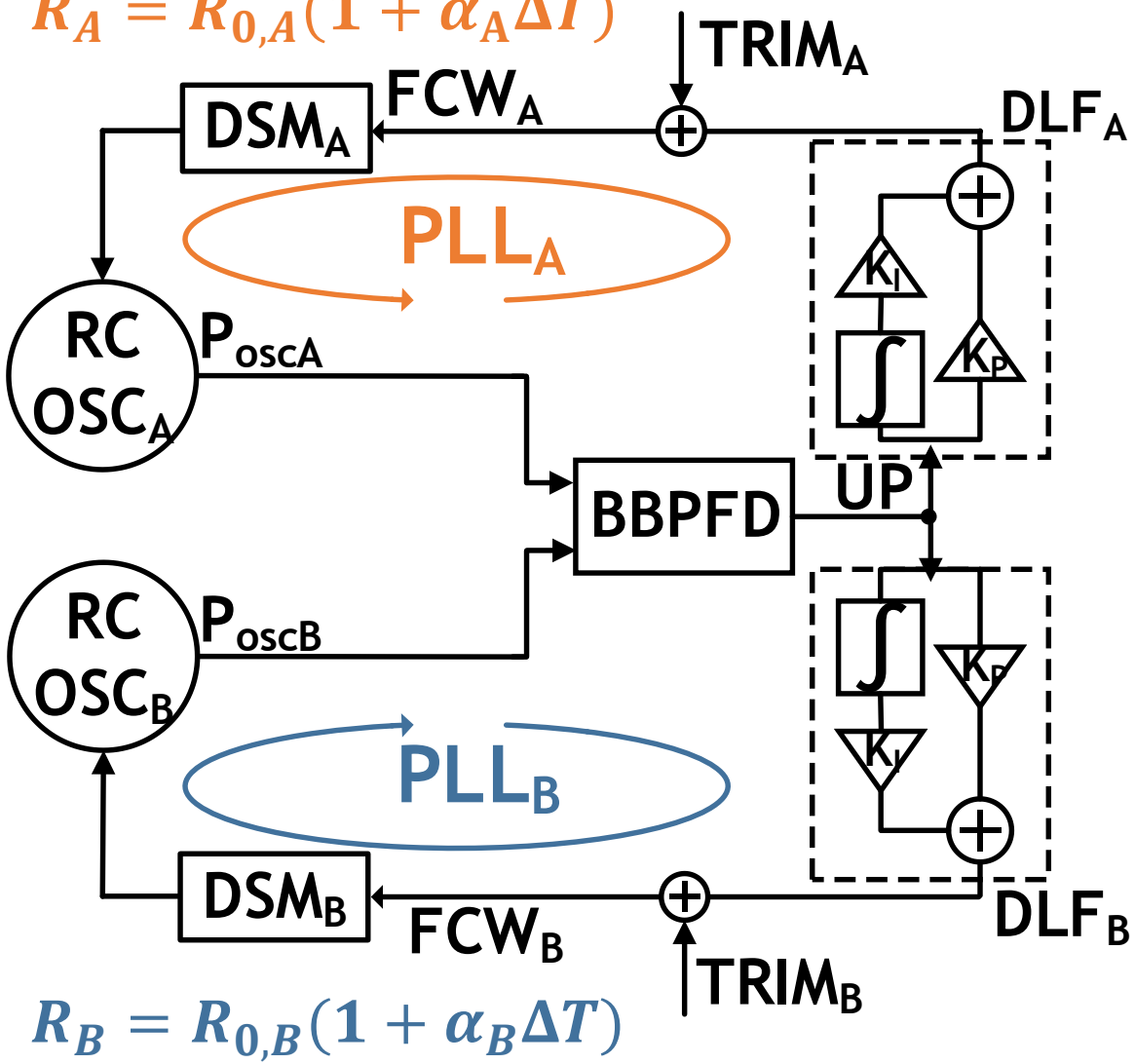

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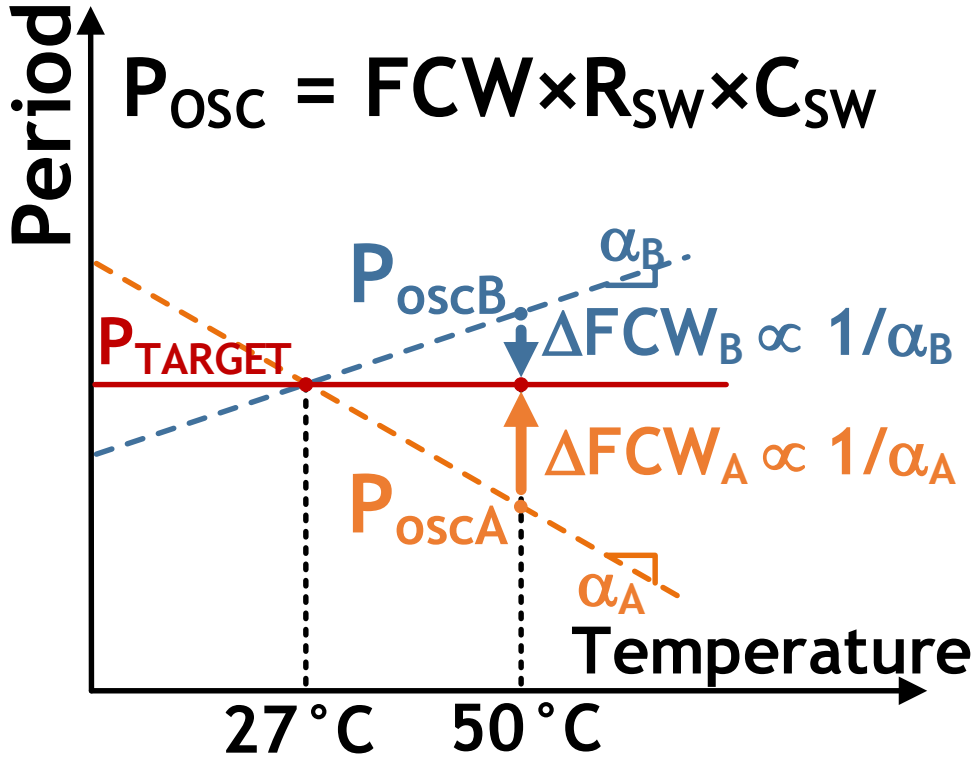

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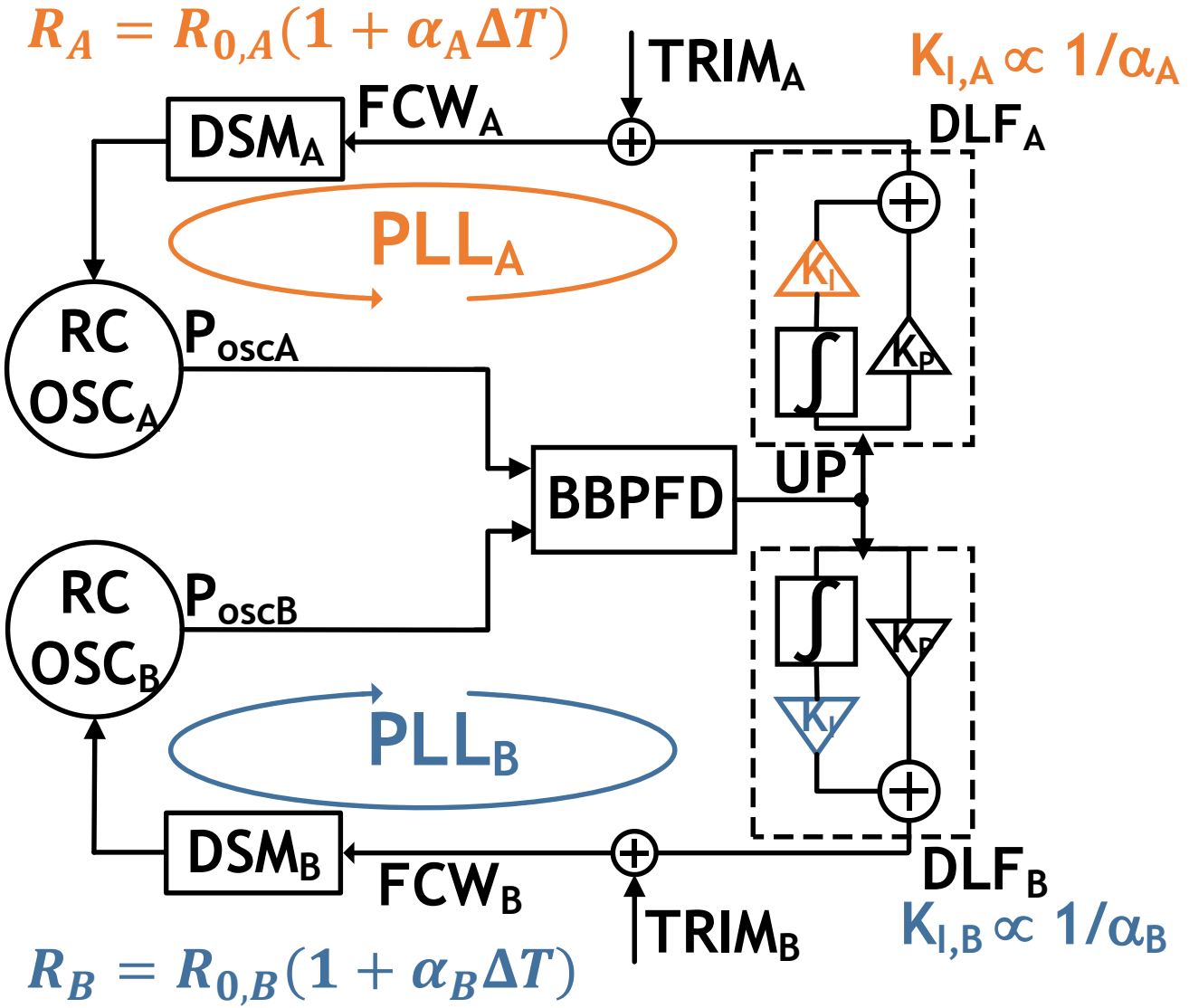

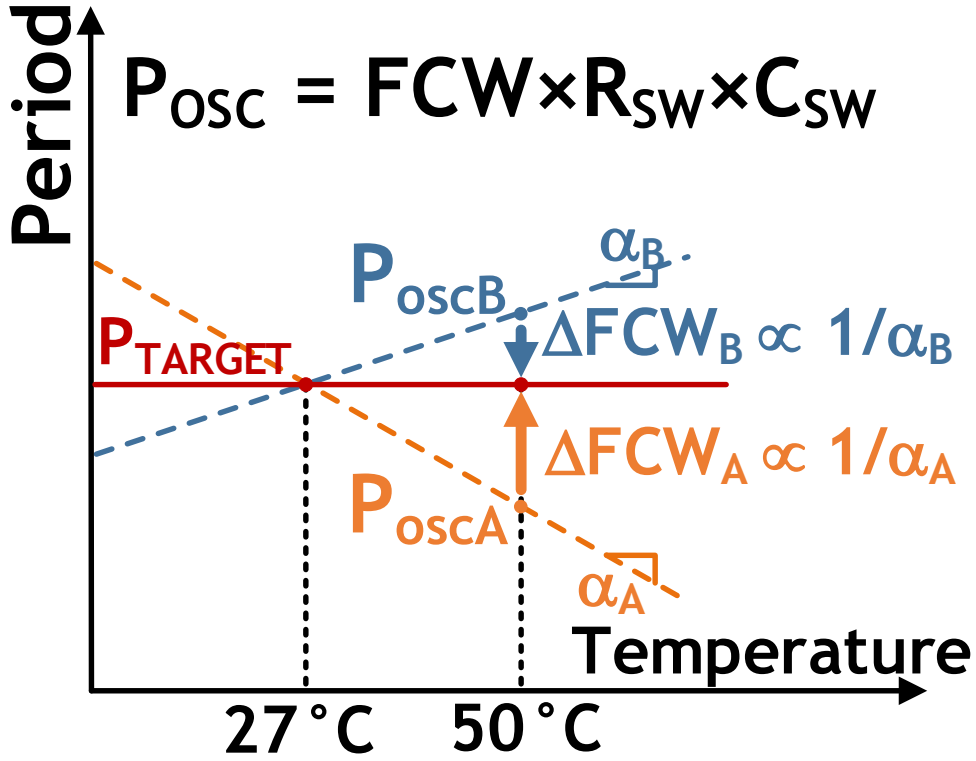

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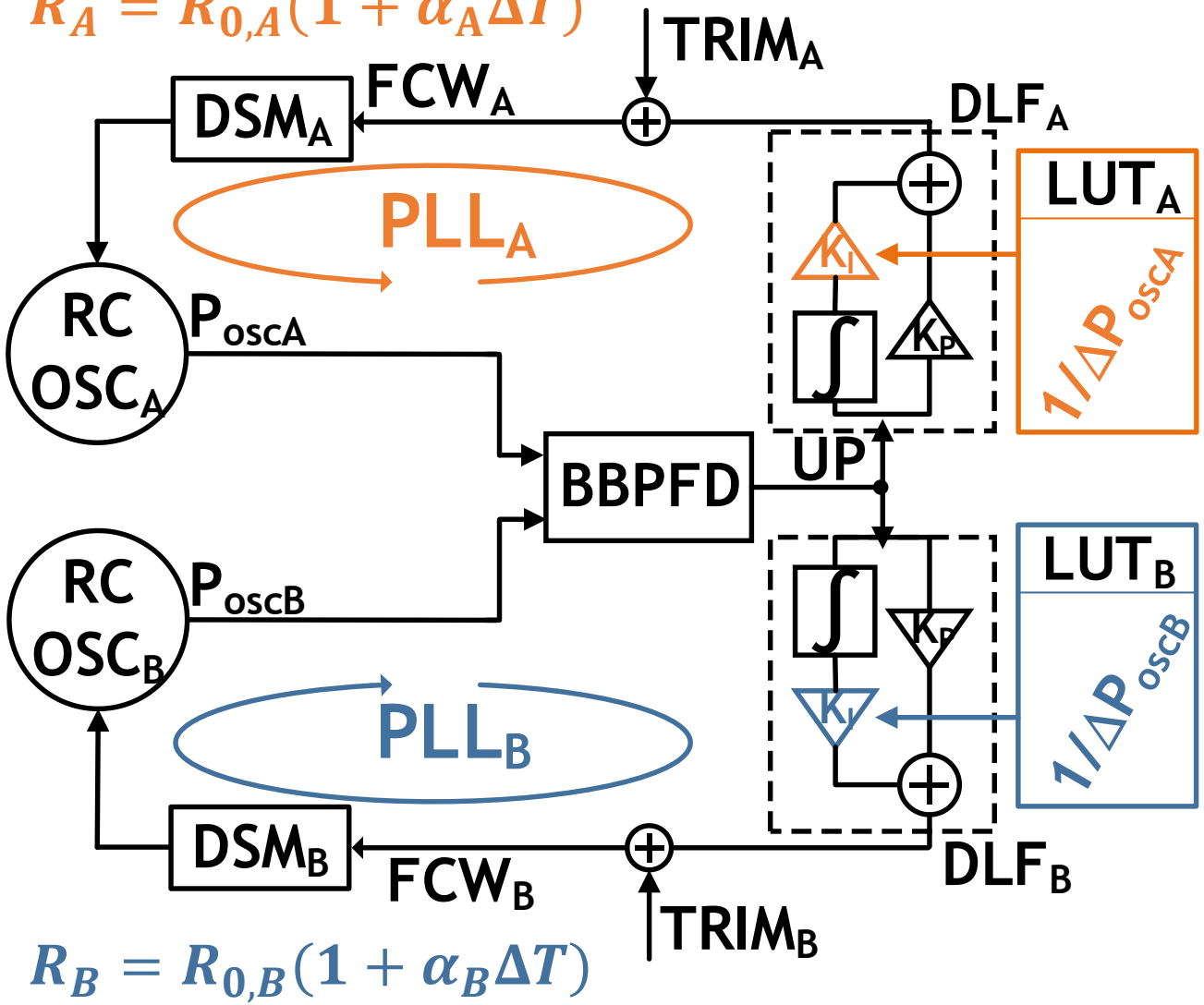

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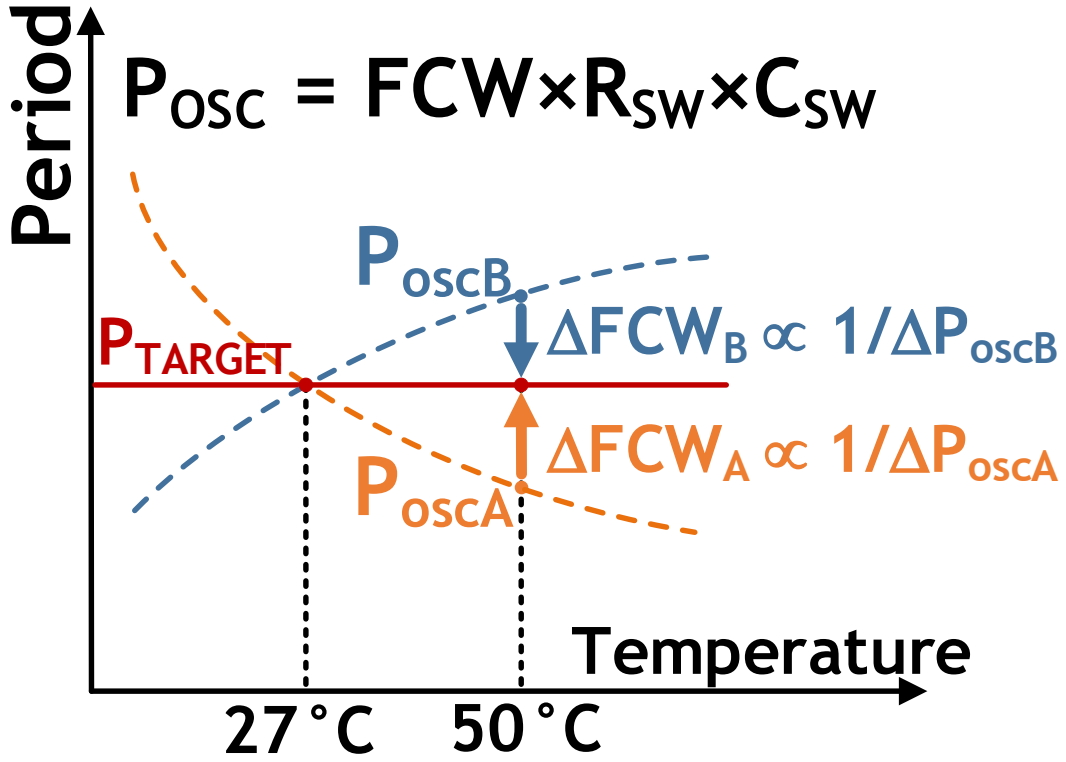

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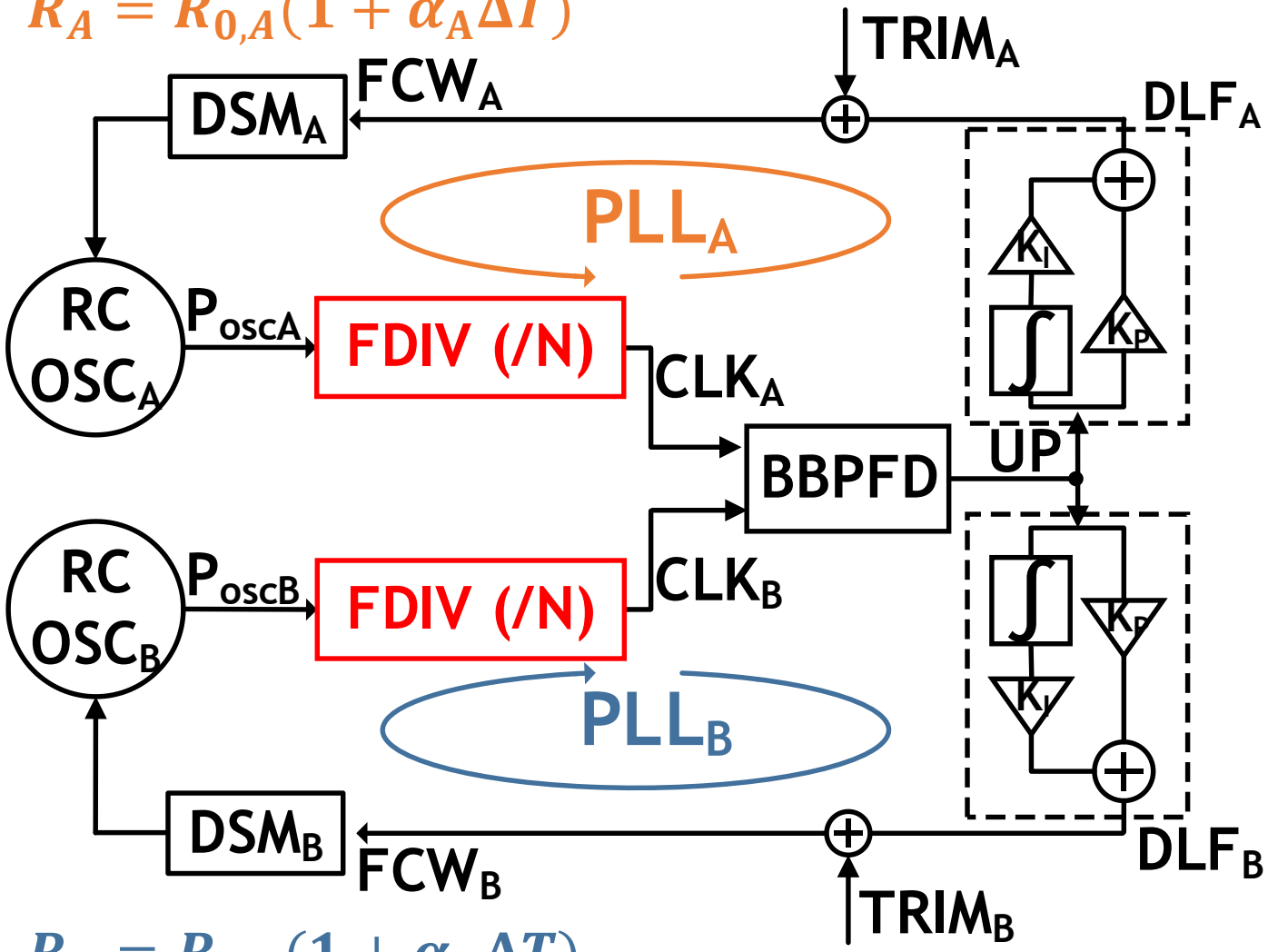

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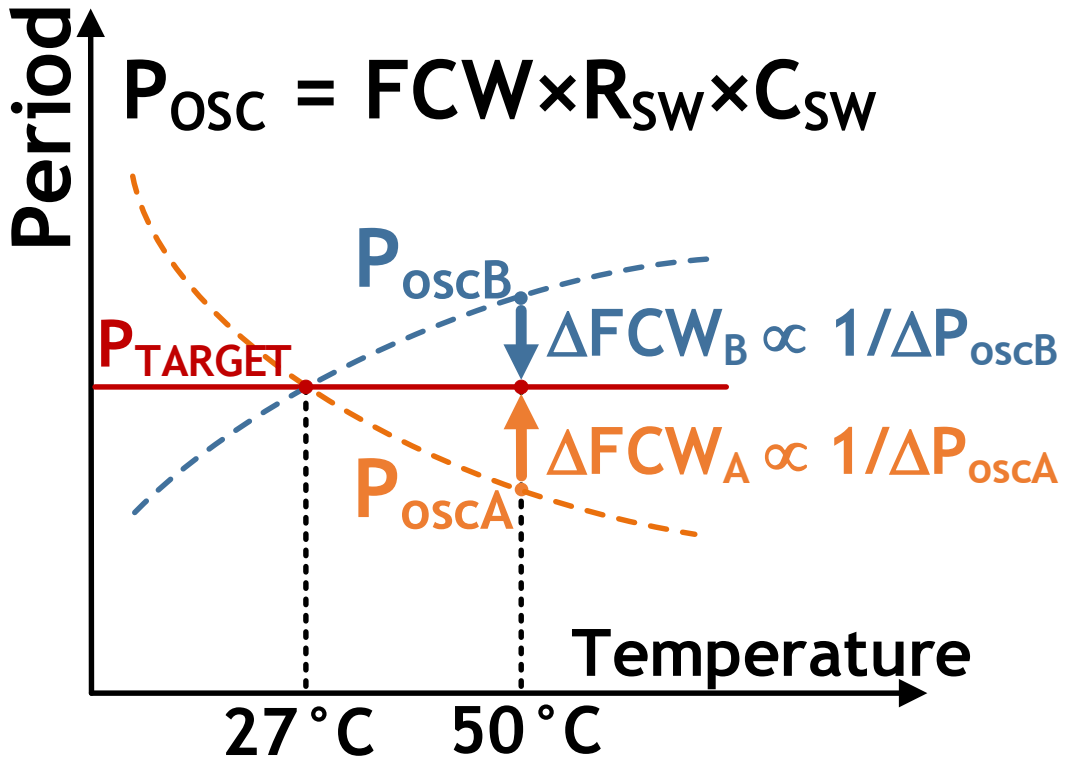

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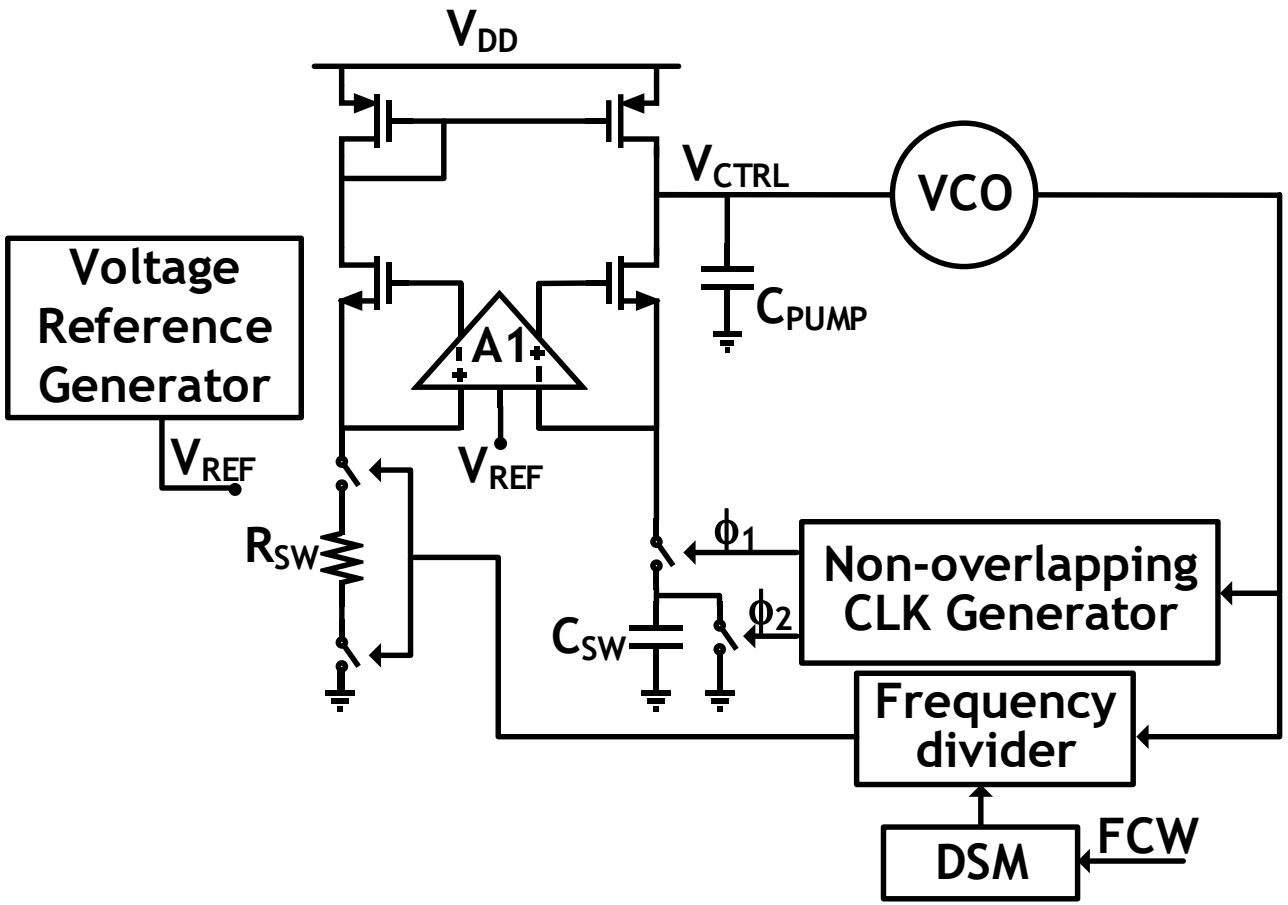
DSM-Controlled FLL



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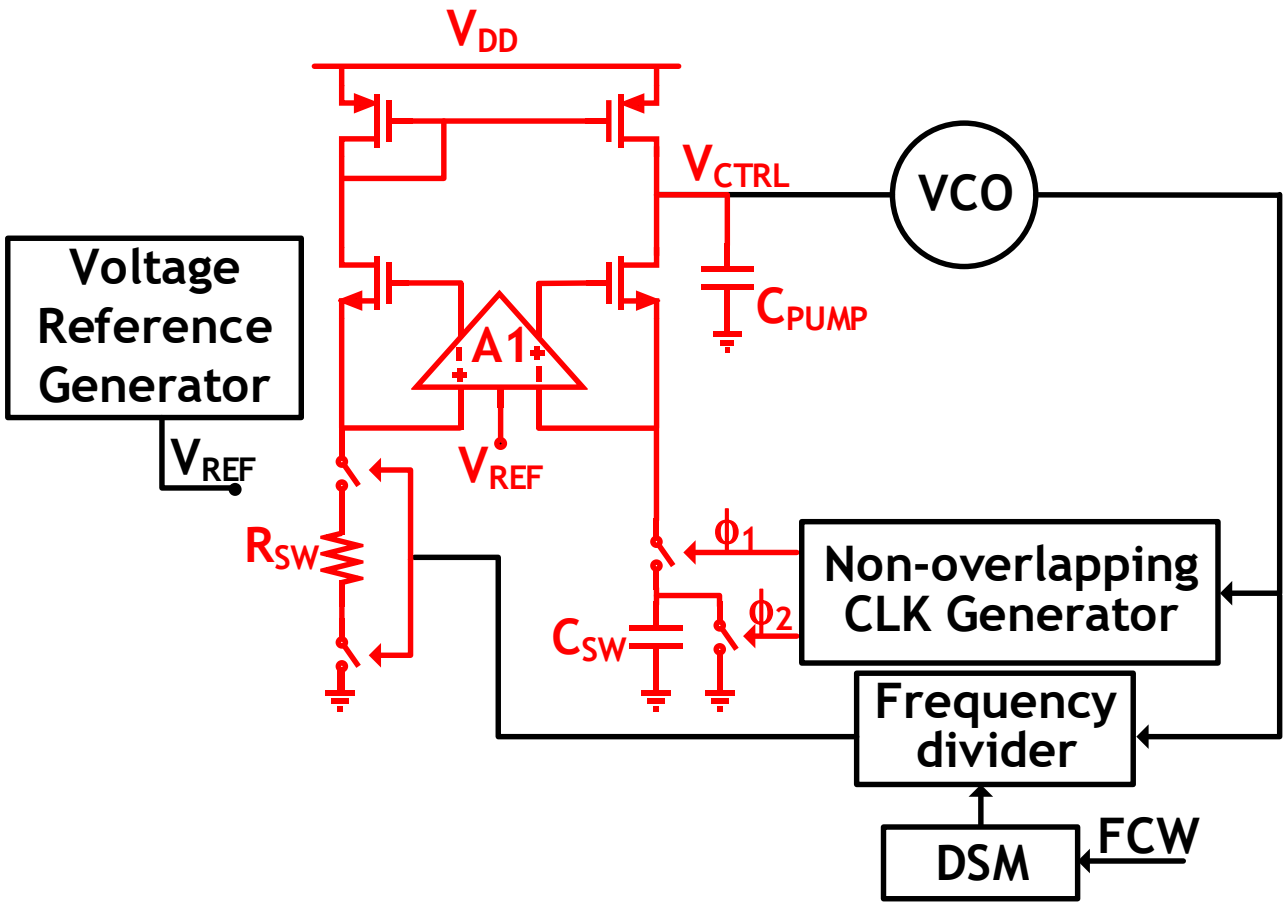

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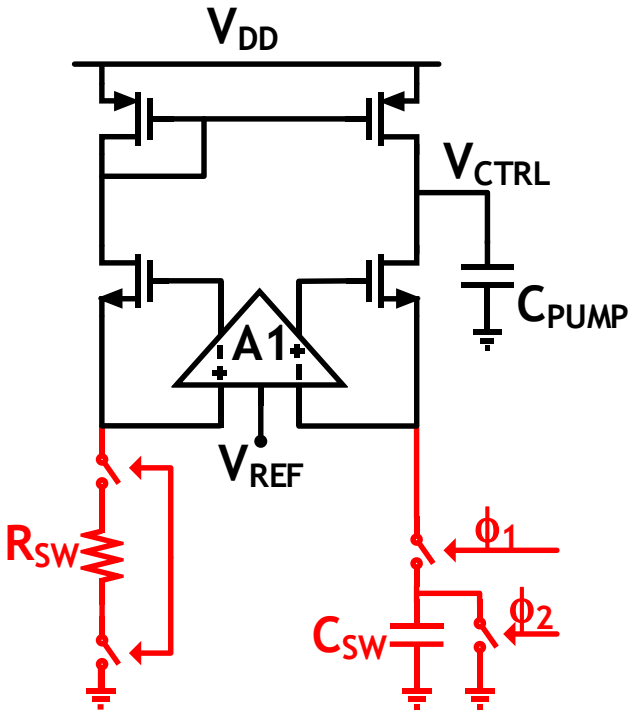
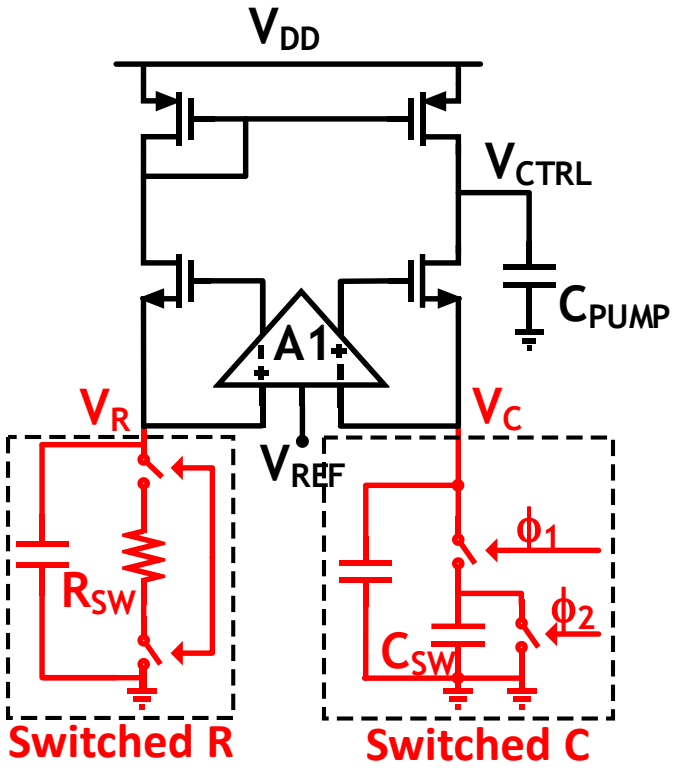


DSM-Controlled FLL

- Capacitors to reduce the ripple on V_R and V_C



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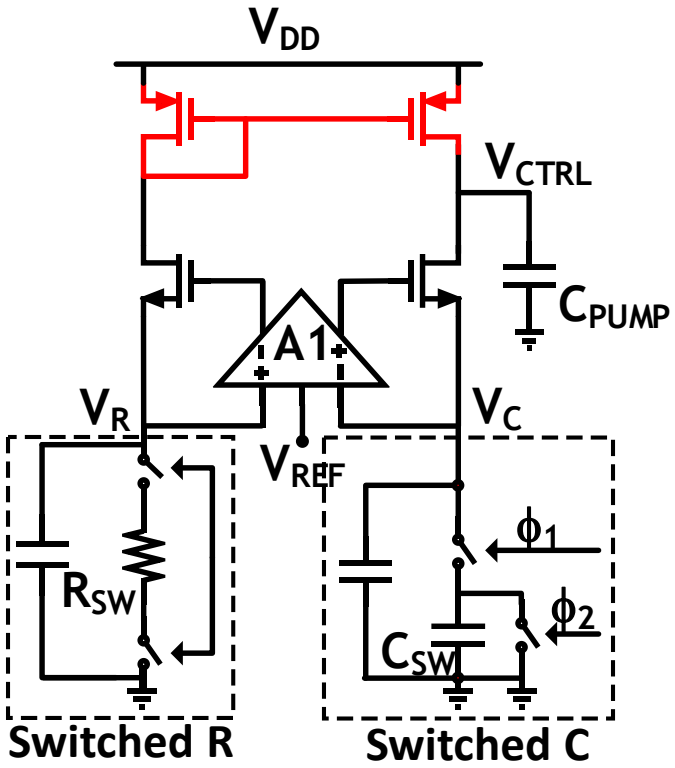

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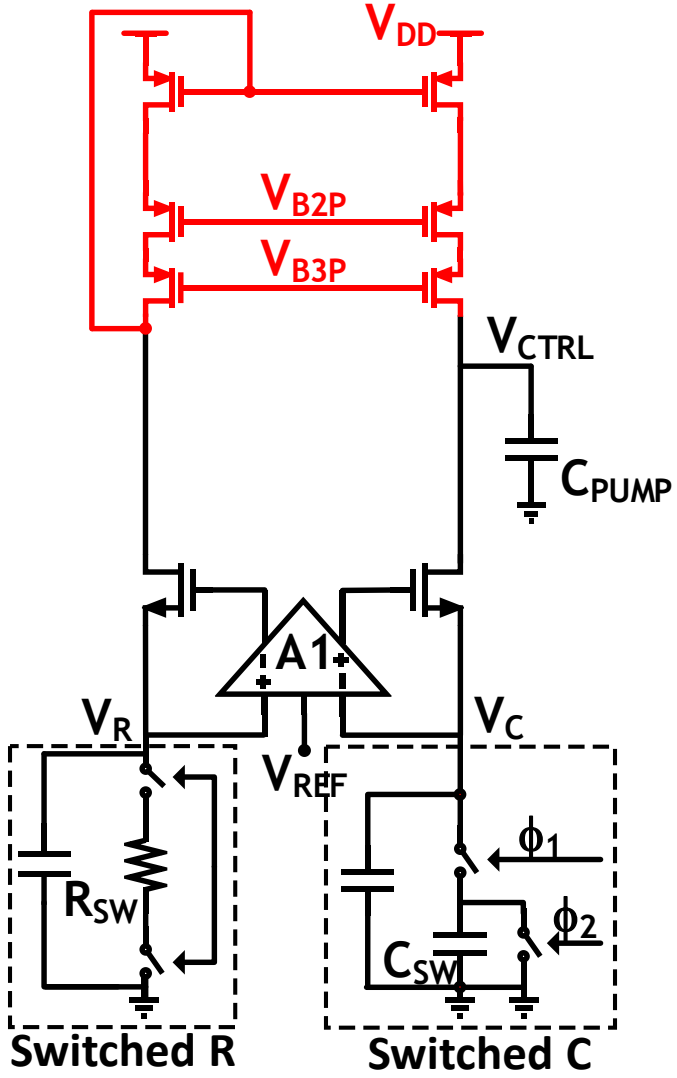
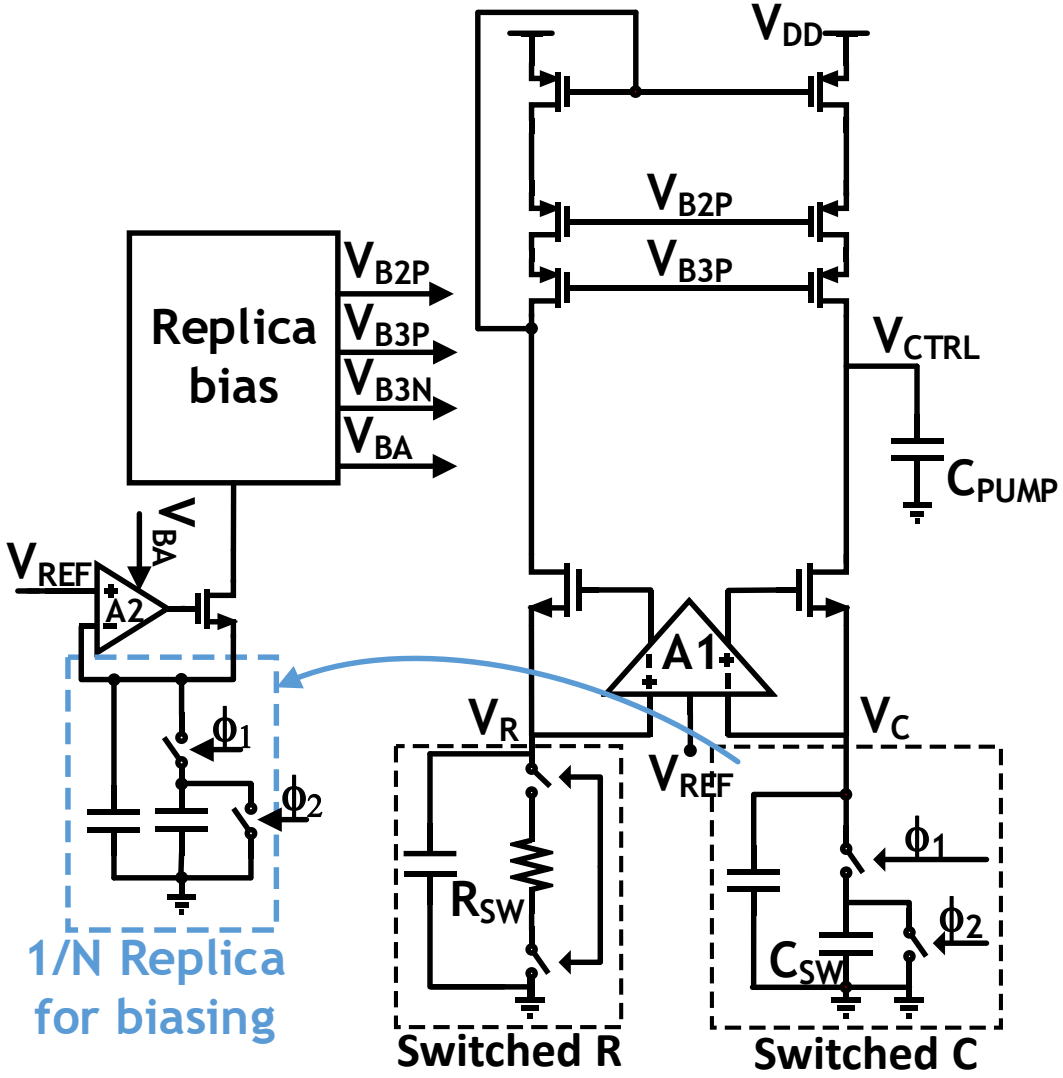


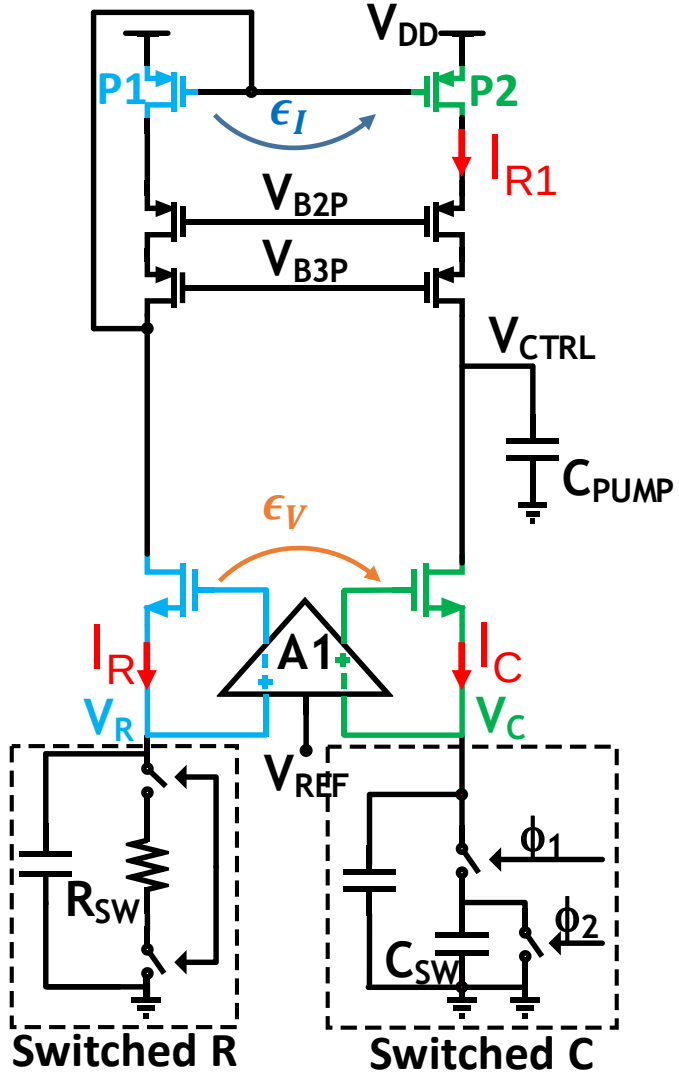
- Cascode stages for accurate mirroring

DSM-Controlled FLL



- Self- biased through a 1/N replica
- Stable across temperature, voltage and process variations

DSM-Controlled FLL



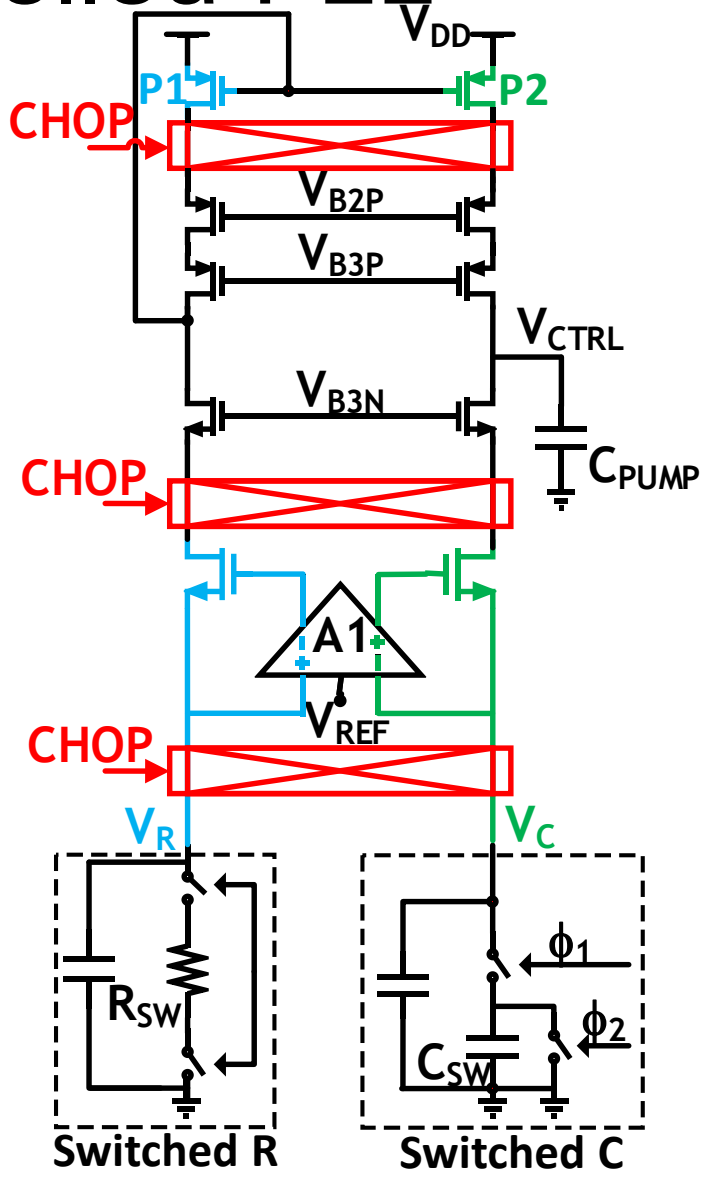
$$I_R = \frac{V_{REF}}{FCW * R_{SW}}$$

$$I_{R1} = I_R + \epsilon_I$$

$$I_C = (V_{REF} + \epsilon_V) * C_{SW} * f$$

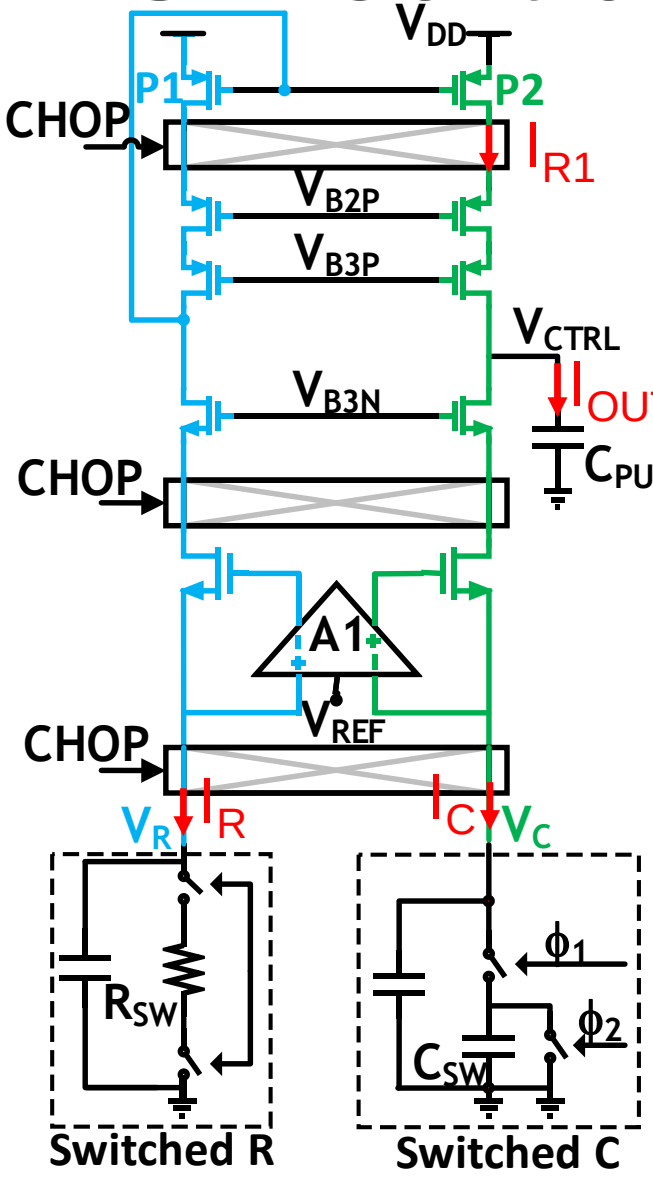
ϵ_I and ϵ_V are temperature dependent and have to be removed

DSM-Controlled FLL



- Chopping minimizes the impact of the amplifier and mirror offset

DSM-Controlled FLL



- **CHOP = 1**

$$I_R = \frac{V_{REF1}}{FCW * R_{SW}}$$

$$I_{R1} = I_R + \epsilon_I$$

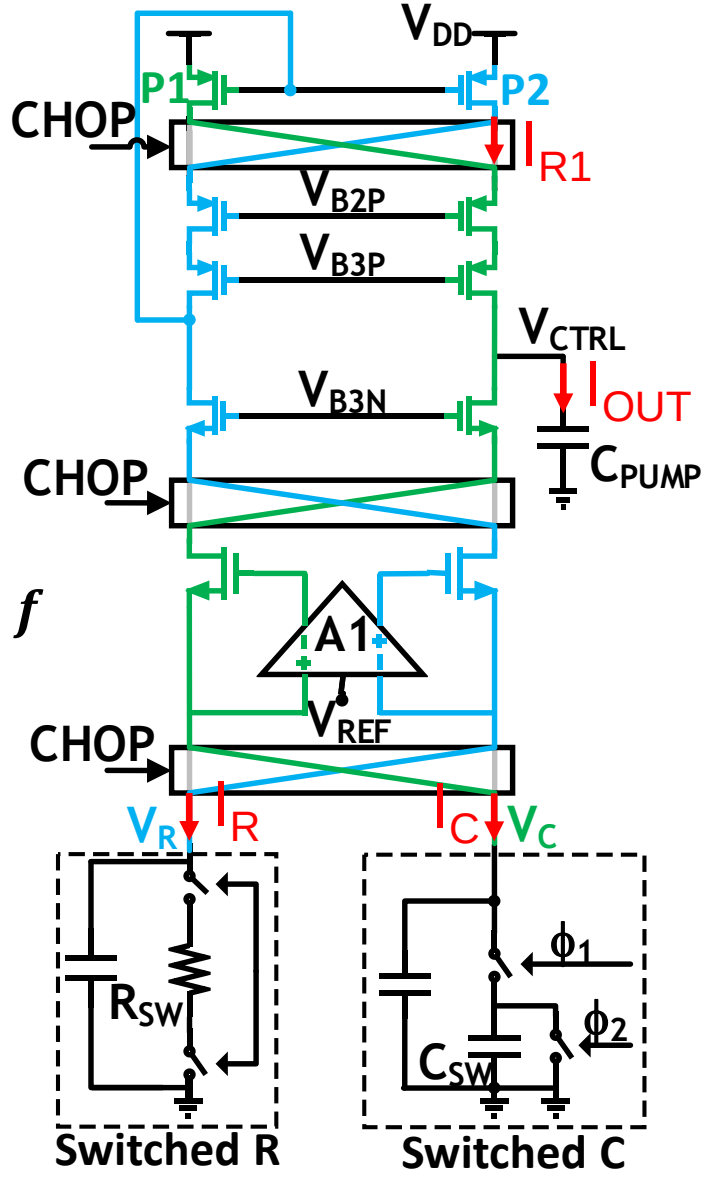
$$I_C = V_{REF2} * C_{SW} * f$$

- **CHOP = 0**

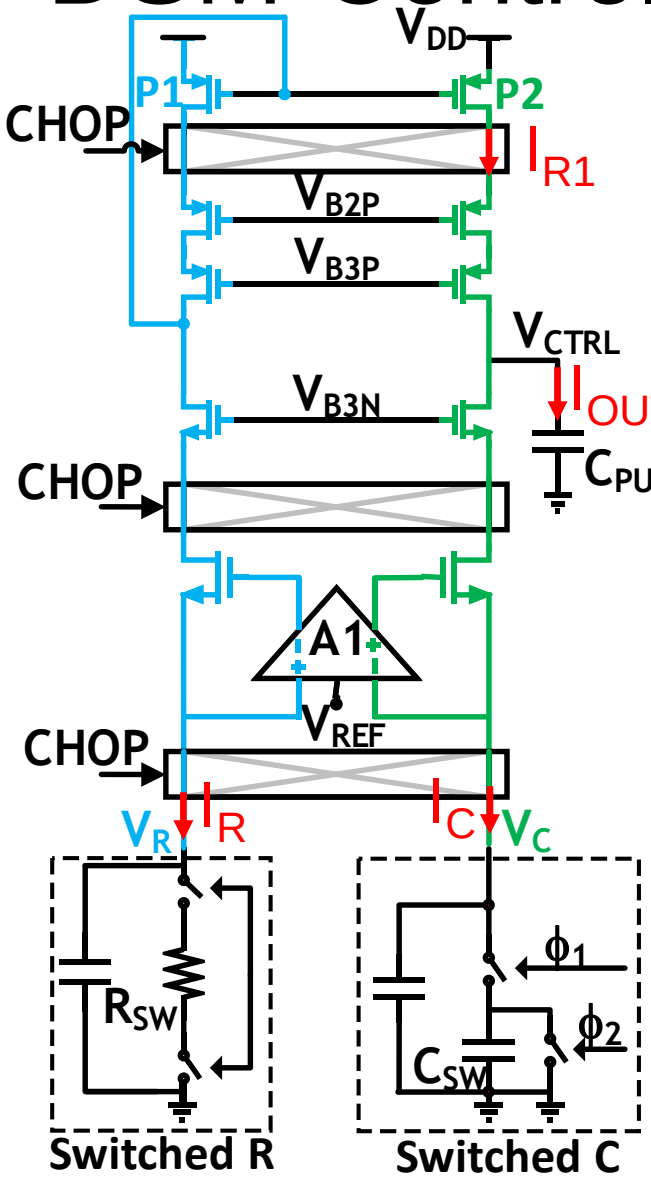
$$I_R = \frac{V_{REF2}}{FCW * R_{SW}}$$

$$I_{R1} = I_R - \epsilon_I$$

$$I_C = V_{REF1} * C_{SW} * f$$



DSM-Controlled FLL



$$I_R = \frac{V_{REF1}}{FCW * R_{SW}}$$

$$I_{R1} = I_R + \epsilon_I$$

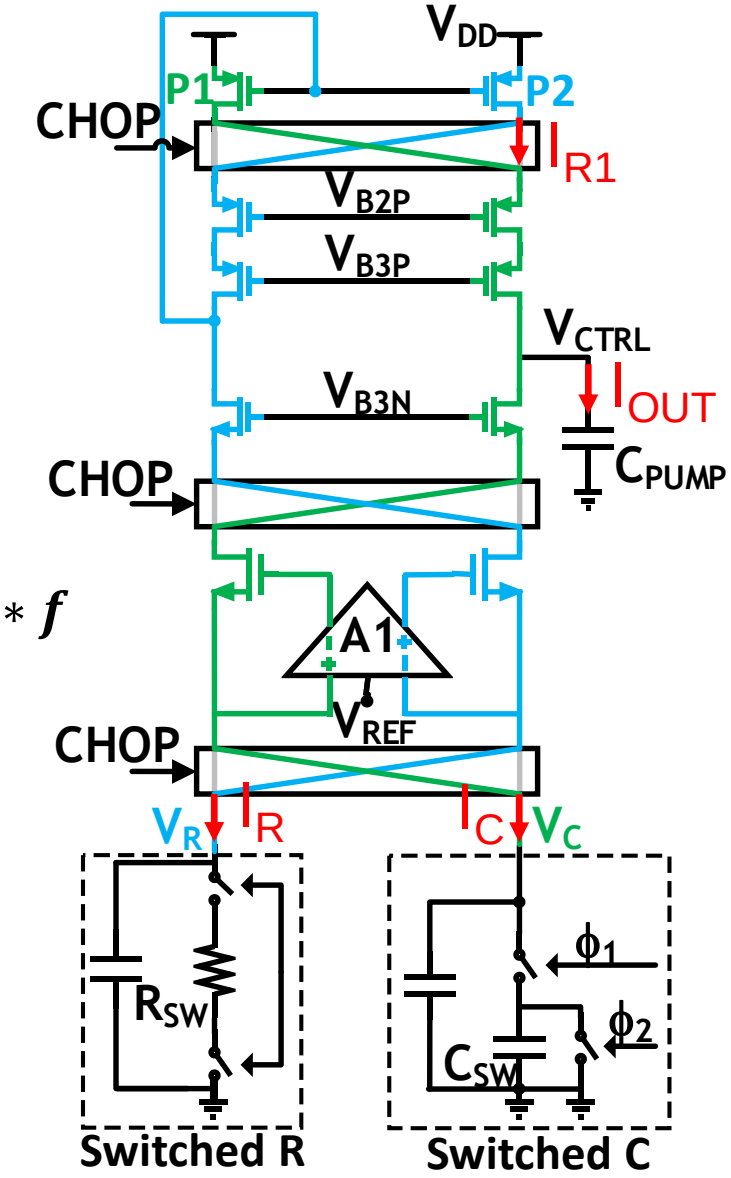
$$I_C = V_{REF2} * C_{SW} * f$$

$$I_R = \frac{V_{REF2}}{FCW * R_{SW}}$$

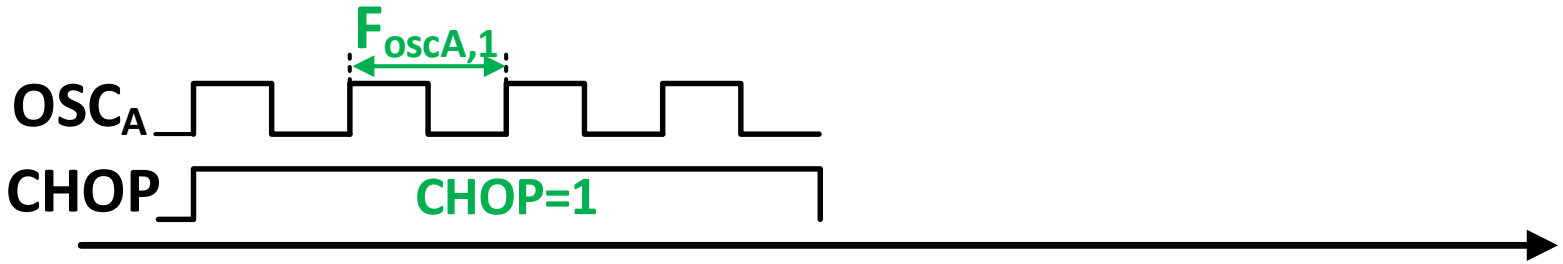
$$I_{R1} = I_R - \epsilon_I$$

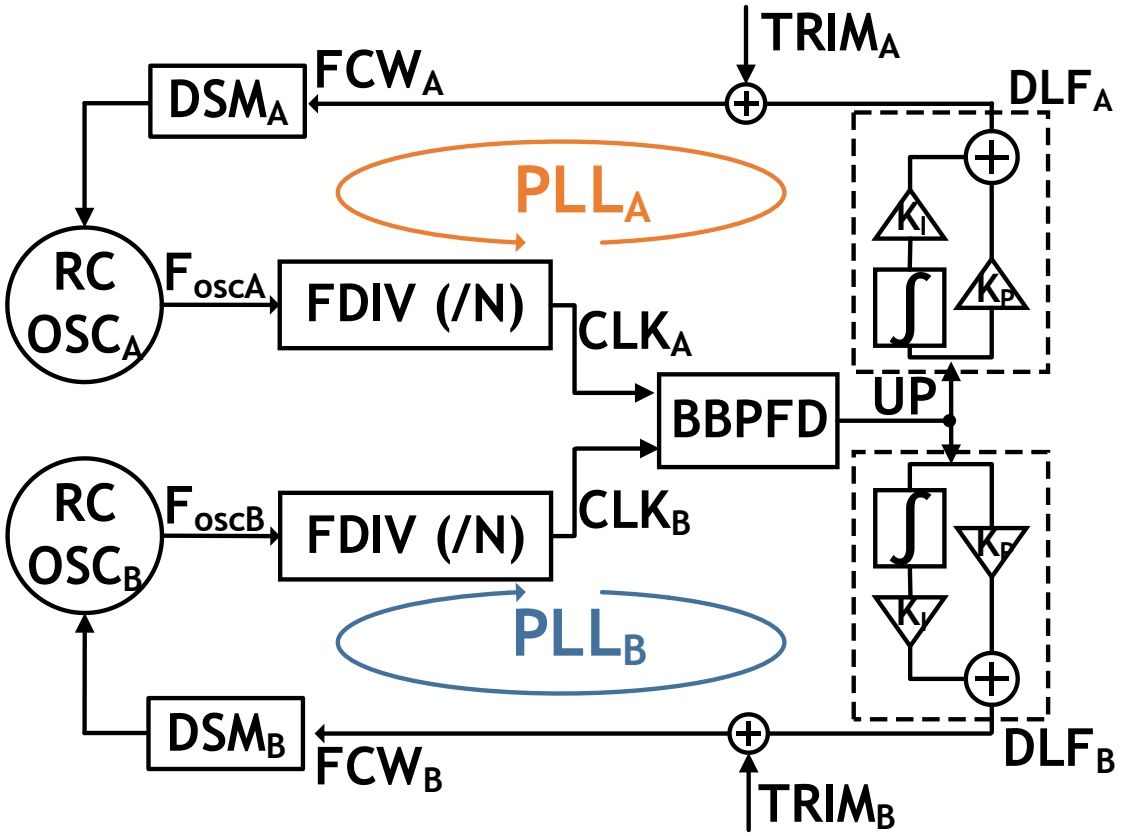
$$I_C = V_{REF1} * C_{SW} * f$$

Which signal should be used for chopping?

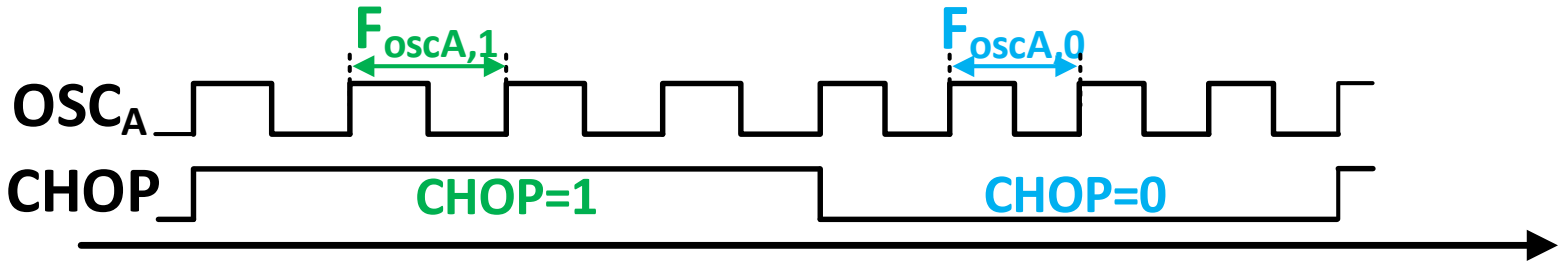


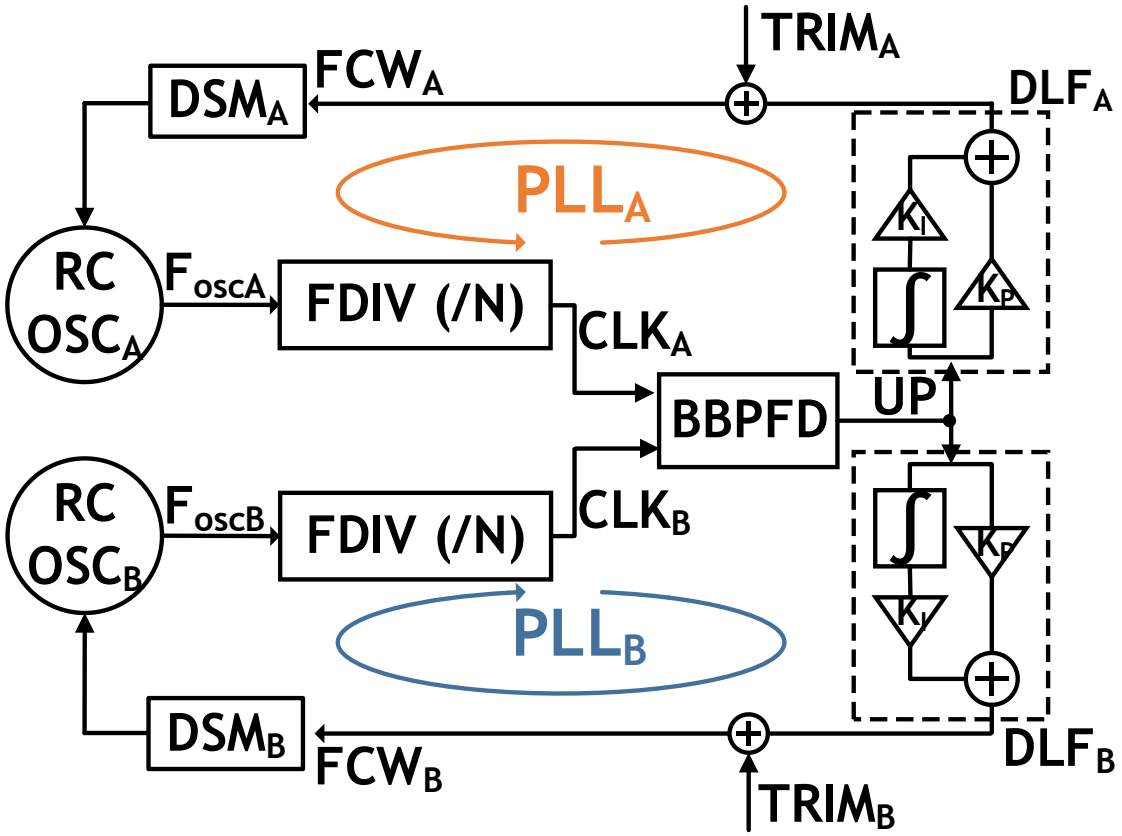
DSM-Controlled FLL



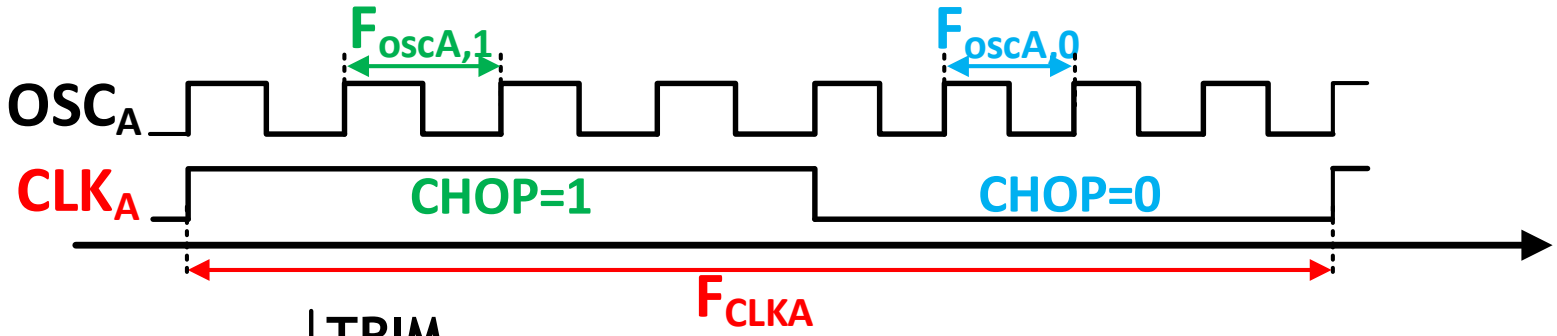


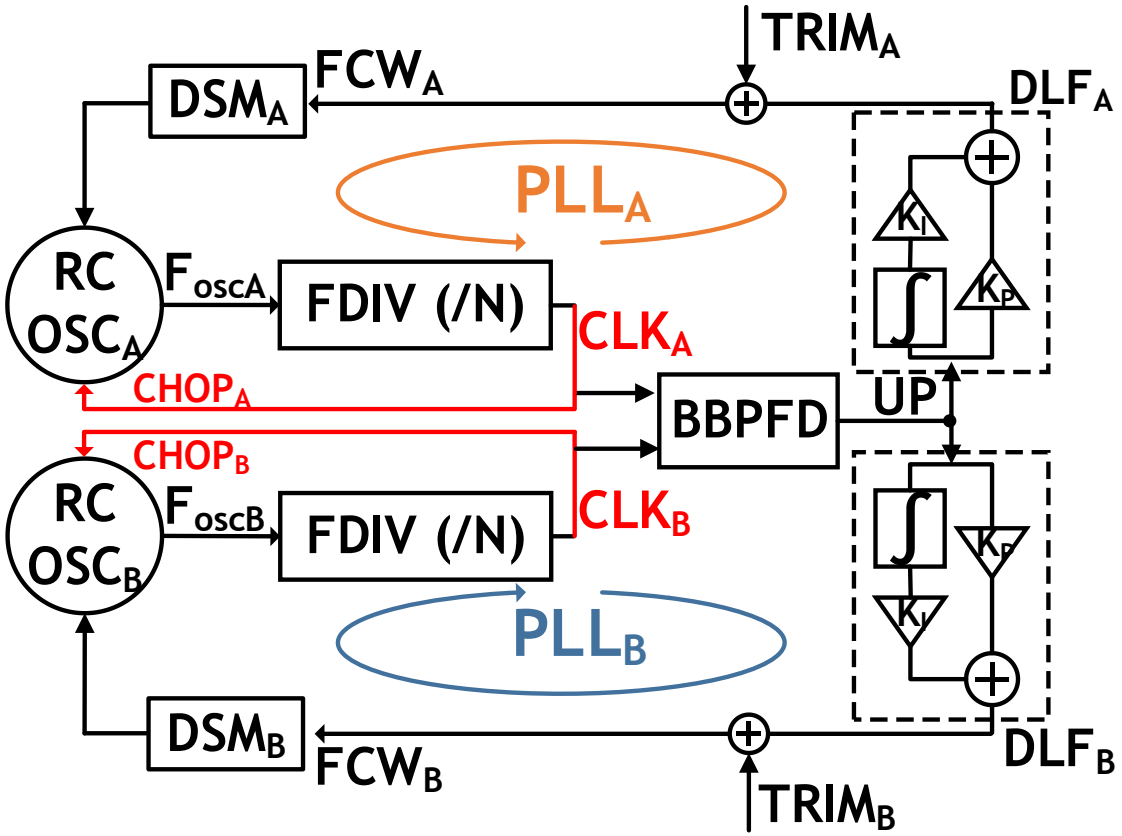
DSM-Controlled FLL





DSM-Controlled FLL





- Each PLL reference period is the average of both chopping phases
- The PLL is not affected by frequency ripples due to chopping

Outline

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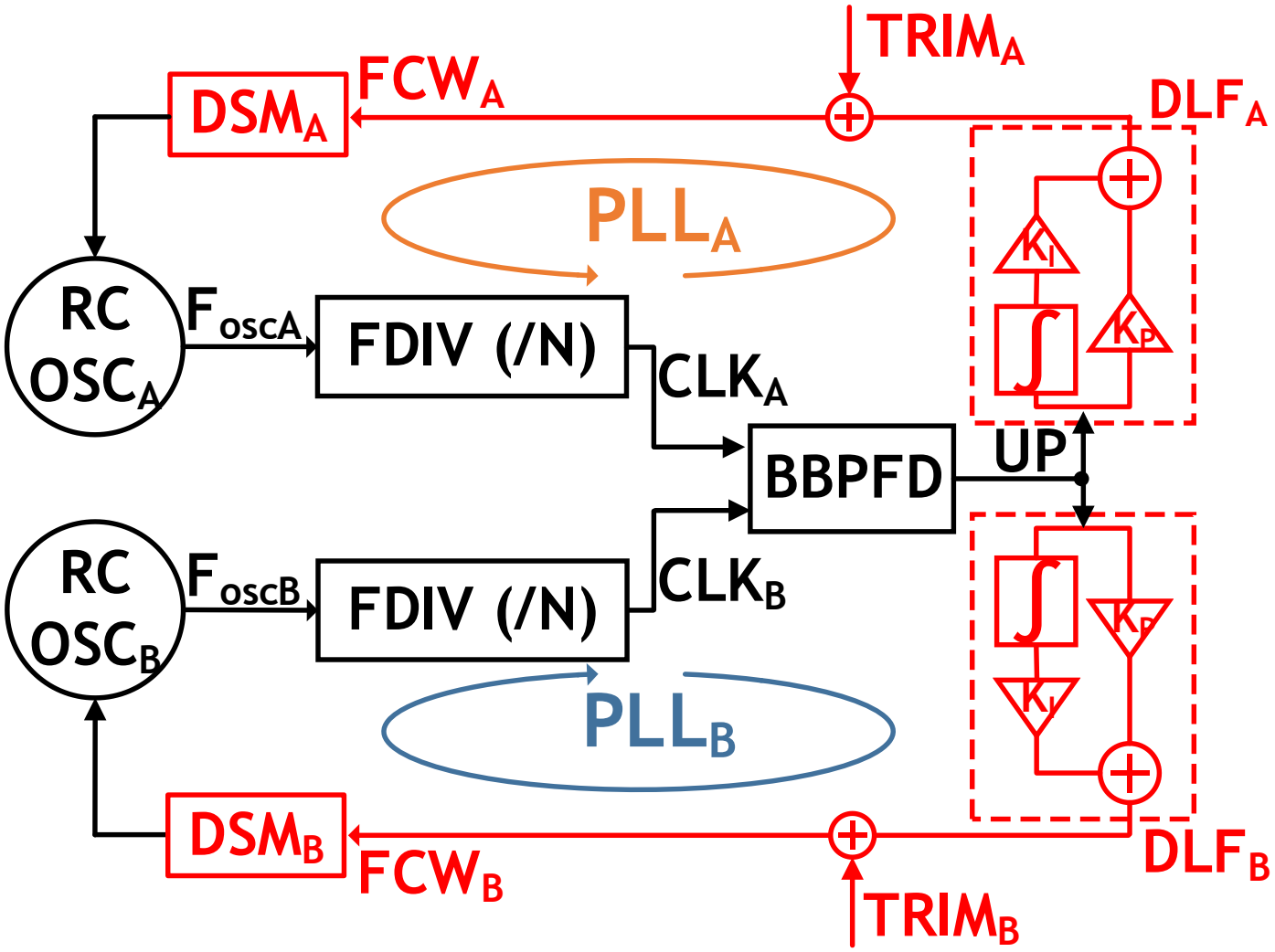
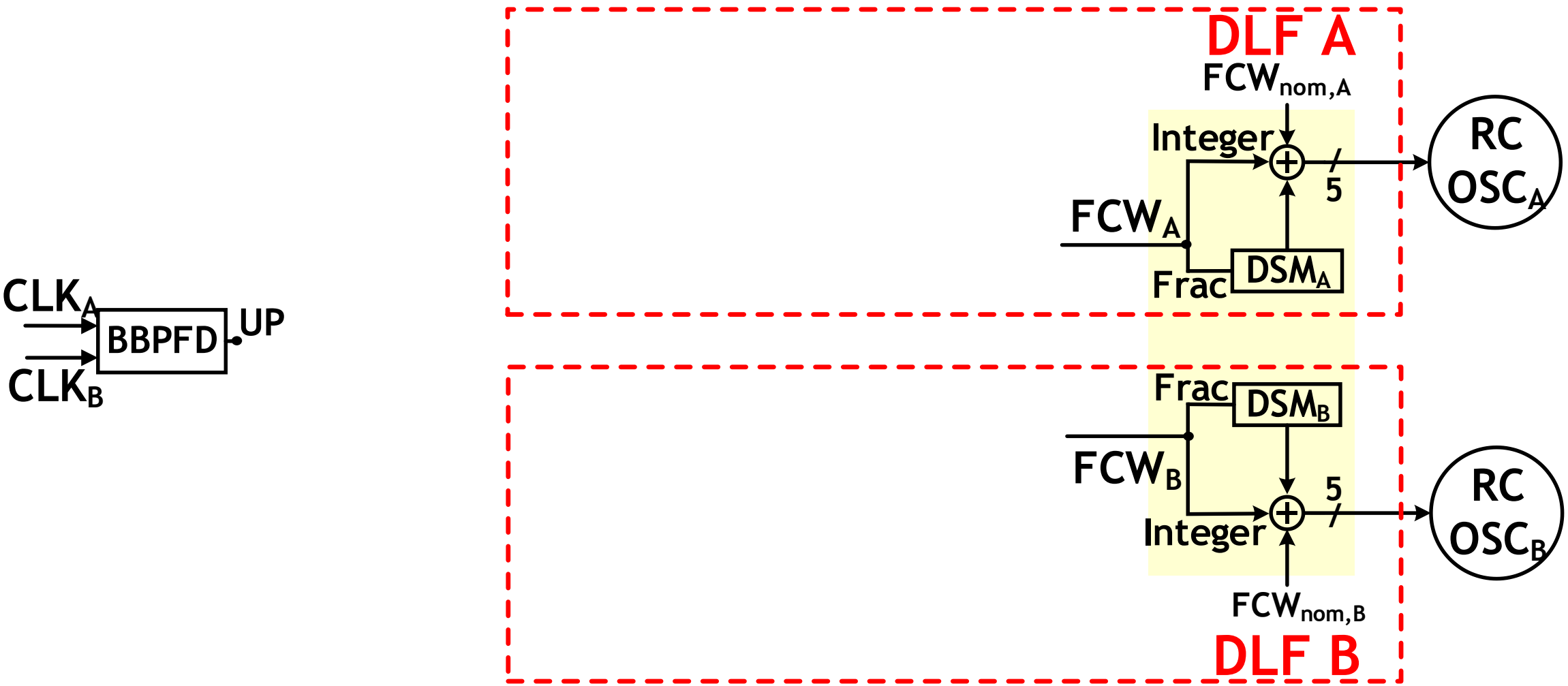
Non-linearity aware DLF



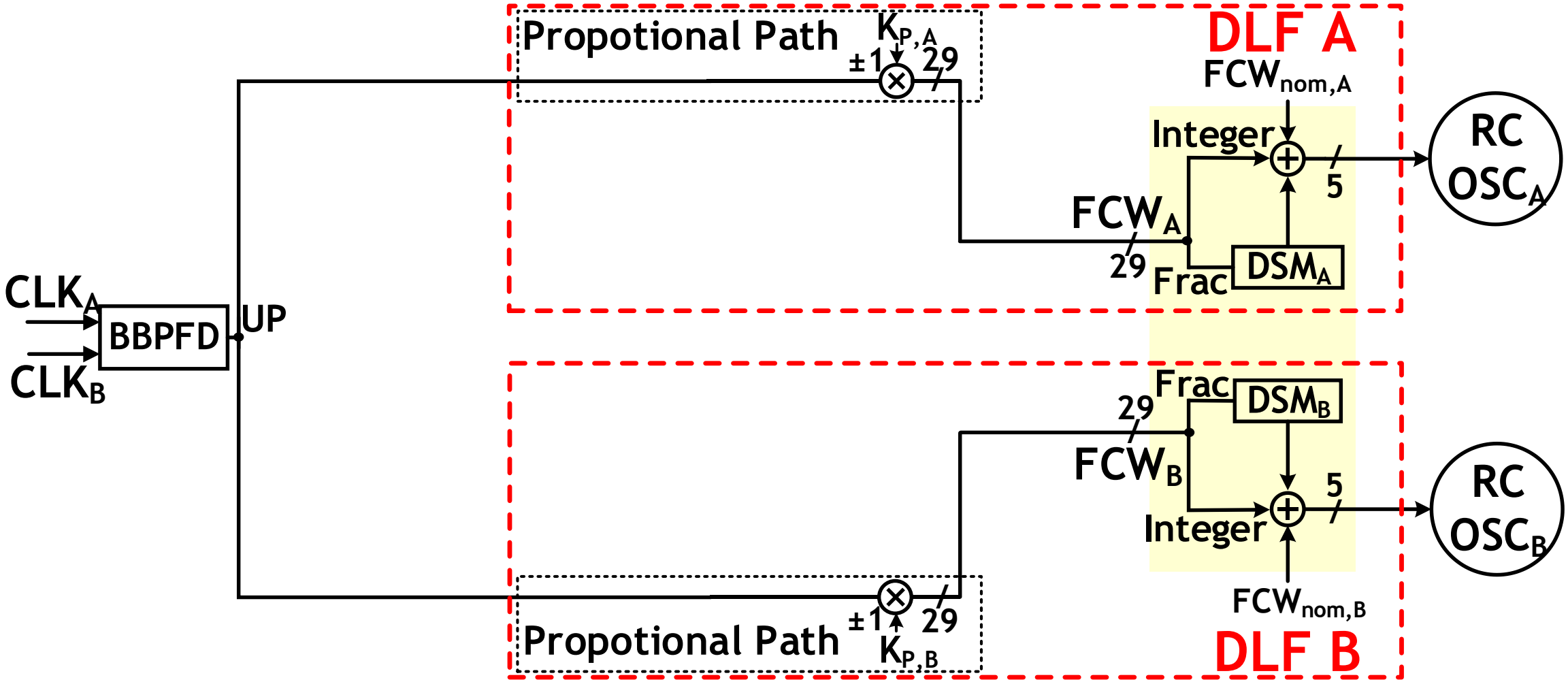
Non-linearity aware DLF

- Input: 1 bit BBPFD
- Output: FCW to FLLs in 5 bits (DSM driven)



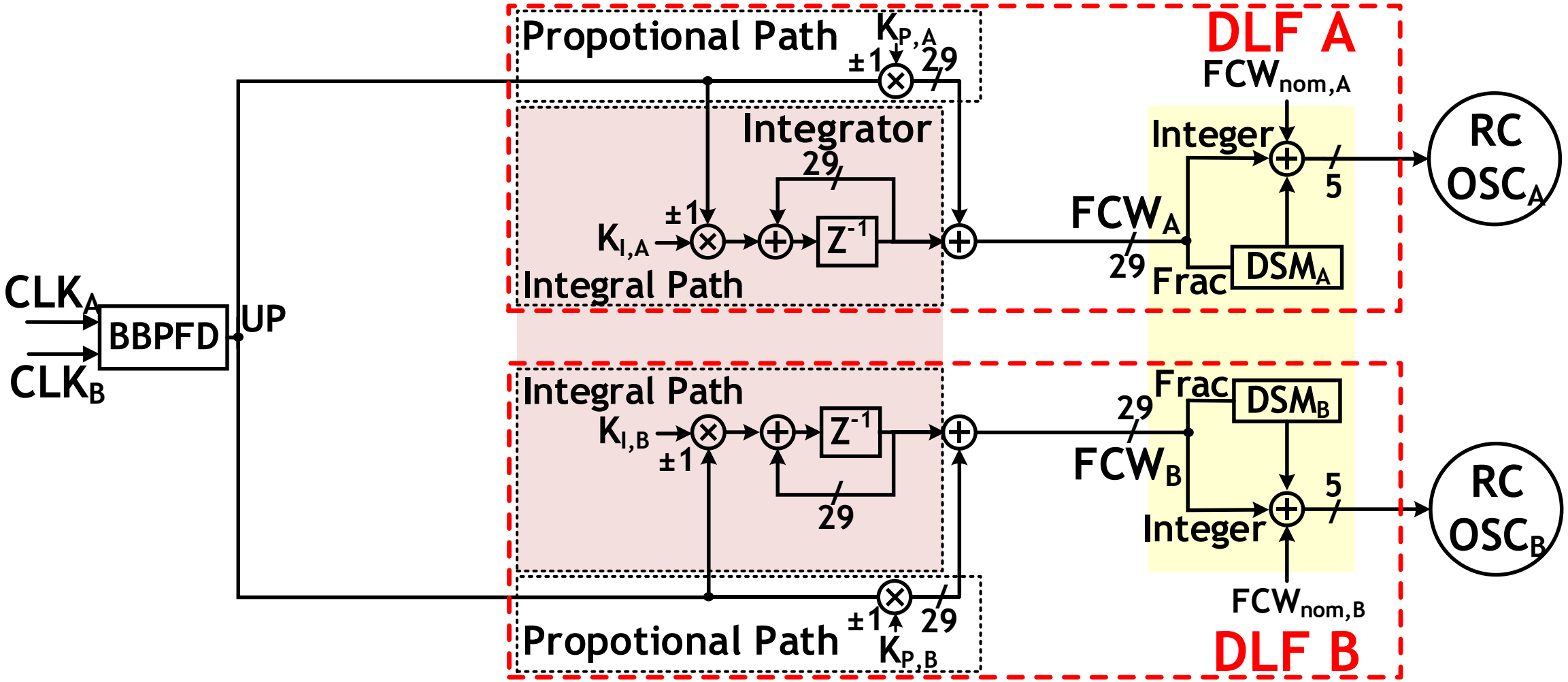
Non-linearity aware DLF

- 29 bits proportional path with programmable gain K_P



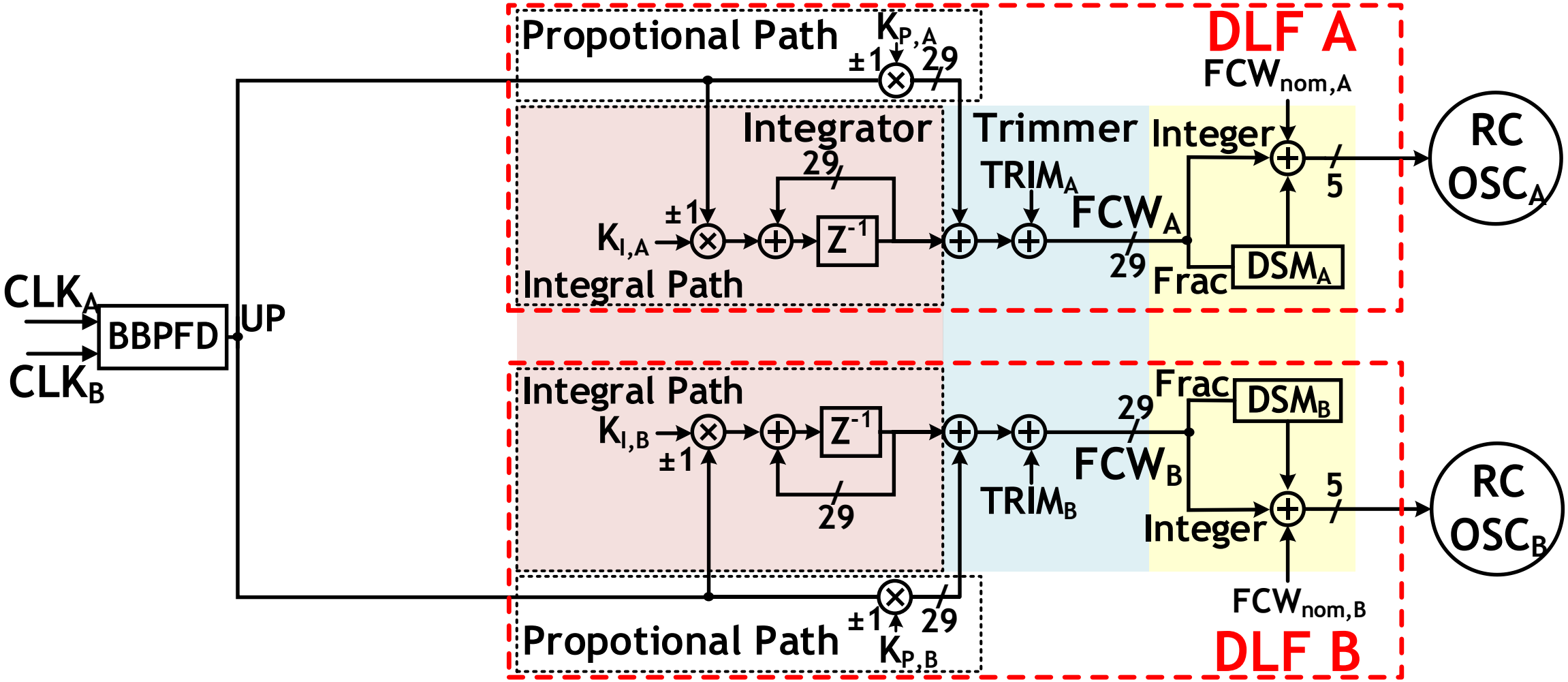
Non-linearity aware DLF

- 29 bits proportional path with programmable gain K_P
- 29 bits integral path with gain K_I



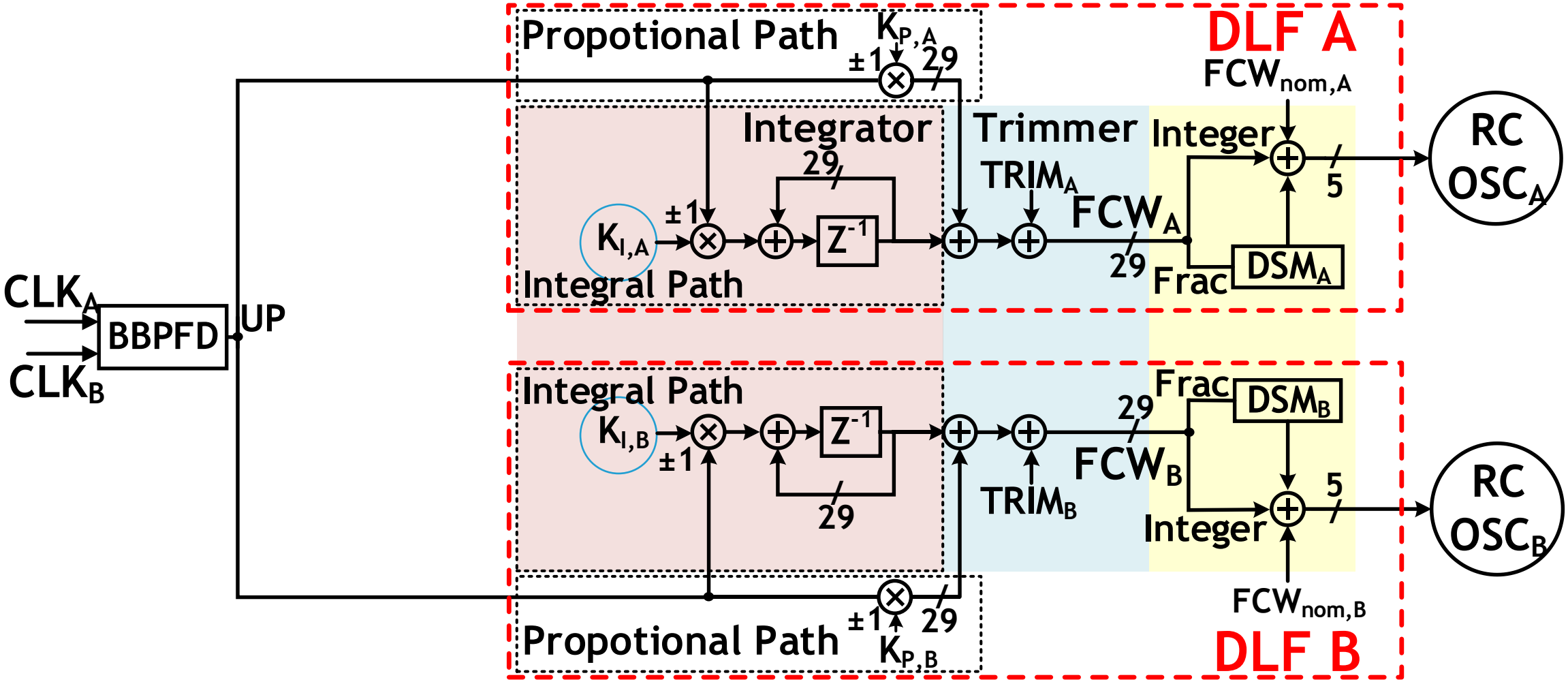
Non-linearity aware DLF

- Additional input TRIM for frequency trimming
- Fractional part (24 LSBs) goes to DSM, which is added to integer part (5 MSBs)

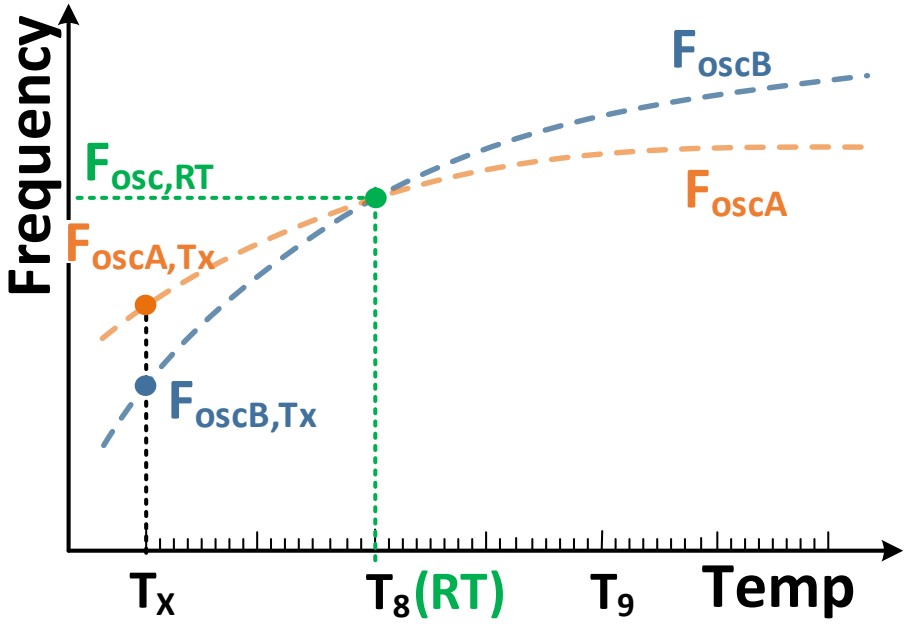


Non-linearity aware DLF

- How are the integral gains generated?



Non-linearity aware DLF



$$(FCW_{RT} = FCW_{nom} + TRIM)$$

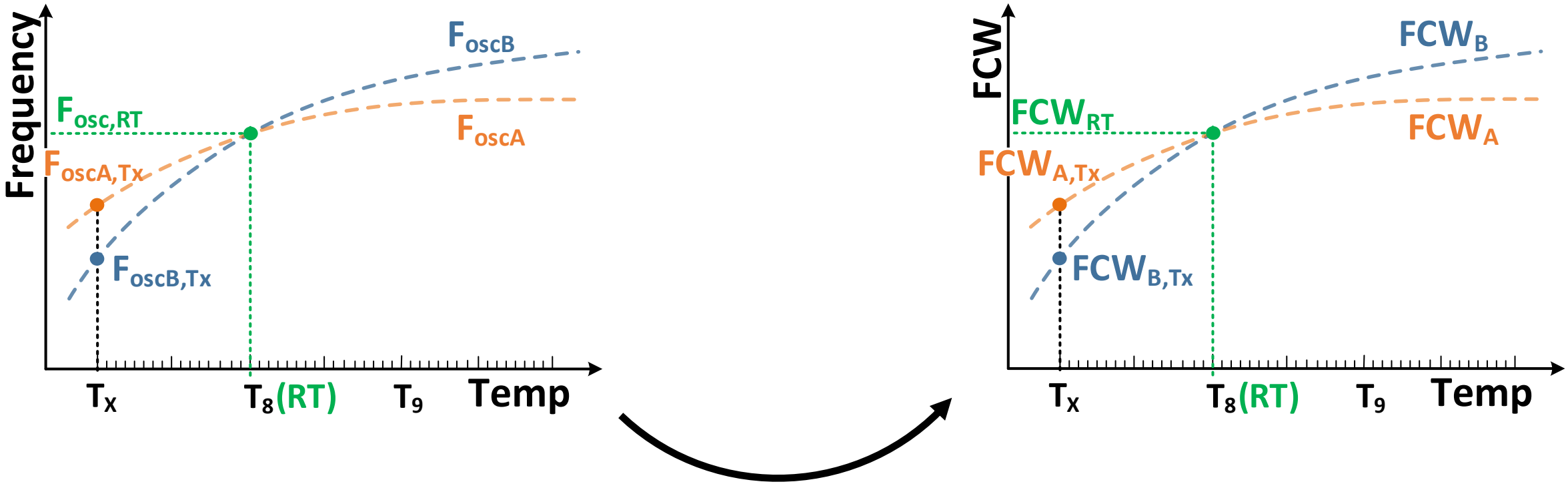
$$F_{osc}(T) = \frac{1}{FCW_{RT} * R(T) * C}$$

Compensate temperature variation through FCW(T)

$$F_{osc,RT} = \frac{1}{FCW(T) * R(T) * C}$$

$$FCW(T) = \frac{1}{F_{osc,RT} * R(T) * C} = FCW_{RT} \frac{F_{osc}(T)}{F_{osc,RT}}$$

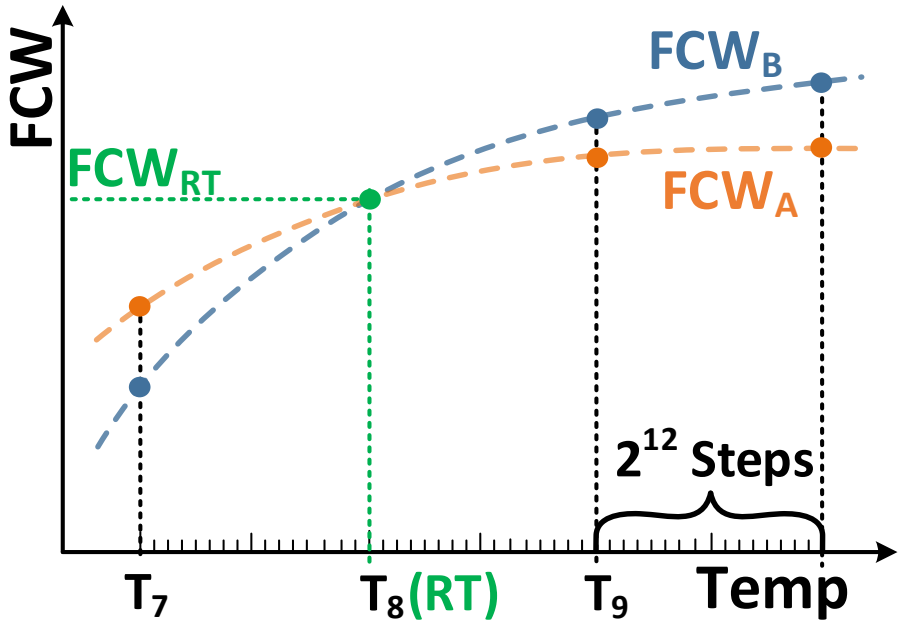
Non-linearity aware DLF



$$FCW(T) = FCW_{RT} \frac{F_{osc}(T)}{F_{osc_{RT}}}$$

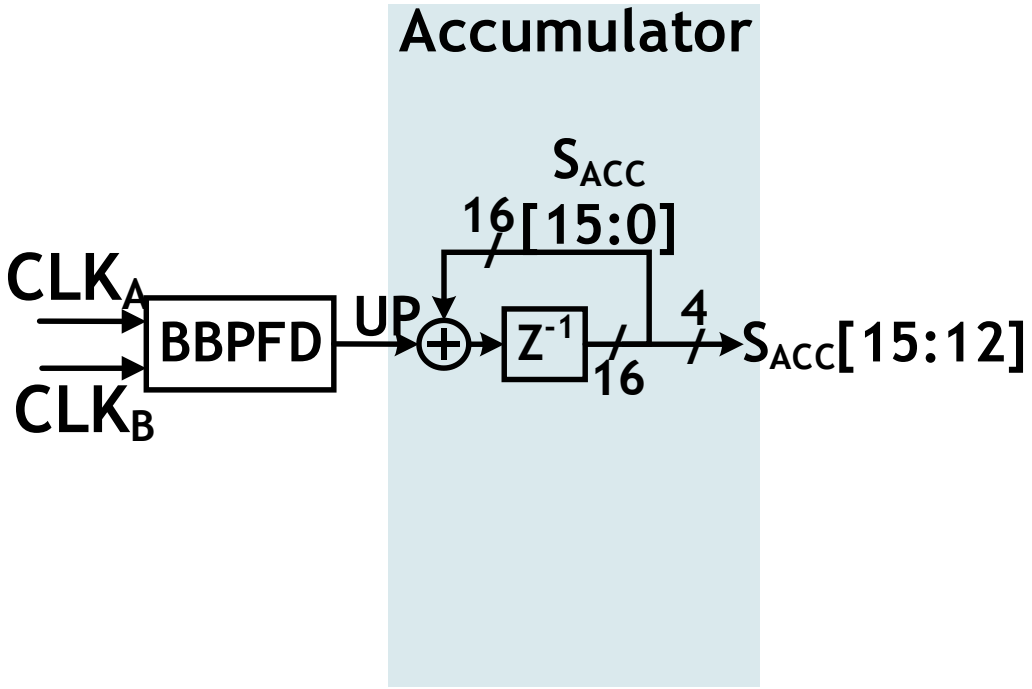
Non-linearity aware DLF

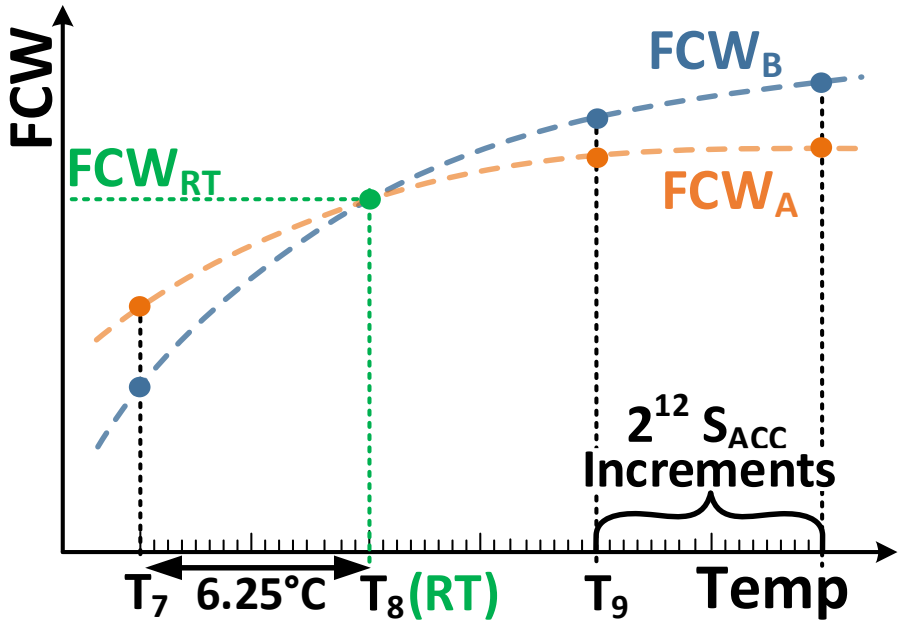
- The FCW function is divided in multiple intervals
- Each interval contains multiple steps



Non-linearity aware DLF

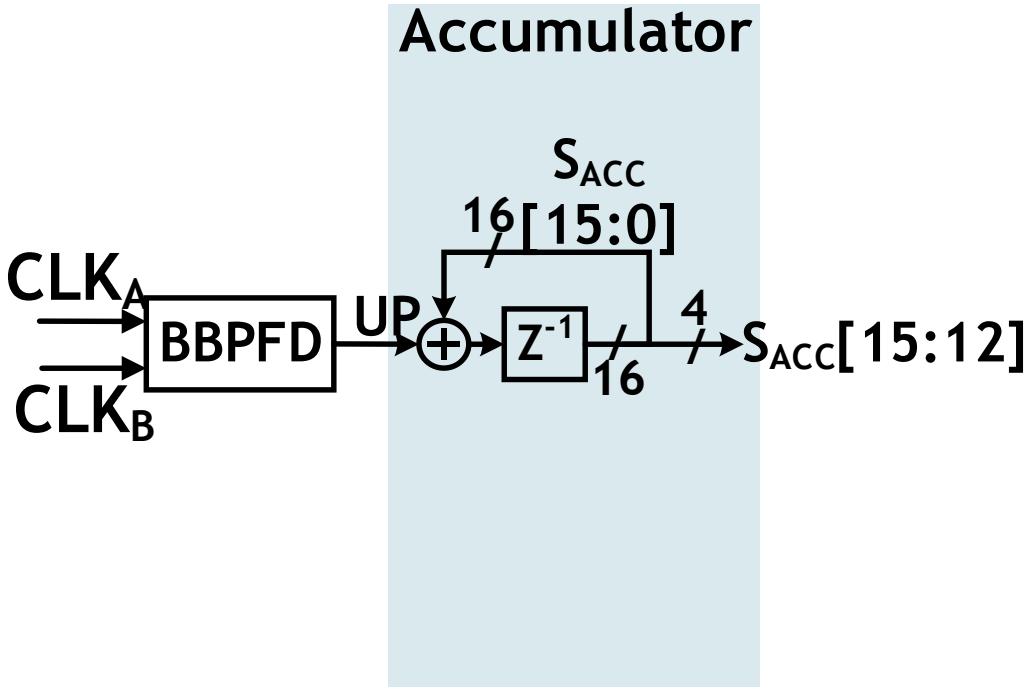
- UP is accumulated on 16 bits, 4MSBs are fed to next stage
- This generates 2^4 intervals of 2^{12} steps each.

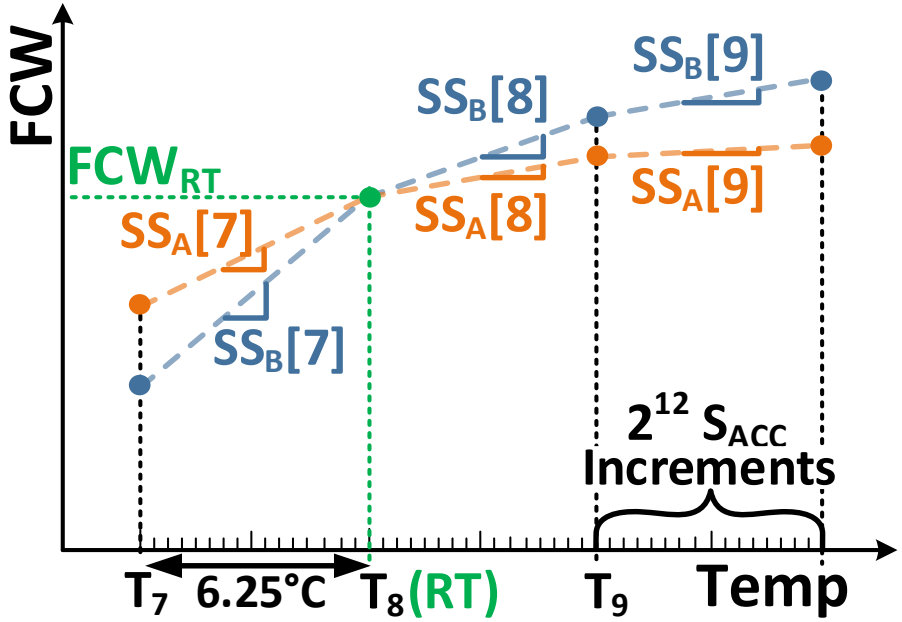




Non-linearity aware DLF

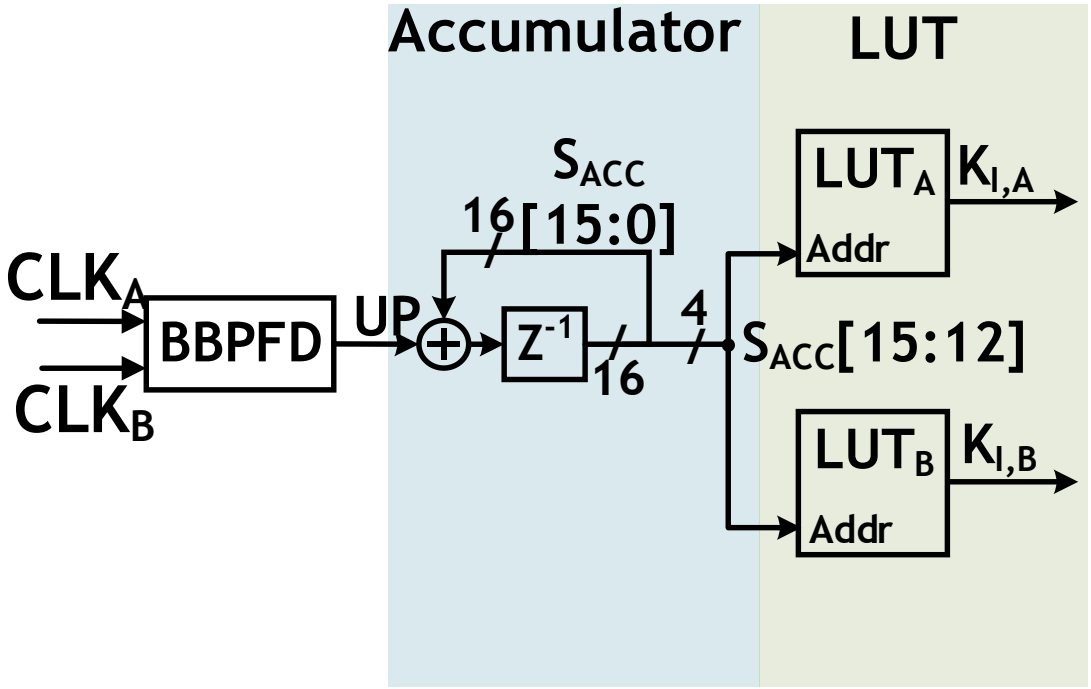
- UP is accumulated on 16 bits, but only the 4MSBs are considered.
- This generates 2^4 intervals of 2^{12} steps each.

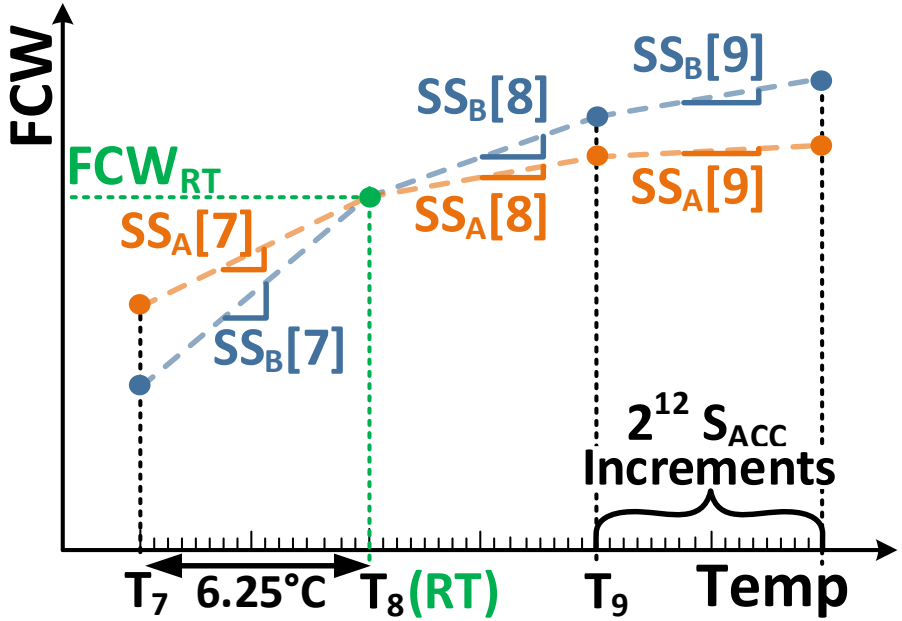


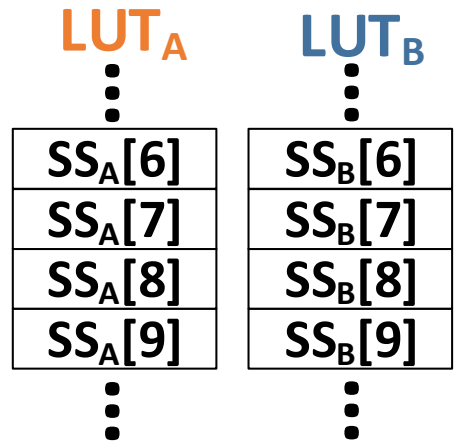


Non-linearity aware DLF

- The slope SS is stored in a LUT
- The 4MSBs of S_{ACC} are used as LUT addresses
- The integral path accumulates the LUT entry value

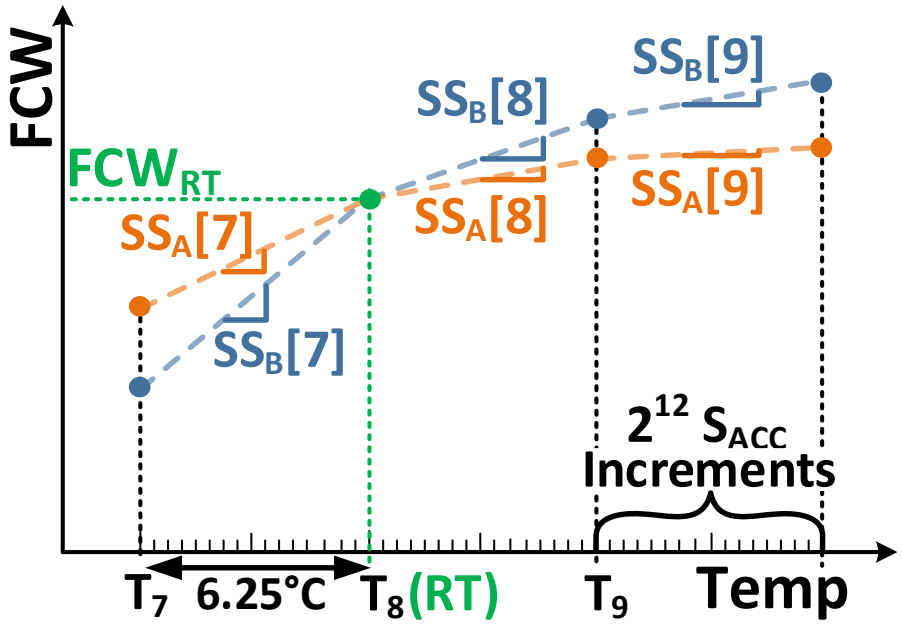


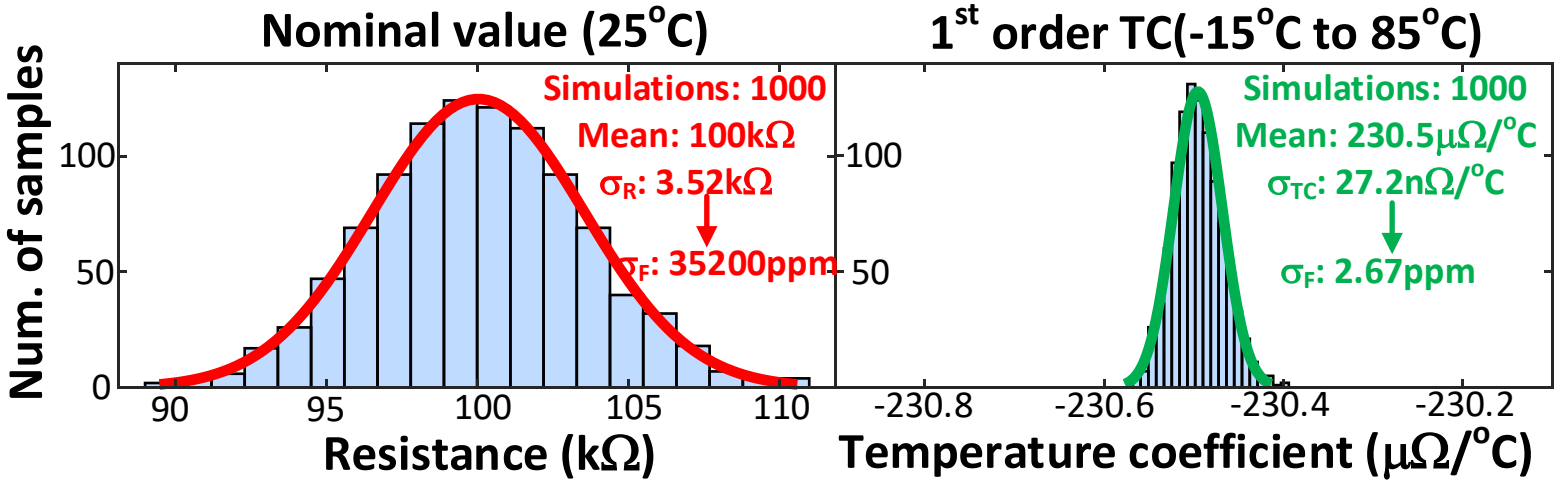


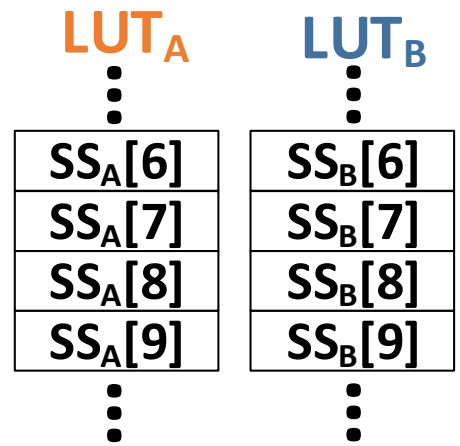


Non-linearity aware DLF

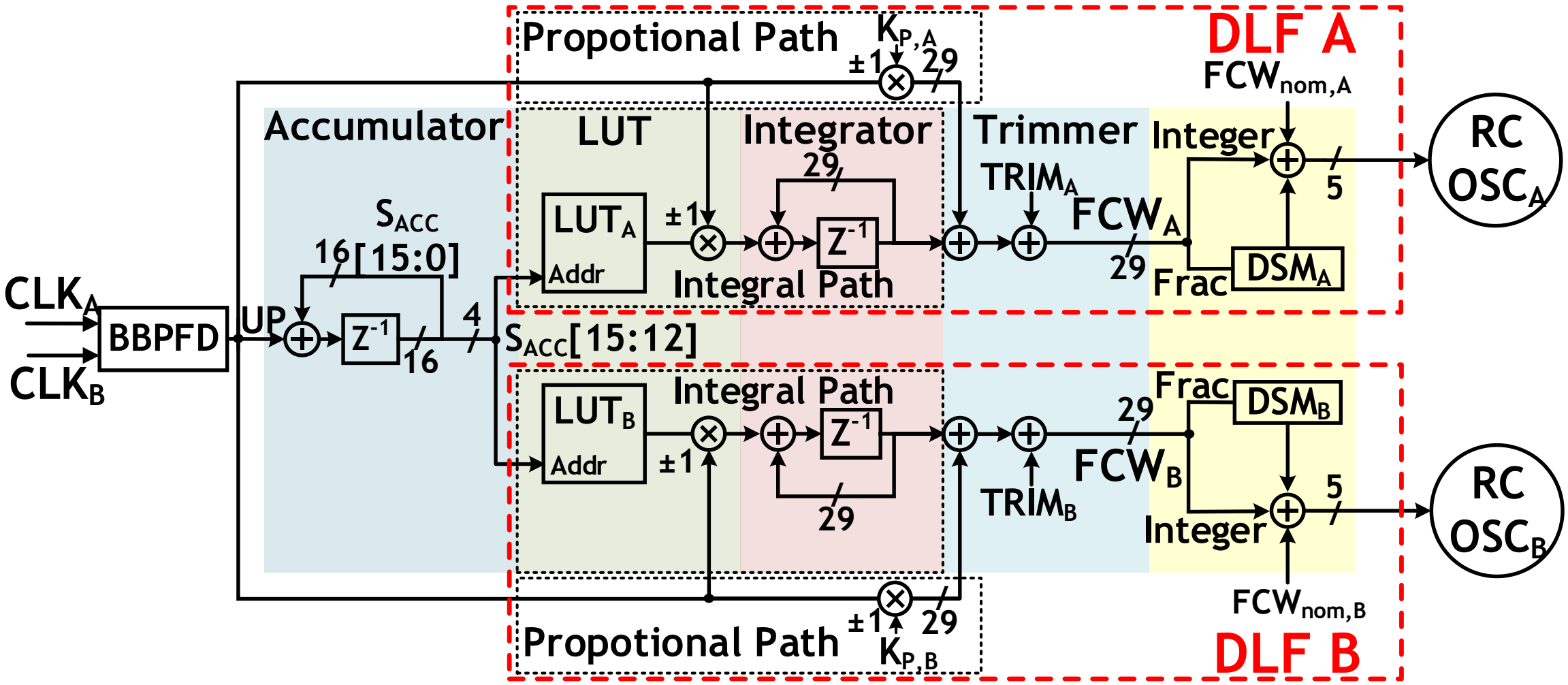
- Thanks to the very low variation of TC, the LUTs are valid for different chips coming from different batches, without the need of changing them
- This approach can also cancel out higher-order repeatable dependencies







Non-linearity aware DLF



Outline

1. Background and Motivation
2. Proposed Timer
    1. One point calibration with a nonlinearity-aware dual PLL structure
    2. DSM-Controlled FLL
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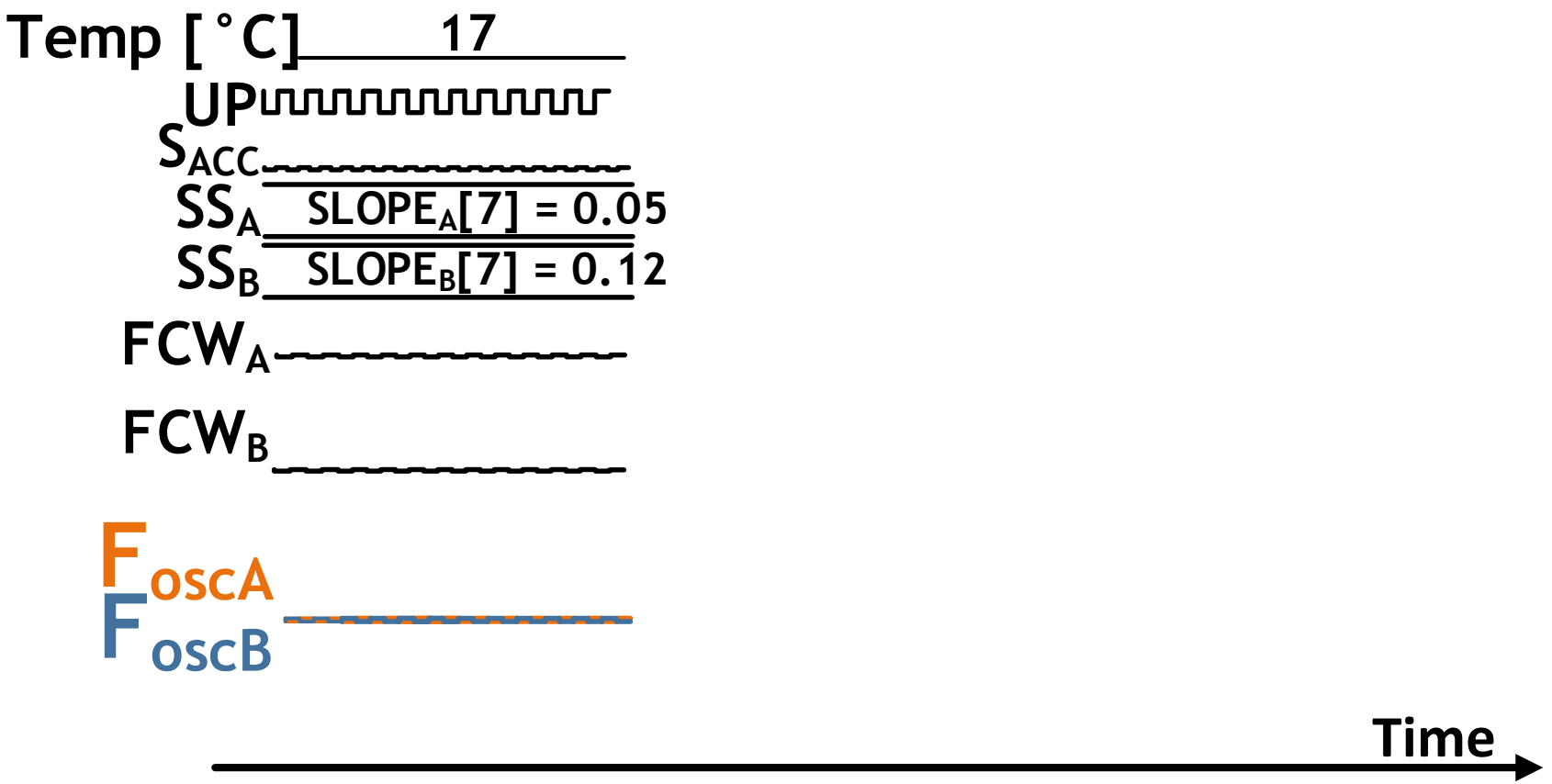
    4. Example of Operation
3. Measurement Results
4. Conclusions

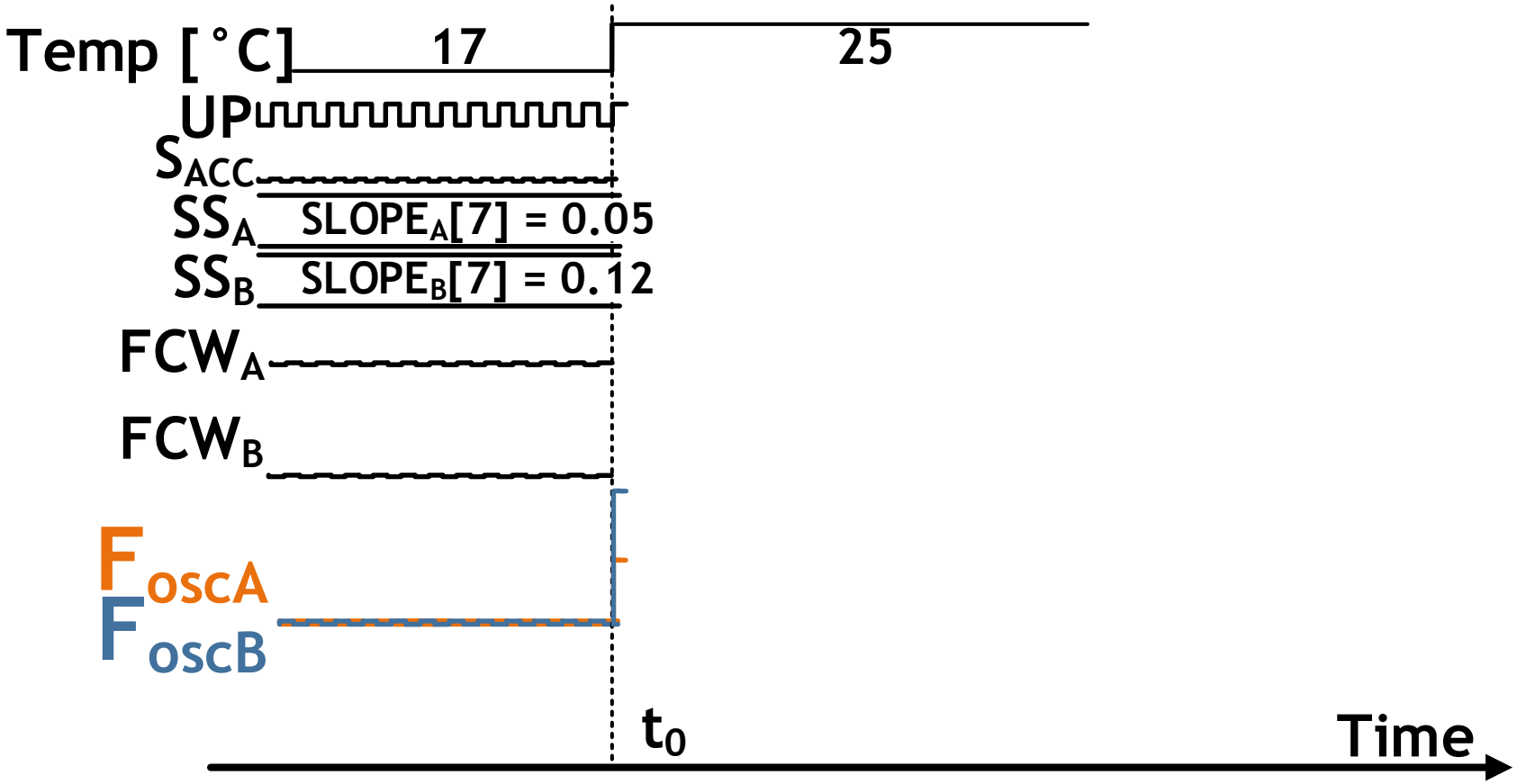
Example of Operation

- LUTs have been populated as previously described
- The circuit has been trimmed, and the PLLs are locked at 17°C



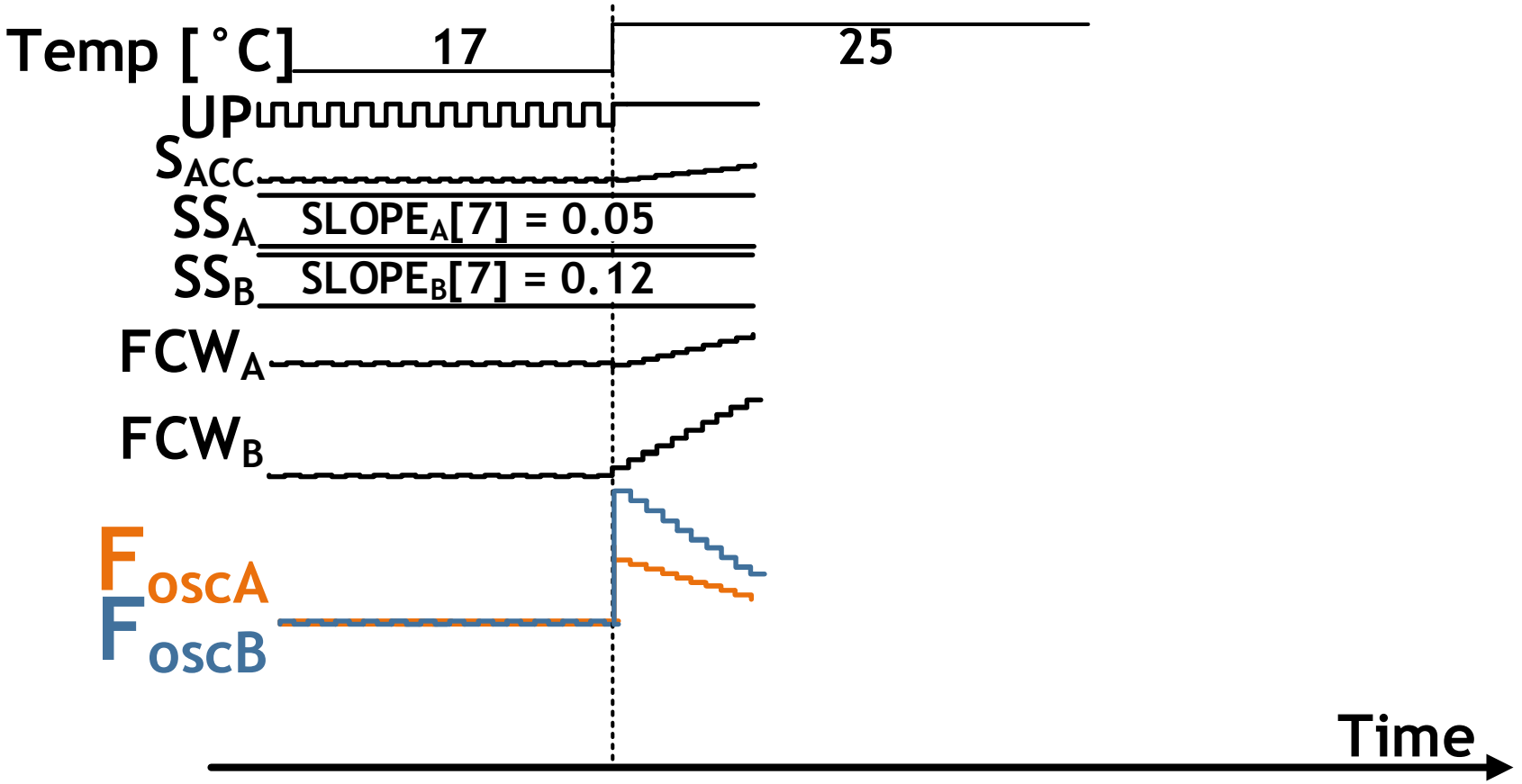
Example of Operation

- At time t_0 the temperature changes to 25°C
- Due to the temperature change, the FLL frequencies change, and $F_{oscB} > F_{oscA}$



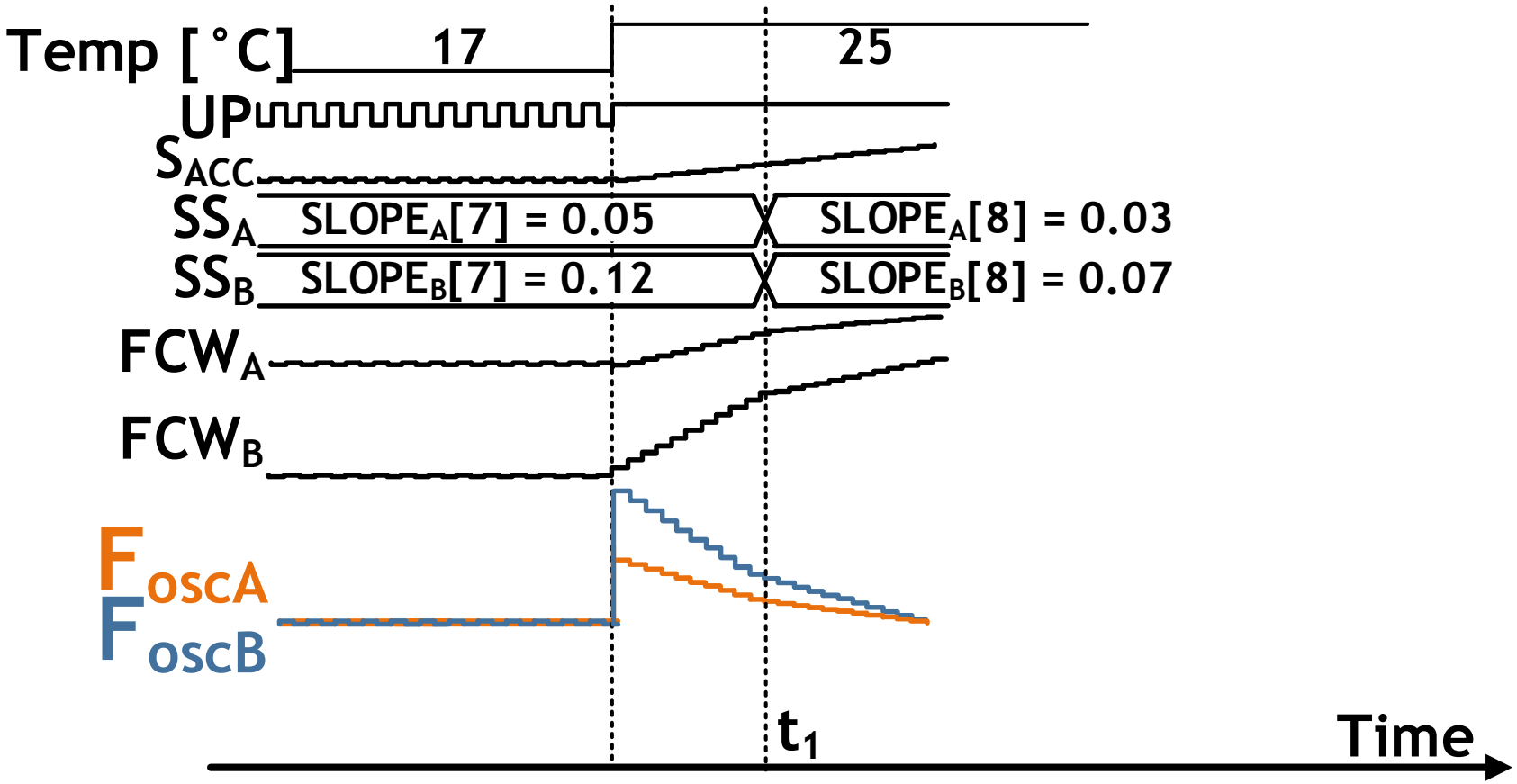
Example of Operation

- $F_{oscB}>F_{oscA}$, so UP=1 accumulates on S_{ACC}.
- The FCWs increase with the step defined by $SS_A[7]$ and $SS_B[7]$



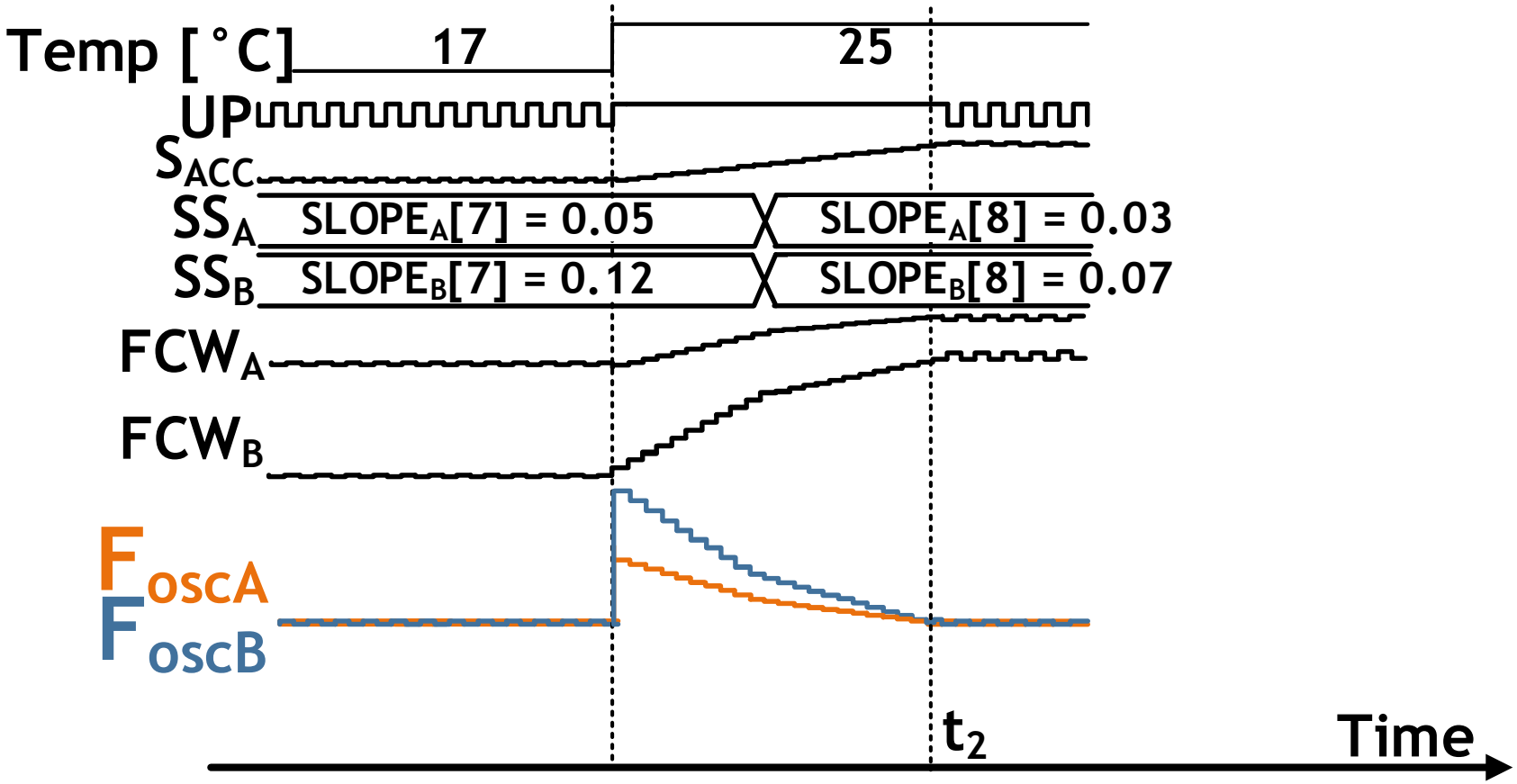
Example of Operation

- At time t_1 S_{ACC} updates the integral gain to the LUT [8] entry
- The FCWs keep changing, but with a different step size



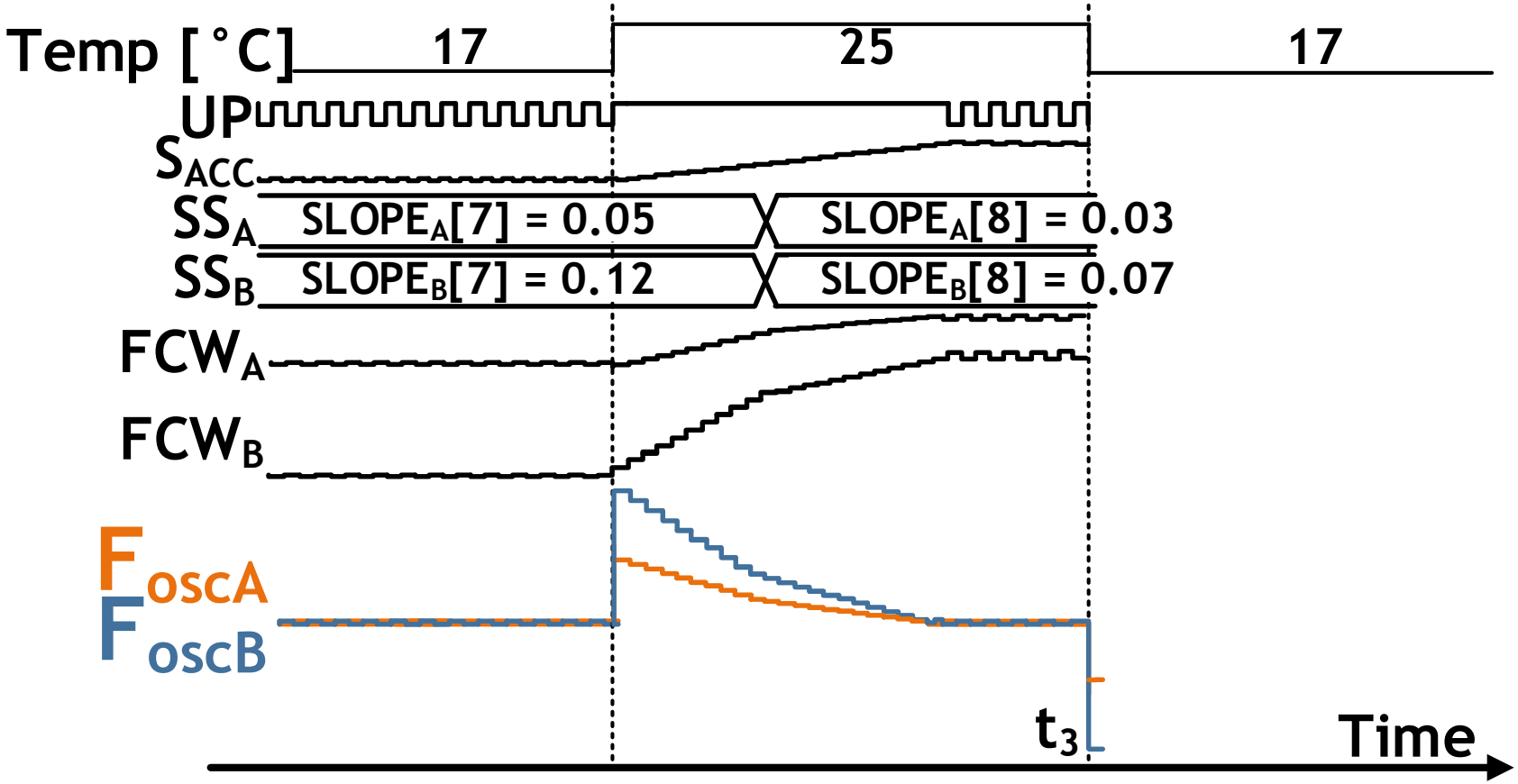
Example of Operation

- At time t_2 F_{oscA}=$F_{oscB.}$ UP oscillates, and S_{ACC} does not change. The circuit is locked
- The locked frequency is the same as the one at 17ºC thanks to the LUT entries



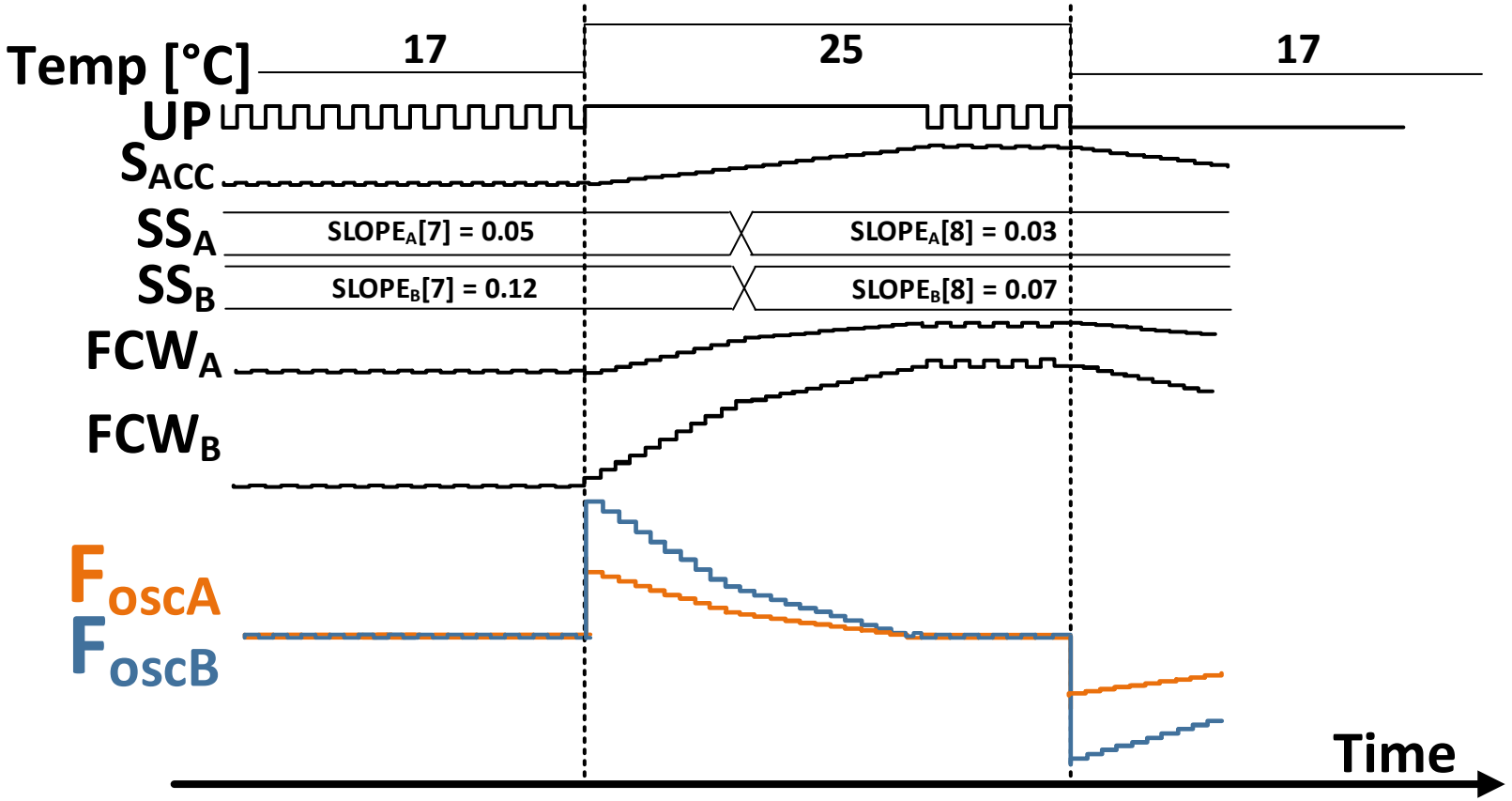
Example of Operation

- At time t_3 the temperature changes to 17°C
- Due to the temperature change, the FLL frequencies change, and $F_{oscA} > F_{oscB}$



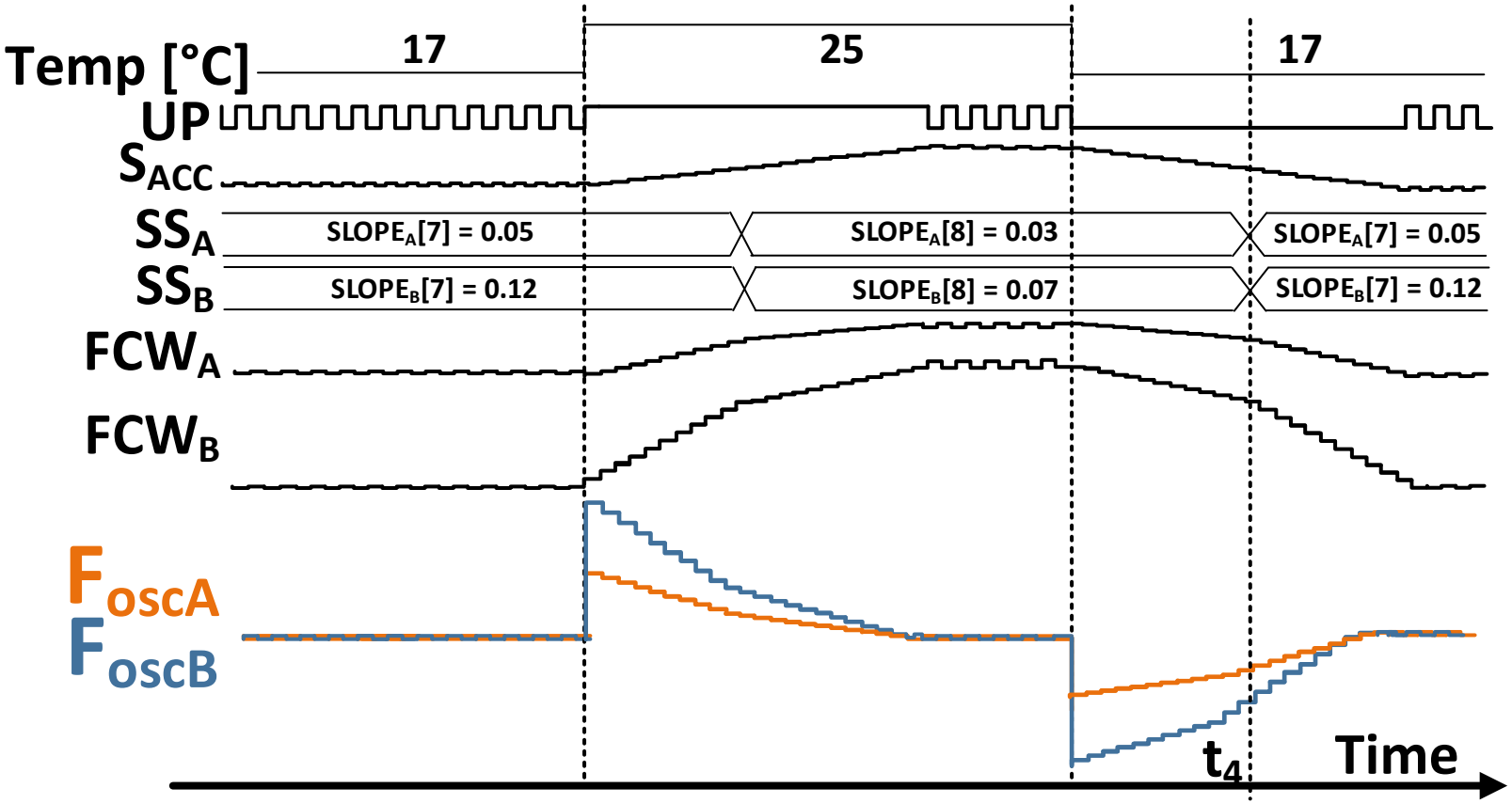
Example of Operation

- $F_{oscB}>F_{oscA}$, so UP=0 decreases S_{ACC}.
- The FCWs decrease with the step defined by the $SS_A[8]$ and $SS_B[8]$



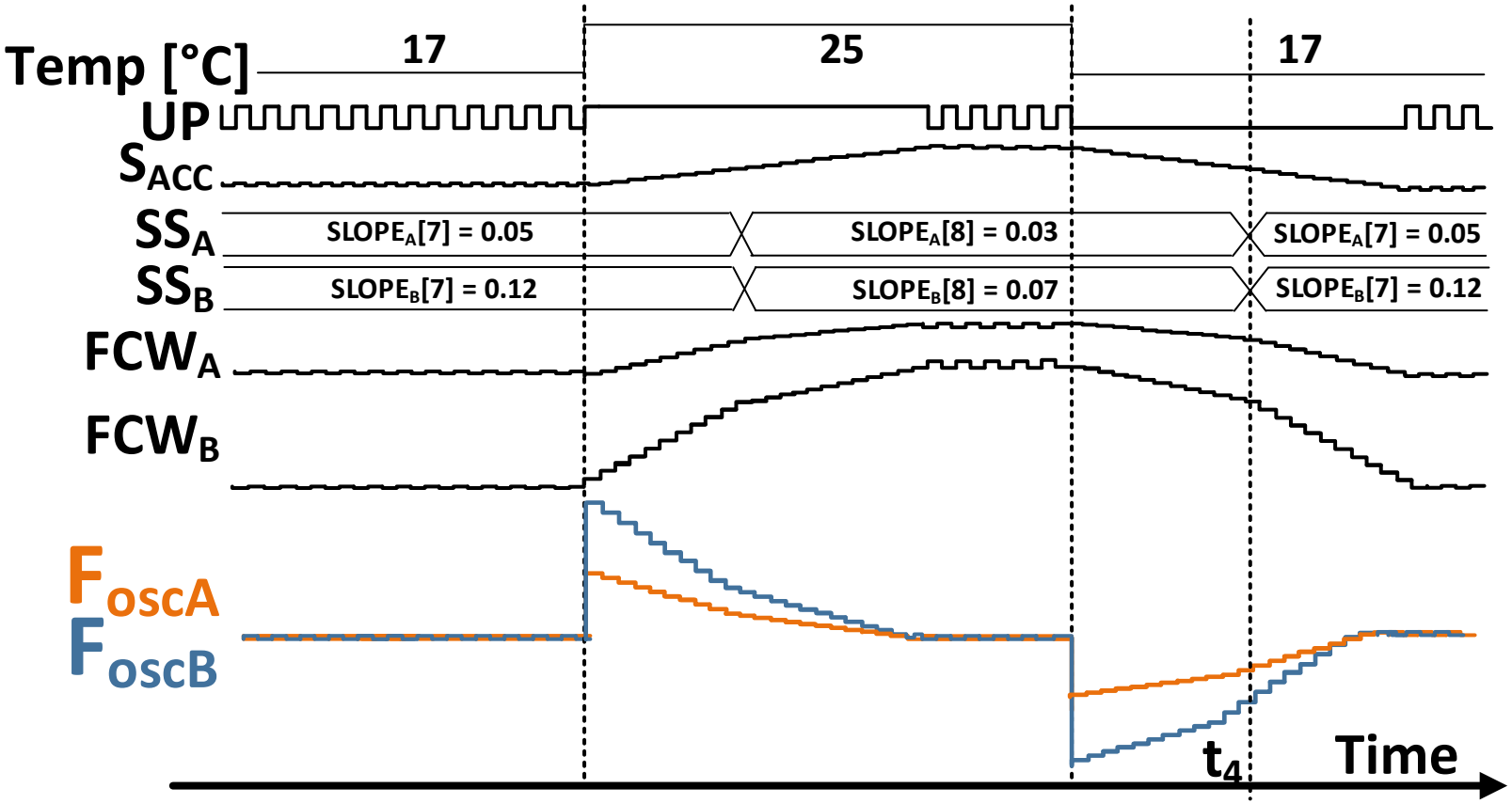
Example of Operation

- At time t_4 S_{ACC} decreases back in the interval [7]
- The two frequencies lock again at the same target frequencies



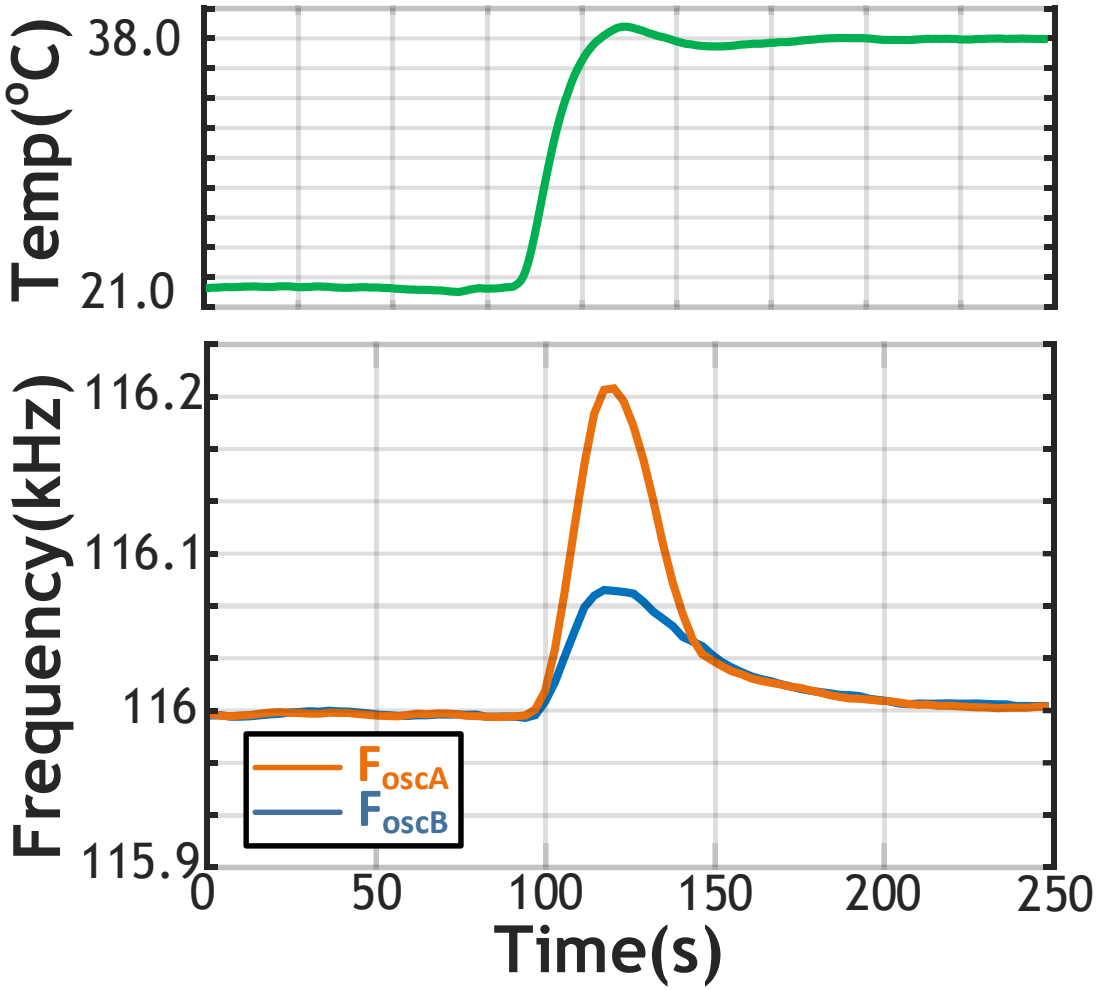
Example of Operation

- The timer requires two resistors with different TC but not necessarily one PTAT one CTAT
- In this example we use two different PTAT



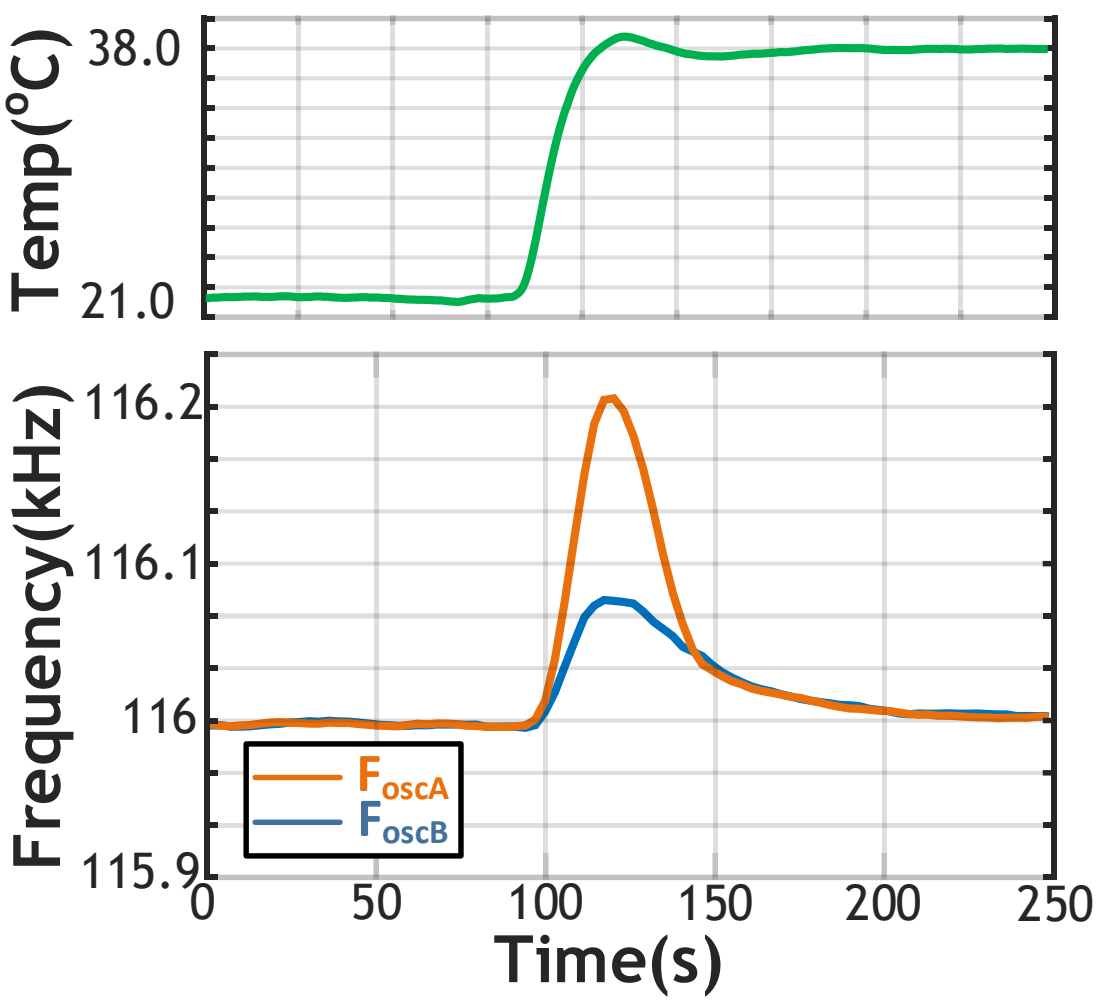
Measured Transient

- **Smaller integral gain**

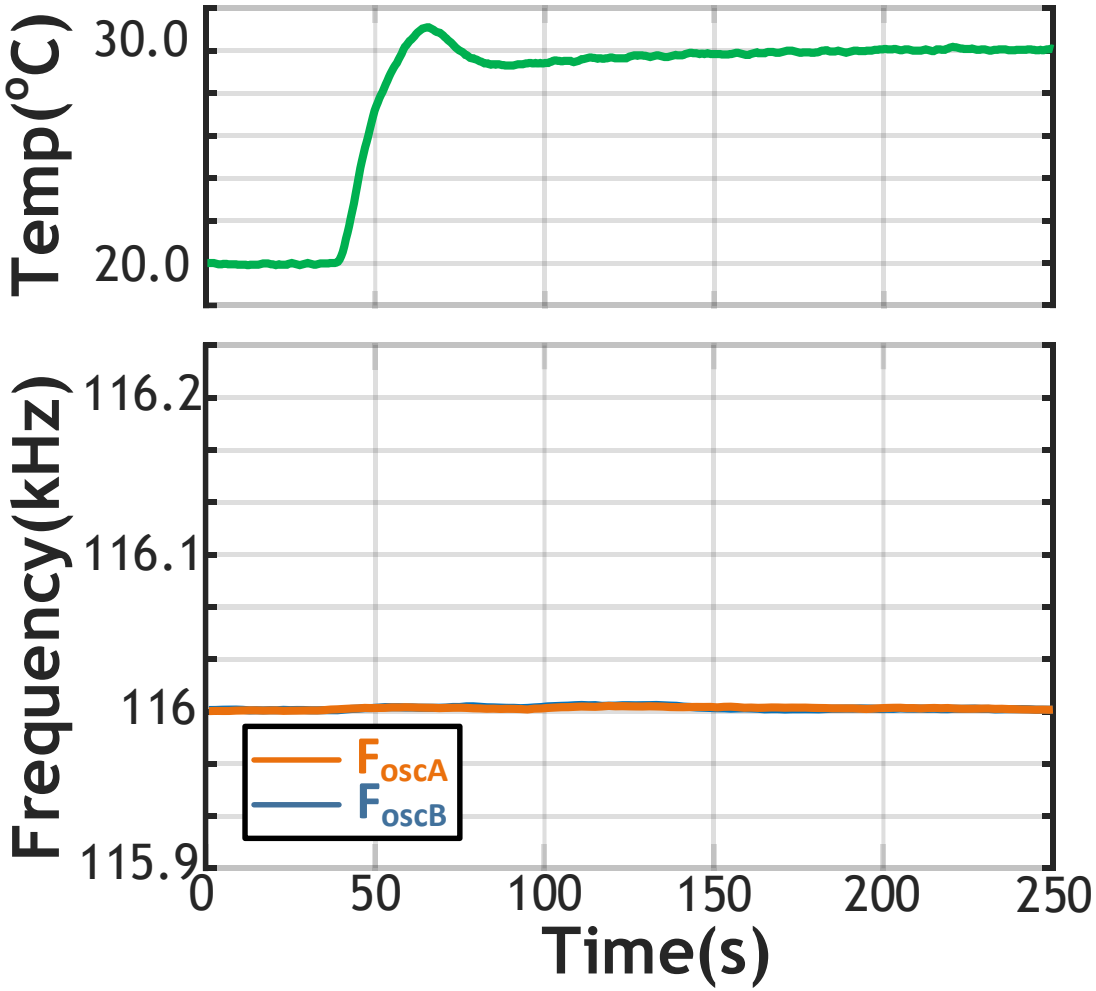


Measured Transient

- **Smaller integral gain**

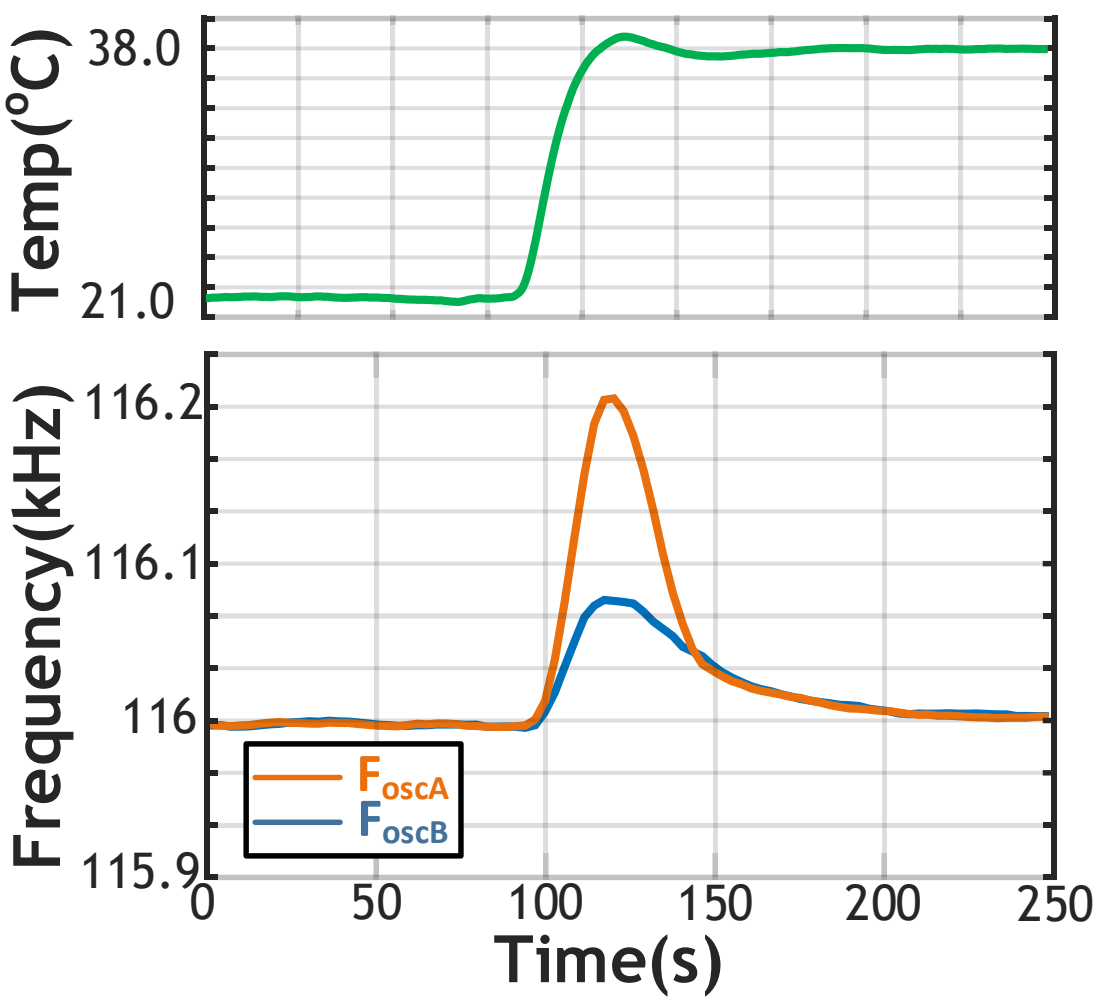


- **Larger integral gain**

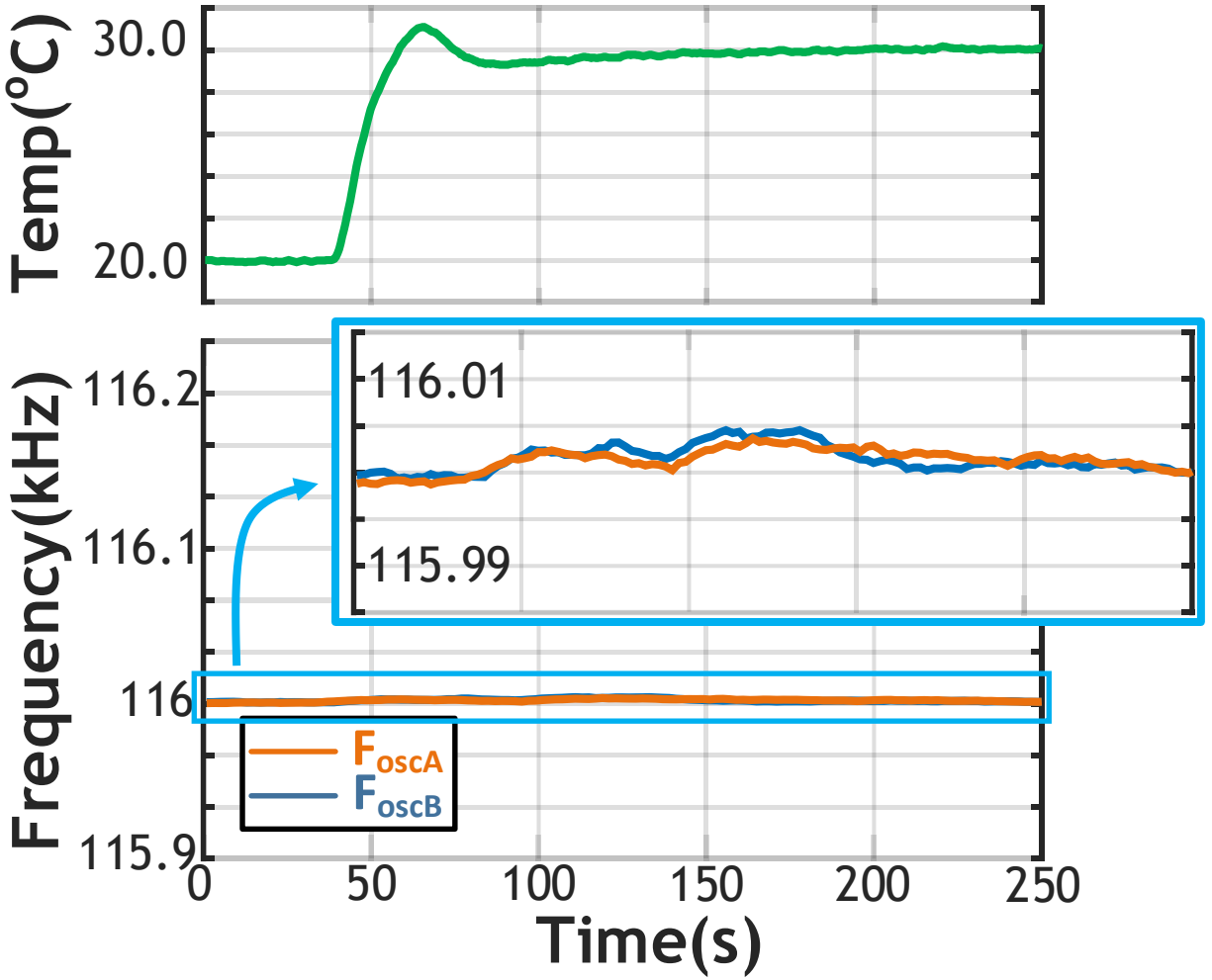


Measured Transient

- **Smaller integral gain**



- **Larger integral gain**



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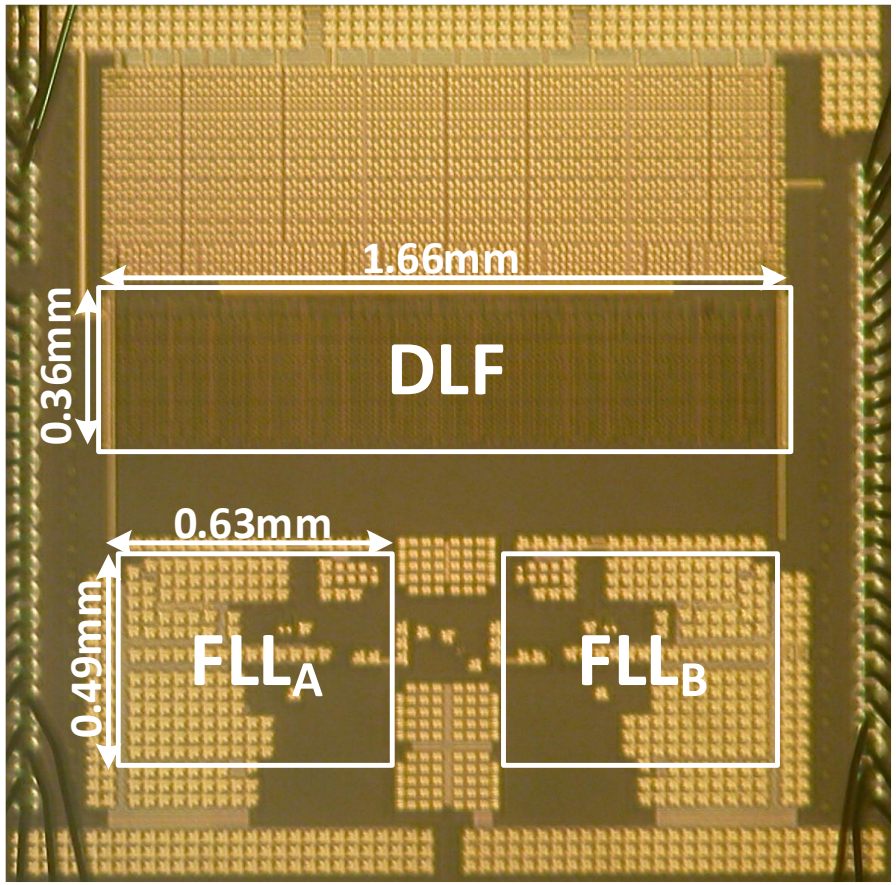
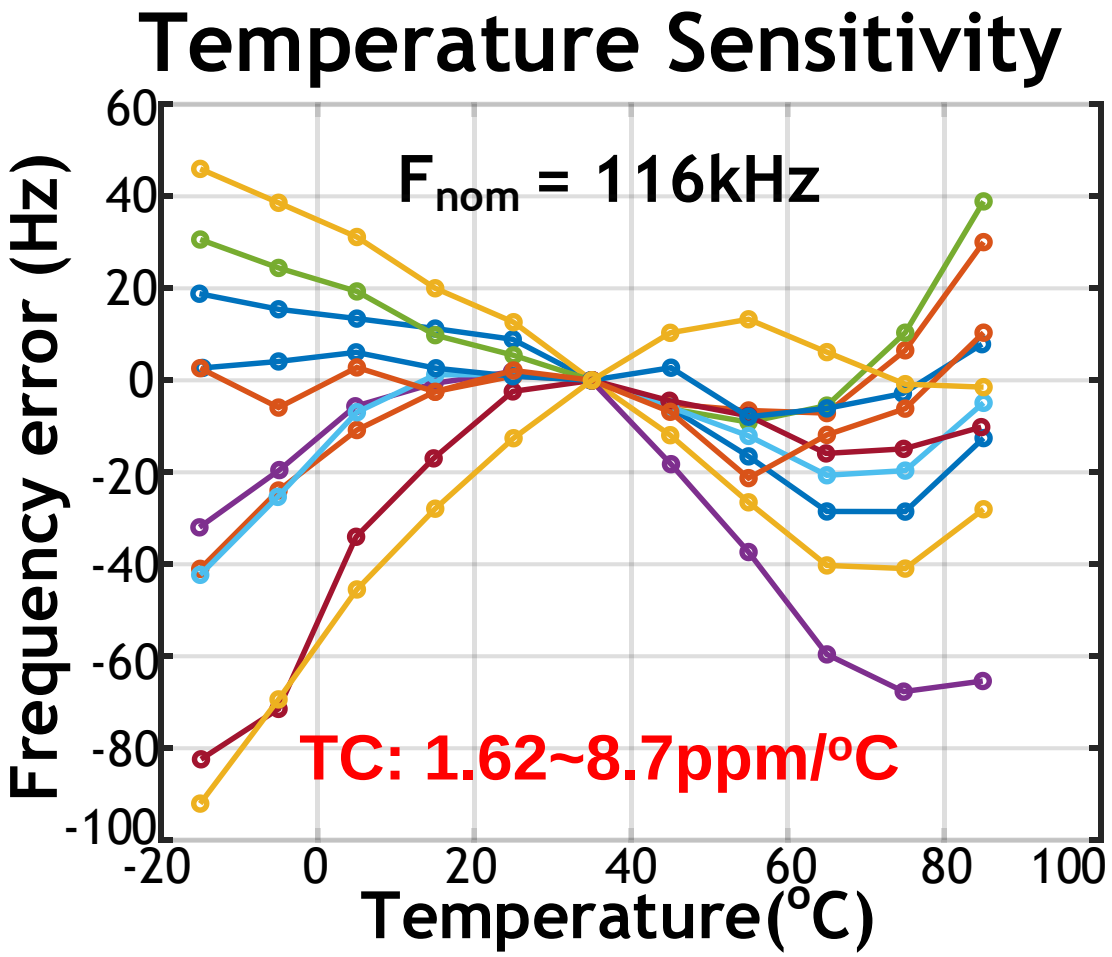
Die Photo

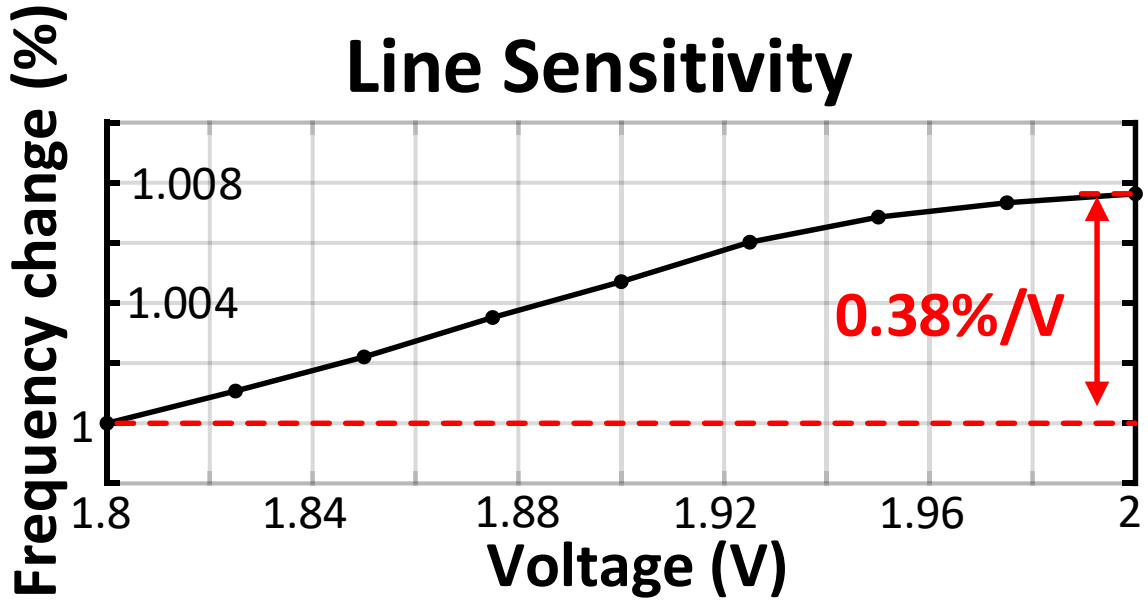


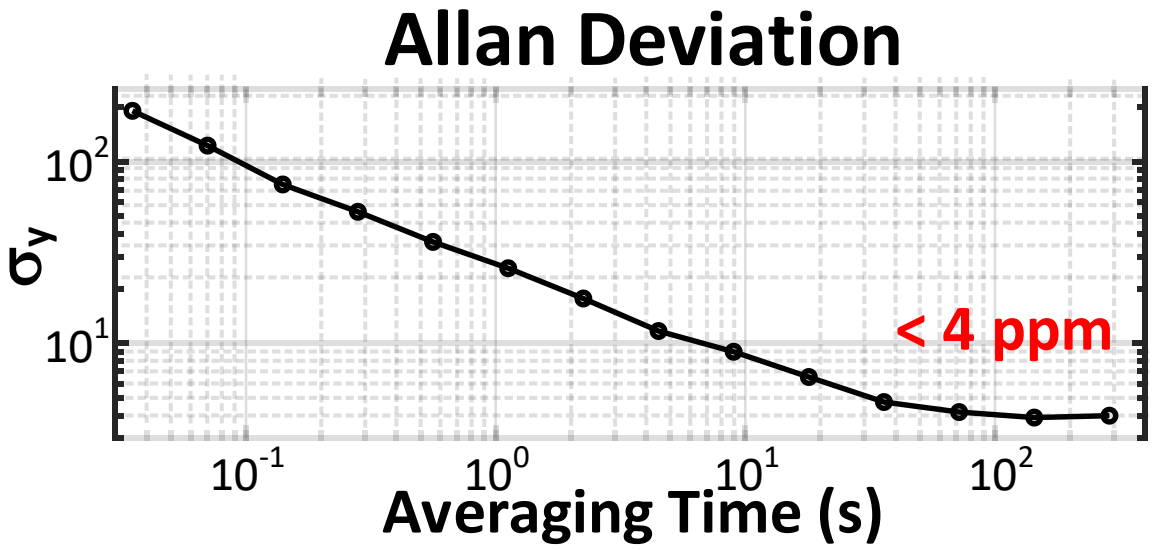
- We have measured 10 different chips coming from 2 different batches
- Each chip was calibrated at a single temperature, and we have used the same LUTs for all measurements
- Target frequency: 116kHz

1.215 mm² in 180nm CMOS Technology

Measurement Results







Performance Summary and Comparison

	This Work	Meng VLSI2019 [4]	Gürleyük ISSCC2018 [1]	Zhang VLSI2017 [5]	Savanth ISSCC2017 [6]	Jang ISSCC2016 [2]	Choi JSSC2016 [7]	Jeong JSSC2015 [3]
Process (nm)	**180**	180	180	180	65	180	180	180
Frequency (Hz)	**116k**	600k	8M	24M	1.35M	3k	70.4k	11
TC (ppm/°C)	**8.7**	48.69	3.85	3.2/14.2[1]	96	13.8	34.3	45
Temp. Range (°C)	**-15 to 85**	-45 to 125	-45 to 85	-40 to 150	0 to 150	-25 to 85	-40 to 80	-10 to 90
Line sensitivity (%/V)	**0.38**	0.046	0.18	0.03	0.49	0.48	0.75	1
Power (nW)	**694**	2200	750000	200000	920	4.7	110	5.8
Allan deviation(ppm)	**4**	-[2]	0.25	-[2]	-[2]	32	7	50
Energy/cycle (pJ)	**5.98**	3.67	93.75	8.33	0.68	1.57	1.56	527.3
Area (mm^2)	**1.2**	0.049	1.59	0.17	0.005	0.5	0.26	0.24
Calibration points	**1**	-[2]	2	3	-[2]	2	2	-[2]
Number of samples	**10**	3	12	200/12[1]	2	1	5	5

[1]tested at wafer level / including package stress
[2]not reported

Performance Summary and Comparison

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Conclusions

1. A low-power on-chip timer, with single point calibration is implemented in 180nm CMOS

2. A Dual-PLL structure, with a non-linearity aware DLF, that controls two chopped FLLs, leads to a very low temperature sensitivity, and Allan deviation floor

3. The measured temperature coefficients of the 10 chips is 1.62~8.7ppm/^{o}C, while consuming 694nW at 116kHz

Thanks for your attention

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