EVENT REPORT

IEEE ELECTRONICS PACKAGING SOCIETY (EPS) SBC INAUGURATION & LOGO LAUNCH

Date : 09 July 2026
Time : 10:30 AM – 1:00 PM
Venue : B V Raju Institute of Technology (BVRIT), Narsapur

Organized by: IEEE Electronics Packaging Society Student Branch Chapter, BVRIT in association with the IEEE BVRIT Student Branch.

Inaugural Session

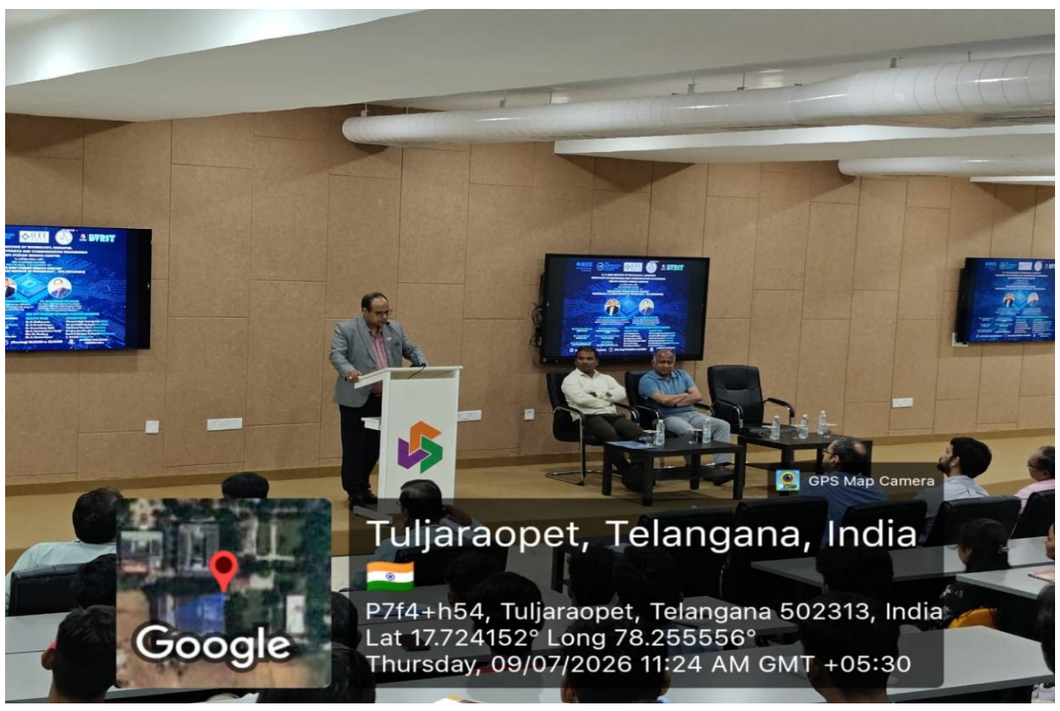
The event commenced with a warm welcome to the distinguished guests, faculty members, IEEE volunteers, students, and participants. The inaugural session marked the official launch of the IEEE Electronics Packaging Society (EPS) Student Branch Chapter at BVRIT, along with the unveiling of its official logo. During the session, the significance of the IEEE Electronics Packaging Society and its role in promoting innovation, research, and technological advancements in electronics packaging were highlighted.

The inauguration was graced by internationally renowned IEEE EPS leaders including:

- Dr. Madhavan Swaminathan, IEEE Fellow
- Dr. Bala Prasad Peddigari, IEEE Vice Chair
- Sri K.Aditya Vissam, Secretary, SVES
- Dr. K Lakshmi Prasad, Director, BVRIT
- Dr. Sanjay Dubey, Principal, BVRIT
- Dr. Sanjeeva Reddy B R, Head of department, BVRIT
- Dr. Avinash Yadlapati, Manager Altera , Malaysia
- Dr. Gnaneshwara chary, EPS Faculty Advisor, BVRIT

Technical Sessions

Prof. Bala Prasad Peddigari delivered an introductory session on the IEEE Electronics Packaging Society (EPS), highlighting its vision, objectives, and the importance of electronic packaging in modern semiconductor technology. He discussed opportunities for students, including research, technical publications, innovation, patents, and industry collaboration. He also introduced emerging areas such as chiplet integration, heterogeneous integration, and advanced packaging, motivating participants to actively engage in IEEE EPS activities and pursue careers in electronic packaging and microelectronics.



Prof. Madhavan Swaminathan delivered a technical talk on "Fundamentals of Device and Systems Packaging", covering modern semiconductor packaging technologies and their role in high-speed electronic systems. He explained signal integrity, IC-to-IC communication, transmission lines, and challenges such as crosstalk, reflection, attenuation, and power noise. The session also highlighted the evolution of semiconductor packaging toward heterogeneous integration and System-in-Package (SiP) technologies.

The technical session focused on the Fundamentals of Device and Systems Packaging with an emphasis on signal integrity in high-speed electronic systems. The speaker explained how electrical signals are transmitted between integrated circuits (ICs) through package interconnections and discussed the impact of parasitic resistance, capacitance, and inductance on signal propagation. Important concepts such as capacitive delay, RC time constants, transmission lines, and IC-to-IC communication were presented to illustrate how interconnects influence circuit performance.

The session also covered key challenges in high-speed signaling, including reflection, crosstalk, attenuation, electromagnetic interference (EMI), thermal noise, radiation, and power supply noise, highlighting their effects on system reliability and data integrity. Additionally, the evolution of semiconductor packaging technologies—from traditional multi-chip modules to modern heterogeneous integration and System-in-Package (SiP) architectures—was discussed.

Organizing Committee

Department IEEE Coordinators

Dr. B. Naresh Kumar

Mrs. M. Anusha

Mr. TPK Nandan

Faculty Coordinators

Mr. C. Ramesh Kumar Reddy

Mrs. Ch. Vandana

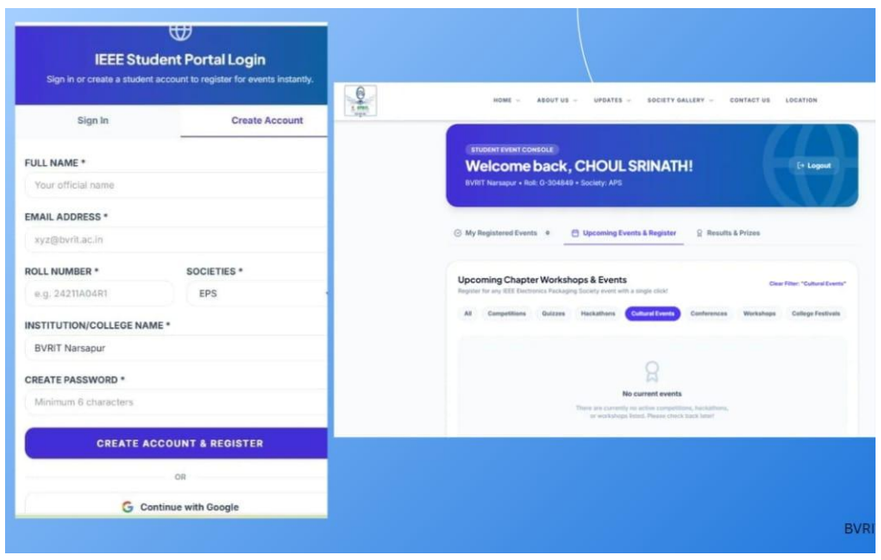
Mr. K. Charan Kumar

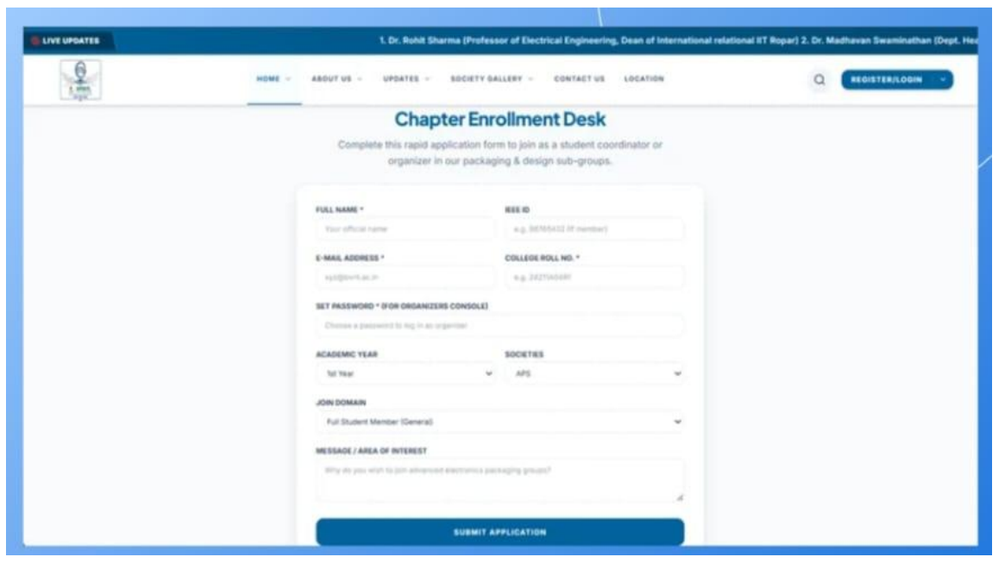
IEEE EPS Team

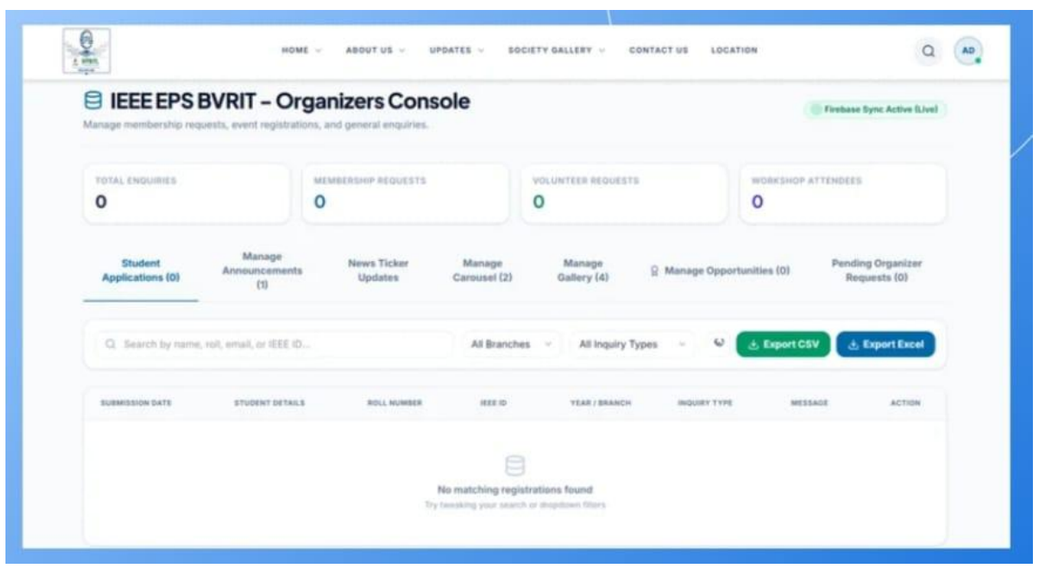
- Charansaiteja Voorugunda - Chair
- Sai Aashritha Vasagiri - Vice Chair
- Vaishnavi Cherukuri - Secretary
- Sreejan goud Routhu – Treasurer
- P V Lalithsurya – Technical Lead
- Bandi Reddappa Venkatesh – Webmaster & Tech Admin
- Avula Hasinipriya – Event Coordinator
- P.Rushitha – Logostics Lead
- Aishwarya Batini – Public and Industry Relation lead
- Bhaskar Akshaya – Design Lead
- B.Yogesh – Social Media Lead
- Niharika Rathod – Membership Development & Outreach Lead
- C.Srinath – Web Master & Tech Admin

The successful execution of the IEEE Electronics Packaging Society (EPS) technical session was made possible through the dedicated efforts of the faculty coordinators, IEEE EPS Student Branch Chapter Team Members, and organizing committee. Their commitment to planning, coordination, participant management, and technical support ensured the smooth conduct of the session and contributed significantly to its overall success.

To further strengthen student engagement and streamline chapter activities, the IEEE EPS Student Branch Chapter, BVRIT, has developed a dedicated web platform for membership management, event registration, and communication. The platform includes a student portal, organizer dashboard, event updates, and membership management, ensuring efficient coordination and improved student engagement.







Outcomes

The IEEE EPS technical sessions enhanced participants' understanding of advanced electronic packaging, chiplet integration, and high-speed system design. The talks encouraged students to undertake research, publish papers, develop innovative projects and prototypes, pursue patents, collaborate globally, and address real-world industrial challenges through advanced packaging technologies.

Conclusion

The IEEE Electronics Packaging Society (EPS) technical sessions were successfully conducted with active participation from students, faculty members, researchers, and IEEE members. The event significantly contributed to enhancing participants' knowledge of advanced electronic packaging, semiconductor technologies, and high-speed system design. The expert talks inspired students to pursue research, innovation, publications, and industry-oriented projects while fostering greater interest in emerging areas such as chiplet integration, heterogeneous packaging, and system-in-package technologies. Overall, the sessions served as an excellent platform for learning, networking, and promoting research in the field of electronic packaging and microelectronics. Building on the success of this event, the IEEE EPS Student Branch Chapter, BVRIT, will be organizing a two-day workshop on Electronics Packaging using Ansys HFSS in August to provide participants with practical, hands-on experience in electronic packaging and simulation.