



CONSOLIDATED REPORT

Event Title: International Workshop on AI Driven Semiconductor and Energy Efficient Hardware

Venue: The Marvel, T-Hub

Dates: July 7 – 8, 2026

Organizing Institutions: Sri Vishnu Educational Society (BVRIT, SVECW, VIT, BVRITH) in association with IEEE Circuits and Systems (CAS) Society Hyderabad Section and Anusandhan National Research Foundation (ANRF)

Executive Summary:

The International Workshop on AI Driven Semiconductor and Energy Efficient Hardware successfully convened a premier global assembly of academic pioneers, industrial executives, and research scholars to deliberate on the critical convergence of Artificial Intelligence (AI) and semiconductor technology. The event served as a high-level forum for exploring how advanced computing demands are reshaping hardware architectures, material science, and manufacturing paradigms.

Participant Demographics and Engagement:

The workshop witnessed an exceptional turnout, drawing a massive and highly engaged audience of over 300 participants. This diverse delegation included prominent faculty members, senior research fellows, and enthusiastic engineering students representing various private engineering colleges across Hyderabad. The active participation of these institutions facilitated a vibrant exchange of ideas, bridging the gap between theoretical academic frameworks and contemporary industrial application requirements.

Day 1: July 7, 2026

The international workshop commenced with a formal and auspicious inaugural ceremony. The session began with the invitation of the esteemed chief dignitaries onto the dias:

Shri Aditya Vissam, Secretary, Sri Vishnu Educational Society

Sri. Ravichandran Rajagopal, Vice Chairman, Sri Vishnu Educational Society

Prof. Madhavan Swaminathan, Department Head of Electrical Engineering, Penn State University, USA

Mr. Navin Bishnoi, VP and India Country Manager, Marvell Technology

Following the presentation of floral welcomes to the dignitaries, the formal proceedings were initiated with the traditional Lighting of the Lamp by the dignitaries on stage.



Dignitaries on stage revealing the official workshop brochure during the inaugural session

Session 1: Keynote Address – The Future of 3D Heterogeneous Integration (3DHI)

- **Speaker:** Prof. Madhavan Swaminathan, Department Head of Electrical Engineering, Penn State University, USA
- **Abstract:** This keynote highlighted technical challenges in thermal dissipation, high-bandwidth interconnects, and signal integrity necessary to sustain power-efficient AI computing infrastructure. There are two challenges emerging, namely, 1) Energy crises with the introduction of AI datacenters and 2) Moore's law reaching a bottleneck limited by the cost of scaling and other performance related issues. Can advanced packaging aka 3D Heterogeneous Integration (3DHI) help to address these challenges? This talk will highlight the problems and potential solutions, including some research highlights, and the importance of ISM investments in this area.



Keynote session by Prof. Madhavan Swaminathan and the felicitation of the Prof. by Principal BVRIT Narsapur

Session 2: FPGA Based Acceleration Enabling AI Driven Network Transformation

- **Speaker: Ms. Nupur Shah, Expert IP Systems and Solutions, USA**
- **Abstract: Highlighting the flexible nature of Field Programmable Gate Arrays (FPGAs), this session detailed how hardware acceleration redefines modern network backbones. Driven by AI processing requirements at the network edge, the speaker demonstrated specialized IP cores designed for low-latency data filtering, dynamic routing, and adaptive workload balancing, maximizing throughput while minimizing power consumption.**



Invited Talk by Ms. Nupur Shah and the felicitation by Director BVRIT Narsapur

Session 3: AI Driven Semiconductor Innovation

- **Speaker: Mr. Navin Bishnoi, VP and India Country Manager, Marvell Technology**
- **Abstract: Mr. Bishnoi explored how semiconductor design methodologies are integrating machine learning algorithms internally. From automated place-and-route optimization to predictive yield analysis during wafer fabrication, AI-driven electronic design automation (EDA) tools drastically compress time-to-market and optimize the Power, Performance, and Area (PPA) metrics of next-generation silicon.**



Invited Talk by Mr. Navin Bishnoi and the felicitation by Principal BVRIT Hyderabad

Session 4: Semiconducting Materials for Precise Biosensing

- **Speaker: Prof. Sharath Sriram, Professor, School of Engineering, RMIT University, Australia**
- **Abstract: Semiconducting substrates particularly silicon offers exceptional chemical and environmental stability. In this work, high-resistivity float-zone silicon is used as the foundation for a new class of biosensors. By integrating micro-scale electrode pairs, surface salinisation to create reactive binding sites, and target-specific functionalisation, we demonstrate a novel category of highly precise conductometric biosensors. These sensors achieve picomolar-level sensitivity and strong specificity even within complex biological mixtures. Their performance is validated across a broad range of targets, including protein biomarkers (inflammatory, cardiac, fertility, and neurological), viral analytes (SARS-CoV-2), and short DNA fragments associated with cancer-related gene sequences (melanoma, liver, stomach, and oral cancers).**



Invited Talk by Prof. Sharath Sriram

Panel Discussion I: Education, Research, and Innovation Ecosystem for VLSI & Semiconductors

- **Moderator:** Dr. Rohit Sharma, Professor & Dean of International Relations, IIT Ropar
- **Panelists:** Prof. Madhavan Swaminathan (Penn State University), Mr. Navin Bishnoi (Marvell Technology), Sri. Ravichandran Rajagopal (Vice Chairman of Sri Vishnu Educational Society,), Dr. Rohin Y. (Founder & CEO, LightSpeed Photonics).
- **Key Takeaways of the Panel discussions:**

Establishment of a collaboration: The panel emphasized the critical necessity of building a collaborative alliance between academia, industry partners, and government funding bodies, specifically highlighting institutions like the Anusandhan National Research Foundation. Curriculum

Preparing Students to face the industry: Cultivating industry-ready VLSI talent requires significant academic curriculum revisions that transition student focus toward practical chip tape-outs.

Hands-on Cleanroom Infrastructure: Educational programs must prioritize providing students with experiential, hands-on cleanroom access to bridge the gap between theoretical knowledge and device fabrication.

Deep Institutional collaboration: Engineering institutions must establish deeper integration paths with technology startups to immerse students directly within contemporary industrial research and engineering environments



A glimpse of the panel discussion I

Session 5: Edge Computing and AI-Integrated Silicon

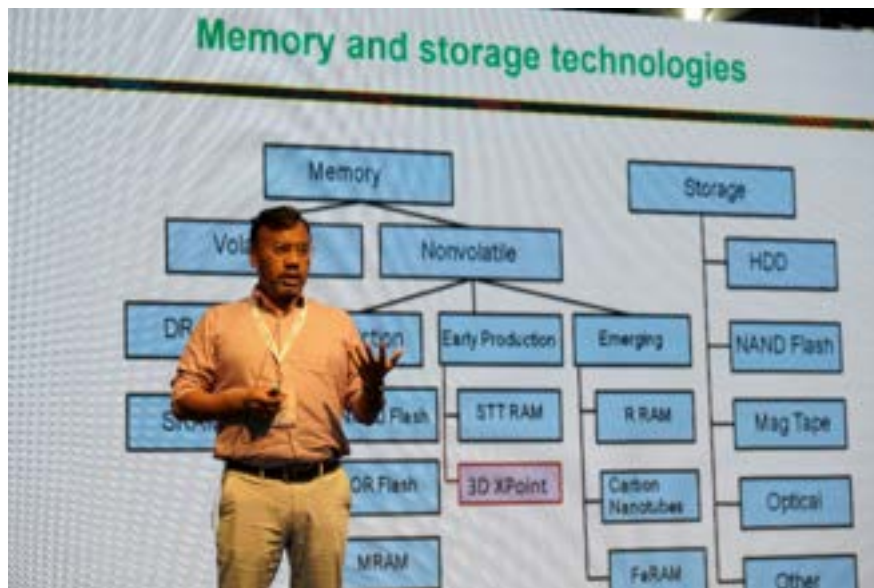
- **Speaker: Mr. P. Ravikanth Reddy, Director & Site Head NXP Hyderabad, 5G & Networking Solutions**
- **Abstract: Focusing on decentralized processing, the speaker presented NXP's latest frameworks for embedding machine learning model inference directly onto microcontrollers and application processors. The session examined hardware-level quantization, pruning techniques, and specialized neural processing units (NPUs) that run autonomous edge applications within strict milliwatt power budgets.**



Invited Talk by Mr. P. Ravikanth Reddy and the felicitation by Prof. M.C. Chinnaiiah

Session 6: Emerging Memory Technologies for AI and IoT

- **Speaker: Dr. Bhagwati Prasad, DEMAND Lab, IISc Bangalore**
- **Abstract: Addressing the classic von Neumann memory bottleneck, this session introduced non-volatile emerging memories such as Ferroelectric RAM (FeRAM) and Resistive RAM (ReRAM). These architectures enable neuromorphic processing-in-memory (PIM), where data storage and computational logic occur within the same physical array, decreasing energy consumption during deep neural network execution**



Invited Talk by Dr. Bhagwati Prasad the felicitation by Prof. Sivakumar Krishnan

Session 7: AI Integration in Advanced Semiconductor Packaging, Test and Assembly Operations

- **Speaker: Dr. Charan Gurumurthy, Senior VP, TATA Electronics Private Limited (TEPL) & Business Head, TATA Semiconductor Assembly & Test (TSAT)**
- **Abstract: Dr. Gurumurthy provided an operational view into domestic semiconductor manufacturing. Beyond the advanced technicalities, his thoughts on leadership, the fundamental importance of basics, and his personal journey of transitioning from a background in mechanical engineering into semiconductors provided an unforgettable lesson for our students and faculty alike.**



Invited Talk by Dr. Charan Gurumurthy

Session 8: Future of Semiconductor with AI and Materials

- **Speaker: Dr. Suraj Rengarajan, Principal Technologist, Applied Materials India**
- **Abstract: The session emphasized material-level innovations underpinning modern fabrication nodes by deploying atomic layer deposition (ALD) and plasma etching enhanced by AI-driven process modeling, researchers can discover and scale novel 2D materials, high-k dielectrics, and sub-nanometer thin films predictably.**



Invited Talk by Dr. Suraj Rengarajan

Panel Discussion II: Edge AI in Semiconductors: Rethinking FPGA Acceleration, Chip Validation, and Processor Architectures

- **Moderator:** Dr. Nikita Ambasana, Customer Success Manager, SimYog Technology, Bangalore.
- **Panelists:** Mrs. Nupur Shah (Expert IP Systems, USA), Mr. Vijay Bolloju (Director of R&D, iVP Semiconductor), Dr. Charan Gurumurthy (TATA Electronics), Mr. P. Venkatesh Kumar (General Manager, PTW Semiconductors), Mr. Varma S Konala (ASIP Technologies Advisor, Pradhi Semiconductors)
- **Key Takeaways:** The experts debated the tradeoffs between flexible FPGAs and dedicated ASICs for edge deployment. Key conclusions highlighted that pre-silicon electromagnetic interference (EMI) simulation and automated verification suites are essential to minimize expensive physical fabrication spins.



A glimpse of the Panel Discussion II

Session 9: Semiconductor Packaging and EDA Industry Perspectives, Emerging Trends, and Thoughts for Students

- **Speaker: Dr. Nikita Ambasana, Customer Success Manager, SimYog Technology, Bangalore**
- **Abstract: Dr. Ambasana detailed the changing landscape of electronic design automation (EDA). The talk provided a clear roadmap for engineering students, mapping technical competencies in signal integrity, thermal simulation, and scripting to career paths in global chip design houses.**



Invited Talk by Dr. Nikita Ambasana the felicitation by Dr. B.R. Sanjeev Reddy

Session 10: Physical AI: Real-World Intelligence

- **Speaker: Mr. Sharat Babu Kotamraju, Sr. Director of Engineering, AMD**
- **Abstract: Closing Day 1, the presentation explored 'Physical AI'—the intersection where digital neural processing interacts directly with structural physical systems. The speaker elaborated on AMD's architectural frameworks combining adaptive compute engines with low-latency sensory interfaces to power robotics, autonomous vehicles, and real-time physical simulation.**



Invited Talk by Mr. Sharat Babu Kotamraju

Day 2: July 8, 2026

Session 11: IEEE Electronics Packaging Society (EPS)

- **Speaker: Prof. Rohit Sharma, Professor of Electrical Engineering & Dean of International Relations, IIT Ropar**
- **Abstract: Day 2 opened with a comprehensive overview of the IEEE Electronics Packaging Society (EPS) and its foundational role in driving the global microelectronics and advanced packaging landscape. The presentation highlighted the society's extensive organizational framework, which encompasses over 6,000 global members, 86 dedicated chapters, and specialized technical committees covering critical fields such as high-density substrates, thermal-mechanical co-design, 3D/TSV integration, and nanophononics. Special emphasis was directed toward the EPS Education Programs, detailing structured professional developmental tracks including the EPS Certificate Program for technical leadership and the EPS Distinguished Lecturer (DL) initiatives.**



Invited Talk by Prof. Rohit Sharma the felicitation by Shri Aditya Vissam

Session 12: Challenges in Startup Management and IP Generation of Semiconductor Research

Speaker: Dr. Manish Kumar Hooda, Director (Technology), India Semiconductor Mission (ISM)

Abstract: Dr. Hooda addressed the strategic and commercial dimensions of the semiconductor domain. The session outlined the financial landscapes, regulatory frameworks, and intellectual property (IP) protection policies managed by the India Semiconductor Mission to support deep-tech entrepreneurs transitioning academic benchwork into commercial silicon.



Invited Talk by Dr. Manish Kumar Hooda and the felicitation by Sri. Ravichandran Rajagopal

Session 13: Terahertz Photonic Technology Using Graphene and EM Phenomena in Nanophotonics

- **Speaker: Prof. Christos Argyropoulos, Professor, Penn State University, USA**
- **Abstract: Exploring the terahertz (THz) spectrum gap, this session evaluated nanophotonic devices utilizing graphene and plasmonic materials. By exploiting electromagnetic surface plasmon polaritons, the presented research paths enable ultra-fast optical switching, advanced modulators, and novel energy-harvesting hardware components.**



Invited Talk by Prof. Christos Argyropoulos

Session 14: Signal and Power Integrity for Advanced Packages Enabling AI Hardware

- **Speaker: Dr. Yutaka Uematsu, Principal Researcher, Hitachi, Japan**
- **Abstract: Dr. Uematsu presented Hitachi's technical solutions for managing power and signal distortion within high-density substrate packaging. The discussion detailed design techniques for decoupling capacitor placement, minimizing simultaneous switching noise (SSN), and maintaining signal fidelity over sub-micron substrate routing lanes.**



Invited Talk by Dr. Yutaka Uematsu

Session 15: Advanced Semiconductor Devices for AI

- **Speaker: Mr. Paul Ilanghovan T., Head of Operations, Kaynes Semicon Pvt. Ltd.**
- **Abstract: Shifting focus to physical execution, this session discussed current domestic deployment efforts for AI-optimized silicon. The speaker elaborated on operational challenges and packaging choices for high-performance processors, emphasizing Kaynes Semicon's scaling strategies within the Indian semiconductor ecosystem.**



Invited Talk by Mr. Paul Ilanghovan T

Session 16: Characterization of Photonics

- **Speaker: Dr. Sai Rama Krishna Malladi, Professor, IIT Hyderabad**
- **Abstract: Precise metrology is vital for optical-electronic co-integration. Dr. Malladi detailed advanced spectroscopic and microscopic characterization methods used to identify defects, trace optical waveguide propagation losses, and measure structural alignment down to atomic scales.**



Invited Talk by Dr. Sai Rama Krishna Malladi

Session 17: Next-Generation MEMS Technology and its Packaging

- **Speaker: Dr. Harsha Sanjeev, Scientist, CMTI Bangalore**
- **Abstract: This talk addressed the miniaturization of Micro-Electro-Mechanical Systems (MEMS). Dr. Sanjeev covered fabrication routines and hermetic wafer-level packaging techniques that protect delicate moving microstructures while maintaining high sensitivity for aerospace, automotive, and consumer IoT sensors.**



Invited Talk by Dr. Dr. Harsha Sanjeev

Panel Discussion III: From Silicon to Systems: Power-Aware AI Computing through Algorithm and Hardware Co-Optimization

- **Moderator:** Dr. Harsha Sanjeev, Scientist, CMTI Bangalore
- **Panelists:** Dr. Yutaka Uematsu (Hitachi, Japan), Prof. Christos Argyropoulos (Penn State University), Dr. Sai Rama Krishna Malladi (IIT Hyderabad), Mr. Pradeep Manohar (Director, Smart Manufacturing & AI, Micron Technology)
- **Key Takeaways:** The discussion focused on full-stack optimization. The panel concluded that true energy-efficient AI cannot be achieved by hardware changes alone; it requires code-design strategies where software neural network layers are intentionally matched to structural hardware properties and silicon floorplans.



A glimpse of the Panel Discussion III

Session 18: VLSI Design for Neural Networks

- **Speaker: Dr. T. Satya Savithri, Professor & Director R&D, JNTUH**
- **Abstract: Dr. Savithri presented circuit-level architectures optimized for matrix-vector multiplication—the fundamental core of deep learning algorithms. The presentation detailed the synthesis of systolic arrays, optimized MAC (Multiply-Accumulate) units, and register-transfer level (RTL) engineering aimed at maximizing processing density within AI accelerators.**

Session 19: Energy-Efficient FPGA-Based Accelerators

- **Speaker: Dr. Asral Bahari Jambek, Associate Professor & Head of MICTEC, UNIMAP, Malaysia**
- **Abstract: This lecture focused on practical optimization techniques for FPGA implementations. Dr. Jambek demonstrated dynamic voltage and frequency scaling (DVFS), clock-gating methodologies, and fixed-point mathematical abstractions that reduce dynamic power dissipation in portable, edge-deployed FPGA systems.**

Session 20: Advanced Packaging and Thermal Management for SiC & GaN Technologies

- **Speaker: Mr. Vijay Bolloju, Director of R&D at iVP Semiconductor**
- **Abstract: Wide-bandgap semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN) operate under demanding thermal and electrical stresses. Mr. Bolloju evaluated innovative packaging solutions, including silver sinter bonding and high-conductivity ceramic substrates, that prevent catastrophic thermal failures in high-power infrastructure.**

Session 21: AI Enabled Metrology Tools for Semiconductor Material Testing

- **Speaker: Mr. Parikshit Sengupta, Segment Head Materials and Semiconductor, Horiba India Pvt. Ltd.**
- **Abstract: This talk introduced AI routines within commercial characterization systems. By integrating automated machine learning classification with Ellipsometry and Raman Spectroscopy, industrial inspection tools can identify line defects, contamination, and material irregularities during production with higher accuracy.**

Session 22: The Role of SiC in AI Infrastructure and Next Gen Power Electronics

- **Speaker: Dr. K. Akshay, Assistant Professor (IIT Bhubaneswar) & Director (Nano Semic)**
- **Abstract: As data centers expand to process heavy AI workloads, their power distribution must be highly efficient. Dr. Akshay detailed how SiC-based power electronic switches minimize energy loss in high-voltage power supplies, driving down total operating overhead for AI data infrastructure.**

Session 23: Metallization in Advanced Glass Substrates

- **Speaker: Prof. Pradeep Dixit, Associate Professor, IIT Bombay**
- **Abstract: Closing out the technical sessions, Prof. Dixit presented glass substrates as an alternative to traditional silicon or organic interposers. The presentation detailed the electrochemical challenges and structural methods for Through-Glass Vias (TGVs), demonstrating how glass provides improved electrical isolation, dimensional stability, and high-frequency capabilities for upcoming chiplet packages.**

Technical Outcomes & Recommendations

1. **Academic Integration:** Establish collaborative laboratories focused on 3DHI, FPGA prototyping, and advanced packaging to match global research standards.
2. **Industry Alignment:** Bridge the student talent gap by updating specialized coursework to focus on practical pre-silicon verification, EDA tool flows, and wide-bandgap material properties.
3. **Strategic Research:** Encourage interdisciplinary research merging material synthesis (such as 2D materials and photonics) with hardware-aware AI algorithms.



Group photograph of the esteemed dignitaries, keynote speakers, and organizers at the valedictory of the International Workshop on AI Driven Semiconductor and Energy Efficient Hardware, held at The Marvel, T-Hub

Few Glimpses of the Workshop:



IEEE Bvrit team with Mr. N Venkatesh, Secretary, IEEE Hyderabad Chapter



BVRIT Organizers team with Professors from JNTUH