State-of-the-Art Silicon Very Large Scale Integrated Circuits: Industrial Face of Nanotechnology

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Troy, NY 12180, USA

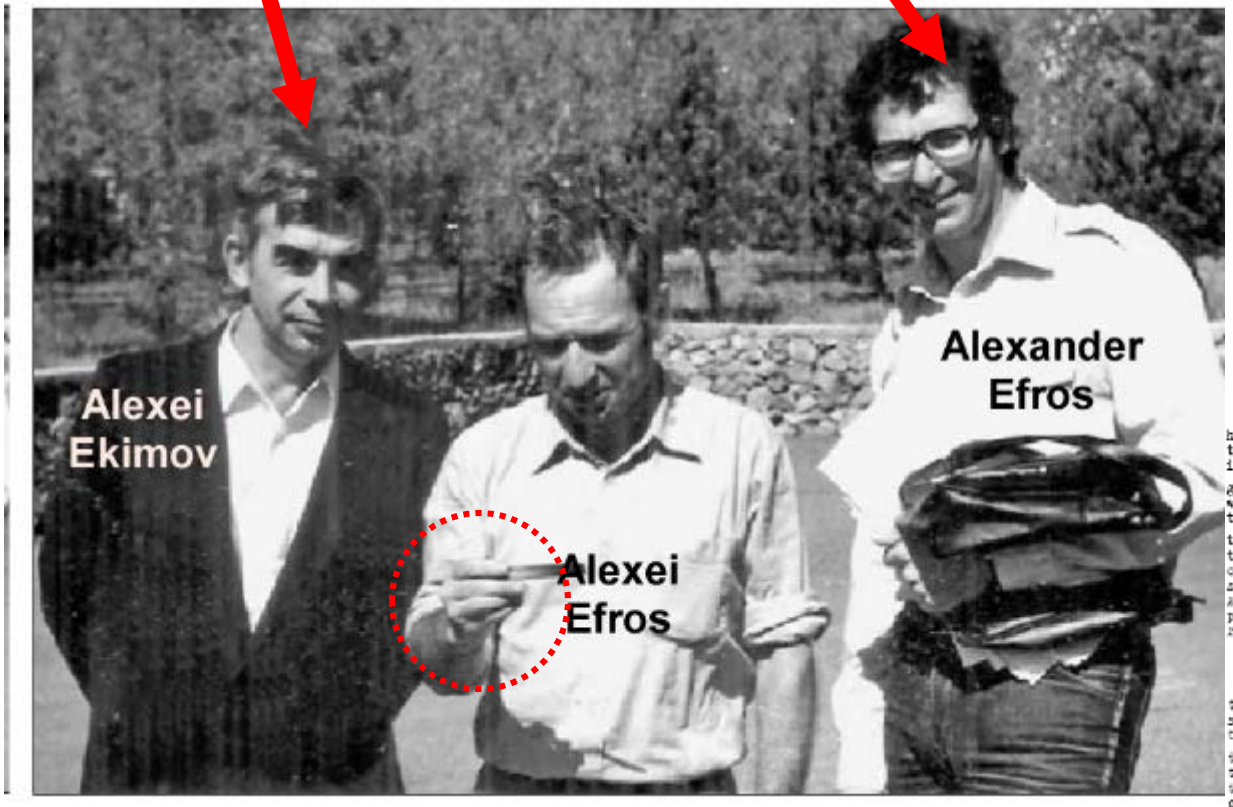
January 21, 2021

Outline

- Silicon VLSI: State of the art, emerging problems and cost
- New counter intuitive physics of VLSI
- Sub-THz and THz Si CMOS
- Thin Film Transistors
- Conclusions

Ekimov, A. I., Efros, A. L., & Onushchenko, A. A. (1985). Quantum size effect in semiconductor microcrystals. Solid State Communications, 56(11), 921–924

FIRST PAPER ON NANOTECHNOLOGY (1985)



QUANTUM SIZE EFFECT IN SEMICONDUCTOR MICROCRYSTALS

A.I.Ekimov, Al.L.Efros, A.A.Onushchenko

Ioffe Physicotechnical Institute, Leningrad, 194021, USSR

(Received 9 September 1985 by V.M.Agranovich)

A growth technique of the semiconductor microcrystals in a glassy dielectric matrix has been developed. This technique permits to vary the size of the grown microcrystals in a controlled manner from some tens to thousands of angstroms. The size dependence of absorption spectra of a number of I-VII and II-VI compounds grown by this technique have been studied. The size of the microcrystals being decreased, a considerable short-wave-length shift of the exciton lines and the fundamental absorption edge has been observed. This phenomenon is due to the size quantization of the free carrier and exciton energy spectra in the microcrystals.

Size effects in semiconductors have attracted much attention within the last few years. They were studied in quasi-two-dimensional structures grown by molecular beam epitaxy[1], as well as in three-dimensional microcrystals prepared by the substrate evaporation technique[2]. In this paper we report the discovery and a spectroscopic study of a new class of objects that exhibits size effects - three dimensional microscopic crystals of semiconductor compounds grown in a transparent dielectric matrix.

1. Microcrystal growth

Microcrystals were grown in a multicomponent silicate glass in which the semiconductor phase of the concentration of about 1 % was dissolved during the synthesis[3]. At the secondary heat treatment of the glass samples, nucleation and growth of semiconductor microcrystals occurred as a result of a diffusive phase decomposition of the supersaturated solid solution. Fig.1 shows experimental dependence of the average radius R of CdS and CuCl microcrystals as a function of the heat time for a number of temperatures. Values of the average radius of micro-

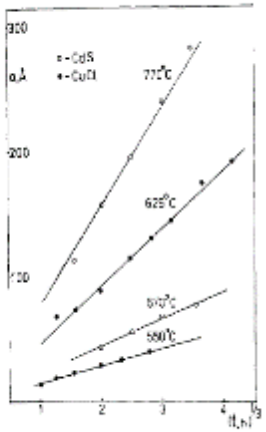


Fig.1. Dependence of the average radius R of the CdS and CuCl microcrystals on heat time t at various temperatures of heat treatment.

Nanotechnology:
40,900,000 entries on GOOGLE

Definition: 100 nm or smaller

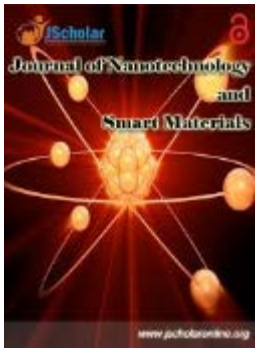
nan·o·tech·nol·o·gy

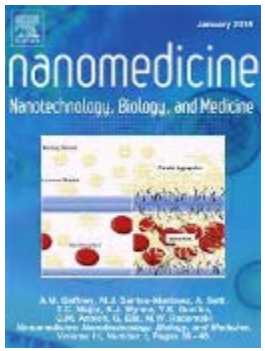
/ˌnanōˌtekˈnäləjē/

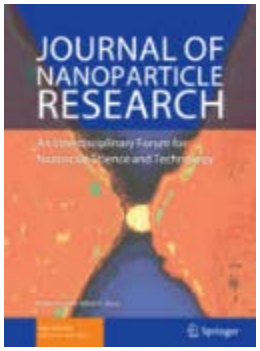
noun

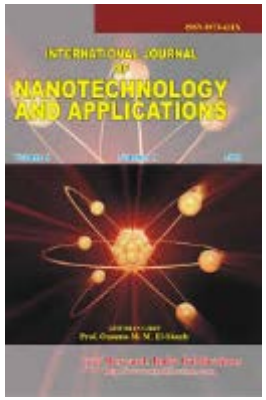
the branch of technology that deals with dimensions and tolerances of less than 100 nanometers, especially the manipulation of individual atoms and molecules.

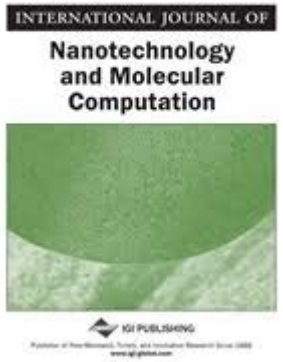
Just a Few of Scores of Nanotechnology Journals

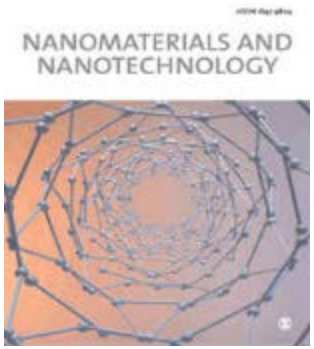


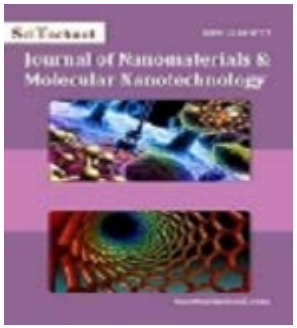


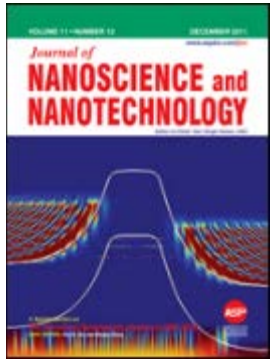




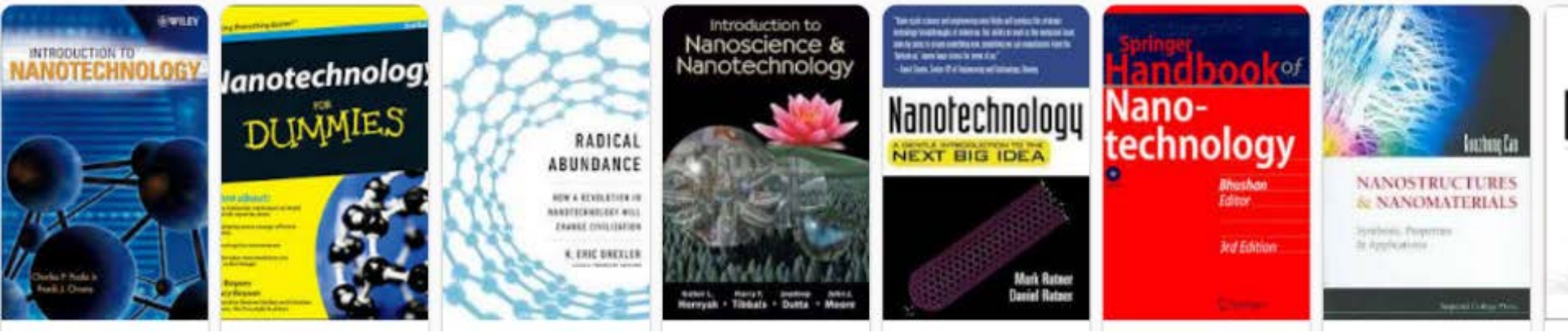








Just a Few of Scores of Nanotechnology Books

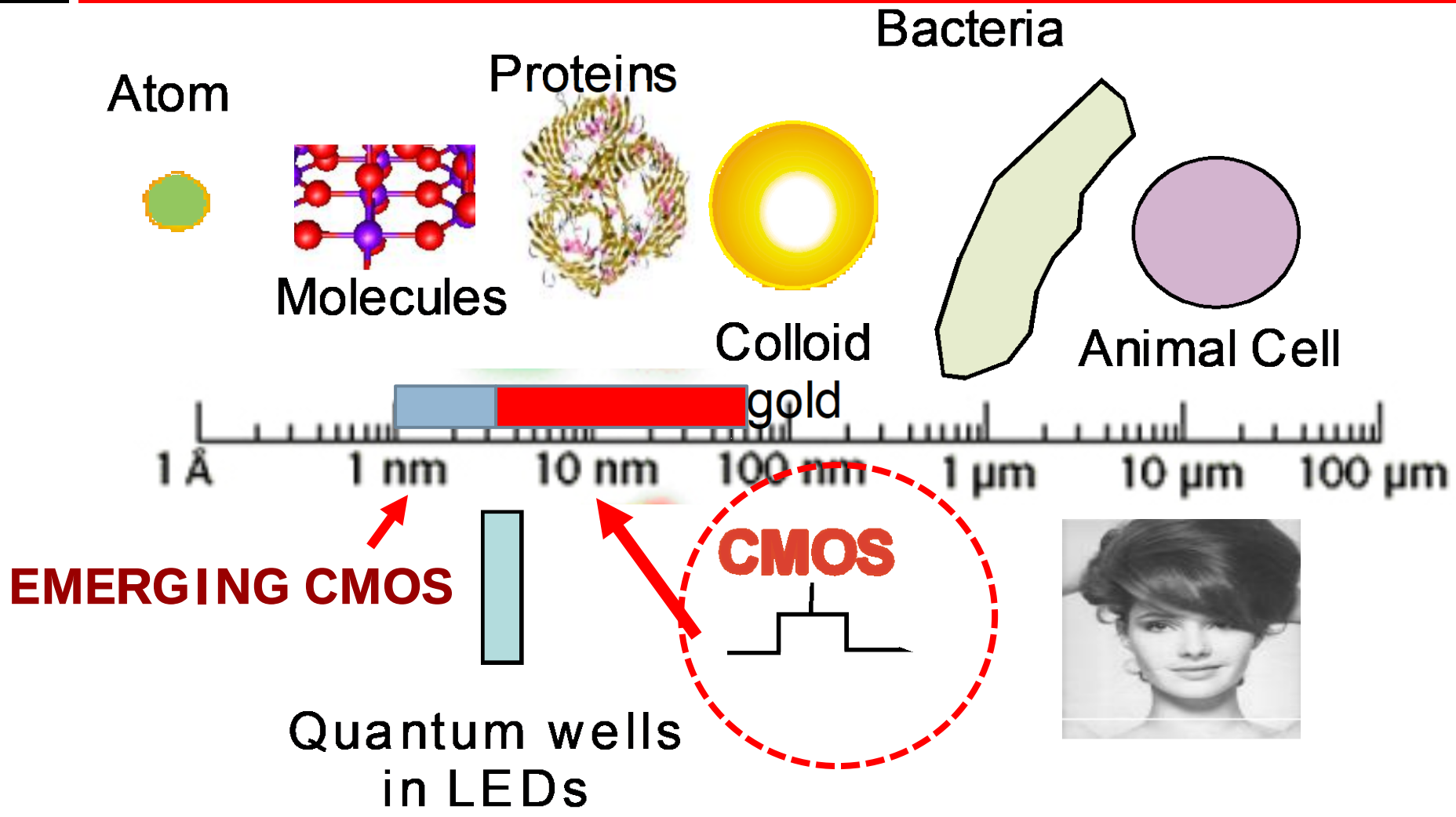


JANUS – A Two Faced Greek God of Beginning and Passages

Industrial face of Nanotechnology

Research face of Nanotechnology

NANOSIZES


Atom
Molecules
Proteins
Colloid gold
Bacteria
Animal Cell
1 Å
1 nm
10 nm
100 nm
1 µm
10 µm
100 µm
EMERGING CMOS
Quantum wells in LEDs
CMOS

Toward 2 nm

TSMC is already on track to develop 2nm node, while 3nm planned for 2022

April 27, 2020 by David

https://optocrypto.com/tsmc-2nm-node-process-3nm-2022/

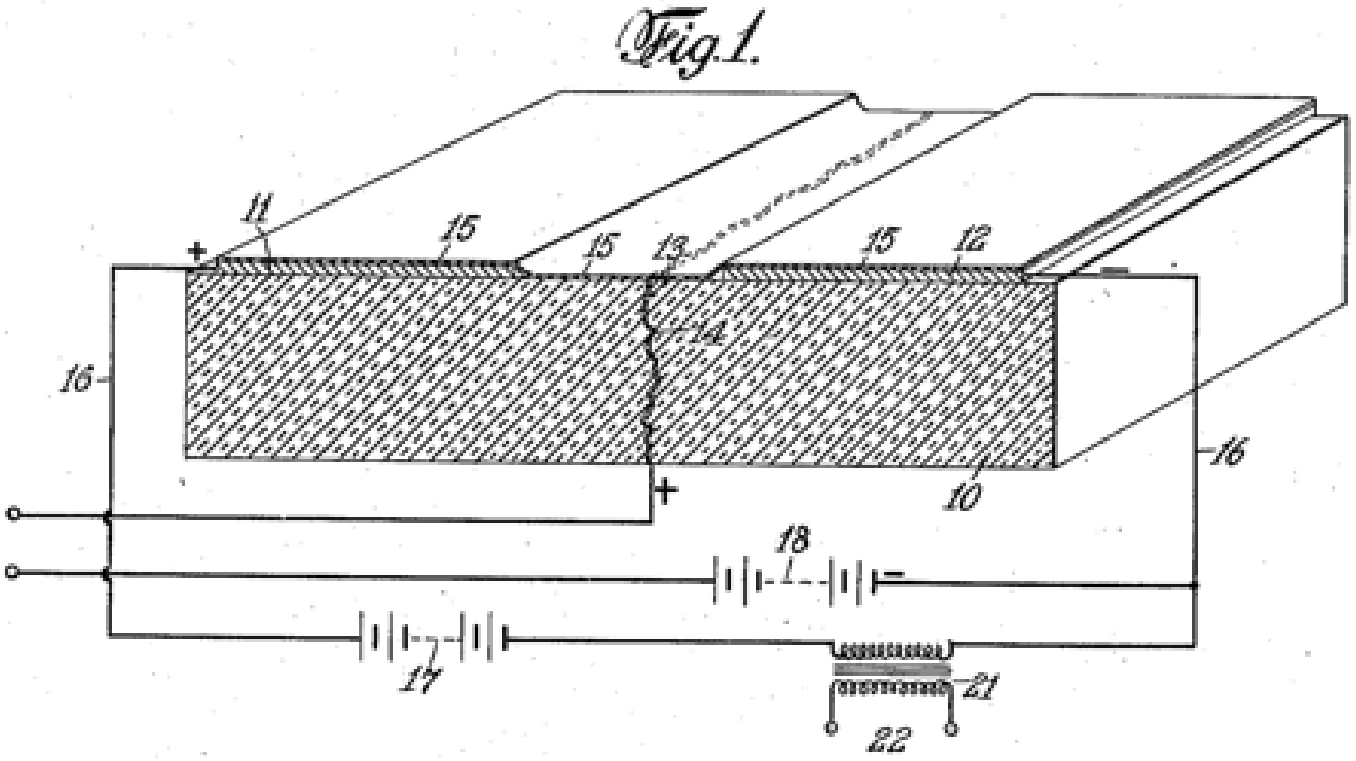
Patent filed 1926

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

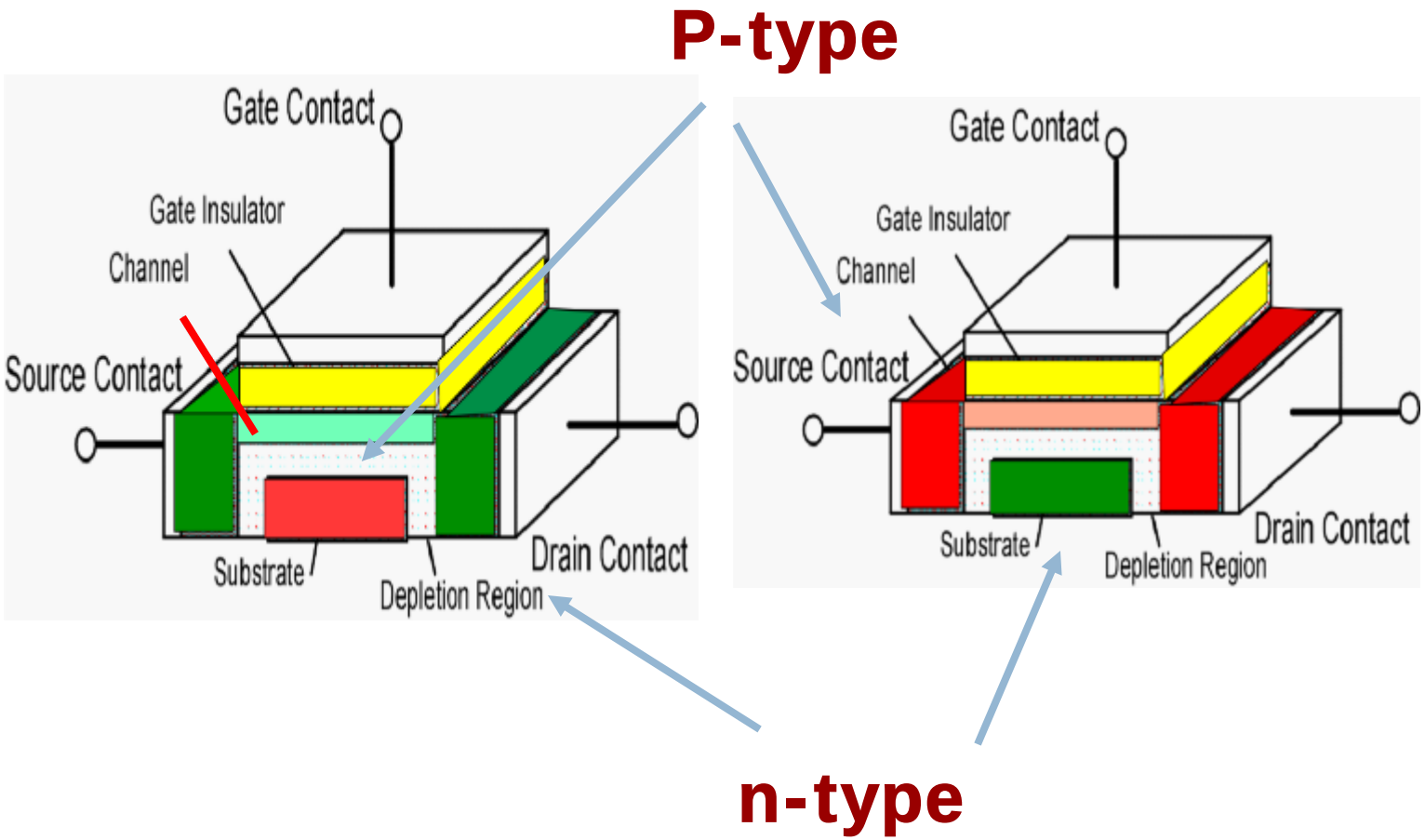
METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

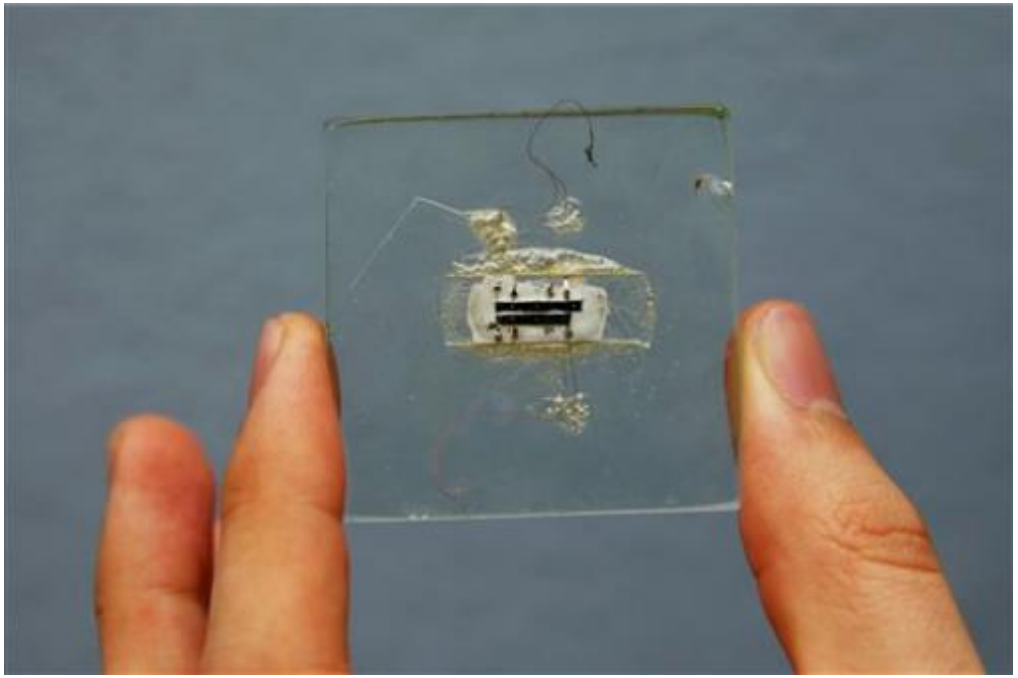
Fig. 1.

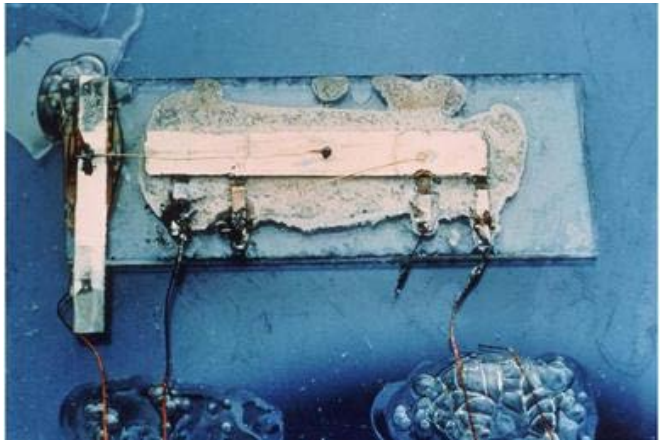


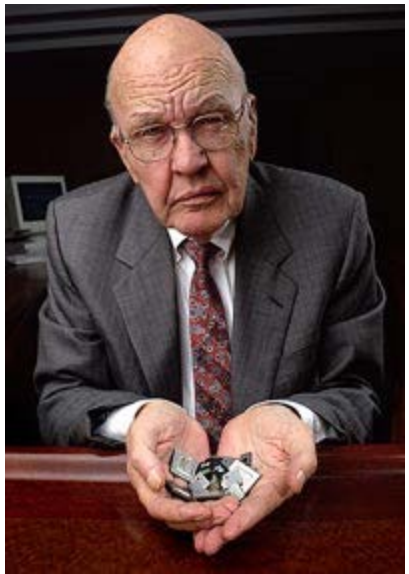
Field Effect Transistor n-MOSFET and p-MOSFET



Integrated circuit chip designed by Noble Prize winner Jack Kirby of TI (1958).



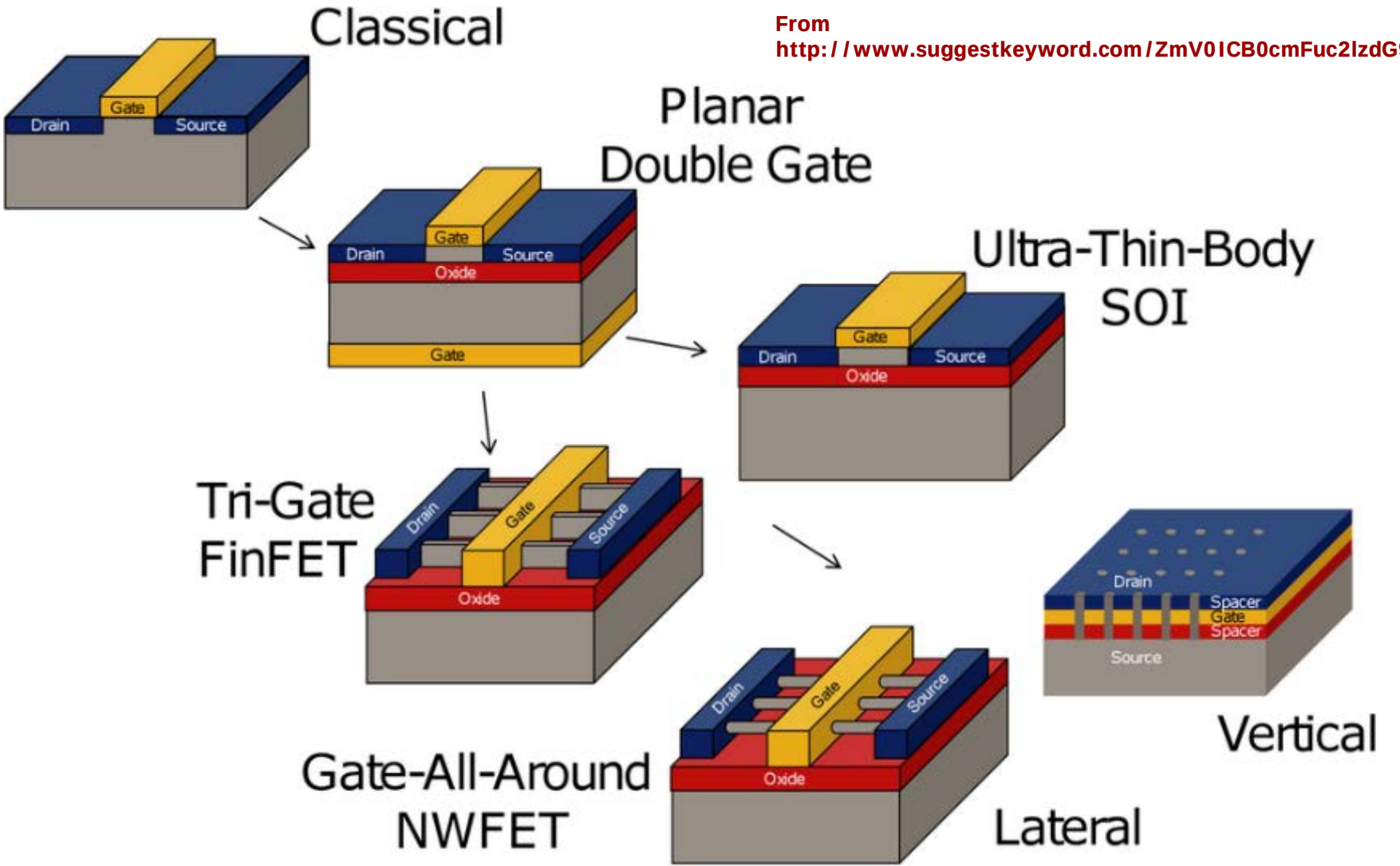




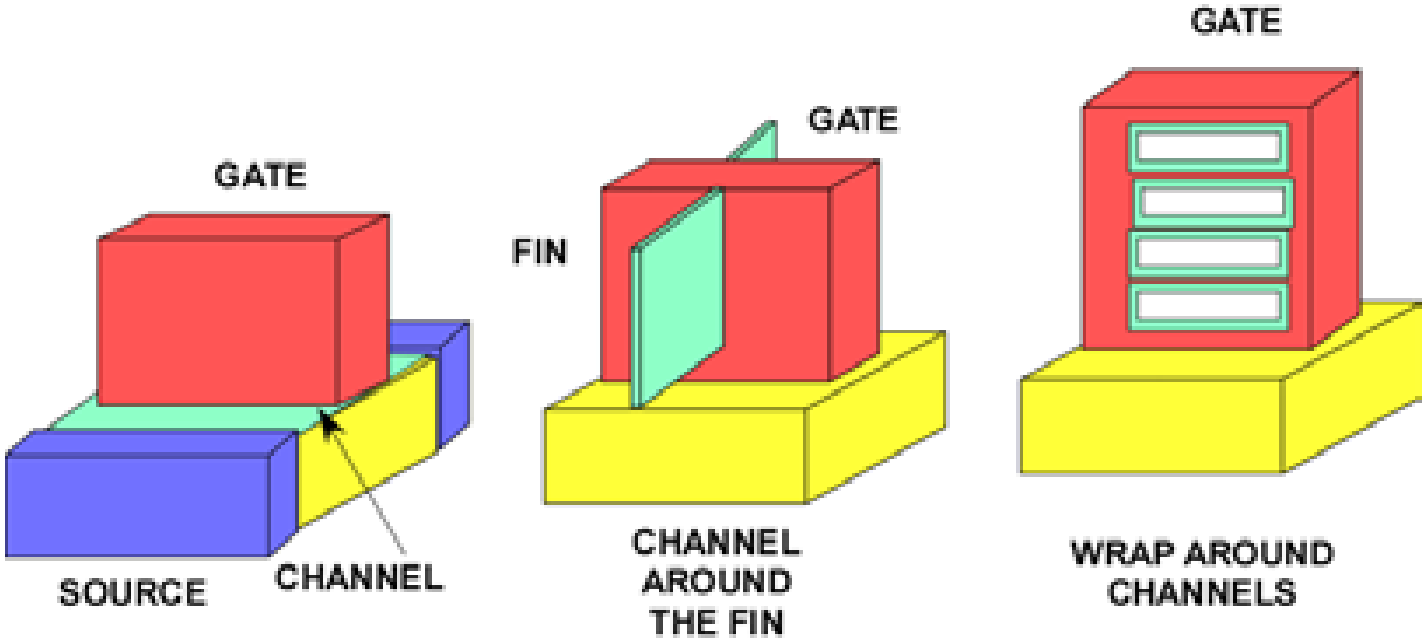
By Source, Fair use,
https://en.wikipedia.org/w/index.php?curid=34183097

MOSFET Types

From
http://www.suggestkeyword.com/ZmV0ICB0cmFuc2IzdG9y/



FROM MOSFET TO ALL AROUND GATE



22 nm **7 nm** **5 - 1 nm**

From M. S. Shur, Terahertz Plasmonic Technology, IEEE Sensors Journal, Invited, DOI: 10.1109/JSEN.2020.3022809

Minimum Transistor size

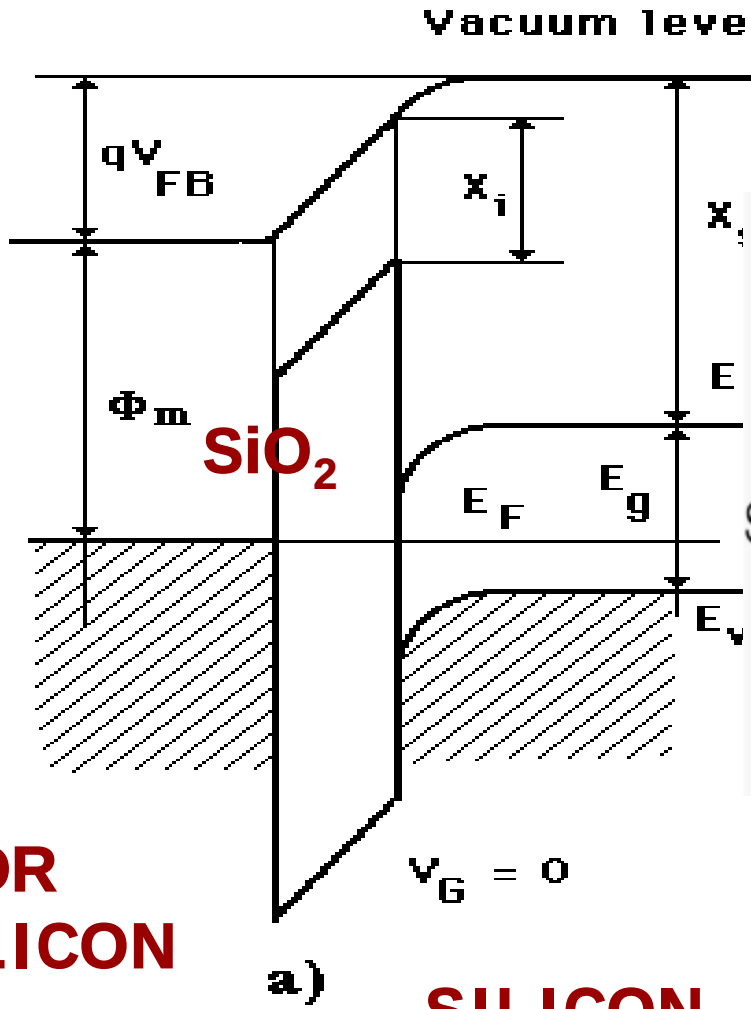
Silicon unit cell 0.543 nm (9 unit cells for 5 nm)

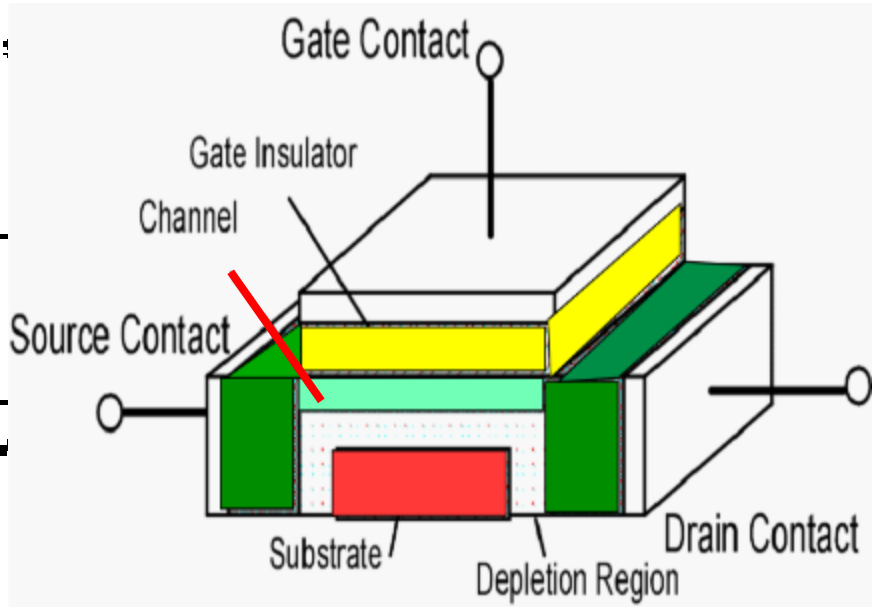
Silicon –Silicon Dioxide interface 0.7 nm

Silicon-Silicon Dioxide layer 1 nm

Ferdinand Hodler, Swiss (March 14, 1853 – May 19, 1918)

Band diagram in the direction perpendicular to the channel



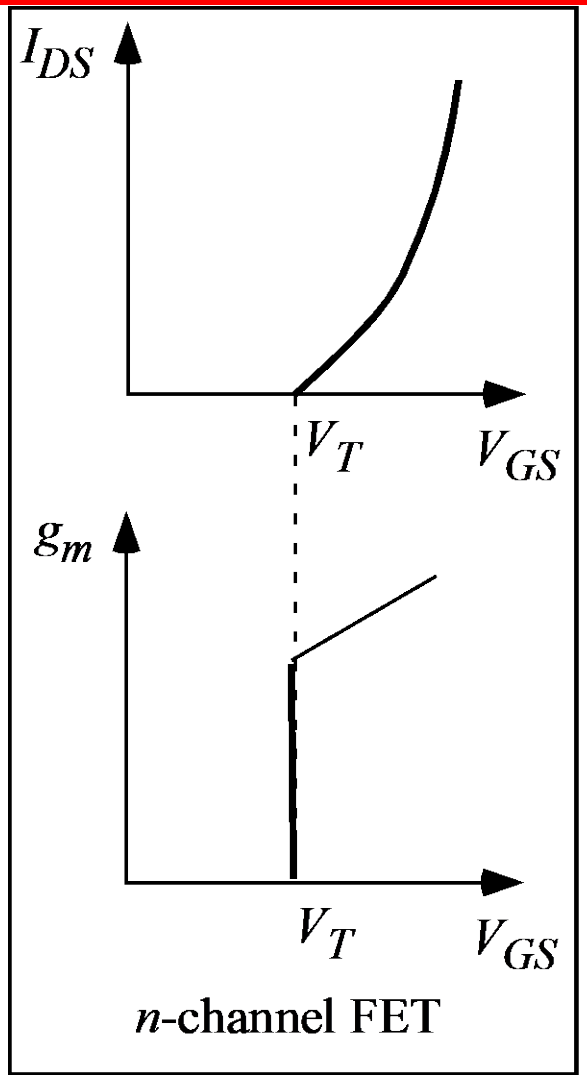


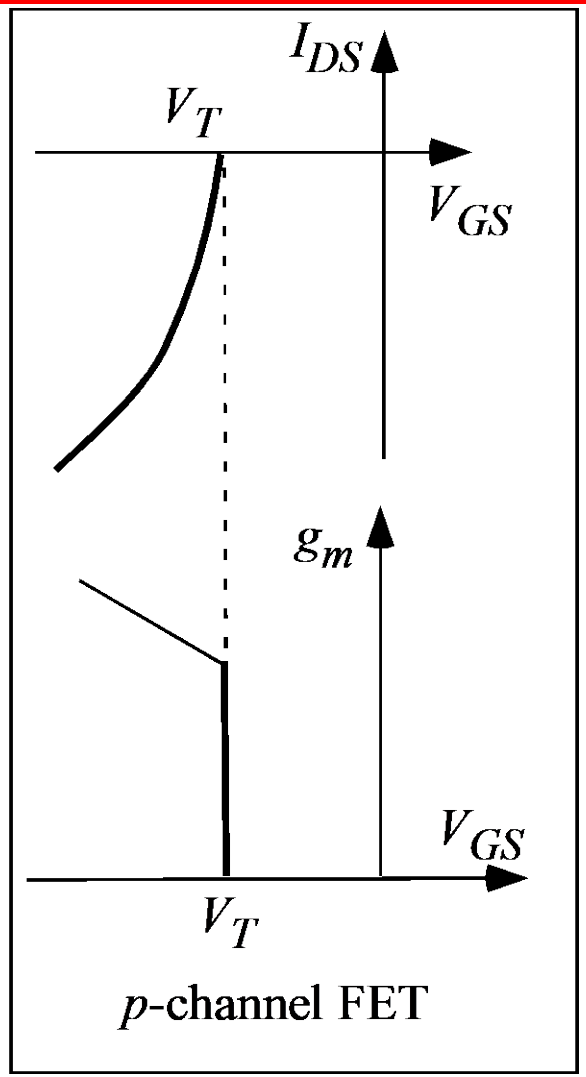
METAL OR POLYSILICON

SILICON

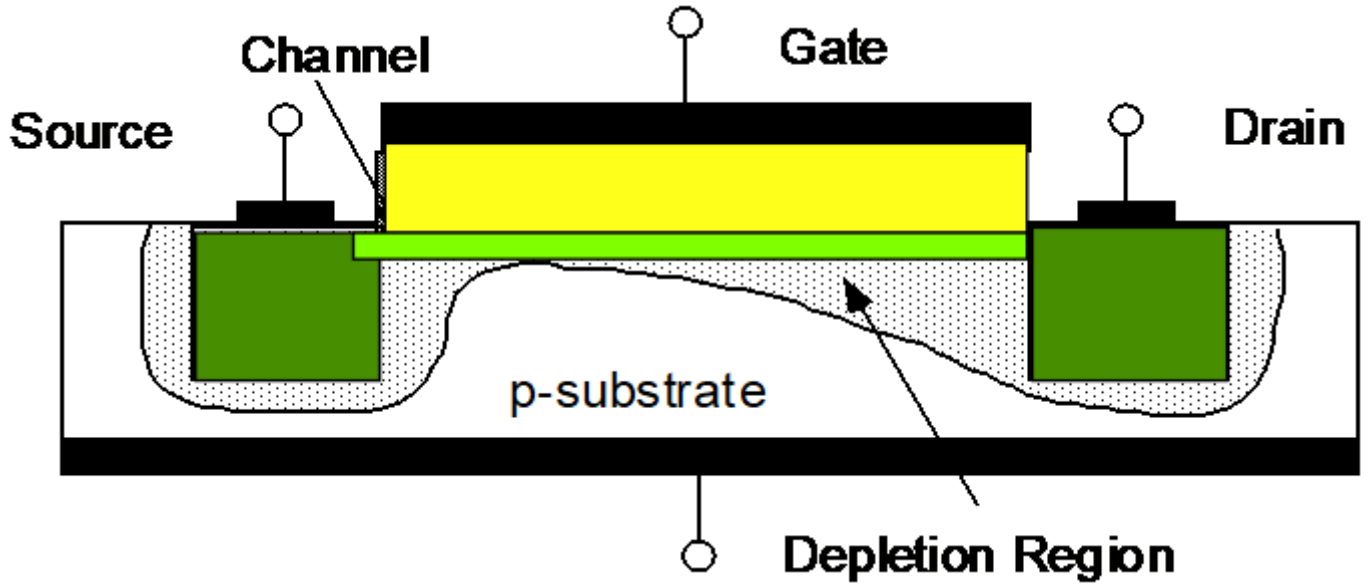
(b)

Idealized MOSFET I-Vs





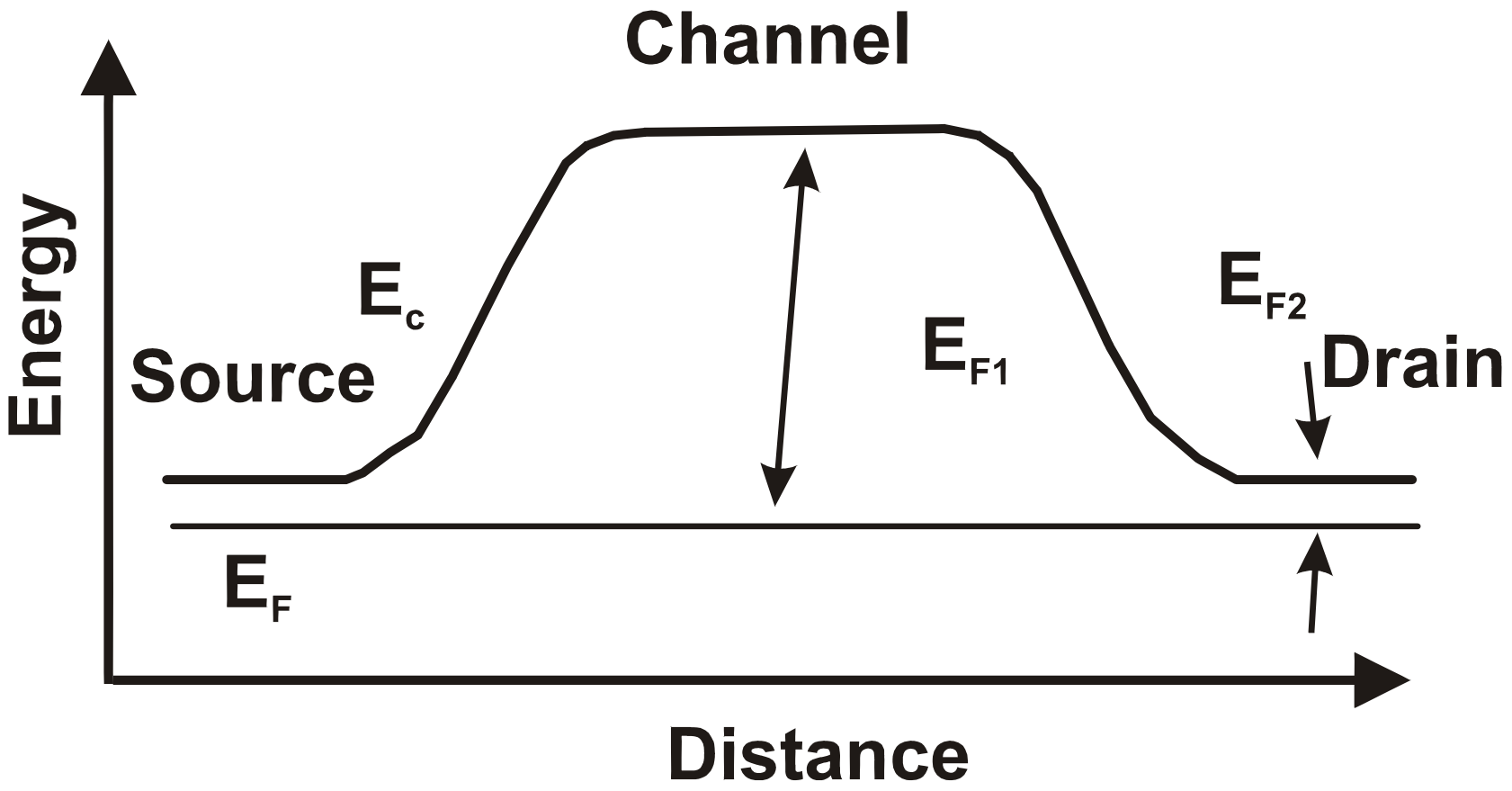
Charge Control Concept



Schematic cross-section of an n-channel MOSFET. The asymmetry in the shape of the depletion region is caused by the applied drain bias.

$$Q = C V$$

Band Diagram for Subthreshold Regime



UNIFIED CHARGE CONTROL MODEL

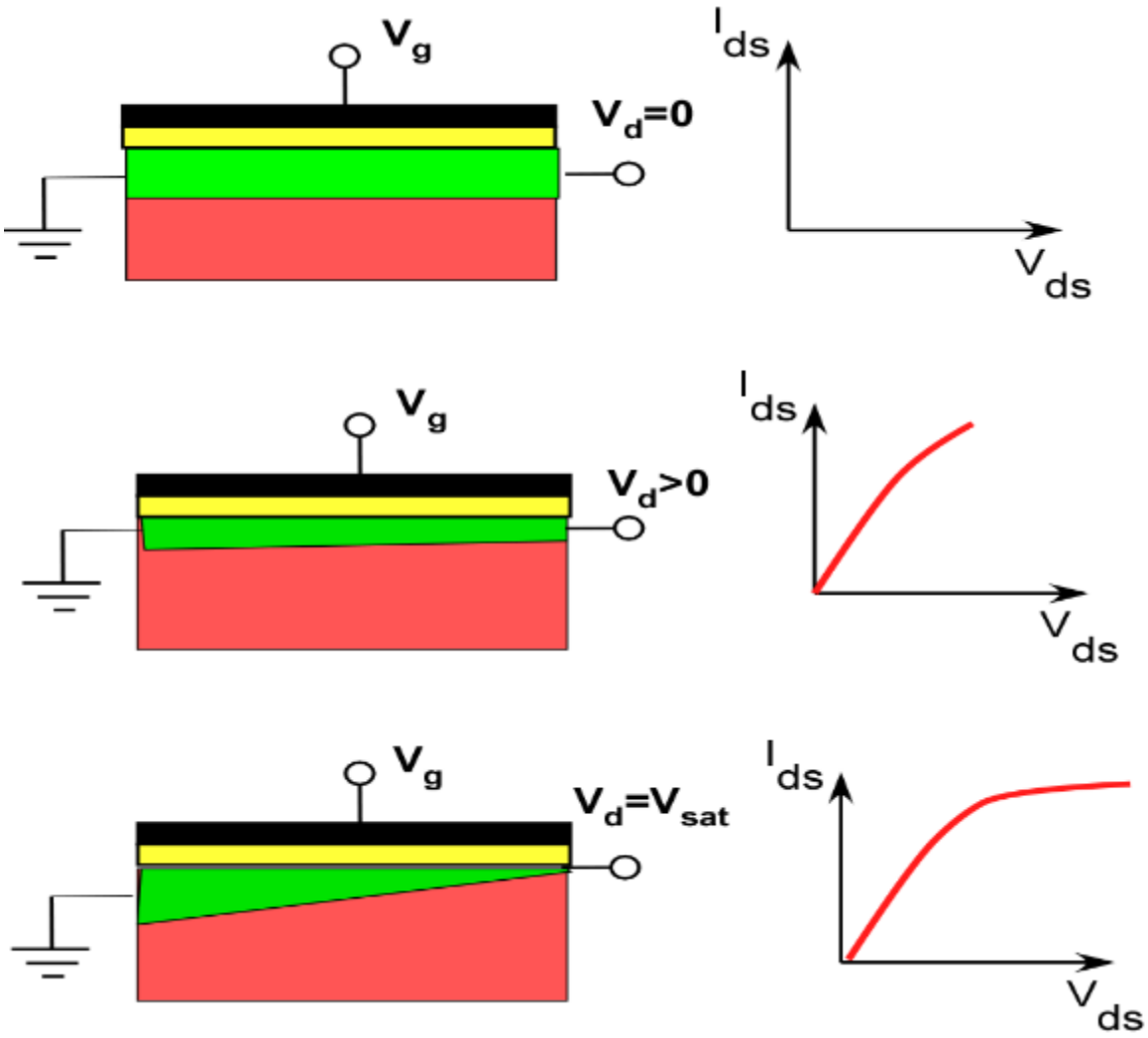
$$V_{GT} - V_F = \eta V_{th} \ln\left(\frac{n_s}{n_o}\right) + a(n_s - n_o)$$

where V_F is the quasi-Fermi potential measured relative to the Fermi potential at the source side of the channel (V_F = 0 at the source side of the channel and $V_F = V_{DS}$ at the drain side), is the ideality factor in the subthreshold region,

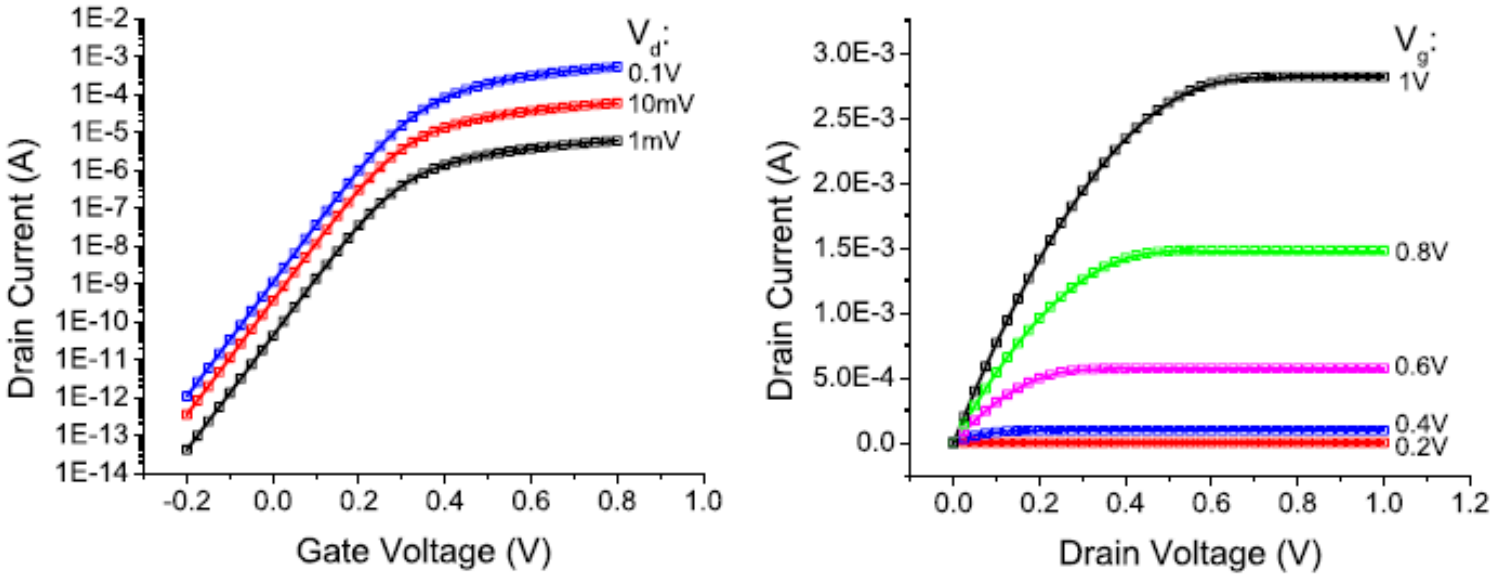
V_{th} is the thermal voltage, and a - q/c_a where

$c_a = \dfrac{\varepsilon_i}{d_i + \Delta d}$ is the effective gate capacitance per unit area above the threshold (when the gate voltage swing $V_{GT} >> V_{th}$).

Current saturation

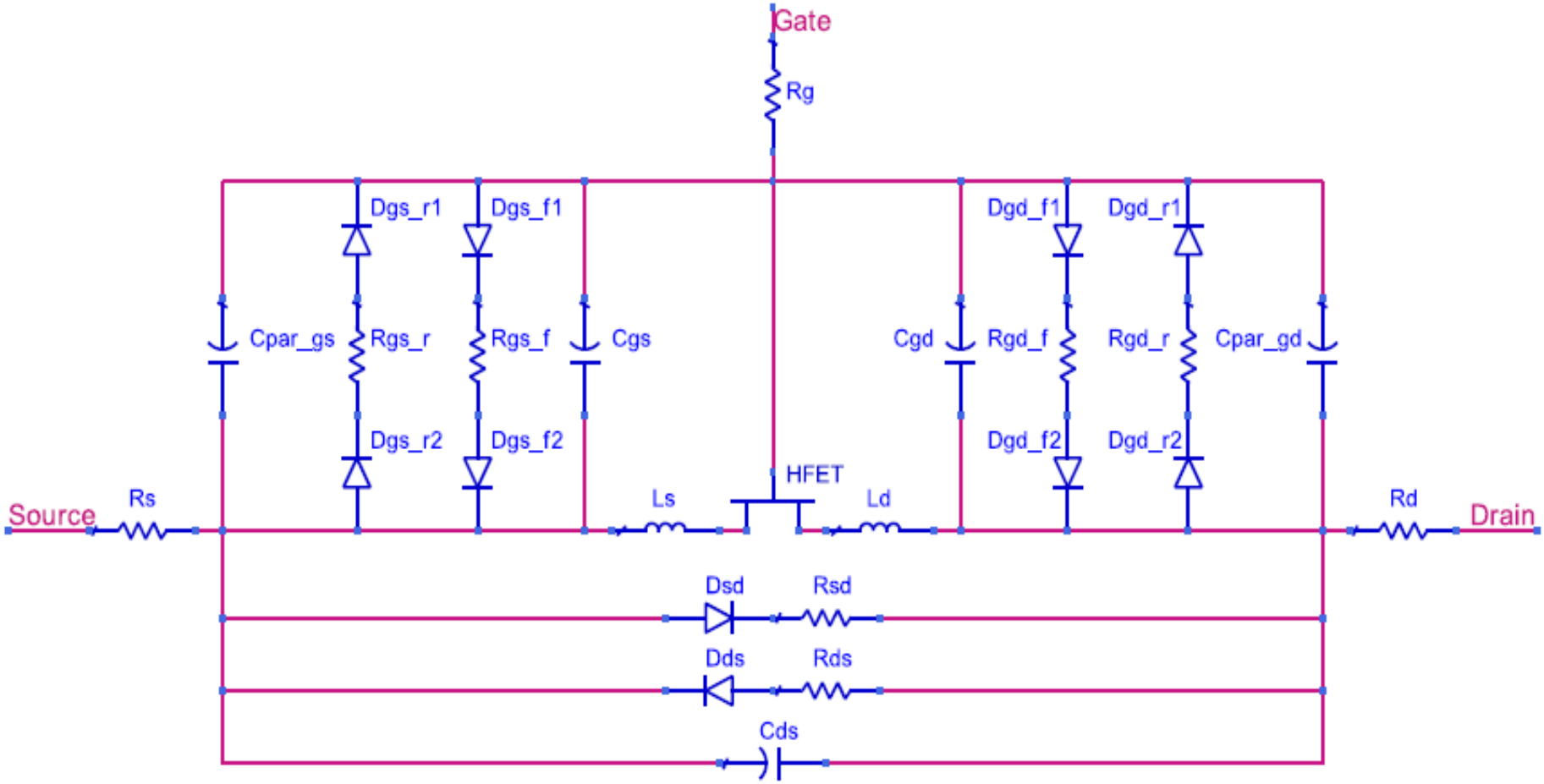


Currnt-Voltage Characteristics



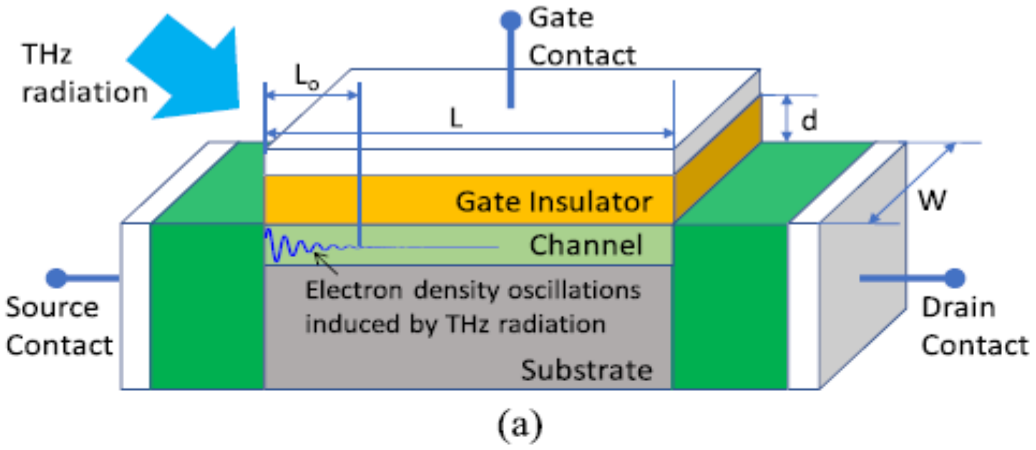
From X. Liu, T. Ytterdal, V. Yu. Kachorovskii, and M. S. Shur, Compact terahertz SPICE/ADS model, IEEE Transactions on Electron Devices, Volume: 66, Issue:6, pp. 2496-2501, June 2019, DOI: 10.1109/TED.2019.2911485

Equivalent Circuit



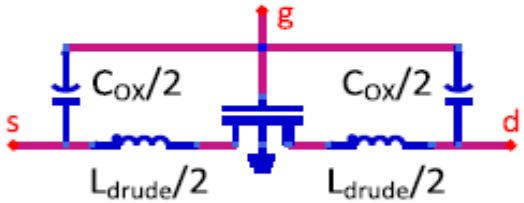
X. Liu, K. Dovidenko, J. Park, T. Ytterdal, and M. Shur, Compact Terahertz SPICE Model: Effects of Drude Inductance and Leakage, IEEE TED, IEEE Transactions on Electron Devices, Volume: 65 Issue: 12, pp. 5350-5356, DOI: 1109/TED.2018.2875345

Multi segment THz SPICE



(a)

From X. Liu, T. Ytterdal, V. Yu. Kachorovskii, and M. S. Shur, Compact terahertz SPICE/ADS model, IEEE Transactions on Electron Devices, Volume: 66, Issue:6, pp. 2496-2501, June 2019, DOI: 10.1109/TED.2019.2911485



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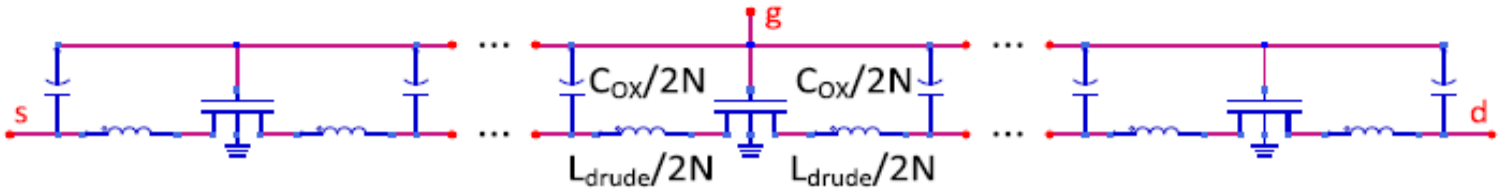
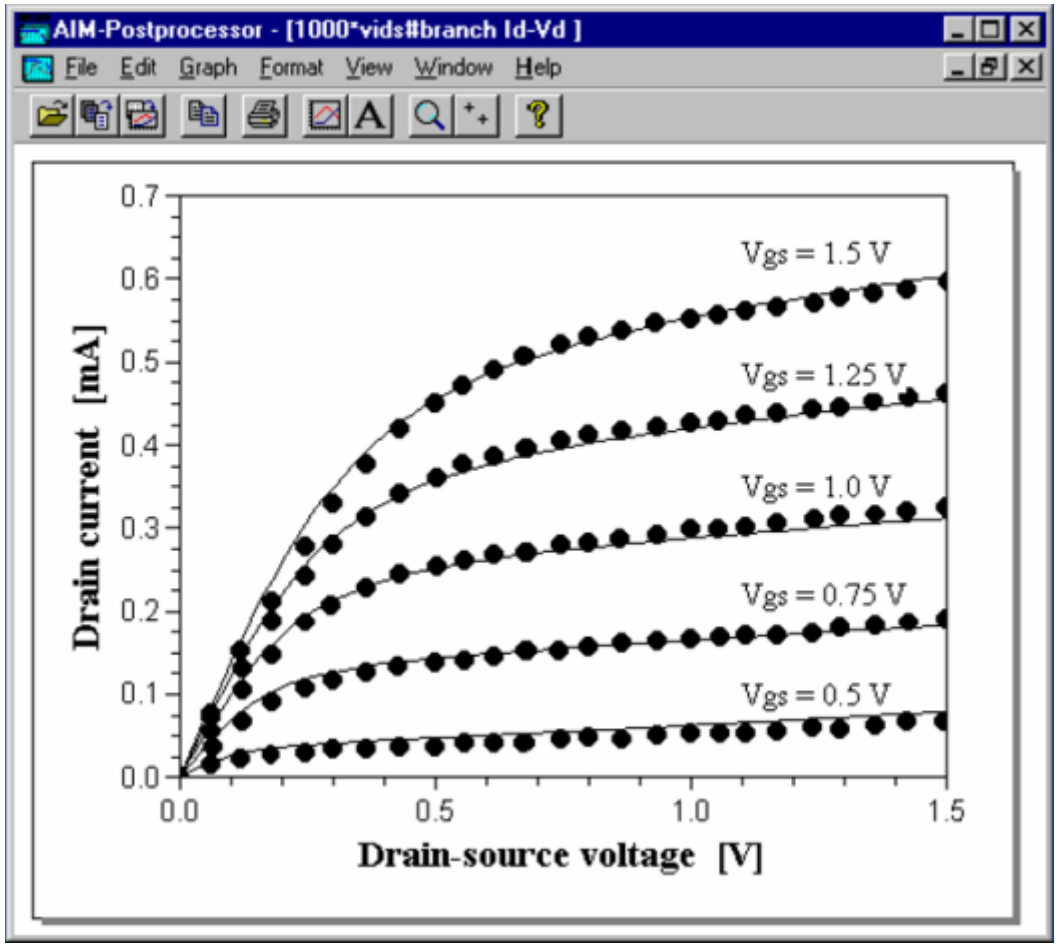
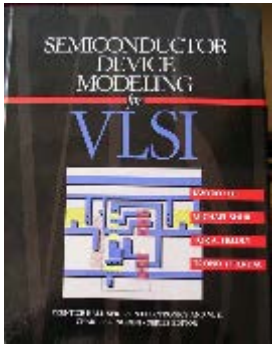


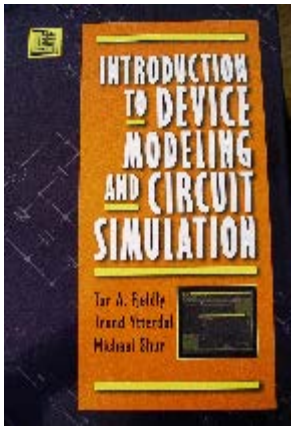
(c)

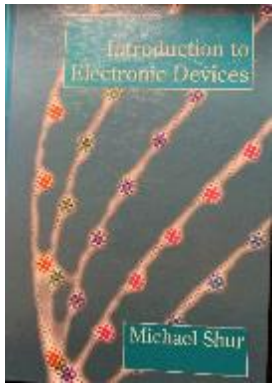
AIM-SPICE


AIM-Postprocessor - [1000*vids#branch Id-Vd]
File Edit Graph Format View Window Help
Vgs = 1.5 V
Vgs = 1.25 V
Vgs = 1.0 V
Vgs = 0.75 V
Vgs = 0.5 V
Drain current [mA]
Drain-source voltage [V]
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.0
0.5
1.0
1.5

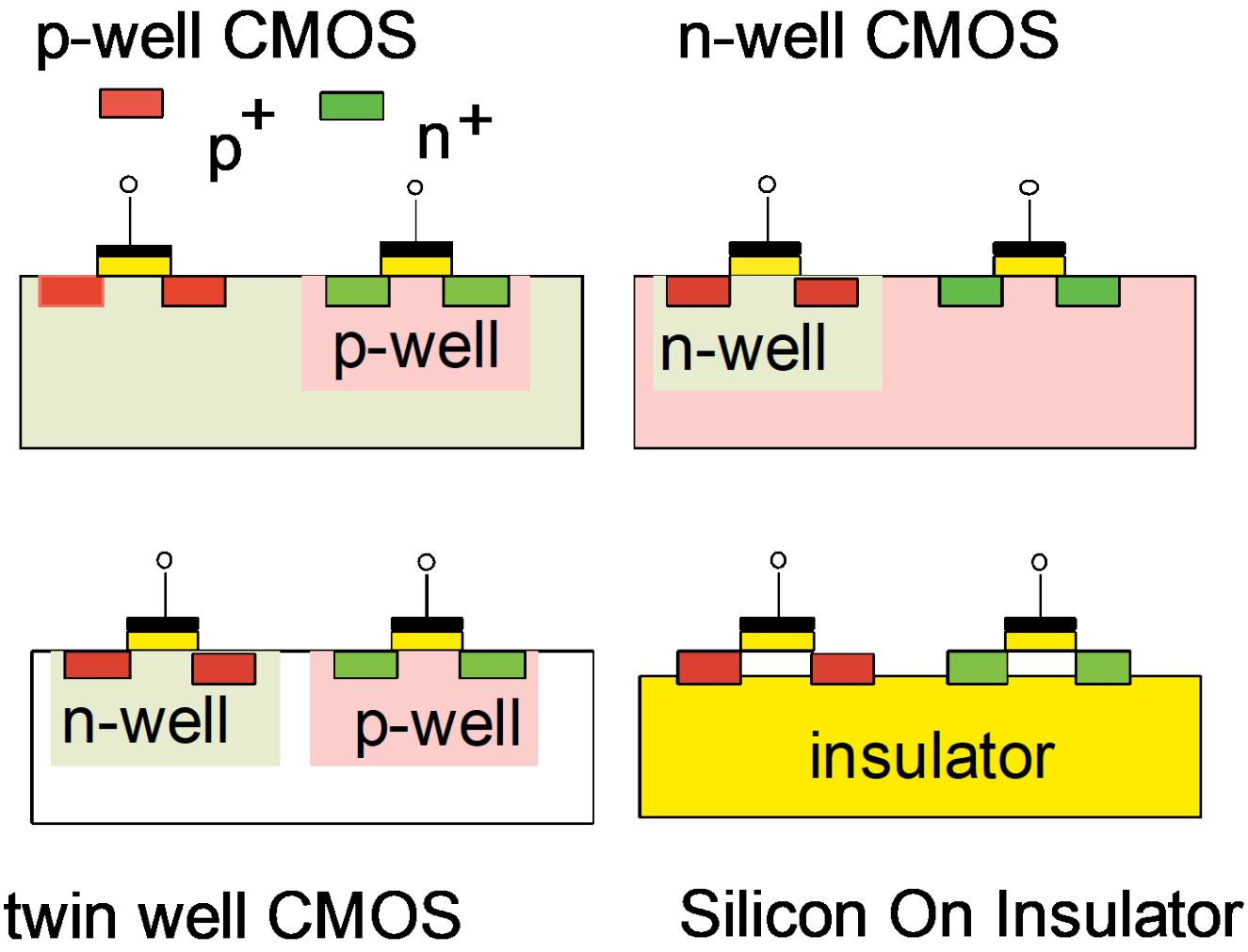

SEMICONDUCTOR DEVICE MODELING for VLSI


Lab on the Web


INTRODUCTION TO DEVICE MODELING AND CIRCUIT SIMULATION

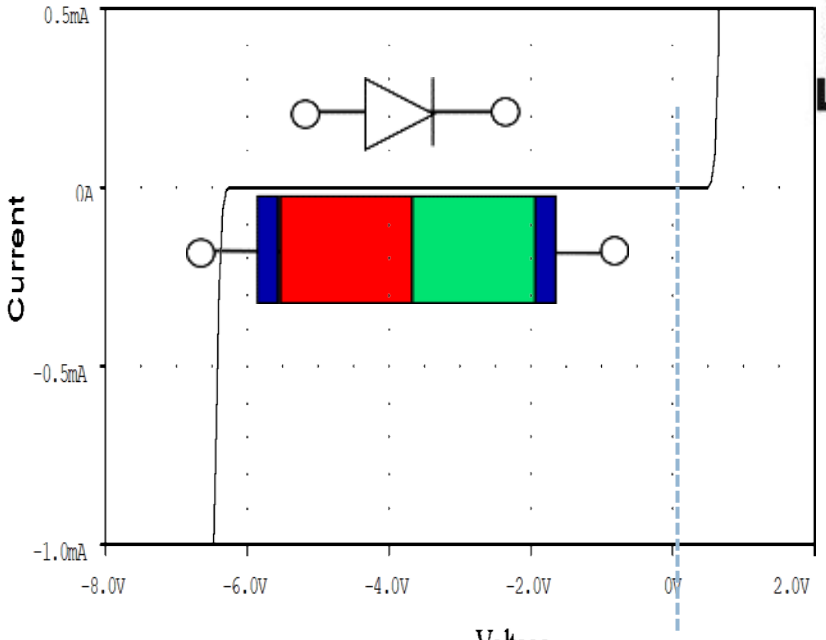

Introduction to Electronic Devices
Michael Shur

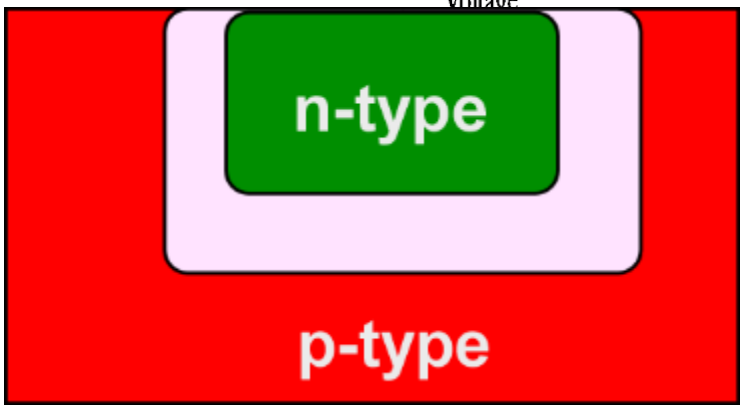
CMOS

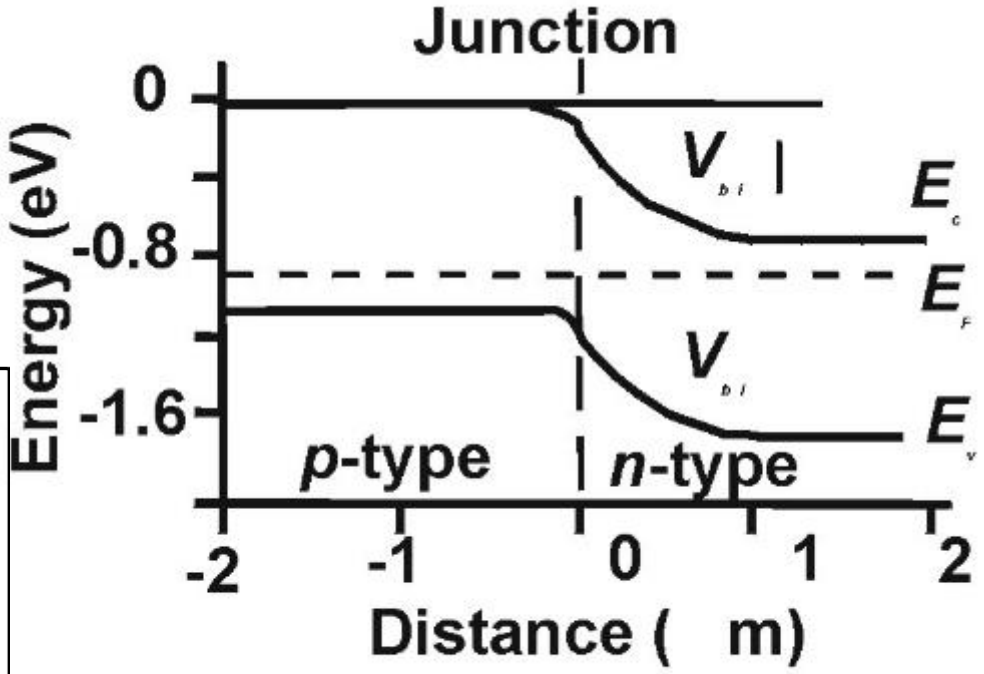


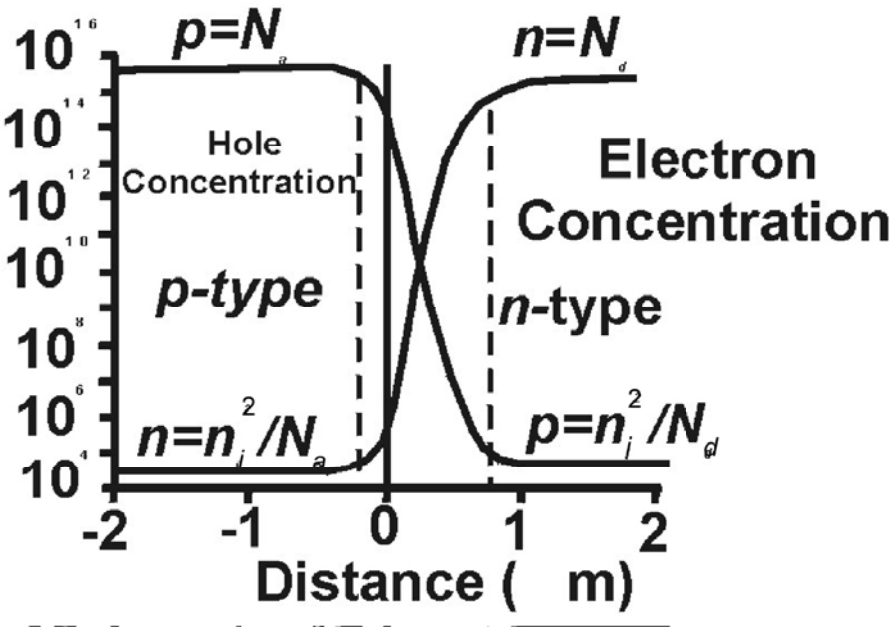
After M. Shur, Introduction to Electronic Devices, Wiley (1996)

p-n junction isolation

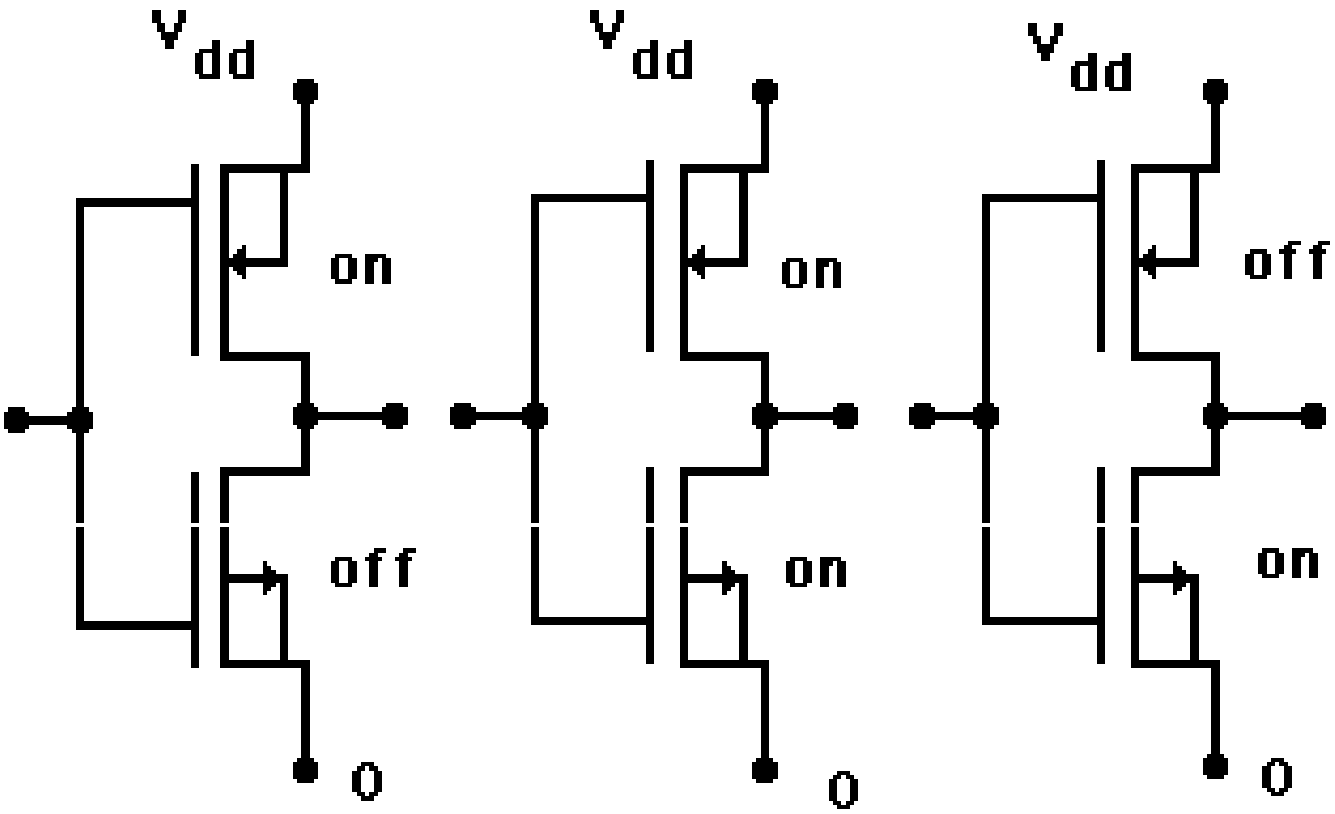






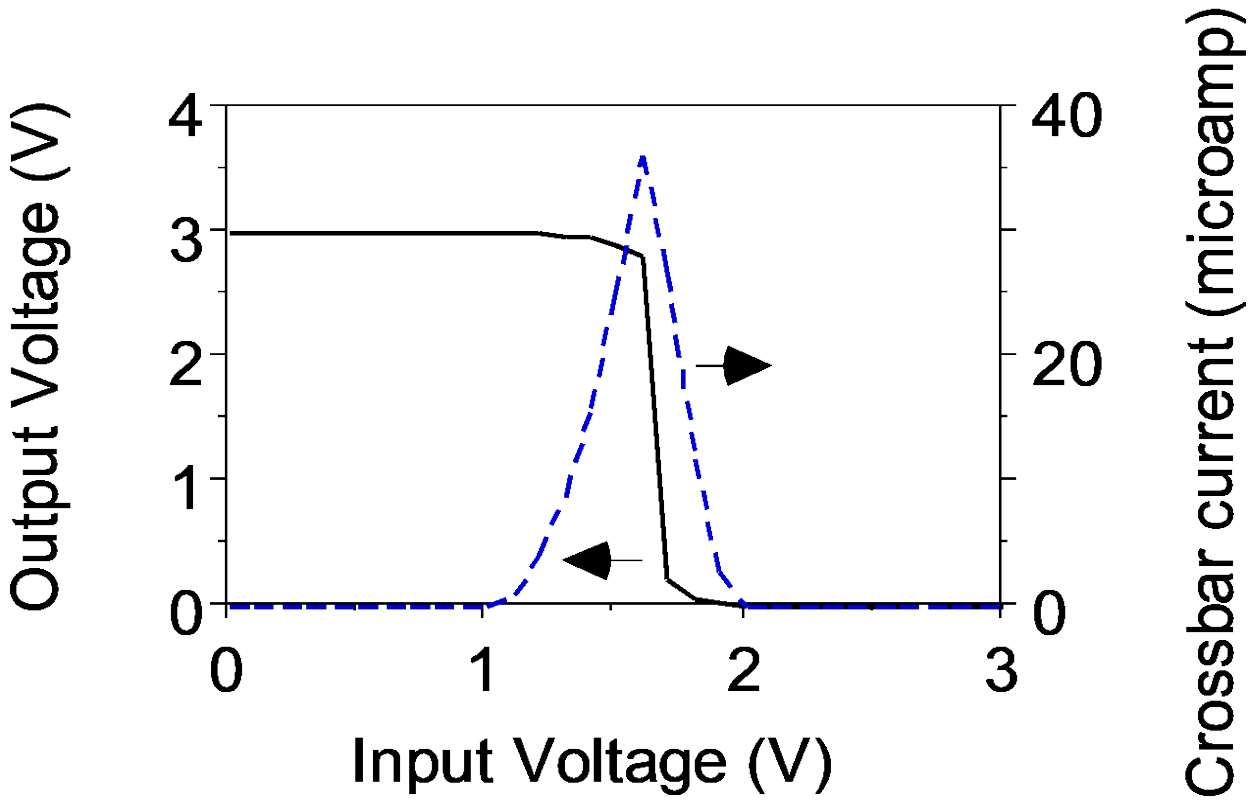


CMOS INVERTER



From M. S. Shur, Physics of Semiconductor devices, Prentice Hall, 1990)

Output Voltage And Crossbar Current



From M. S. Shur, Physics of Semiconductor devices, Prentice Hall, 1990)

Other FETs

BICMOS

HFETs

a-Si TFTs

poly-Si TFTs

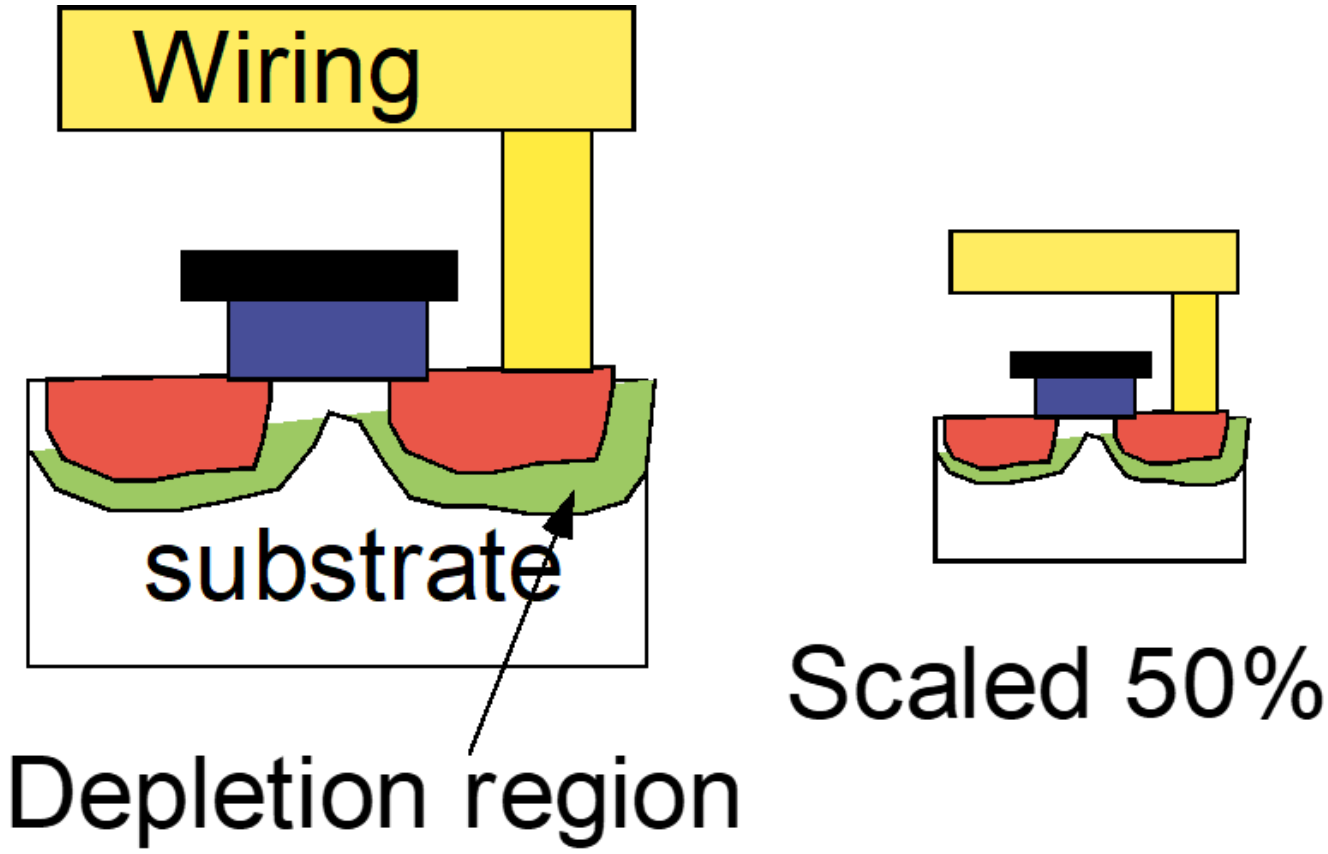
MOS Controlled Thyristors

Vertical FETs

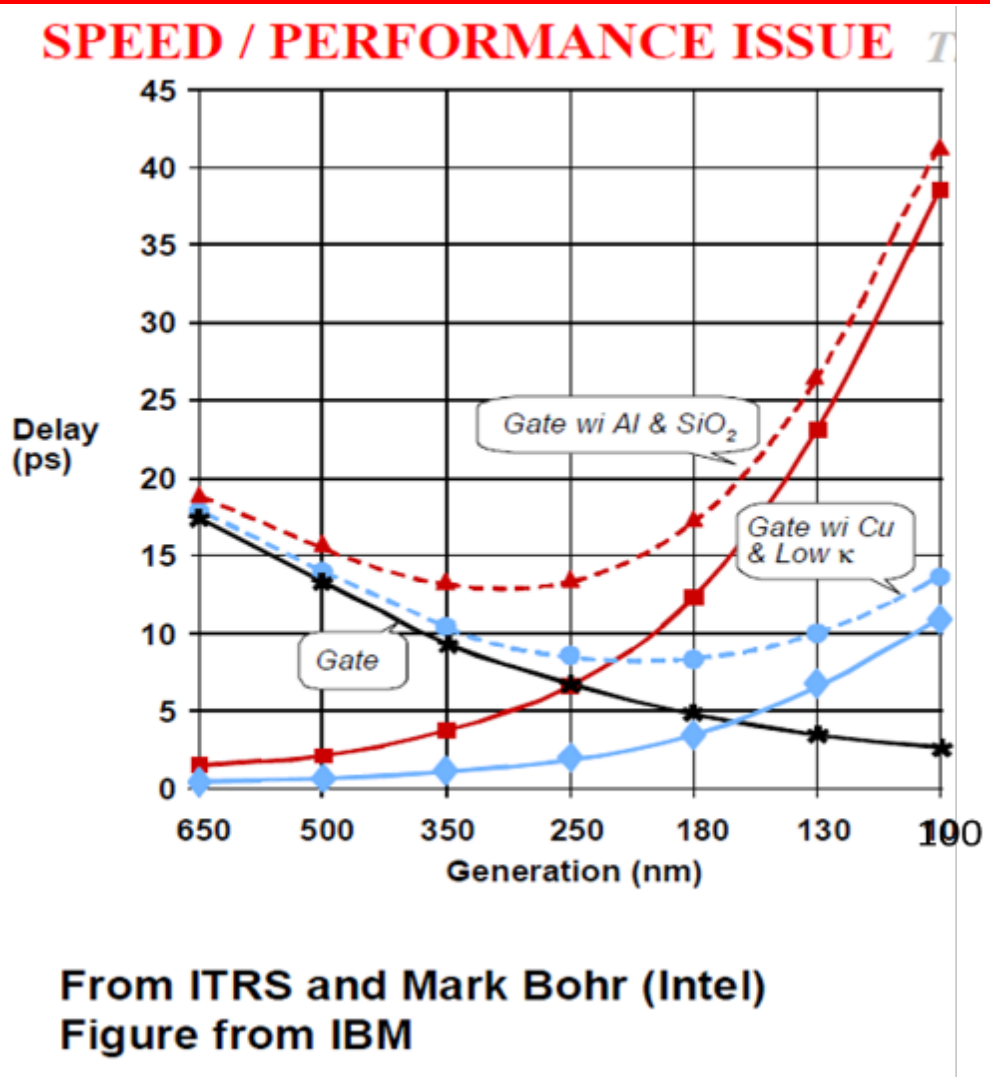
Ballistic FETs

NERFETs

SCALING

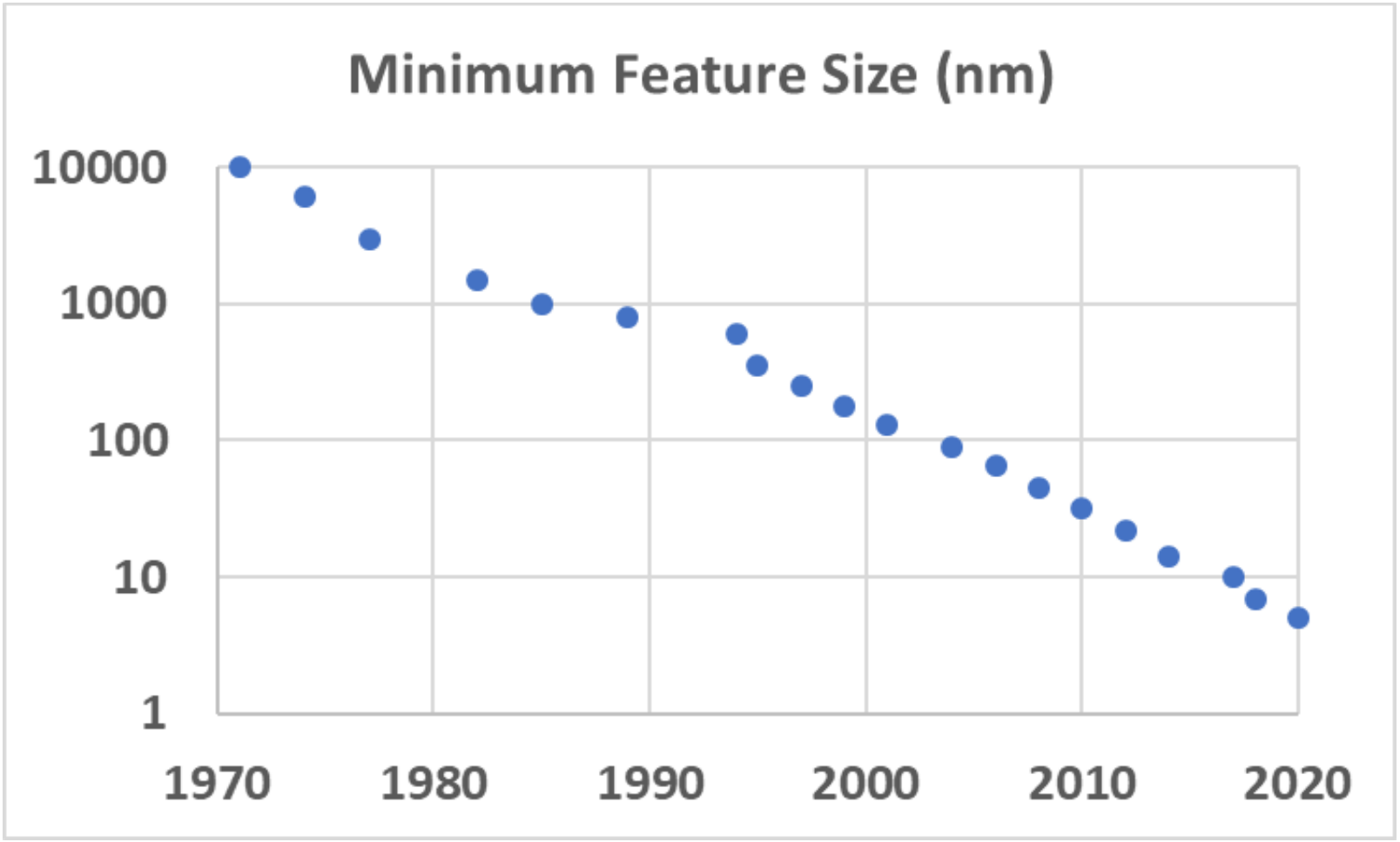


Interconnects and Contacts Problems



From ITRS and Mark Bohr (Intel)
Figure from IBM

Minimum Feature Size (1971 – 2020)

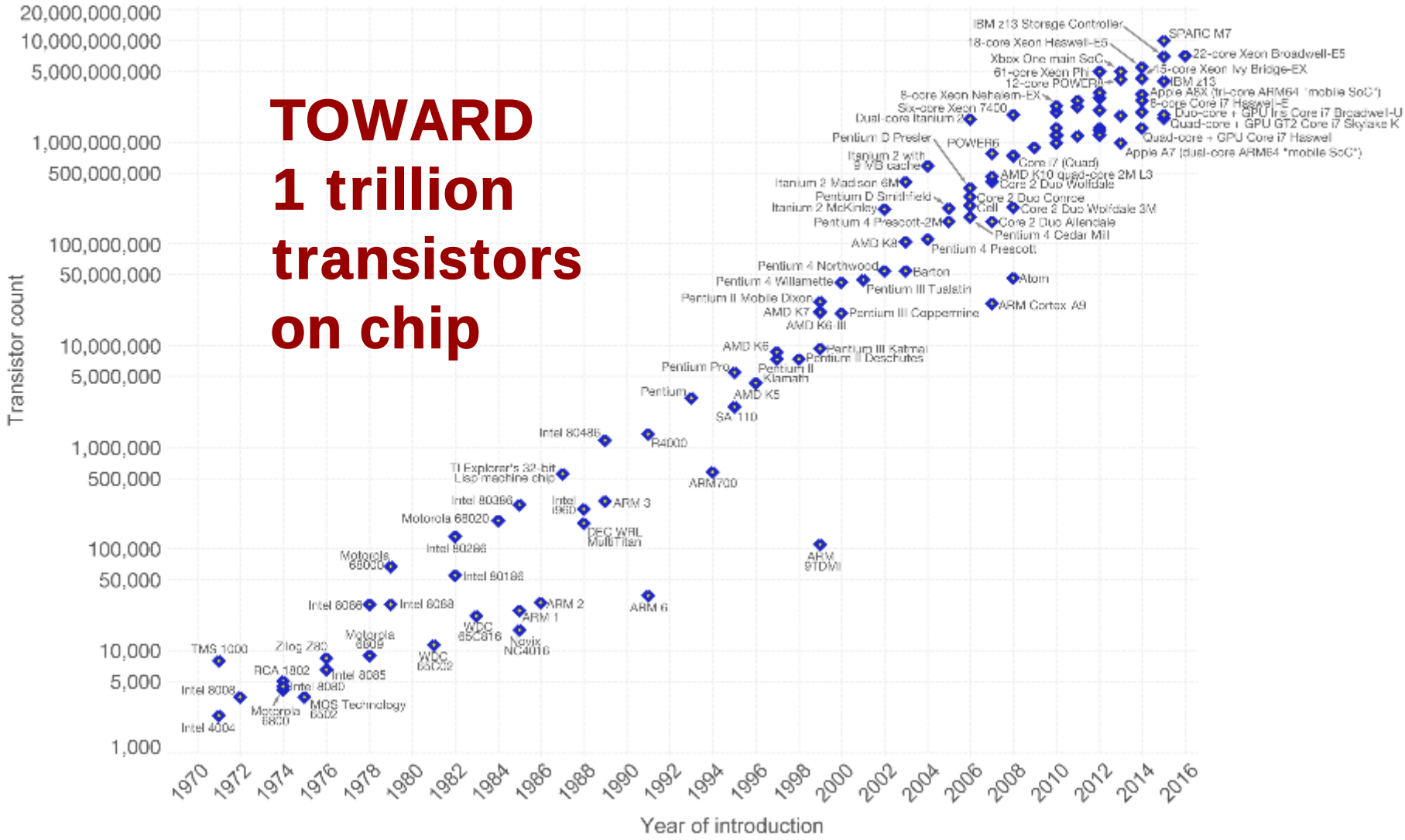


Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.

TOWARD 1 trillion transistors on chip



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

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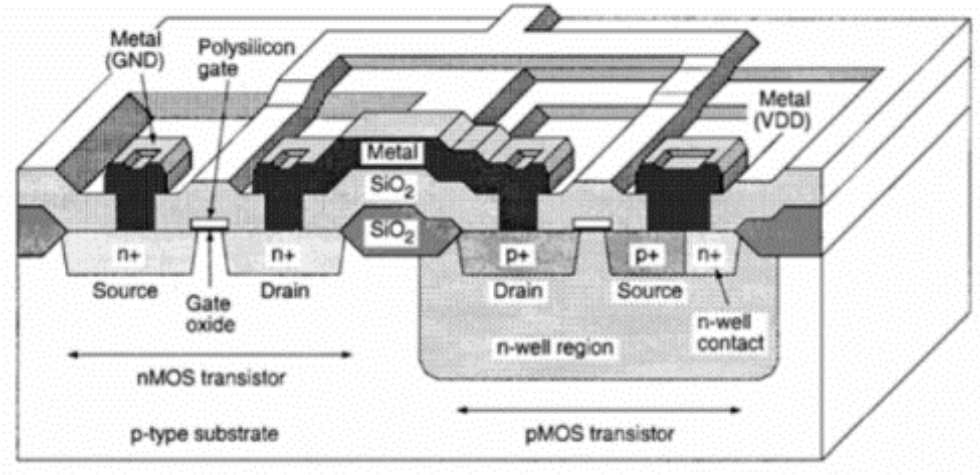
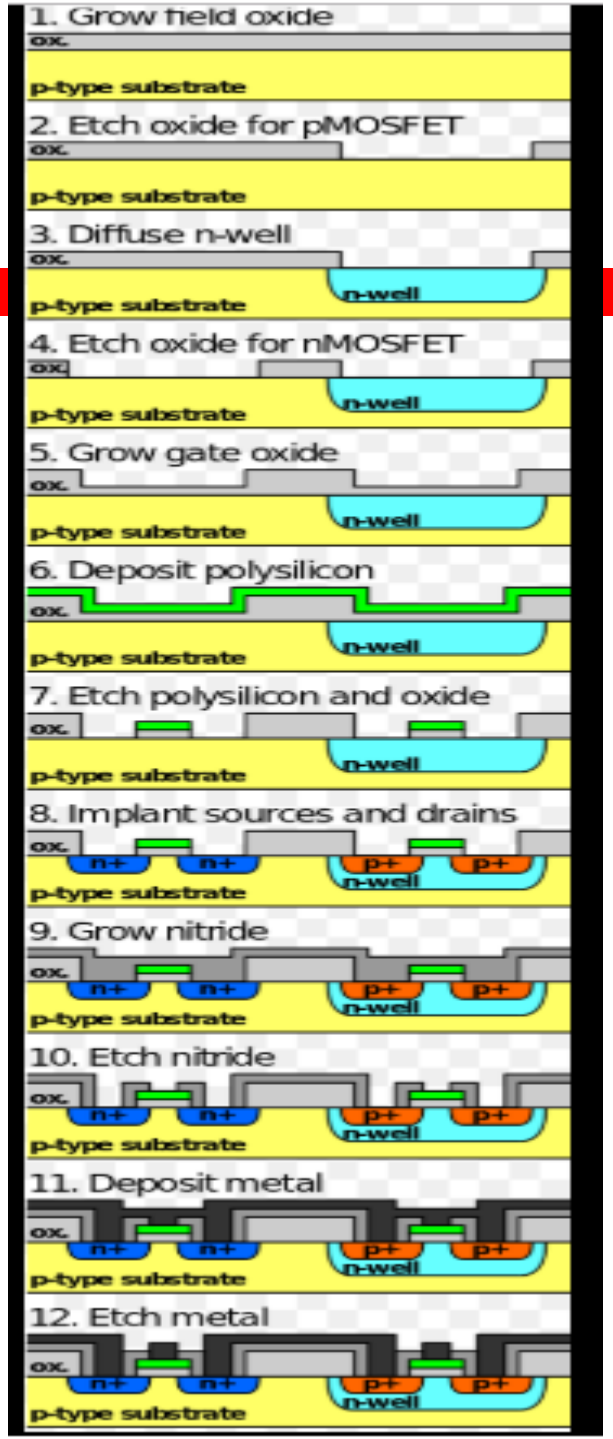
Making MOSFETs

- Step 1: Logic Design (Boolean algebra)
- Step 2: Circuit Design
- Step 3: Layout Design
- Step 4 Mask Making
- Step 5 Fabrication
- Step 6: Wafer Probing, Scribing and dicing
- Step 7: Die Attachment, Wire Bonding, Encapsulation
- Step 8: Testing



Fabrication

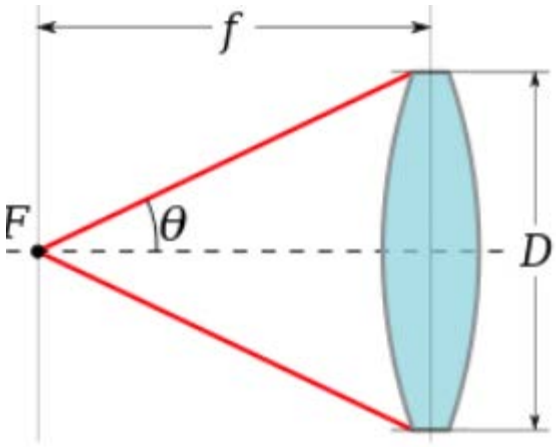
- Oxidation
  - Dry: lower rate; higher quality
  - Wet: higher rate; lower quality
- Deposition
- Implantation/diffusion
- Etch (dry and wet etch)



Photolithography

- Covers of the substrate with photoresist
- Selectively expose using masks (70 to 90 masks)
- Develops the photoresist to define the patterns

$$C_D \approx k_1 \frac{2\lambda f}{nD}$$



C_D – critical dimension

k_1 – process related factor (~0.4)

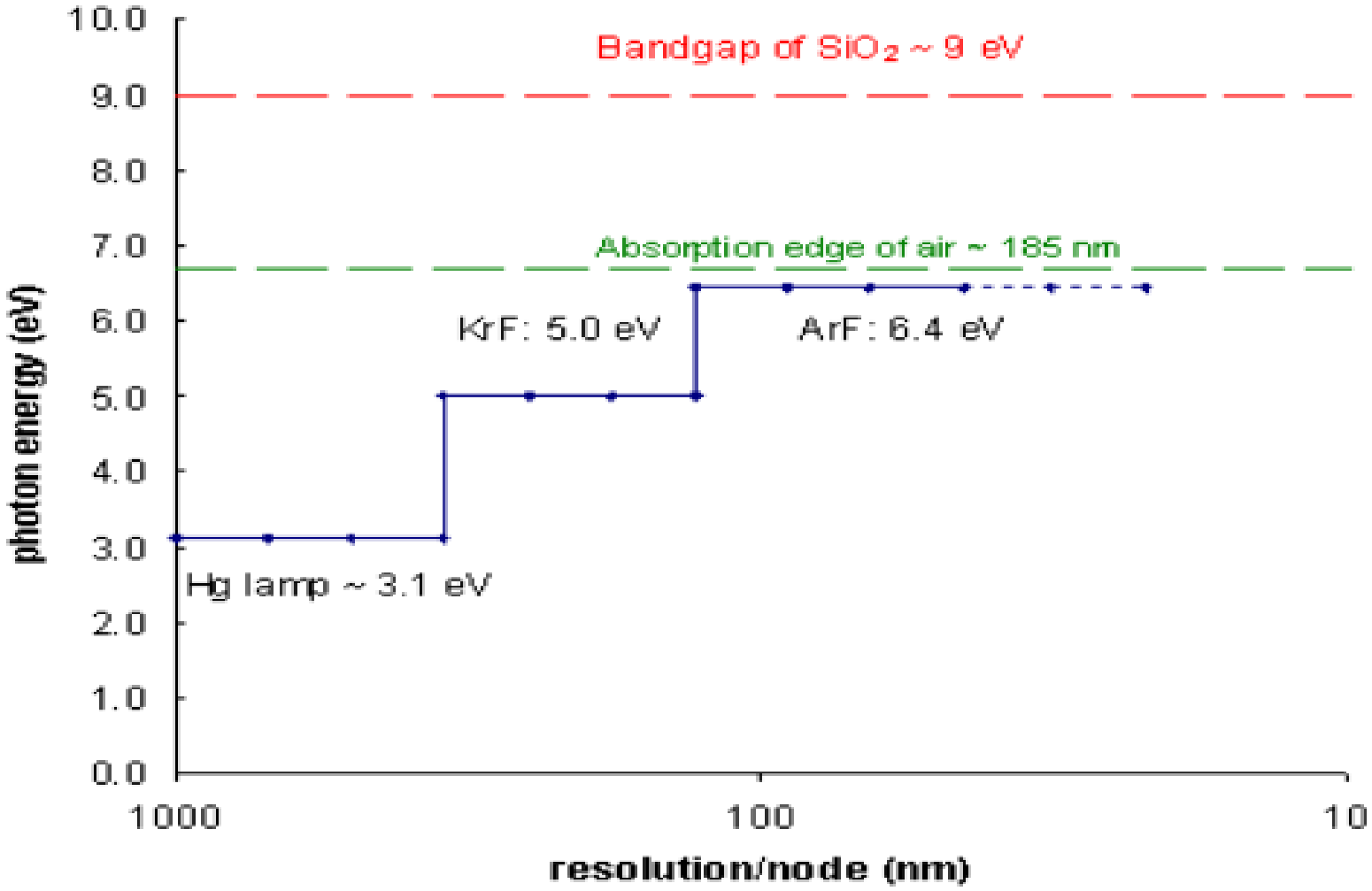
λ – wavelength of light

n – index of refraction

D – lens diameter

f – f-number

Using UV light



EUV Laser

J. Hruska ,EUV Integration at 5nm Still Risky, With Major Problems to Solve, 3/6/2018, https://www.extremetech.com/

Global Foundries Stops All 7nm Development: To Focus on Specialized Processes

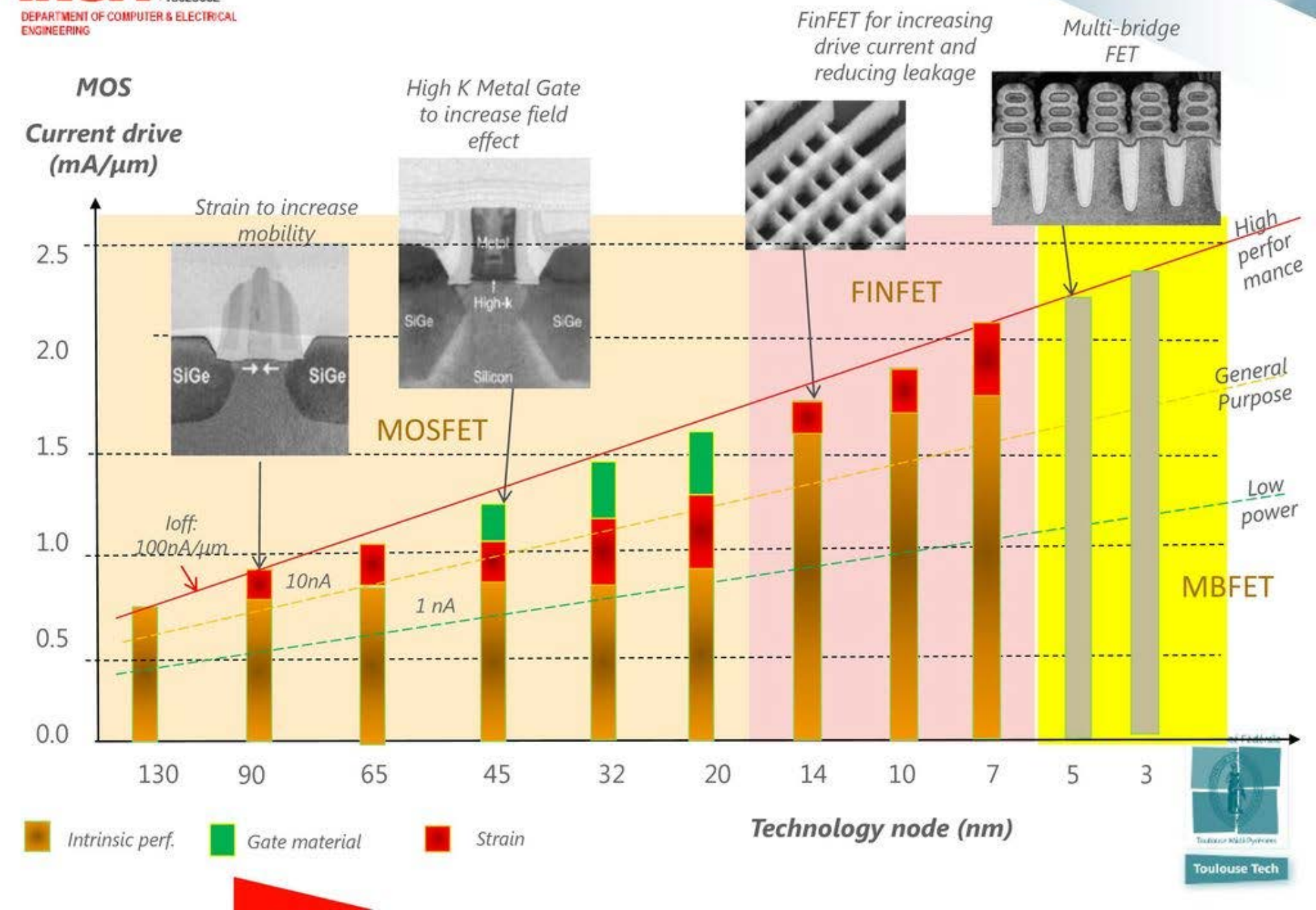
20 billion dollars invested by Mudalaba Investment Company,

Abu Dhabi

by Anton Shilov & Ian Cutress https://www.anandtech.com/, 8/27/2018

INSA NATIONAL INSTITUTE OF APPLIED SCIENCES TOULOUSE
DEPARTMENT OF COMPUTER & ELECTRICAL ENGINEERING

ROADMAP TO 3-NM



Toulouse Tech

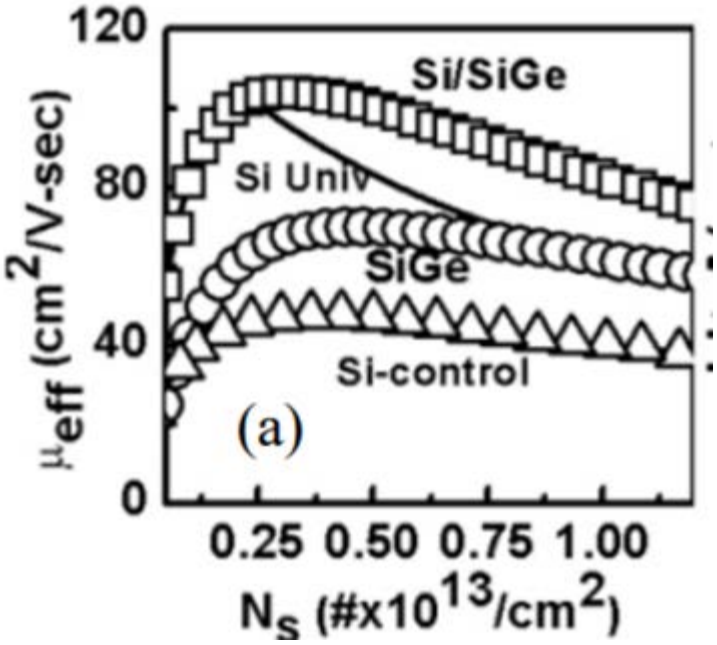
Evolutionary scaling down to 130 nm

- 130 nm

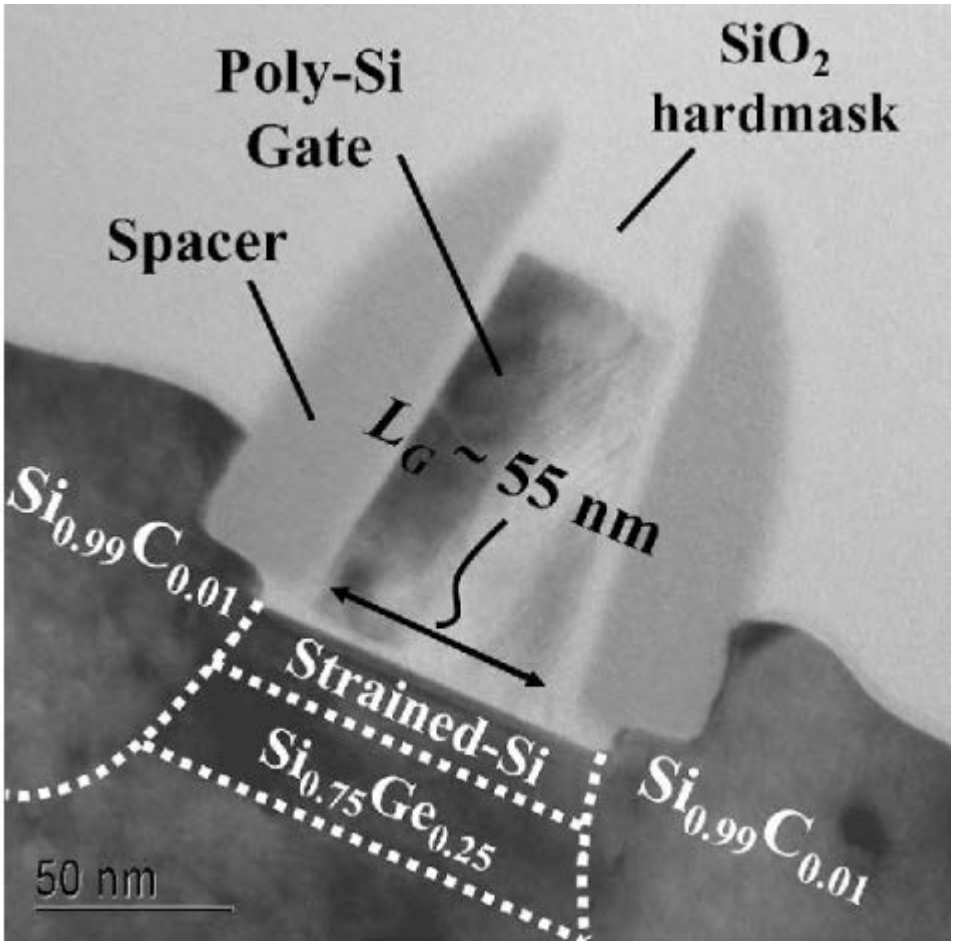
Motorola PowerPC 7447 and 7457 2002

90 nm and below strained Si-SiGe to increase mobility

Up to 4.17% lattice mismatch

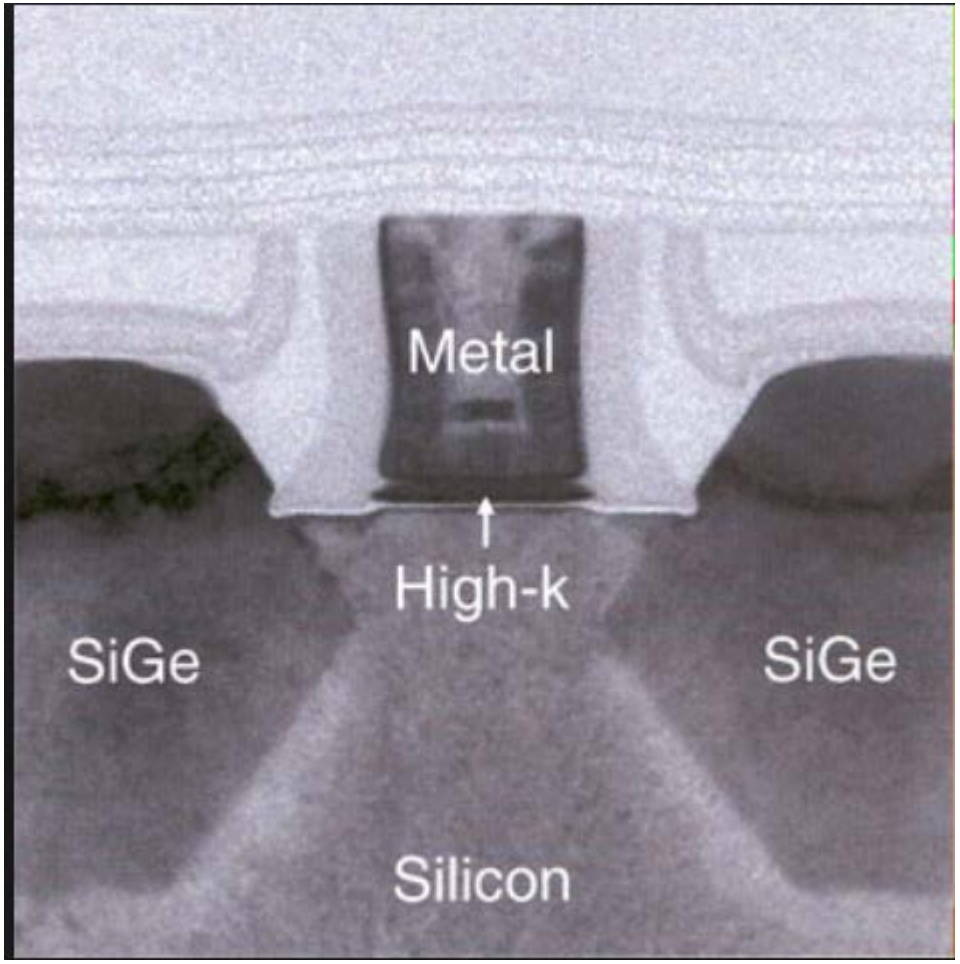


S. Deora, A. Paul, R. Bijesh, J. Huang, G. Klimeck, G. Bersuker, et al. Intrinsic reliability improvement in biaxially strained SiGe p-MOSFETs IEEE Electron Dev Lett, 32 (3) (2011), pp. 255-257

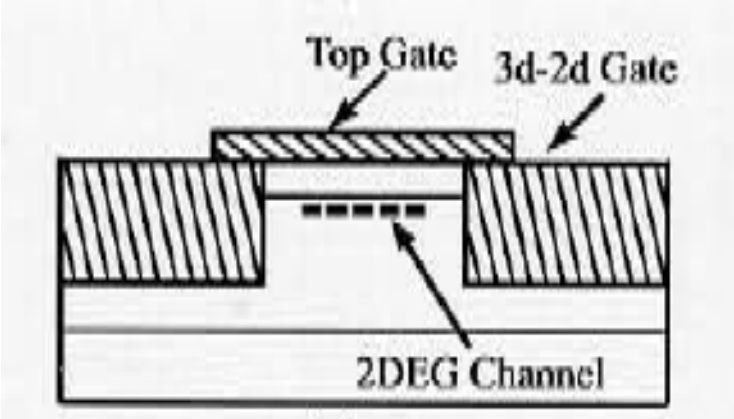


K.-W. Ang, J. Lin, C.-H. Tung , N. Balasubramanian, G. S. Samudra and Y. C. Yeo, IEEE Trans. ED, Vol. 55, pp. 850-857 (2008)

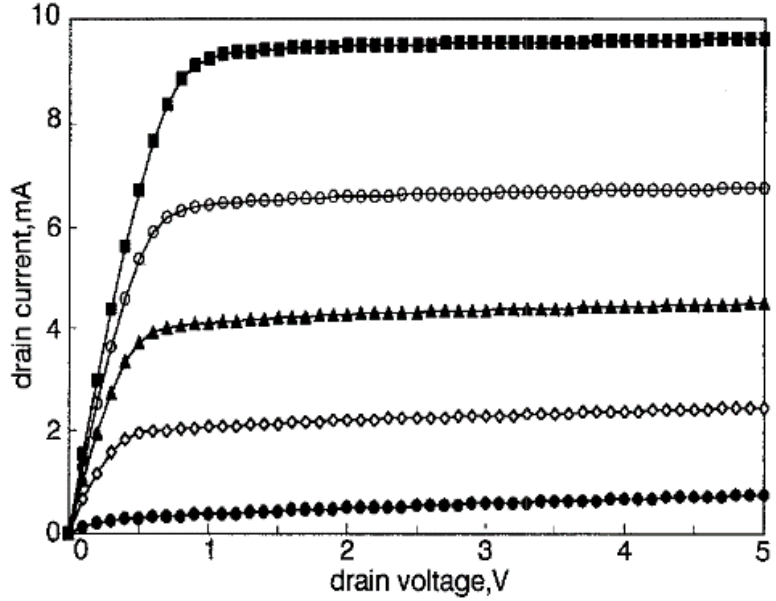
65 nm down to 20 nm High K dielectric

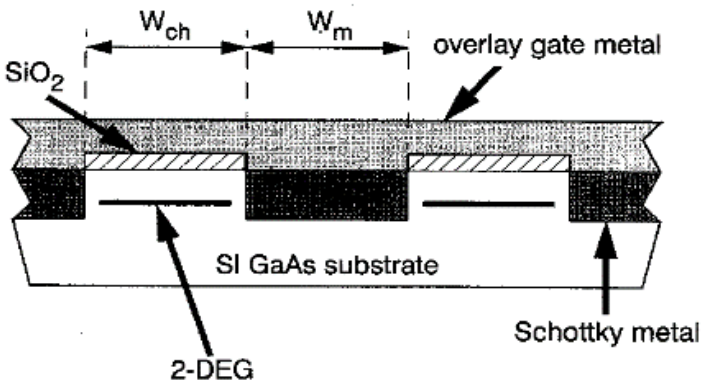


1998 coaxial HD FET (FINFET prototype)



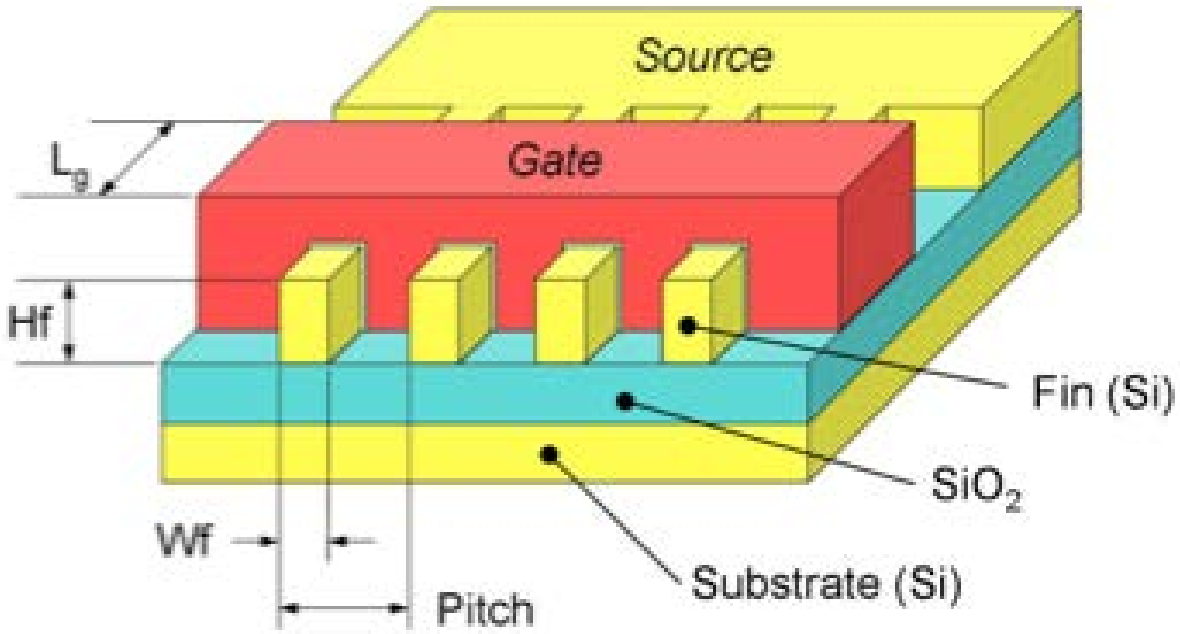
Ji.-Q. Lu, M. J. Hurt, W. C. B. Peatman, and M. S. Shur, Heterodimensional Field Effect Transistors for Ultra Low Power Applications, GaAs IC Symposium 20-th Annual Technical Digest, Atlanta, Georgia, 98CH36260, pp. 187-190 (1998)





W. C. B. Peatman, R. Tsai, R. M. Weikle, II, and M. S. Shur, Microwave Operation of Multi-Channel 2-D MESFET, Electronics Letters, Vol. 34, No. 10, pp. 1029-1030, 14 May, 1998

24 nm down to 7 nm: FINFET



W. Stillman, C. Donais, S. Rumyantsev, M. Shur, D. Veksler, C. Hobbs, C. Smith, G. Bersuker, W. Taylor and R. Jammy, Silicon FIN FETs as detectors of terahertz and sub-terahertz radiation, International Journal of High Speed Electronics and Systems, vol. 20, No. 1, pp. 27-42 March (2011)

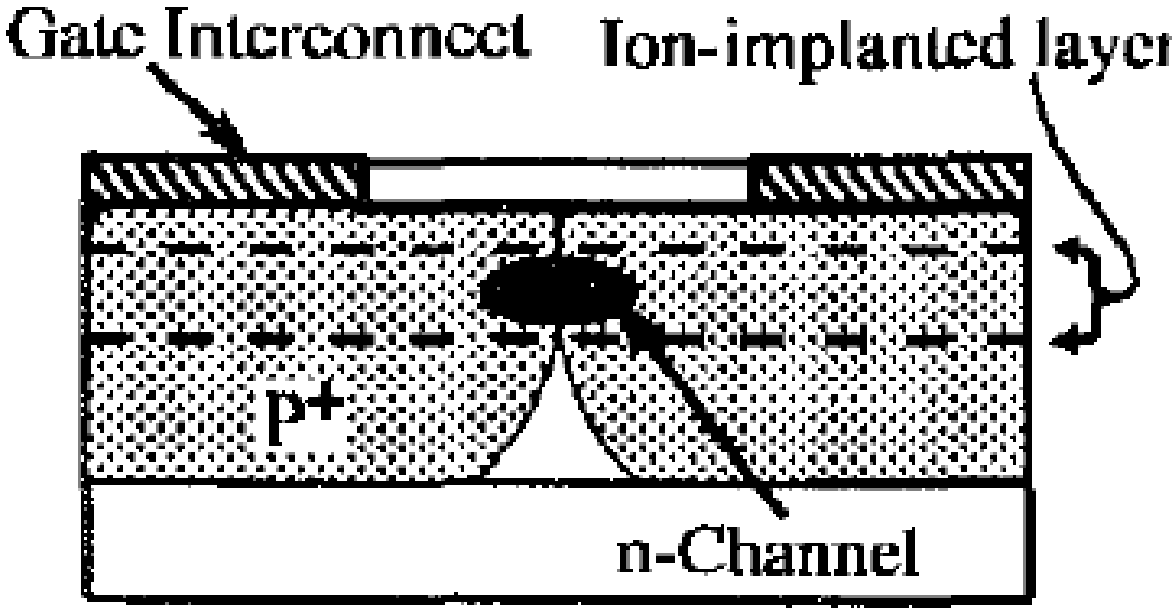
First FINFET 1999: Huang, X. et al. (1999) "Sub 50-nm FinFET: PMOS" International Electron Devices Meeting Technical Digest, p. 67. December 5–8, 1999.

INTEL: 10 nm in iPhone X

Image: Intel

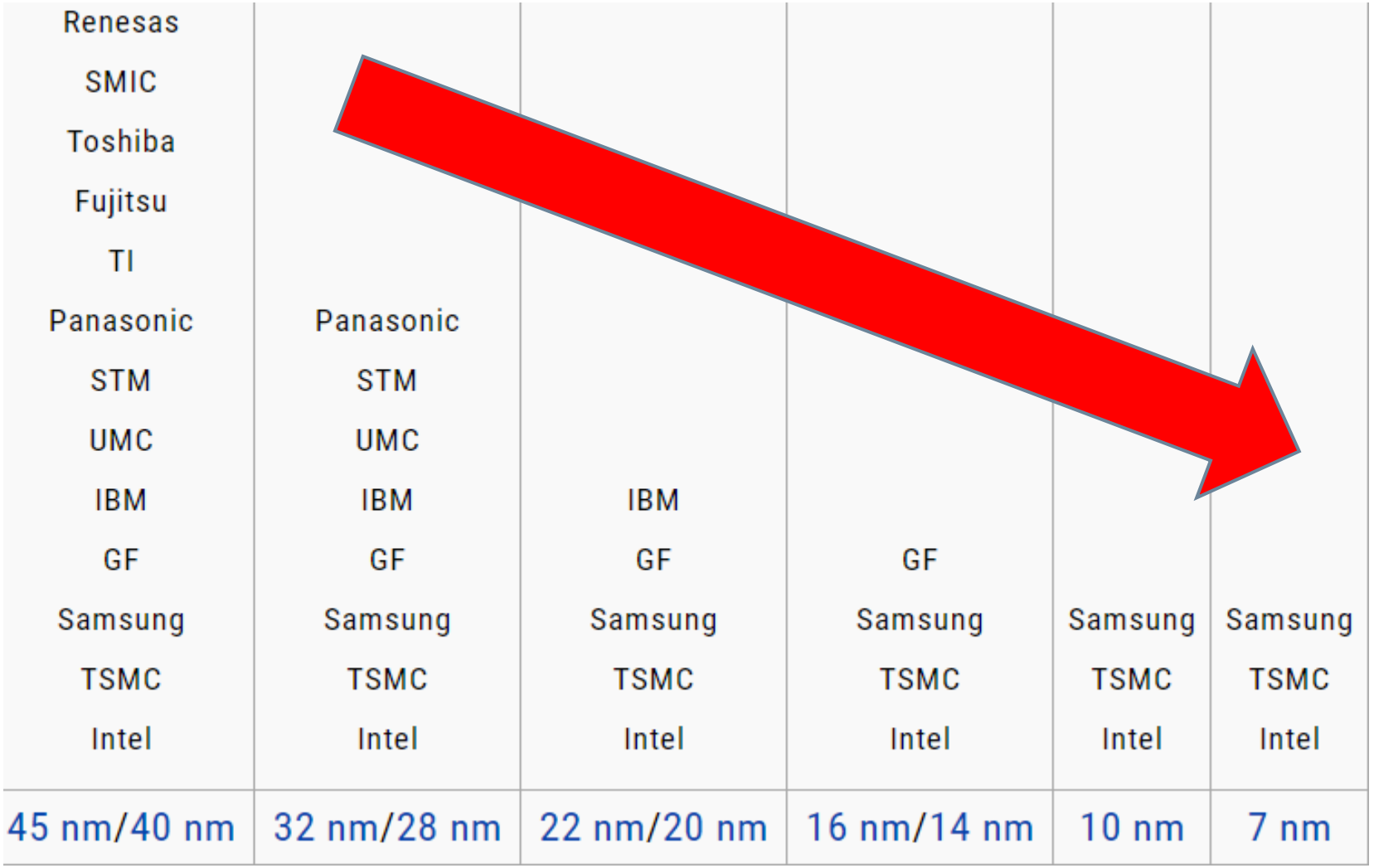
From Rachel Cortland, posted 30 March 2017
https://spectrum.ieee.org/nanoclast/semiconductors/processors/intel-now-packs-100-million-transistors-in-each-square-millimeter

5 nm to 3 nm: All Around FET



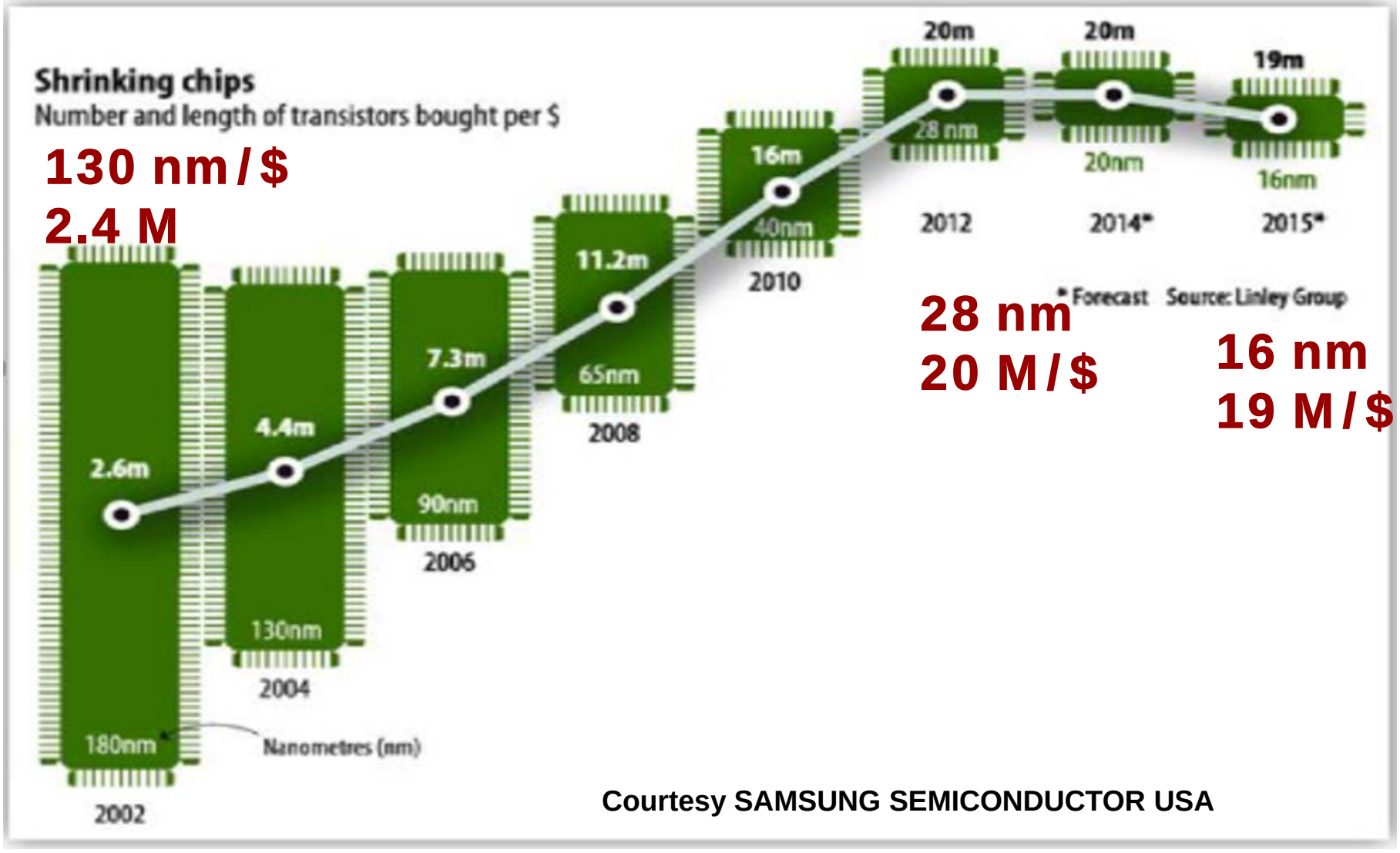
FIRST PROPOSED in 1998: Ji.-Q. Lu, M. J. Hurt, W. C. B. Peatman, and M. S. Shur, Heterodimensional Field Effect Transistors for Ultra Low Power Applications, GaAs IC Symposium 20-th Annual Technical Digest, Atlanta, Georgia, 98CH36260, pp. 187-190 (1998)

Who is left at 7 nm?



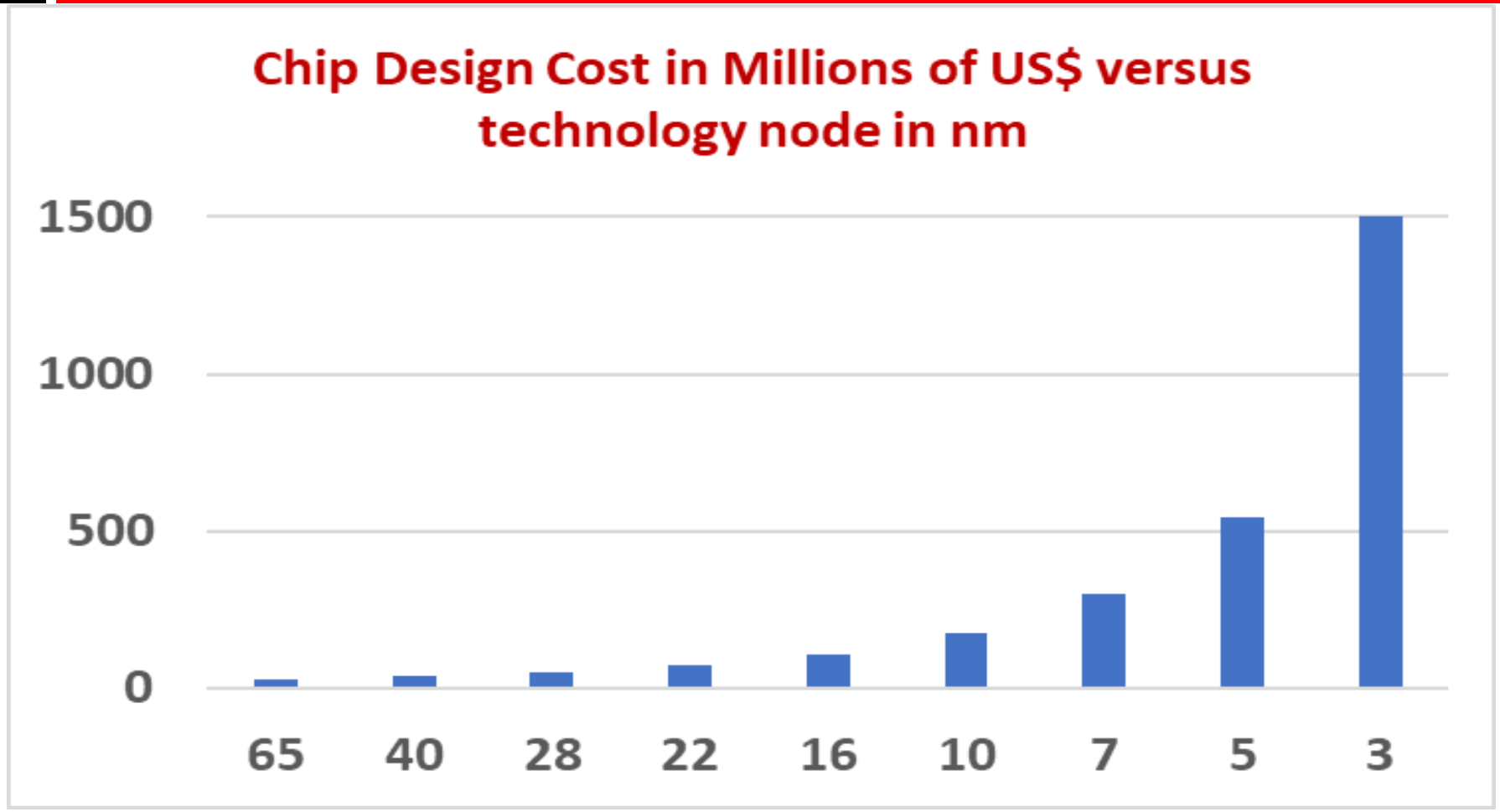
45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm
Renesas					
SMIC					
Toshiba					
Fujitsu					
TI					
Panasonic	Panasonic				
STM	STM				
UMC	UMC				
IBM	IBM	IBM			
GF	GF	GF	GF		
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel

Number of Transistors Per 1US$



Courtesy SAMSUNG SEMICONDUCTOR USA

Chip Design Cost in Millions of US$ versus technology node in nm



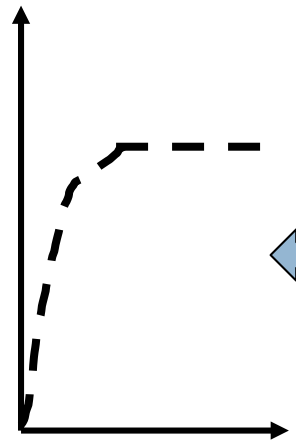
Data form: M. LaPedus, Semiconductor Engineering. https://semiengineering.com/big-trouble-at-3nm/

Collision Dominated, Overshoot, and Ballistic Transport

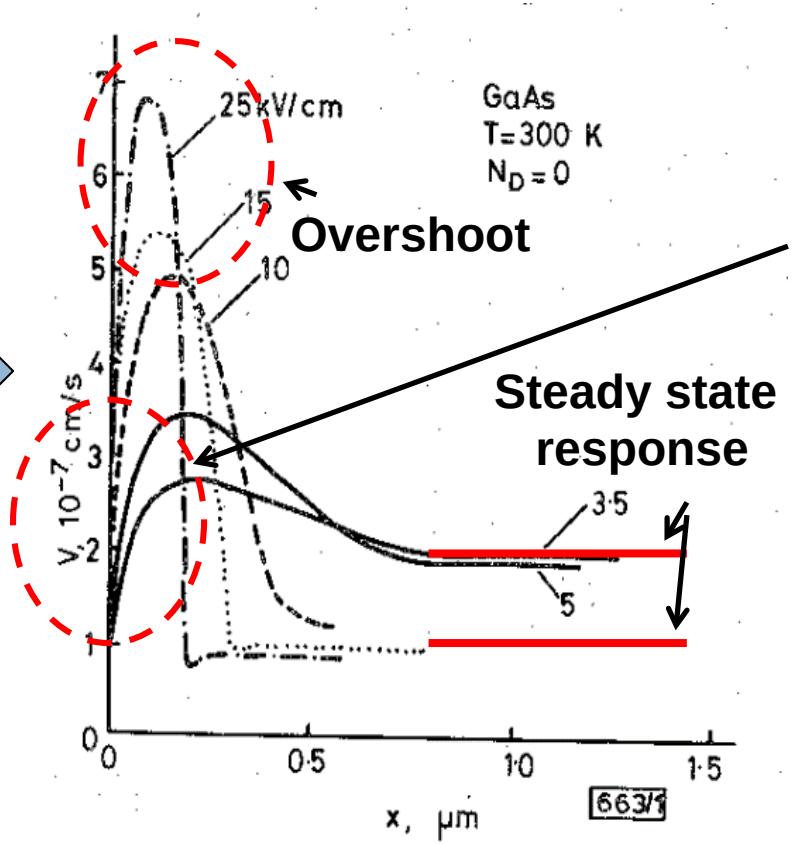
Collision dominated

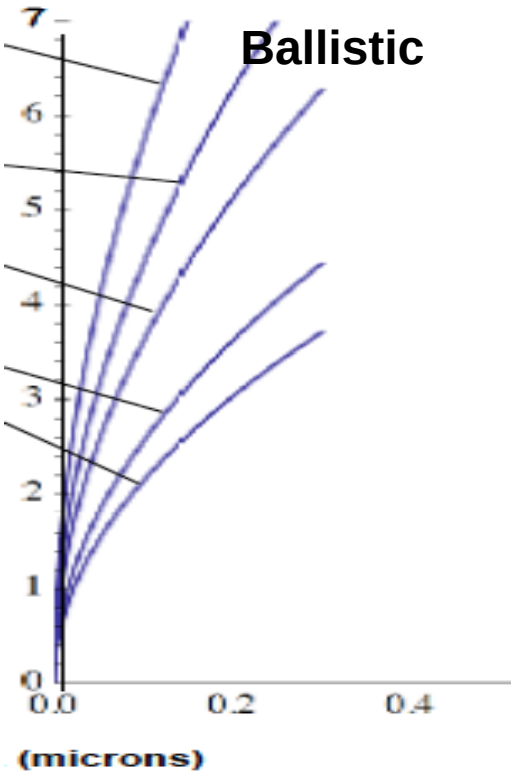
M. Shur, EL. Lett. Vol. 12, 615 (1976))

Velocity



Field



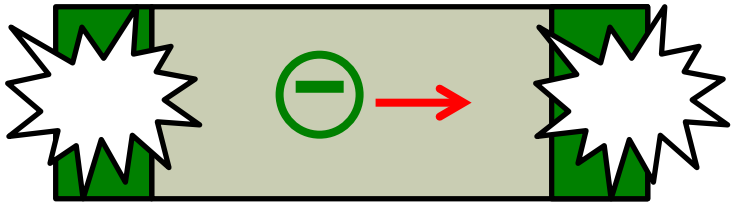


$$v = \sqrt{\frac{2qEx}{m}}$$

DC Ballistic mobility

Transit time L/v

A. A. Kastalsky and M. S. Shur, Conductance of Small Semiconductor Devices, Solid State Comm. Vol. 39, No. 6, p. 715-718 (1981)



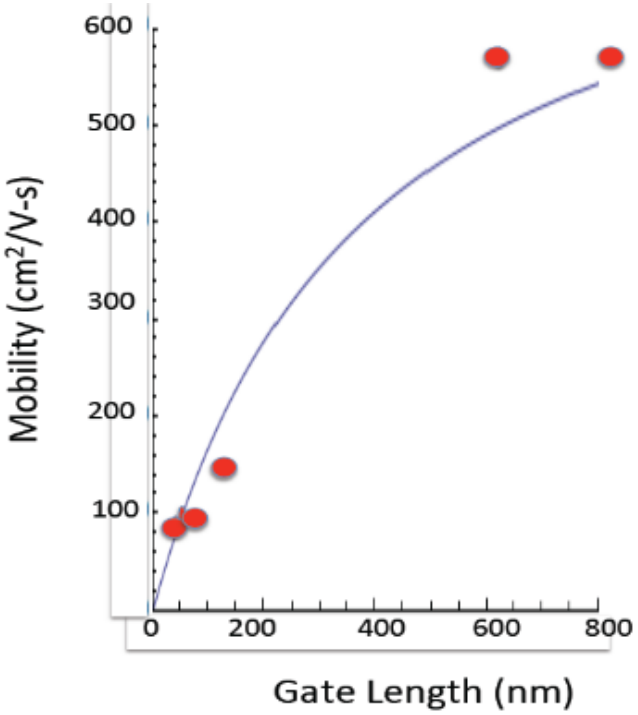
$$\mu_{bal} = \frac{e\tau_{eff}}{m};\ \tau_{eff} = \alpha\frac{L}{v};\ \mu_{bal} = \alpha\frac{eL}{mv}$$

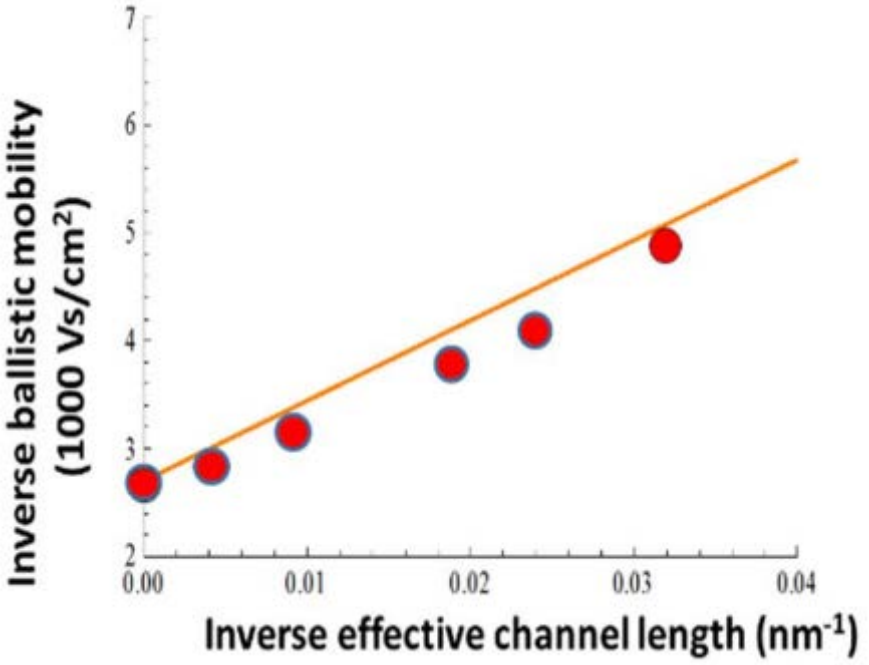
Values of constant α and thermal and Fermi velocities for 2D and 3D geometries (see Eq. (1)). k_B is the Boltzmann constant, T is temperature (K).

Geometry	Degenerate	Non-degenerate
2D	$\alpha = \frac{2}{\pi}$ $\quad v_F = \frac{\hbar}{m}\sqrt{2\pi n_s}$ [8]	$\alpha = \frac{1}{2}$ $\quad v_{th} = \left(\frac{\pi k_B T}{2m}\right)^{1/2}$ [4]
3D	$\alpha = 3/4$ $\quad v_F = \frac{\hbar}{m}\left(3\pi^2 n_s\right)^{3/4}$	$\alpha = \frac{2}{\pi}$ $\quad v_{th} = \left(\frac{8k_B T}{\pi m}\right)^{1/2}$ [3]

From: A. P. Dmitriev and M. S. Shur, Ballistic admittance: Periodic variation with frequency, Appl. Phys. Lett, 89, 142102, (2006);

Ballistic mobility in Si: proportional to length

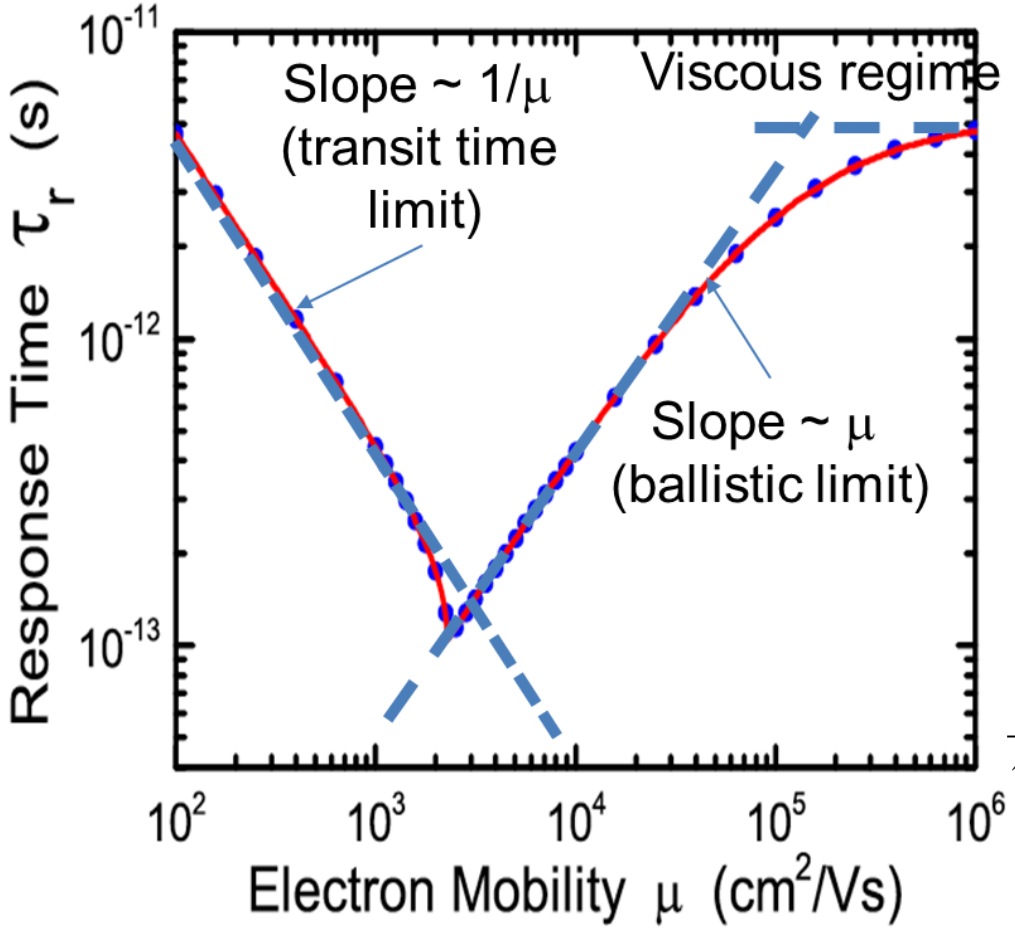




Data from W. Knap, F. Teppe, Y. Meziani, N. Dyakonova, J. Lusakowski, F. Bouef, T. Skotnicki, D. Maude, S. Rumyantsev and M. S. Shur, Appl. Phys. Lett, Vol. 85, No 4, pp. 675-677 (2004)

D. Antoniadis, IEEE Transactions on Electron Dev. Vol. 63, No 7, pp. 2650 – 2656 (2016)

Speed is in the femtosecond range



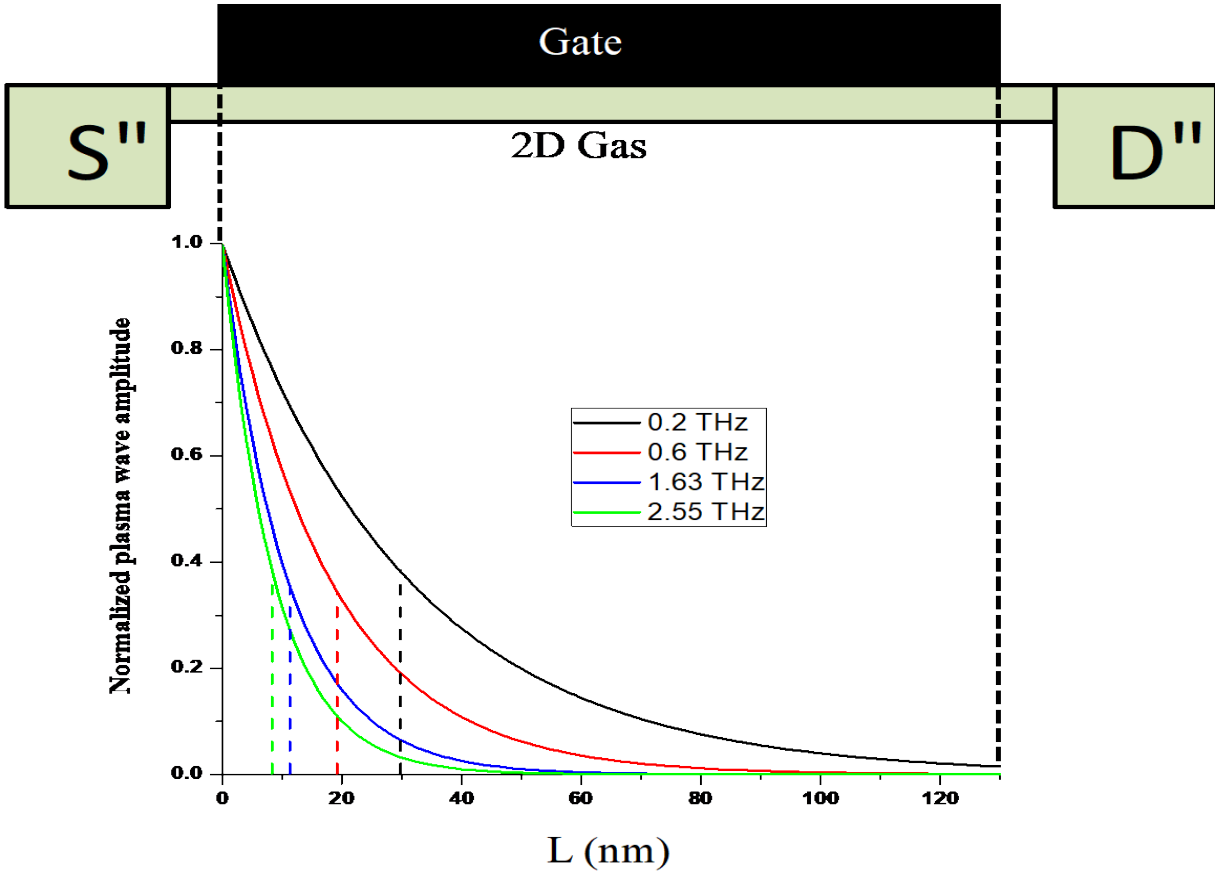
ELECTRON TRANSPORT

- **Collision dominated**
- **Ballistic**
- **Viscous regime**

$$\frac{1}{\tau_r} = Re\frac{1}{2}\left[-\left(\frac{1}{\tau}+\frac{\pi^2\nu}{4L^2}\right)+\sqrt{\left(\frac{1}{\tau}+\frac{\pi^2\nu}{4L^2}\right)-\frac{\pi^2 s^2}{L^2}}\right]$$

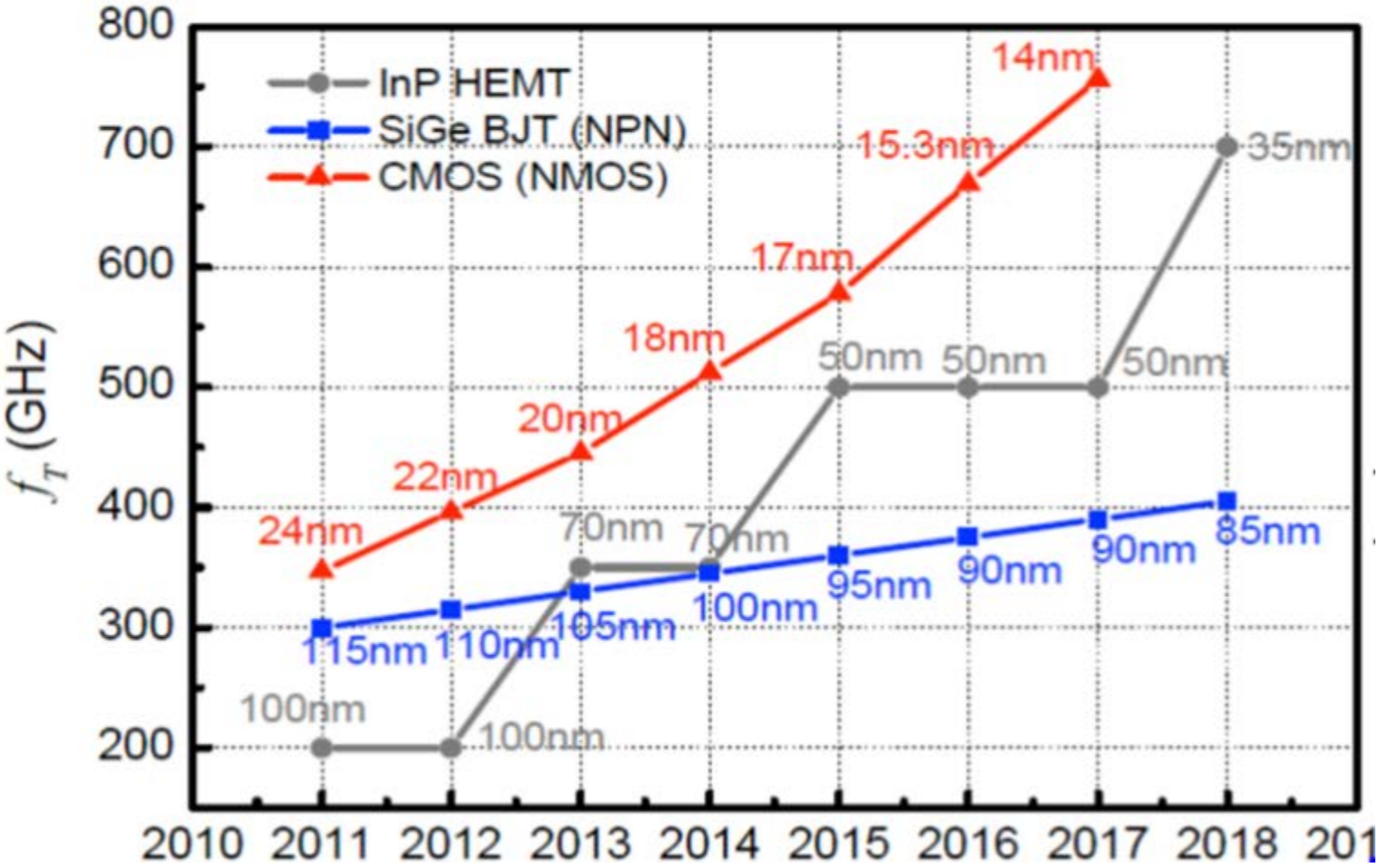
M. Shur, A. Muraviev, G. Rupper, and S. Rudin, THz Pulse Detection by Photoconductive Plasmonic High Electron Mobility Transistor with Enhanced Sensitivity, Device Research Conference (DRC) 2016

Spatial decay of overdamped plasma waves



A. Gutin, S. Nahar, M. Hella, and M. Shur, Modeling Terahertz Plasmonic Si FETs With SPICE, IEEE Trans. on Terahertz Science and Technology, issue 99. Pp. 1-5, (2013)

Si CMOS operate in THz range



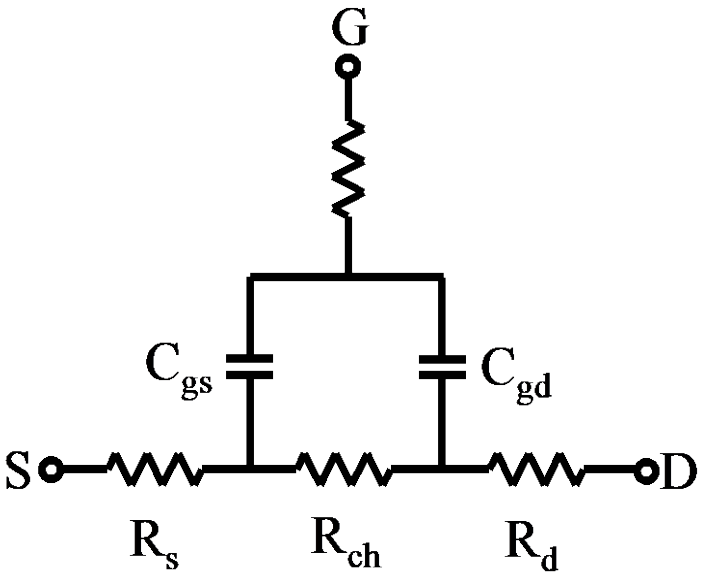
From International Technology Roadmap for Semiconductors (ITRS) http://public.itrs.net

Problems to solve and Applications

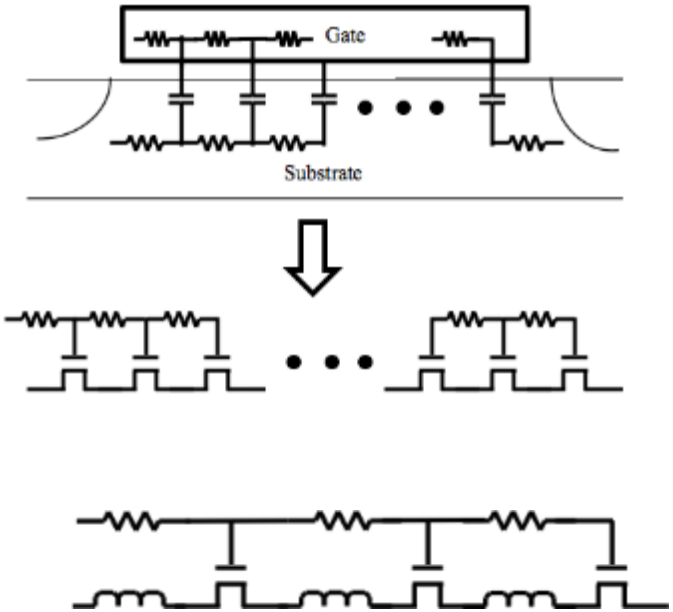
Problem	Solution	Benefits
Foundry models work up to 30 GHz for technology that works up to 300 GHz or higher	Use, improve, and maintain THz SPICE validated by foundry models	Dramatically reduced design cost, more efficient robust design, for sub-THz range using Si technology
THz applications are limited by technology cost	Use 22 nm and under Si technology and decrease the design cost	Multibillion market in THz communications, robotics. Sensing, IoT, security, biomedicine Education, industrial control, VLSI testing

Conventional SPICE and THz SPICE

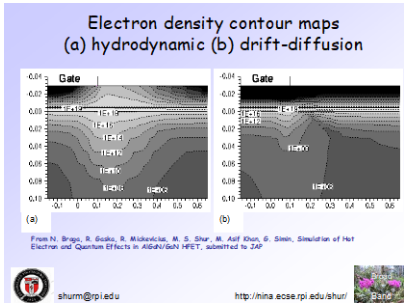
Conventional SPICE



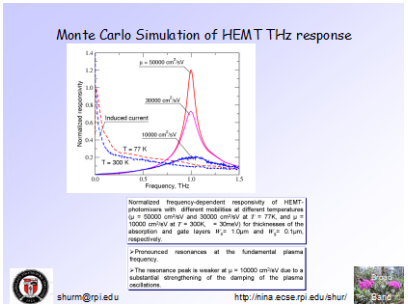
THz SPICE



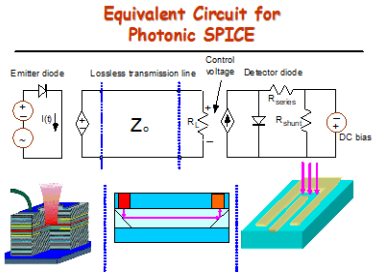
Modeling and Simulation of Advanced Semiconductor Devices



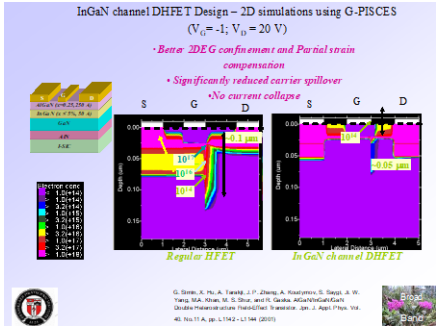
Device Physics



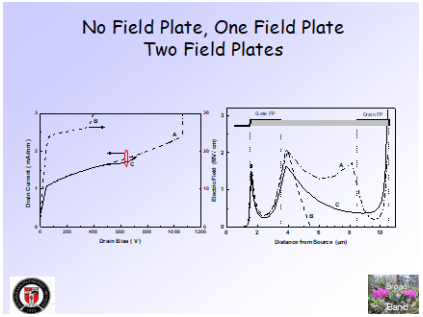
Monte Carlo Modeling



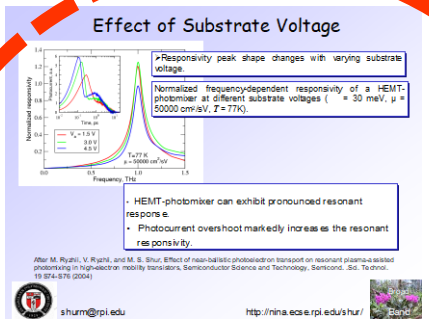
Modeling of Electronic/ Photonic VLSI



Modeling for Device Optimization

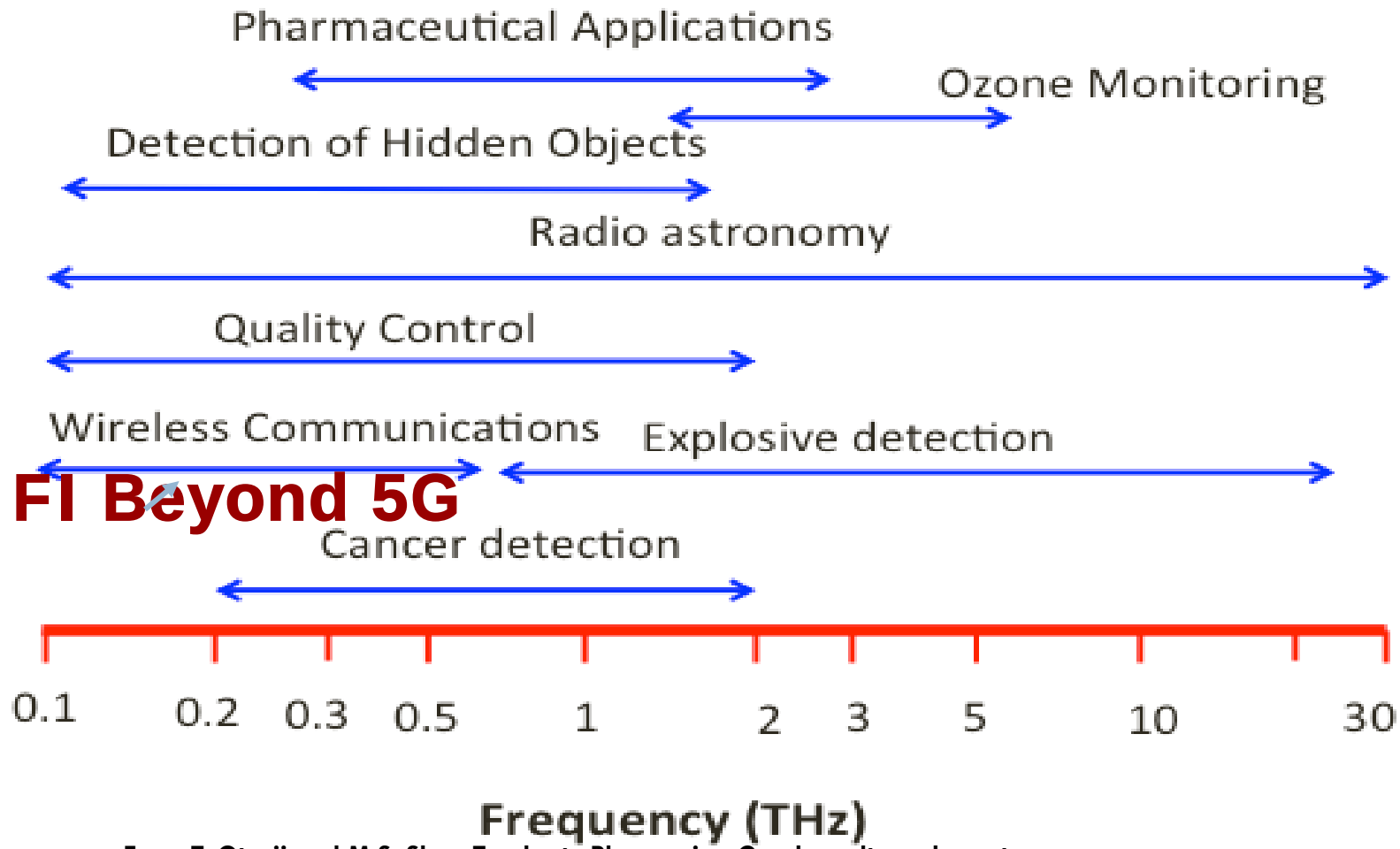


Modeling for Device Design



Modeling for New THz Devices

THz Applications



WI FI Beyond 5G

From T. Otsuji and M.S. Shur, Terahertz Plasmonics. Good results and great expectations, IEEE Microwave Journal October 2014

Cyber security problem?

Super Micro China super spy chip super scandal: US Homeland Security, UK spies back Amazon, Apple denials

Officials: Not saying Bloomberg was wrong, we just believe biz saying Bloomberg was wrong

By Richard Chirgwin 8 Oct 2018 at 06:01 90 SHARE ▼

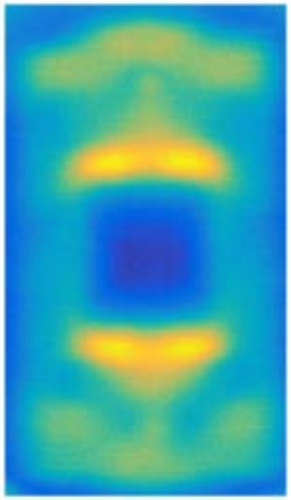
UPDATED UK spymasters and US Homeland Security officials have supported Western tech companies' denials that Chinese agents were able to smuggle hidden surveillance chips into Super Micro servers.

THz testing of VLSI

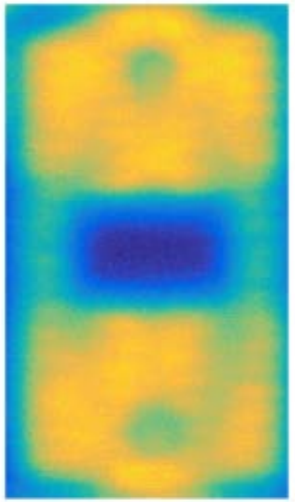
Optical

Counterfeit

Genuine



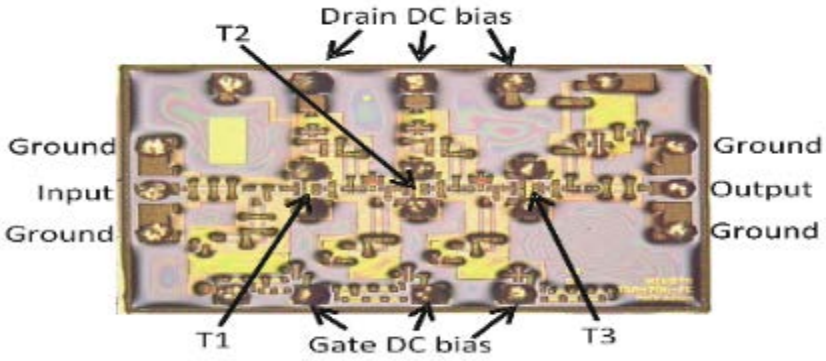
THz



From K. Ahi, S. Shahbazmohamadi, and N. Asadizanjani, "Quality control and authentication of packaged integrated circuits using enhanced-spatial-resolution terahertz time-domain spectroscopy and imaging," Optics and Lasers in Engineering, vol. 104, pp. 274–284, 2018

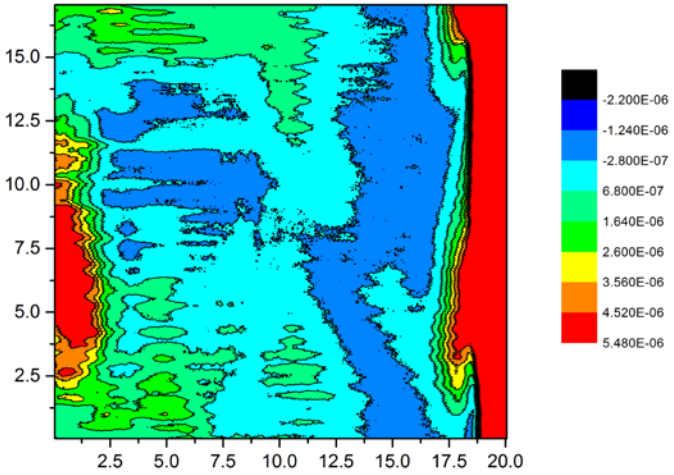
Testing VLSI under bias

MMIC under test

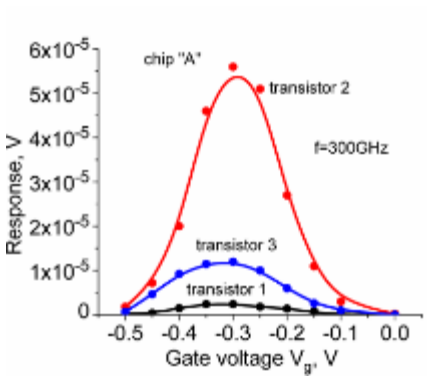


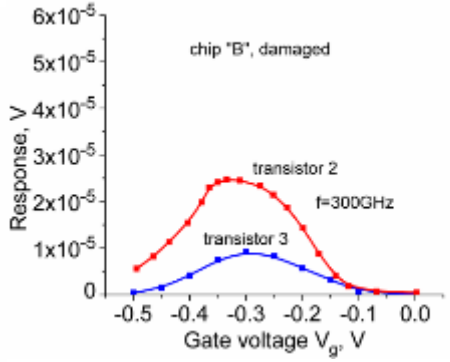
Conventional

THz testing



Plasmonic signals at pins





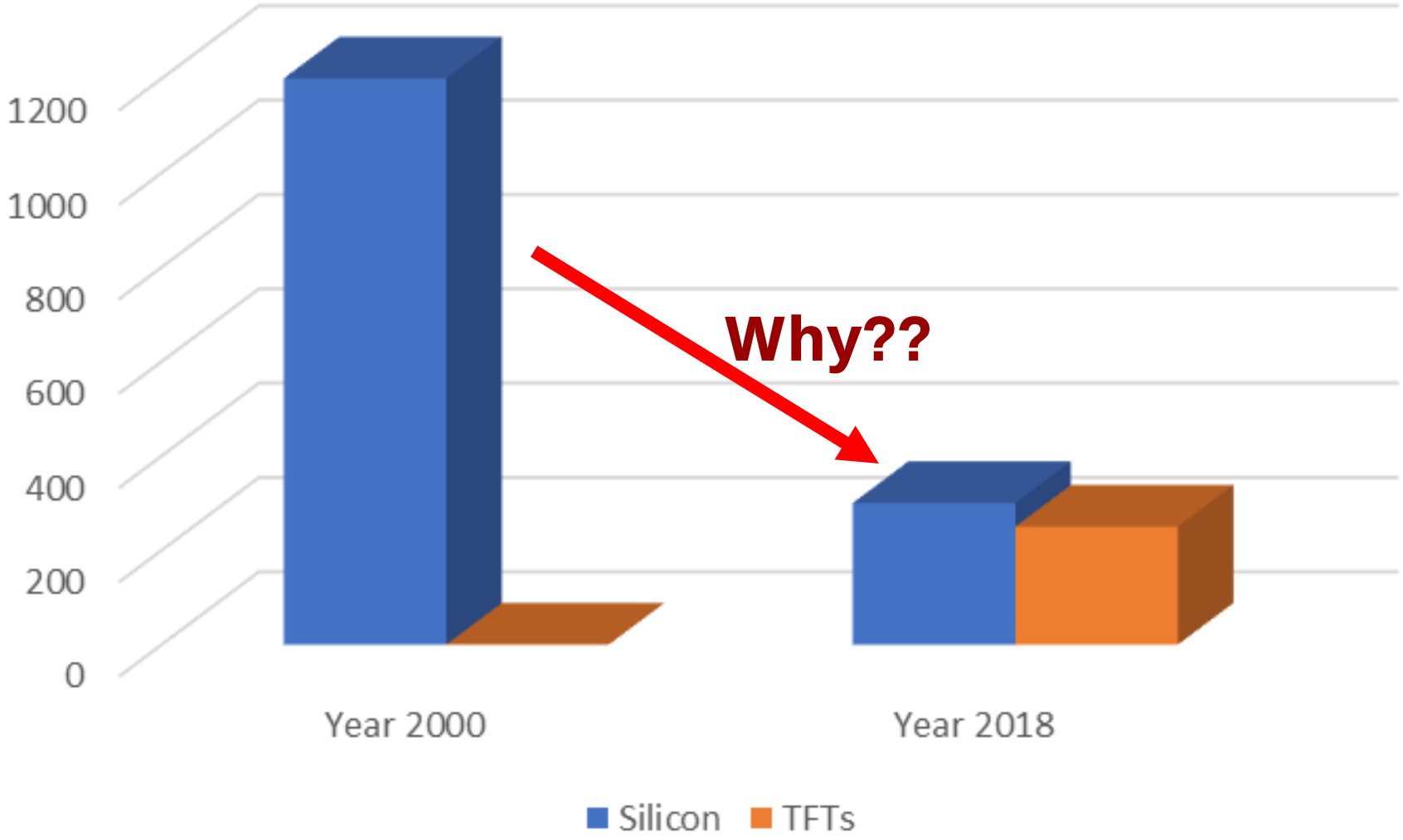
Virgin

Damaged

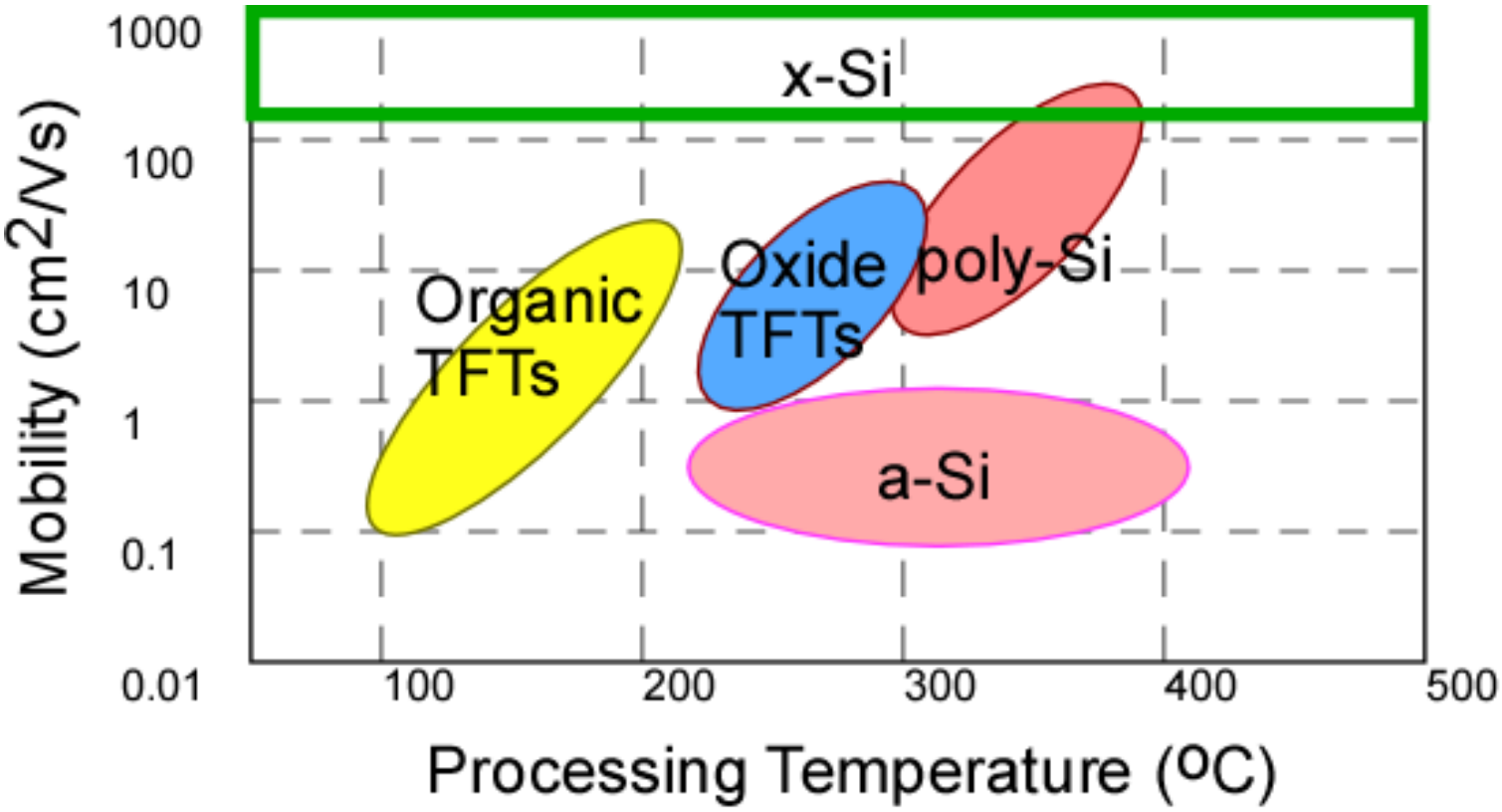
Sources S. S. Rumyantsev, A. Muraviev, S. Rudin, G. Rupper, M. Reed, J. Suarez and M. Shur, Terahertz Beam Testing of Millimeter Wave Monolithic Integrated Circuits, IEEE Sensors Journal, IEEE Sensors J., Vol. 17, No. Sep. 1, pp. 5487-5490 (2017)

THIN FILM TRANSISTORS

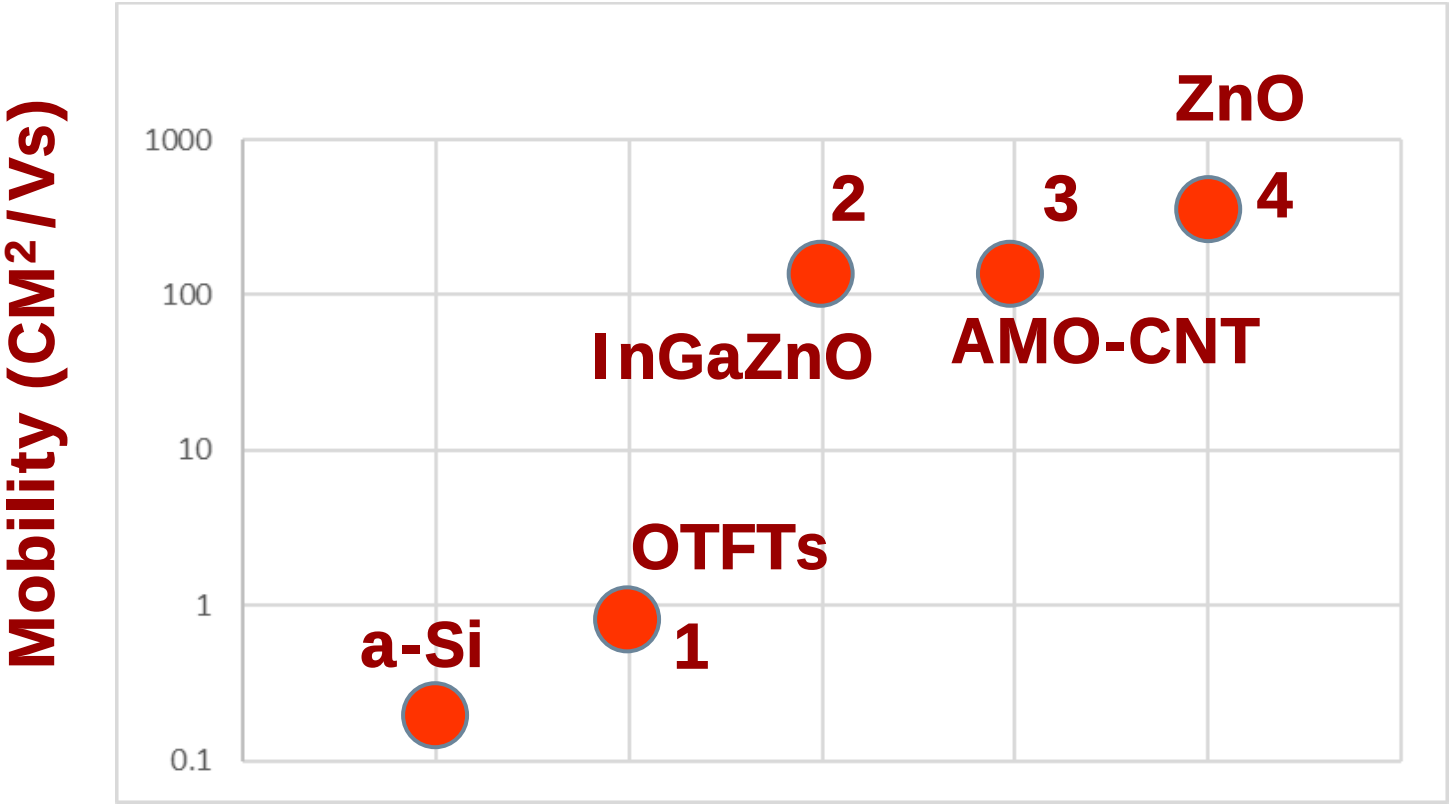
Mobility gap between Si and TFTs is shrinks.



TFT Field Effect Mobility



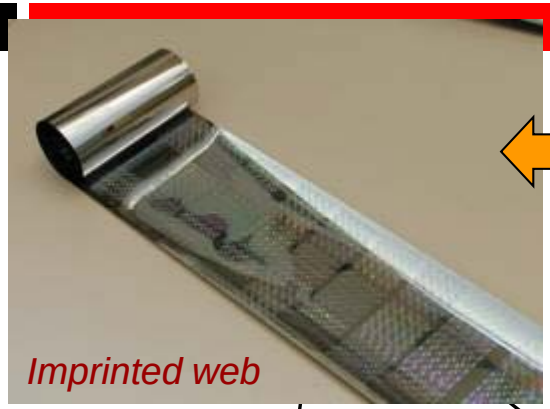
New Materials Enable High Mobility TFTs



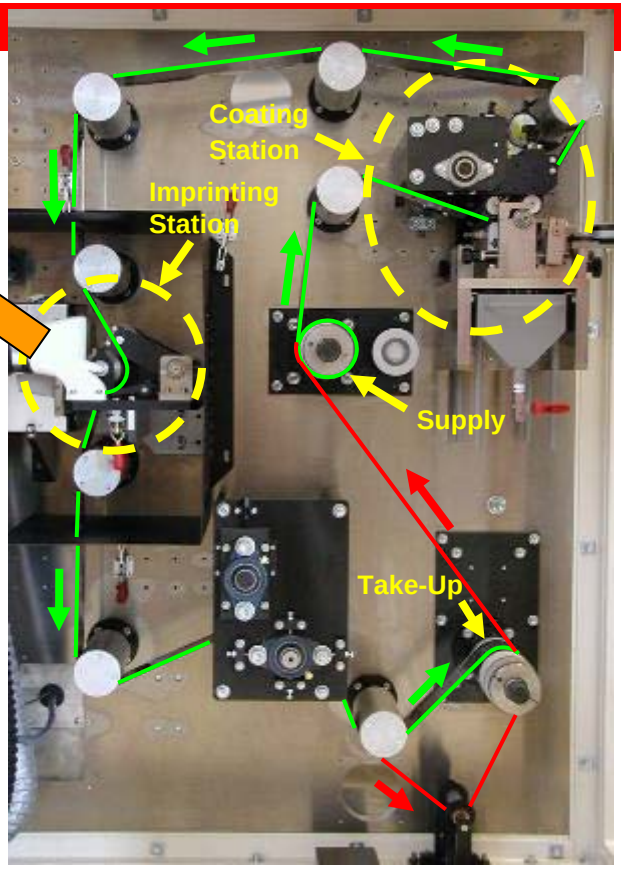
Large Area Inexpensive Flexible Electronics (LIFE)

Electronic Clothing, Paper, Jewelry, Signs,
"Sensitive Skin" for robots, vehicles and smart wall paper

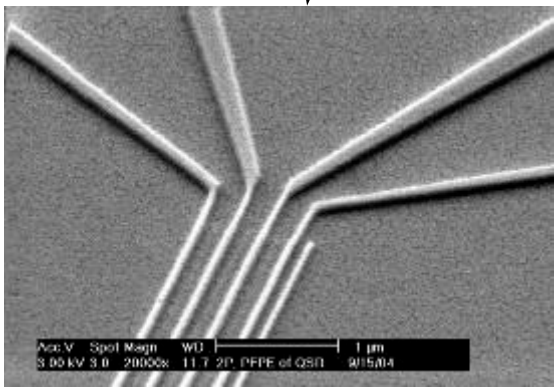
Actual Implementation (up to 250 m x 30 m DISPLAYS)



Imprinting roller with elastomeric stamp

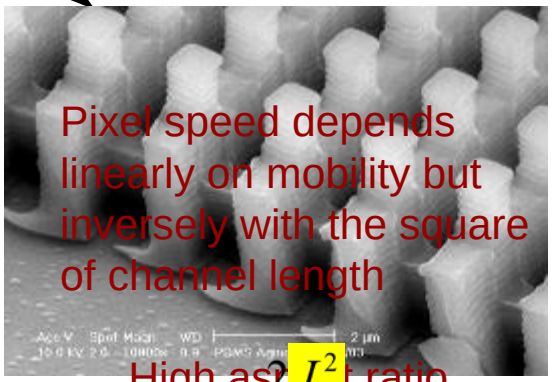


House-built R2R coating & imprinting machine



High resolution

→ **40 nm** line width



$$t_{pixel} \approx \frac{2L^2}{\mu (V_G - V_T)}$$

High aspect ratio & multiple step heights

→**sub-micron** features with

4 levels and **5:1 aspect ratio**

(Throughput rate = **5 m/min**)

Conclusions

- Overcoming numerous technology challenging industrial nanotechnology is reaching 3 nm technology and planning a 1 nm node but only 3 companies reached the 7 nm node
- Astronomical cost of chip design should be reduced by accounting for new ballistic/plasmonic physics
- Si CMOS technology enabled sub-THz and THz technology
- This film transistors shrink the performance gap with Si CMOS reaching dimensions< 50 nm at 2 m x 2 m sizes

Acknowledgment

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