

# **Integrated Power Management Circuits for Energy-Efficient IoT Systems**

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**University of Tokyo**



# Outline

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- ◆ **Energy-efficiency in IoT systems**
- ◆ **0.45-V input buck converter**
- ◆ **Wide  $I_{OUT}$  buck converter**
- ◆ **80-mV input boost converter**
- ◆ **Switched capacitor DC-DC converter**
  - **Integration of MLCCs on die**
- ◆ **Summary**

# Emerging Applications

| Area         | IoT                 | Wearable     | Implantable     |
|--------------|---------------------|--------------|-----------------|
| Target       | Environment, Things | Body surface | Inside the body |
| Applications | Management          | Healthcare   | Medical care    |

IoT



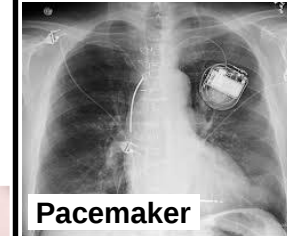
Wearable



Implantable



Brain computer interface



Pacemaker



Cochlear implant

# Requirements for IoT / Wearable Devices



**Wearing-unconscious**

**(1) Ultra flexible / small-size**

**(2) Wireless**

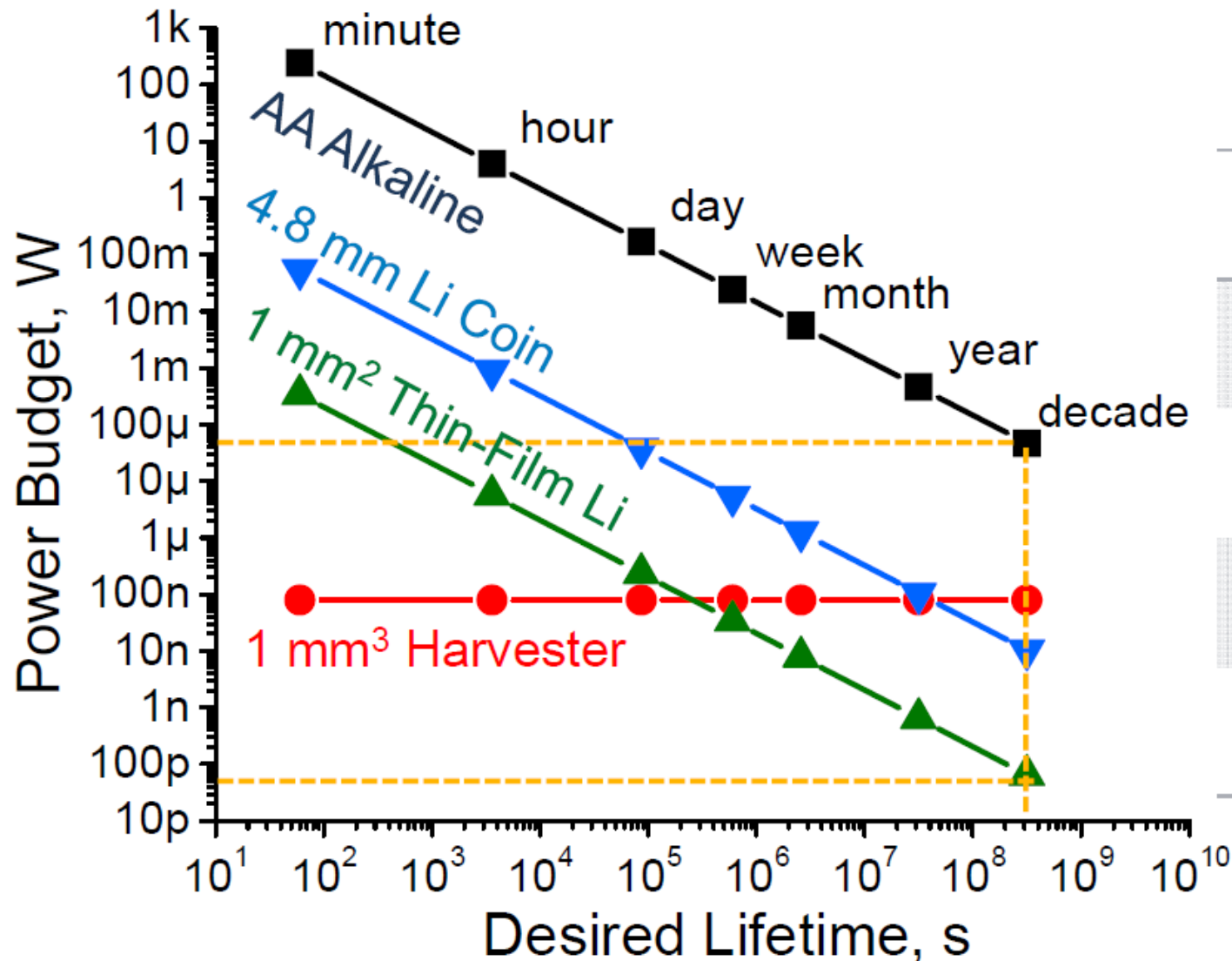


**Maintenance-free**

**(3) Energy autonomy**

**(Low energy) + Wireless powering/  
Energy harvesting)**

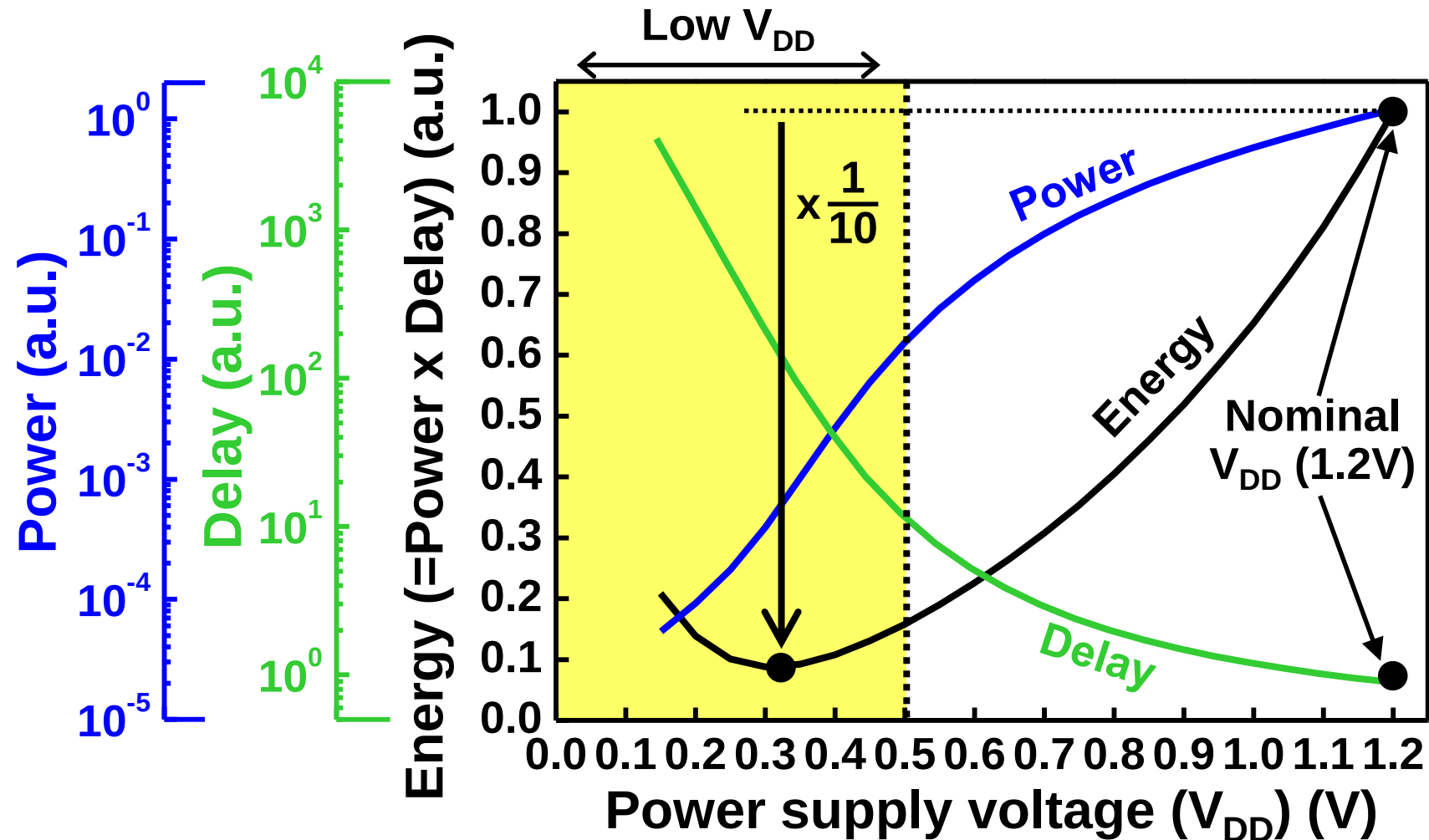
# Ultra-Low Power for IoT



| Battery                        | Peak Power  |
|--------------------------------|-------------|
| AA Alkaline                    | 1.5 W       |
| 4.8 mm Li Coin                 | 600 $\mu$ W |
| 1 mm <sup>2</sup> Thin-Film Li | 40 $\mu$ W  |
| 1 mm <sup>3</sup> Harvester    | 80 nW       |

◆ nW to  $\mu$ W are required.

# Minimum Energy at Low $V_{DD}$

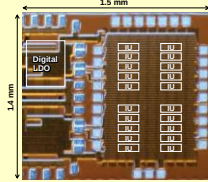


◆ Energy efficient operation at  $V_{DD} = 0.3$  V

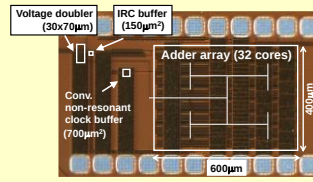
# Our Sub-0.5V Circuits

## Logic

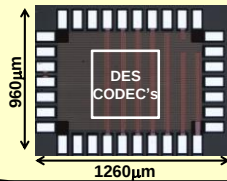
**Adaptive  $V_{DD}$**   
(ISSCC2012)



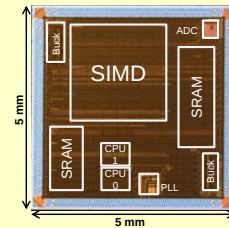
**Resonant clock**  
(ISSCC2013)



**Fine-grained  $V_{DD}$**   
(ESSCIRC2011)  
(ISQED2012)

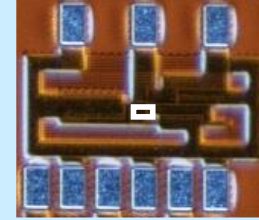


**High  $V_{DD}$  clock**  
(VLSI2013)

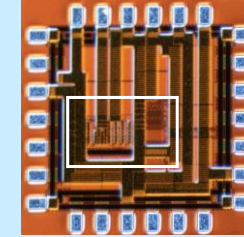


## RF

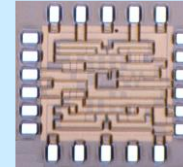
**0.5V TX**  
(ESSCIRC2012)



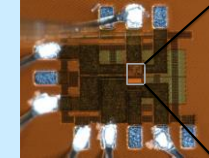
**0.5V RX**  
(VLSI2012)



**Power gated XO**  
(VLSI2013)

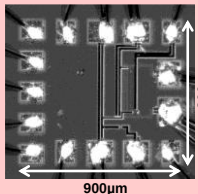


**0.35V XO**  
(ISLPED2012)

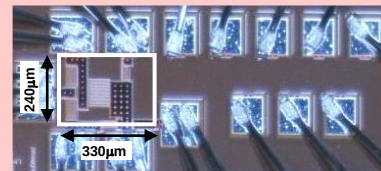


## Power management

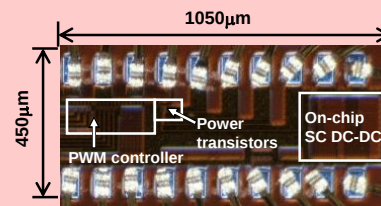
**0.5V LDO**  
(CICC2010)



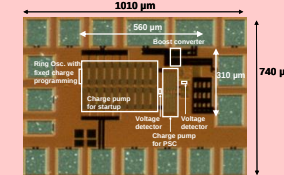
**1V switched cap.**  
(VLSI2011)



**0.45V buck**  
(VLSI2012)



**0.1V boost**  
(ISSCC2011)  
(A-SSCC2011)



# Key Techniques for Sub-0.5V Circuits

## Logic

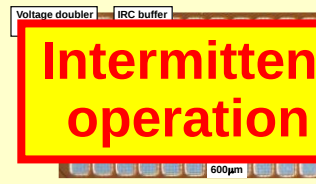
**Adaptive  $V_{DD}$**   
(ISSCC2012)

**$V_{DD}$  control**



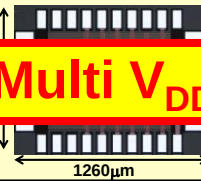
**Resonant clock**  
(ISSCC2013)

**Intermittent operation**



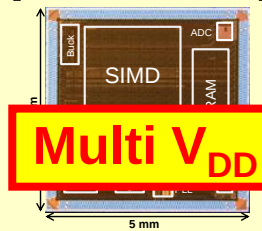
**Fine-grained  $V_{DD}$**   
(ESSCIRC2011)  
(ISQED2012)

**Multi  $V_{DD}$**



**High  $V_{DD}$  clock**  
(VLSI2013)

**Multi  $V_{DD}$**



## RF

**0.5V TX**  
(ESSCIRC2012)

**Multi  $V_{DD}$**



**Power gated XO**  
(VLSI2013)

**Intermittent operation**



**0.5V RX**  
(VLSI2012)

**Intermittent operation**



**0.35V XO**  
(ISLPED2012)

**Gate width sizing**



## Power management

**0.5V LDO**  
(CICC2010)

**Analog  
→ Digital**



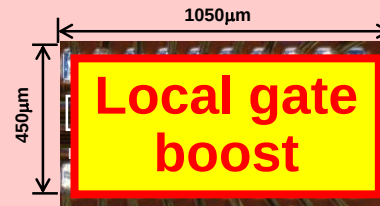
**1V switched cap.**  
(VLSI2011)

**Intermittent operation**



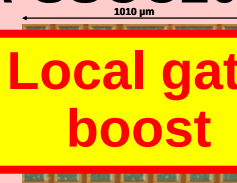
**0.45V buck**  
(VLSI2012)

**Local gate boost**

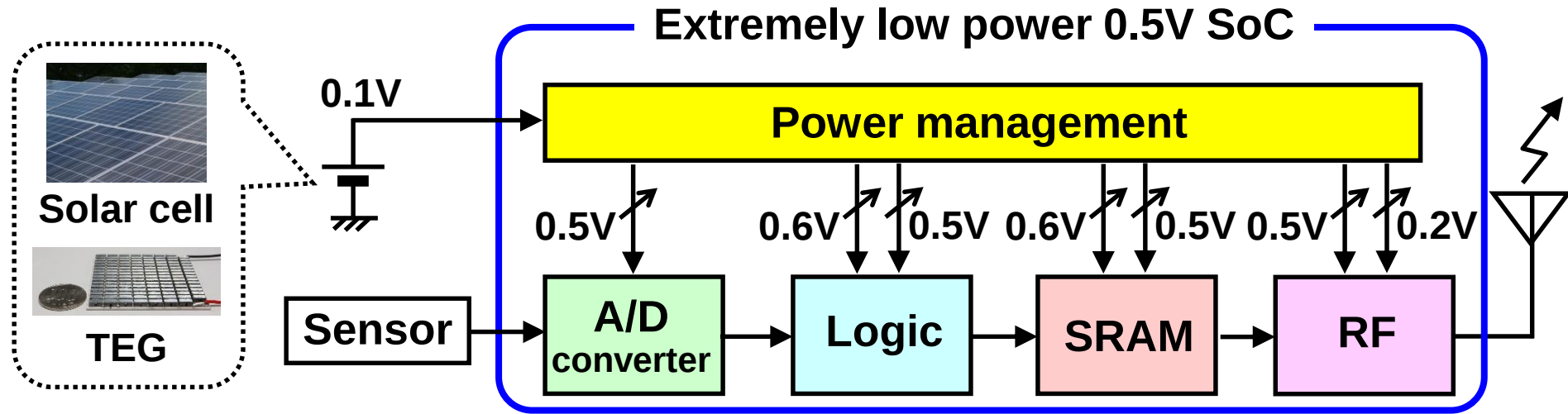


**0.1V boost**  
(ISSCC2011)  
(A-SSCC2011)

**Local gate boost**

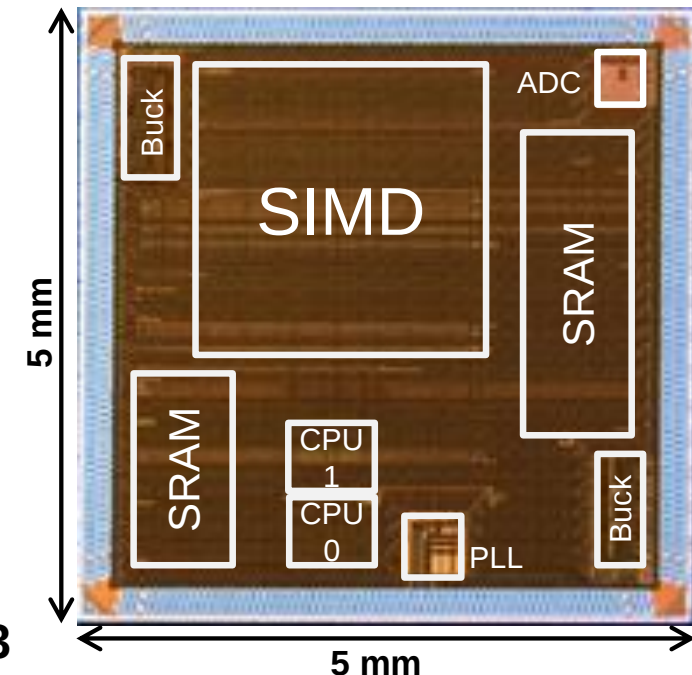


# 0.5V SoC for Image Processing

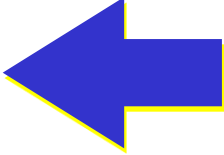


TEG: Thermoelectric generator

**Integrated power management circuits** are important to achieve energy-efficient IoT systems.



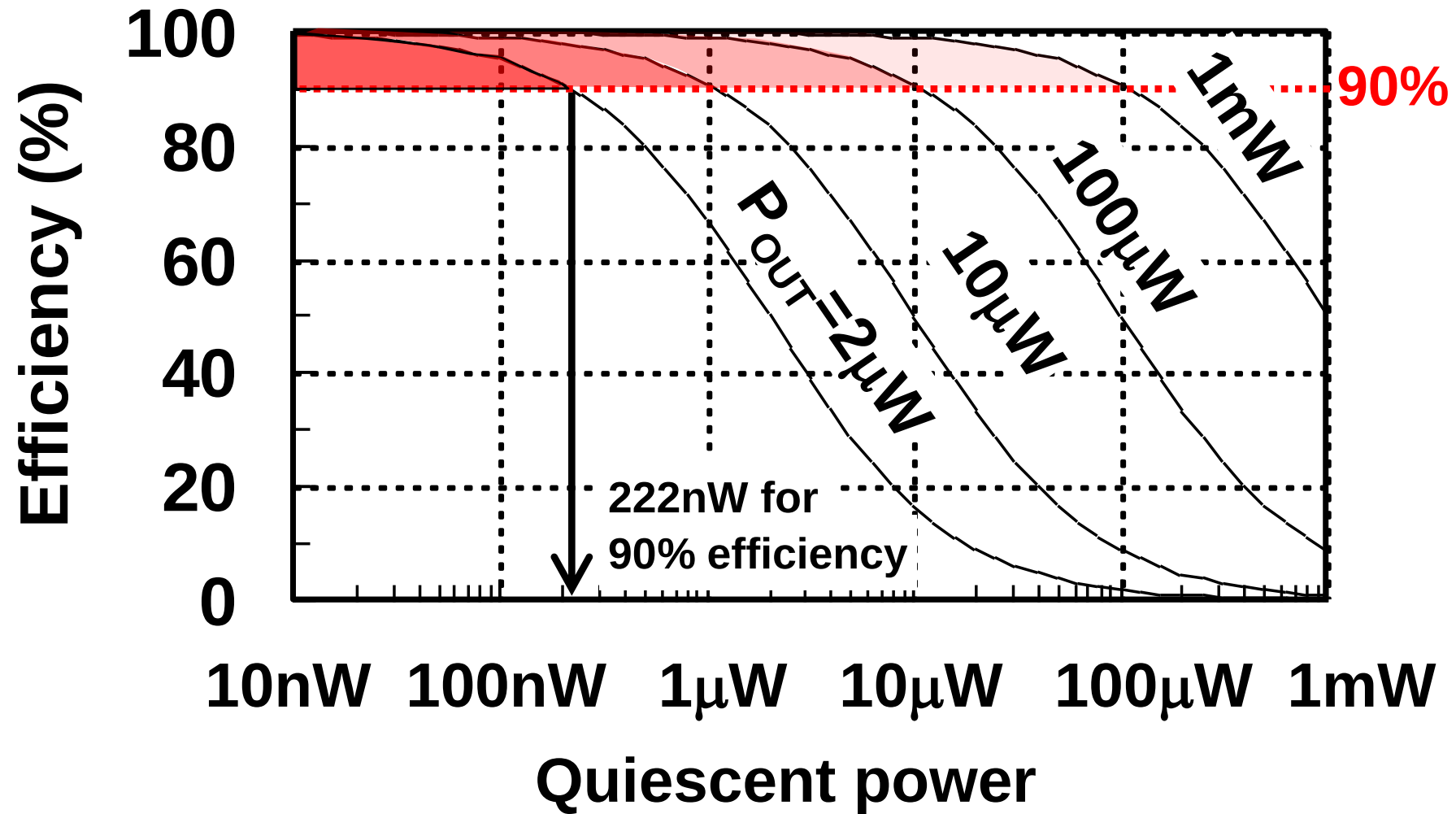
# Outline

- ◆ Energy-efficiency in IoT systems
- ◆ **0.45-V input buck converter** 
- ◆ Wide  $I_{OUT}$  buck converter
- ◆ 80-mV input boost converter
- ◆ Switched capacitor DC-DC converter
  - Integration of MLCCs on die
- ◆ Summary

- 
- The diagram illustrates an LSI system with an adaptive  $V_{DD}$  control mechanism. The system is enclosed in a light blue rounded rectangle labeled "LSI". Inside, a yellow rectangle represents the "Adaptive  $V_{DD}$  control for near- $V_{TH}$  logic circuits". This yellow area contains a "Control" block (blue box) and a "Power transistor" (green box). The "Control" block is connected to the gate of the "Power transistor". The "Power transistor" is connected to the input and output lines. The input line is connected to a voltage source  $V_{IN} (>0.45V)$  and is labeled "Input power ( $P_{IN}$ )". The output line is connected to a "Logic (Load)" block and is labeled "Output power ( $P_{OUT}$ )". The output voltage is  $V_{OUT} (0.4V)$ . Arrows indicate the flow of power and control signals.

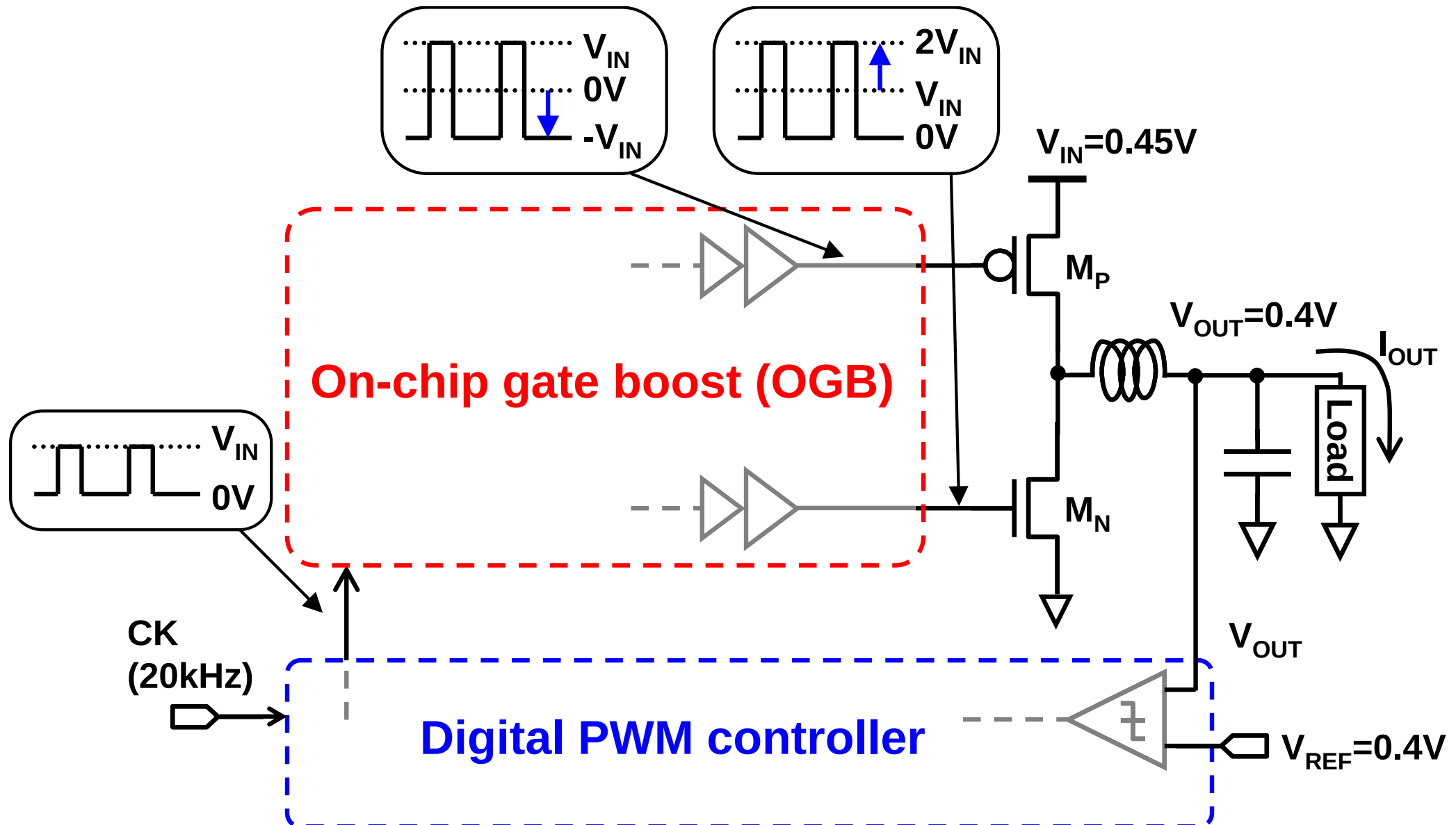
- Low  $V_{IN} \rightarrow$  Loss in power transistors increases.

# Low Quiescent Power ( $\approx$ Controller Power)

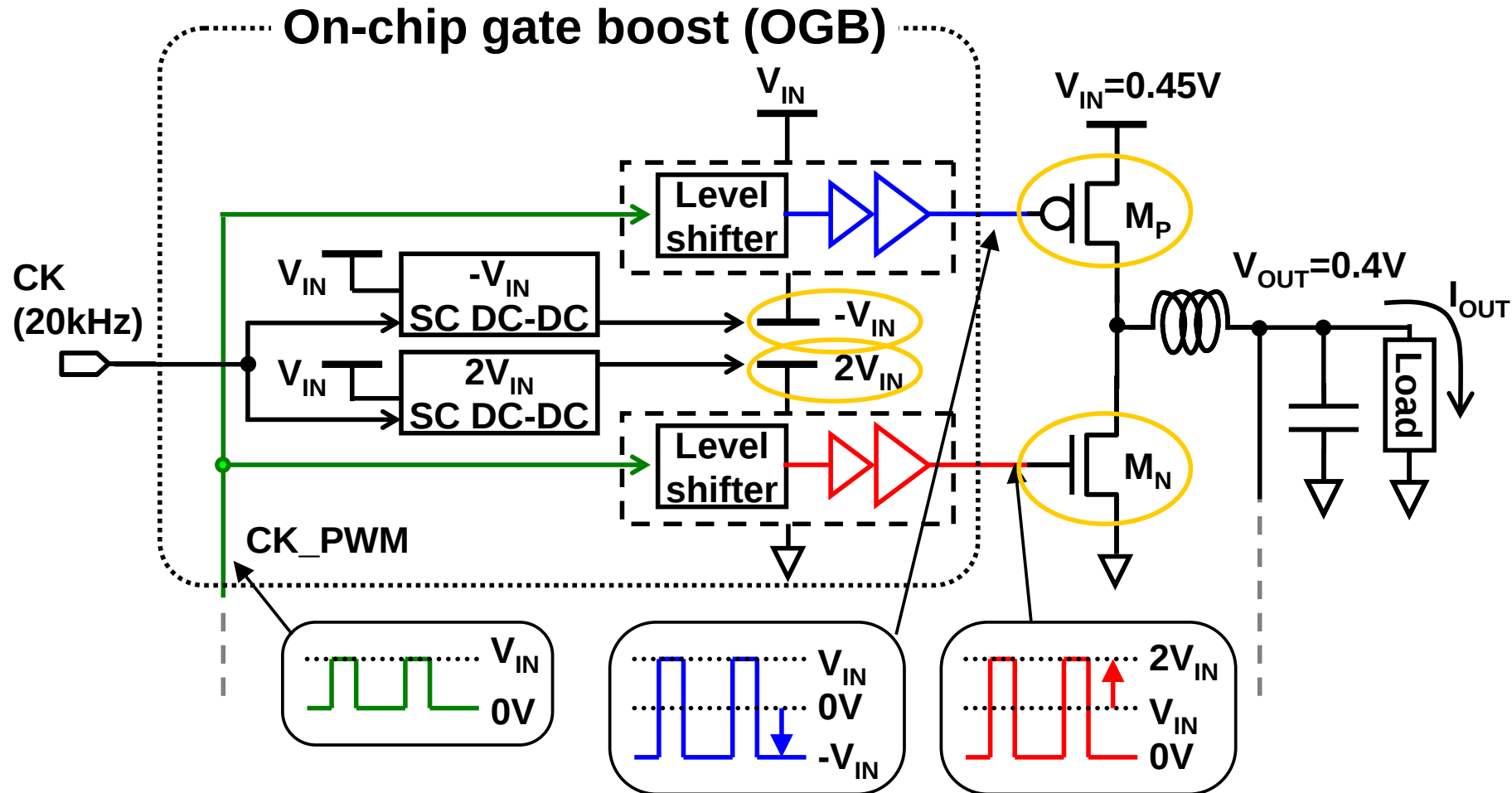


- As the quiescent power increases, the efficiency decreases.
- For 90% efficiency @  $P_{OUT}=2\mu W$ , target quiescent power is 222nW.

# Concept of Proposed Buck Converter



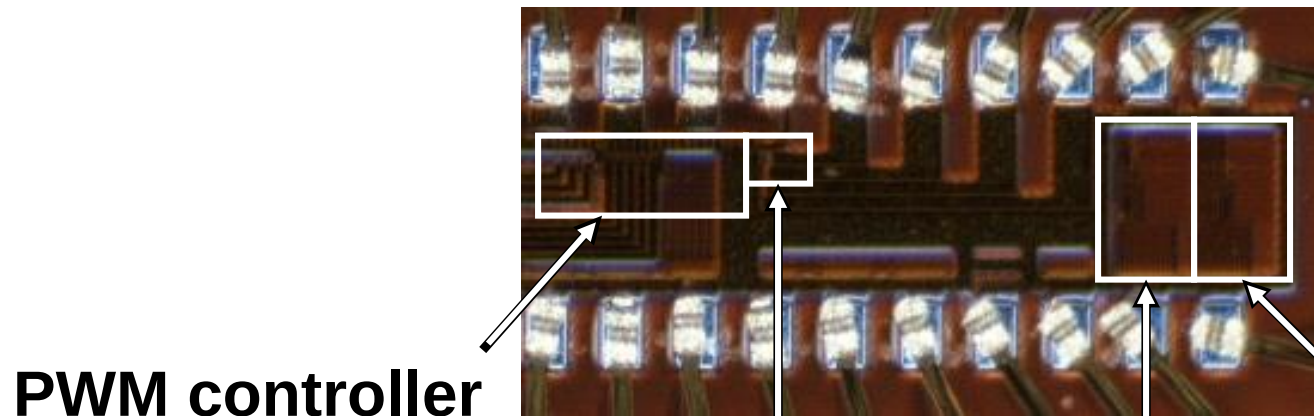
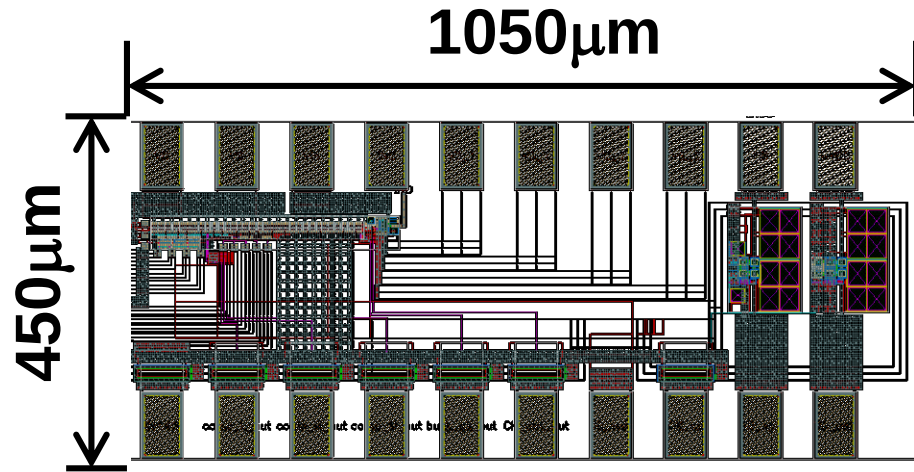
# On-chip Gate Boost for Power Transistors



■ 2 power rails are generated by on-chip switched-capacitor (SC) DC-DC converters.

➔ Loss in  $M_P$  and  $M_N$  is reduced.

# On-chip Gate Boosted Buck Converter



PWM controller

Power transistors

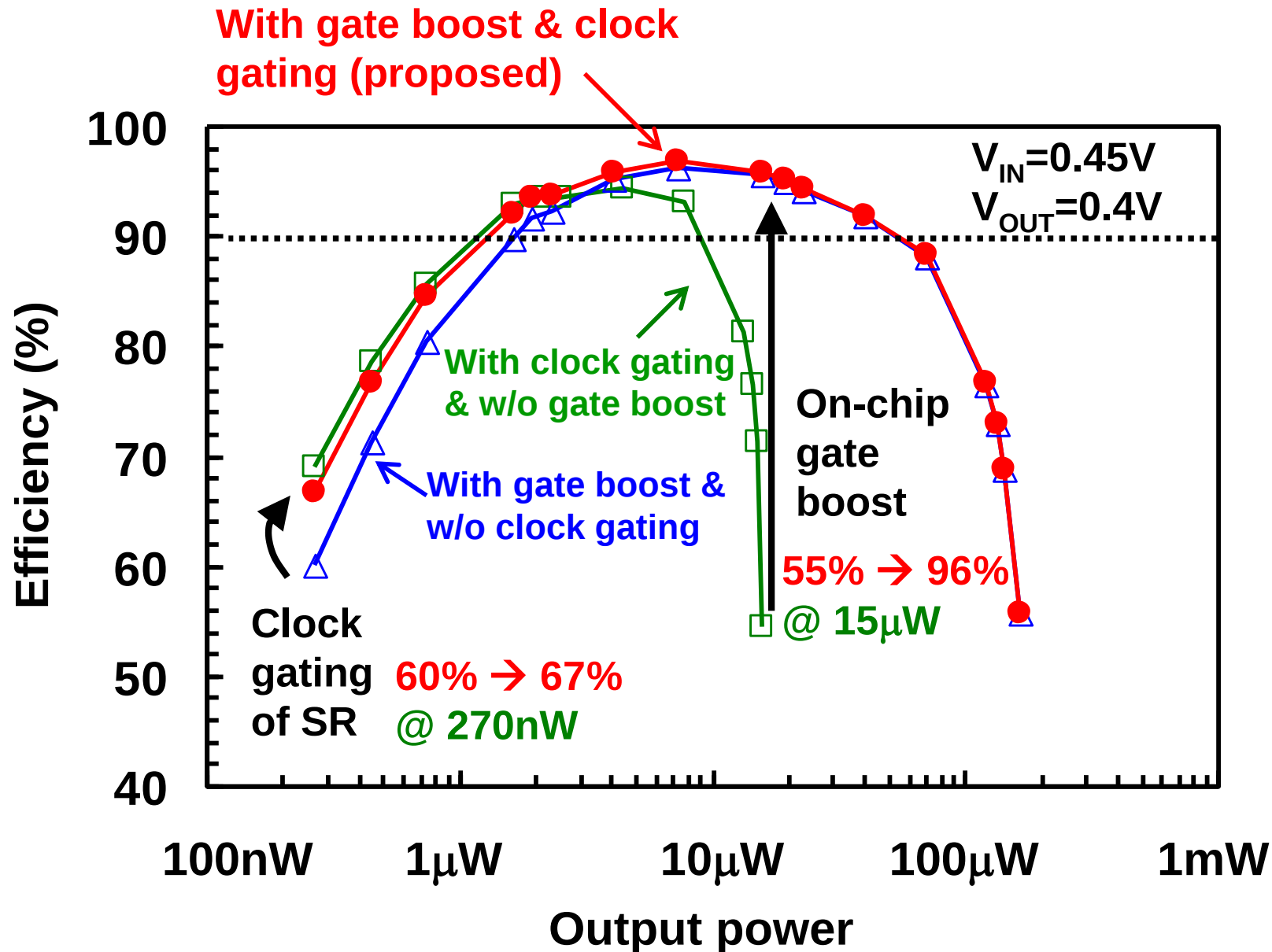
$2V_{IN}$  SC DC-DC

$-V_{IN}$  SC DC-DC

40nm CMOS

|                                |                       |
|--------------------------------|-----------------------|
| Technology                     | 40-nm CMOS            |
| Input voltage                  | 0.45V                 |
| Output voltage                 | 0.34V~0.44V           |
| Output power                   | 270nW~165μW           |
| Output ripple                  | <5mV                  |
| Max. efficiency                | 97% at 7μW            |
| Quiescent power at $I_{OUT}=0$ | 140nW                 |
| Active area                    | 0.043 mm <sup>2</sup> |

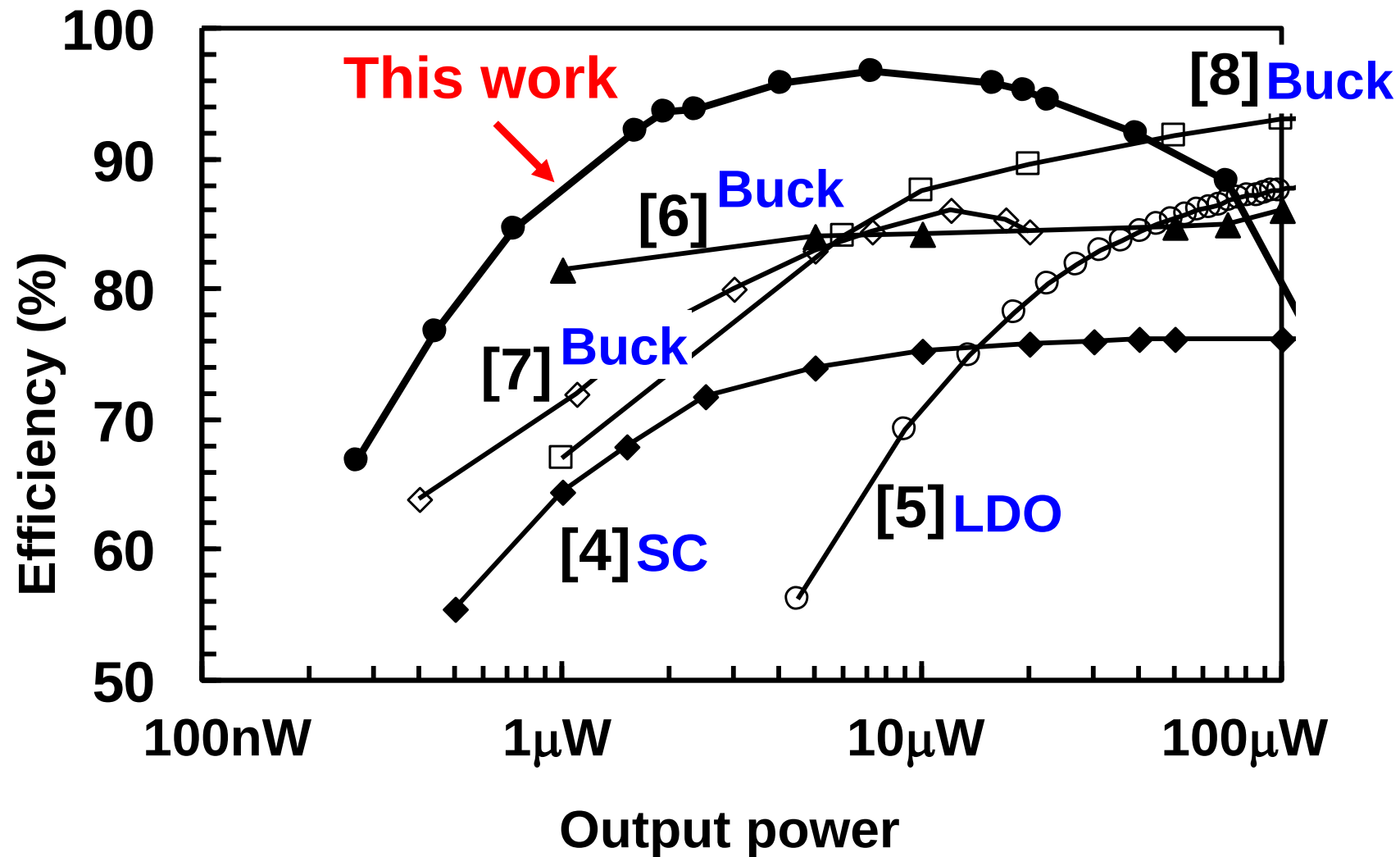
# Measured Efficiency vs. Output Power



**>90% efficiency is achieved from 2μW to 50μW.**

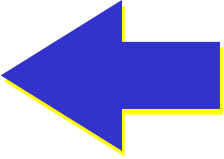
$$\text{(Ideal LDO)} = \frac{0.4V}{0.45V} = 89\%$$

# Comparison with DC-DC Converters



■ By virtue of OGB and low-power controller (**140nW**), the highest efficiency (<40μW) is achieved.

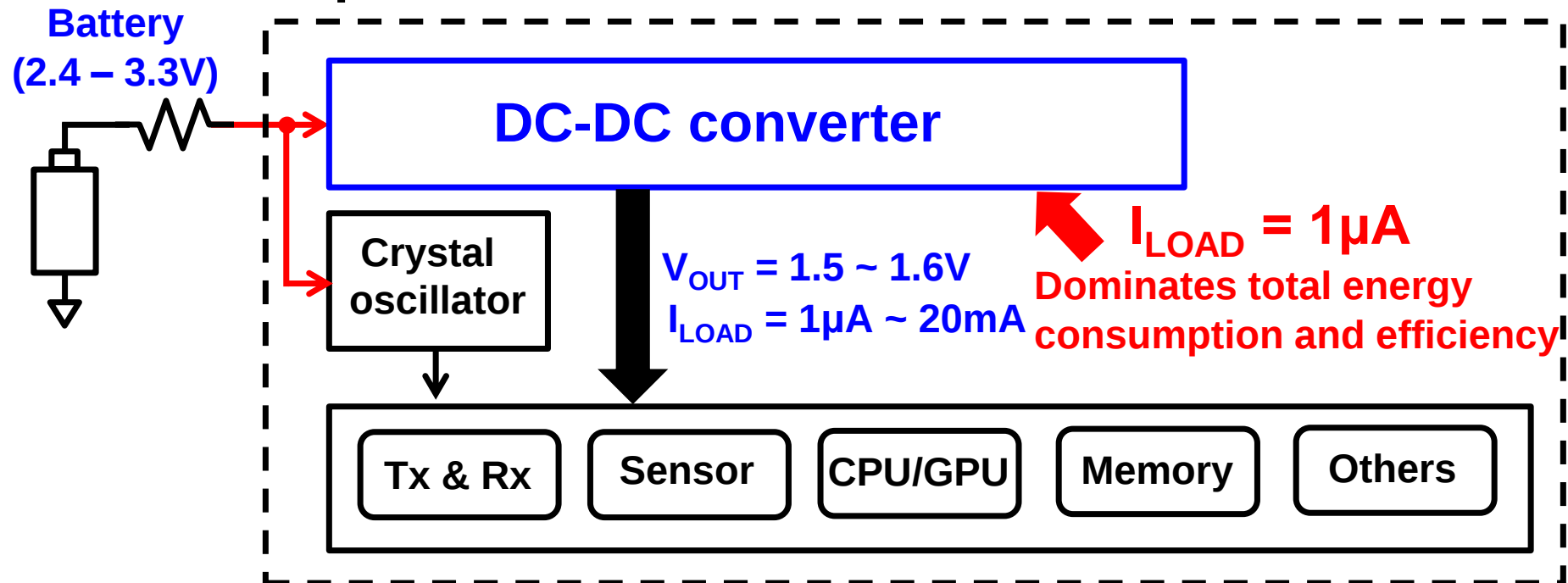
# Outline

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# Buck Converter for Wide $I_{OUT}$

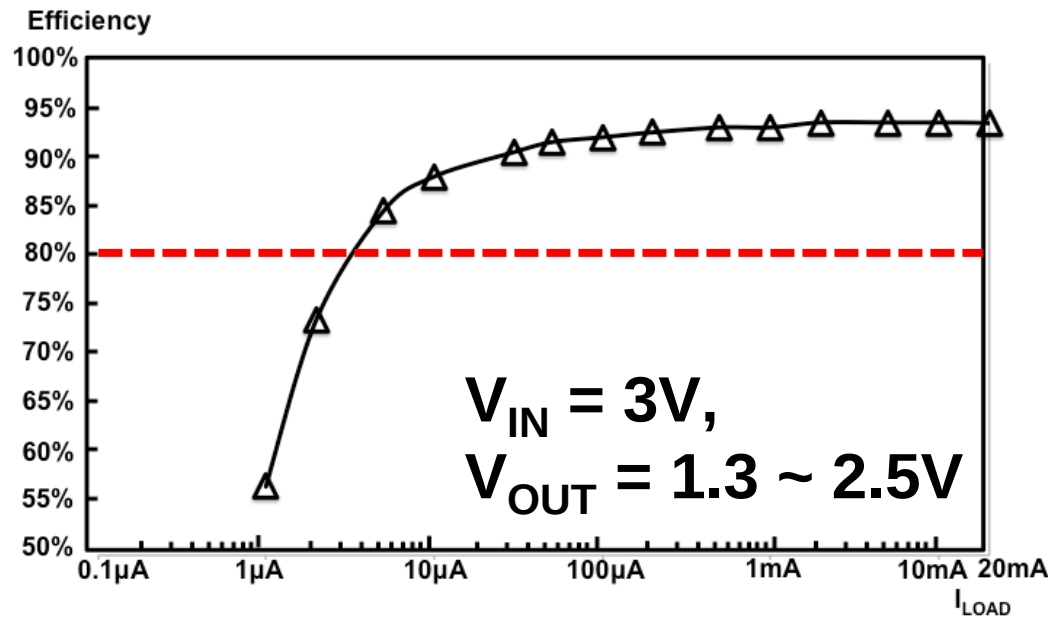
- Sleep mode consumes more than 95% energy
- BLE specifications: 15 mA (active), 1  $\mu$ A (sleep)
- Load current range  $> 10^4$

LSI system in IoT, wearable devices, implantable electronics, etc.



# Low Efficiency at $I_{OUT} < 1\mu A$

## Buck converter for IoT



□  $I_{LOAD}$  range  $> 10^4$

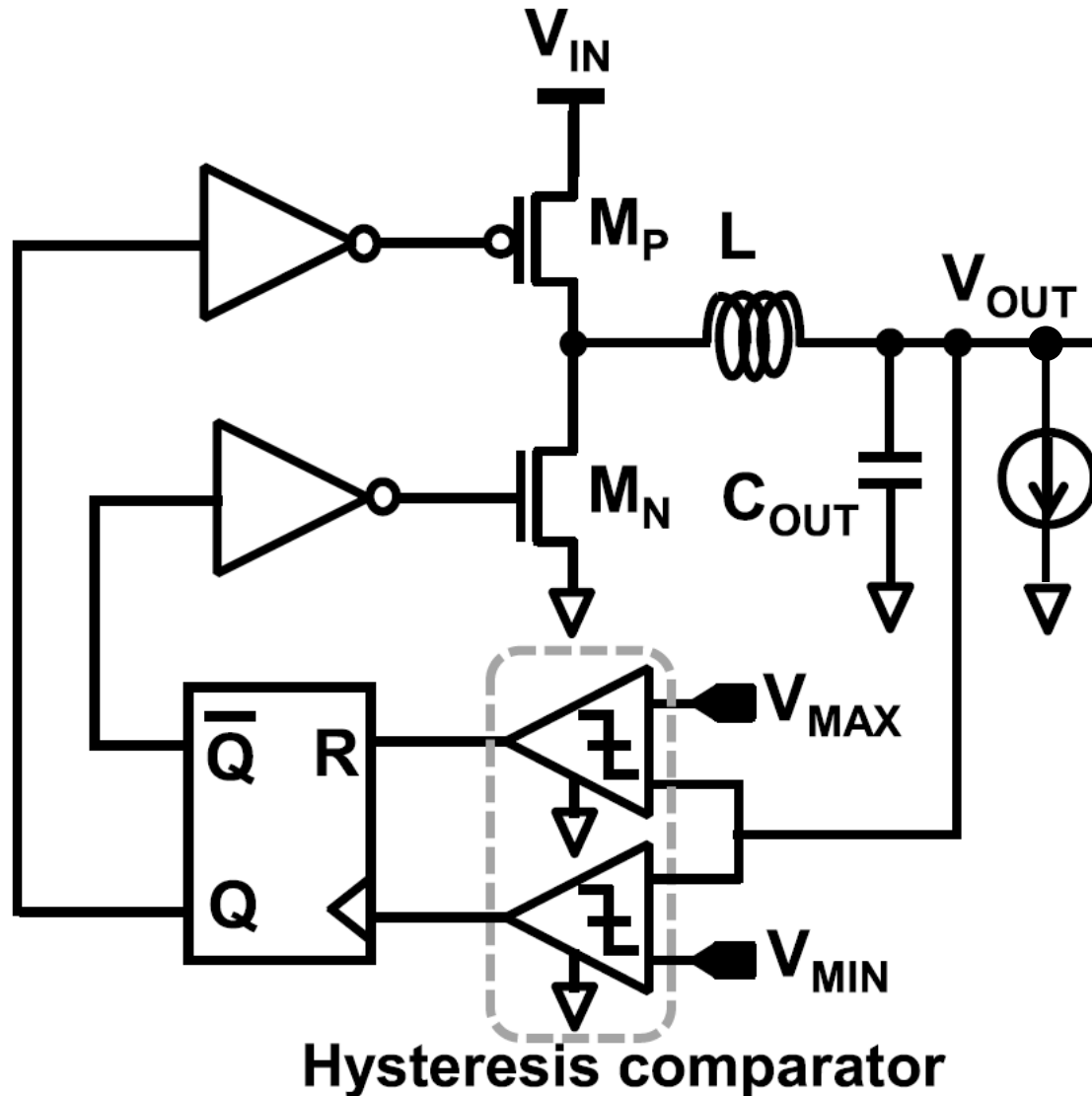
□  $\eta < 80\%$  @  $I_{LOAD} < 4\mu A$

□  $\eta \sim 55\%$  @  $I_{LOAD} = 1\mu A$

- Efficiency should be improved in  $\mu$ -A region
- Save energy consumption and extend battery lifetime

# Conv. Buck Converter in DCM

Discontinuous conduction mode (DCM)

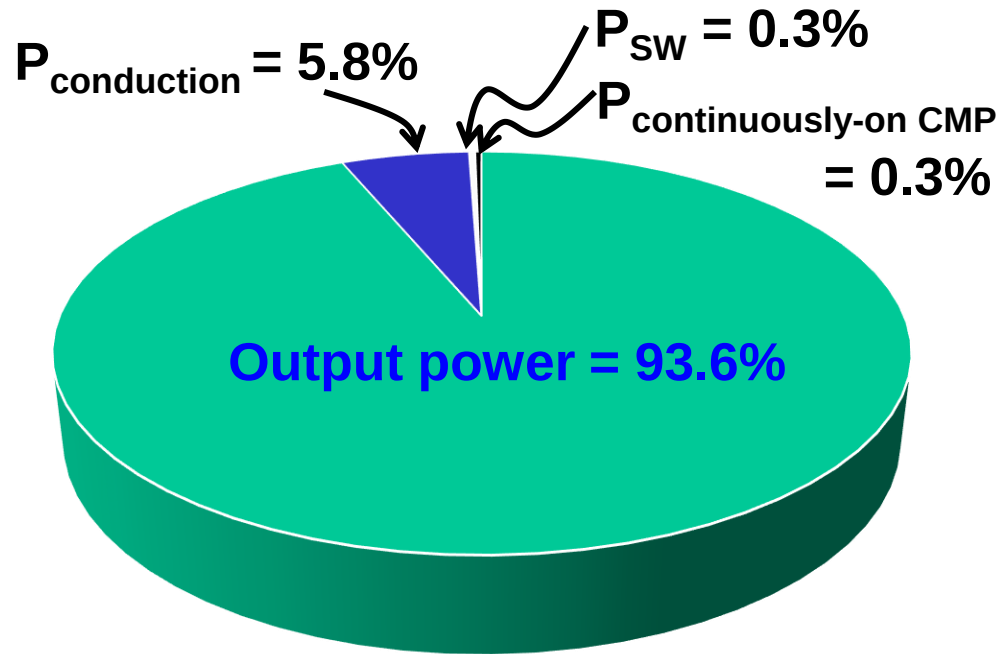


DC power of the **continuous-time comparator** degrades the efficiency of buck converter.

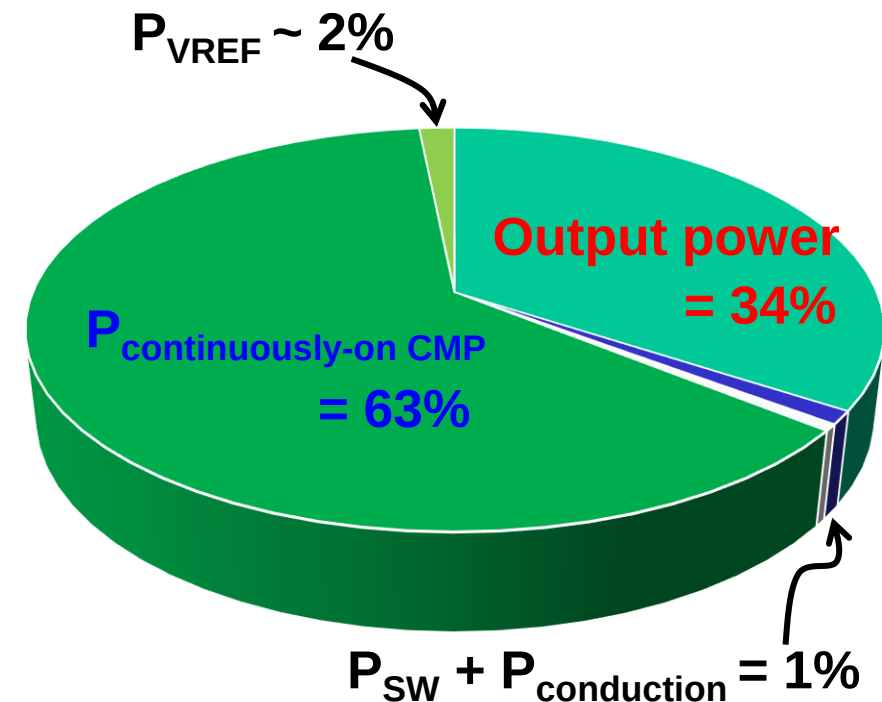
# Simulated Power Dissipation

## ■ Power dissipation of hysteresis buck converter:

Active mode ( $I_{LOAD} = 10\text{mA}$ )

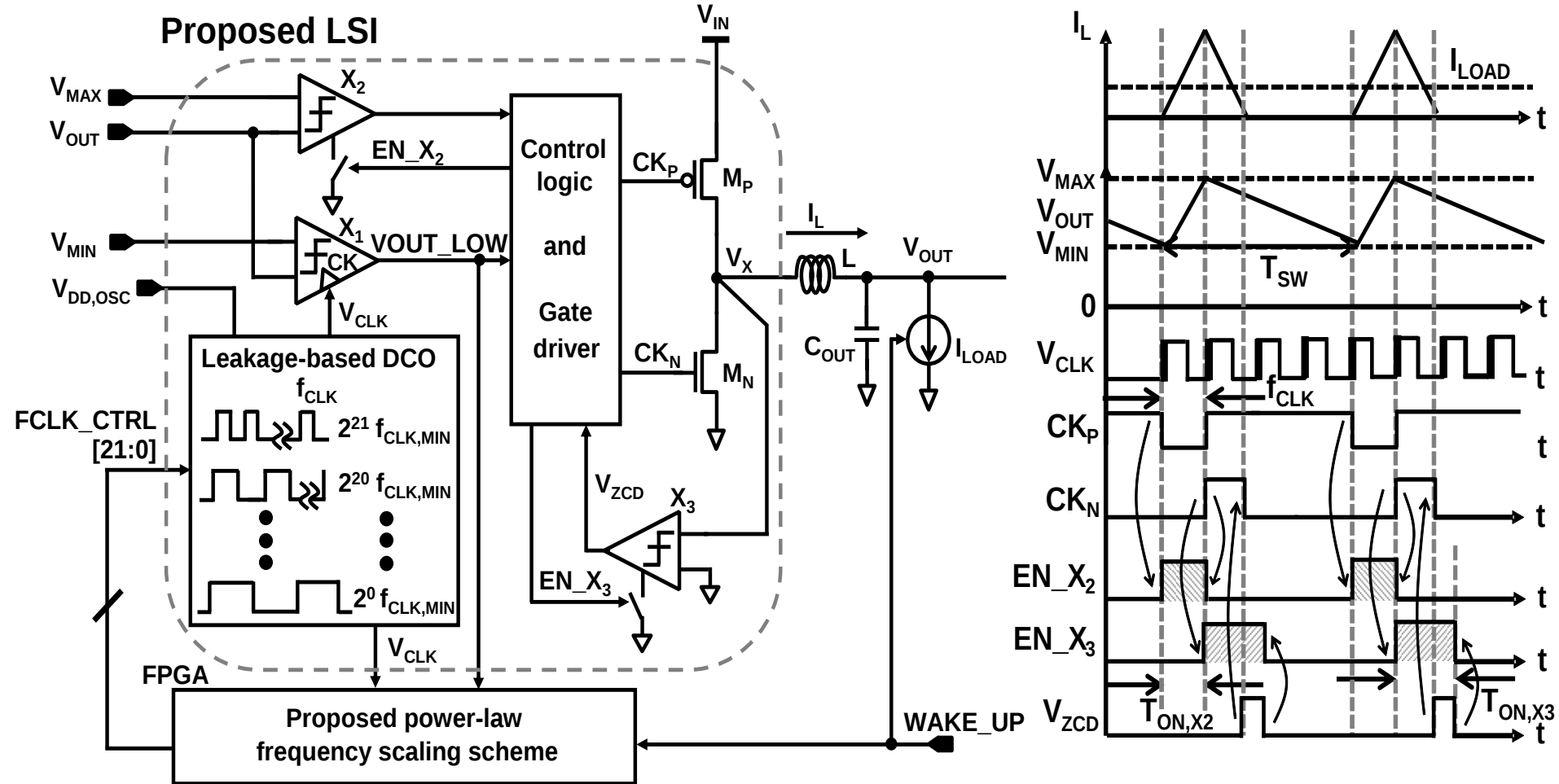


Sleep mode ( $I_{LOAD} = 1\mu\text{A}$ )

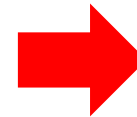


■ Even the  $I_{BIAS} = 1\mu\text{A}$  also decreases  $\eta$  to 34% @  $I_{LOAD} = 1\mu\text{A}$   
→ Remove the continuously-on Comparator

# Proposed Clocked Hysteresis Control Buck Converter

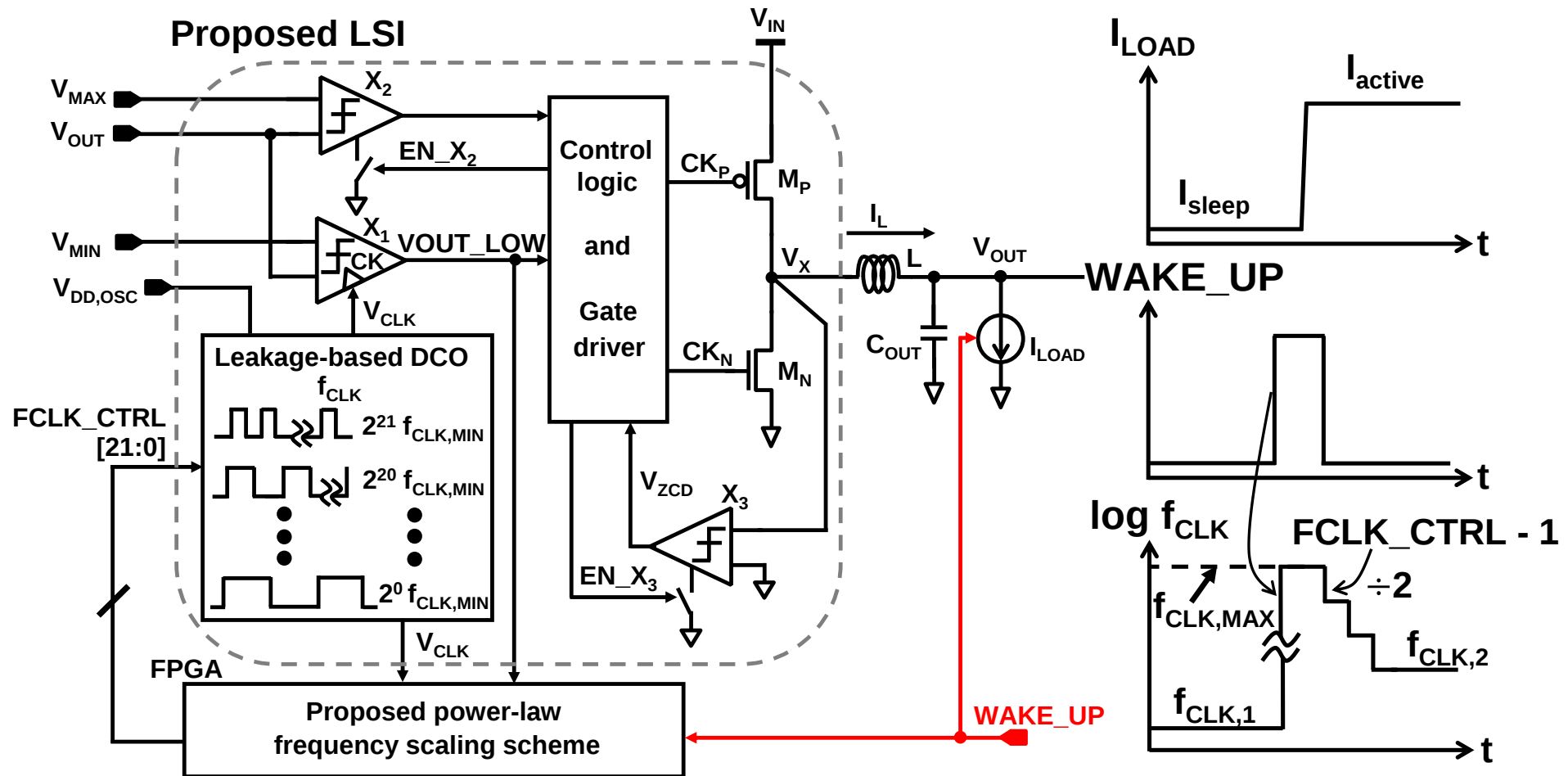


- $X_1$ : Clocked comparator
- $X_2, X_3$ : Power-gated comparator



**No DC power in comparators**

# Load Wake-up Operation

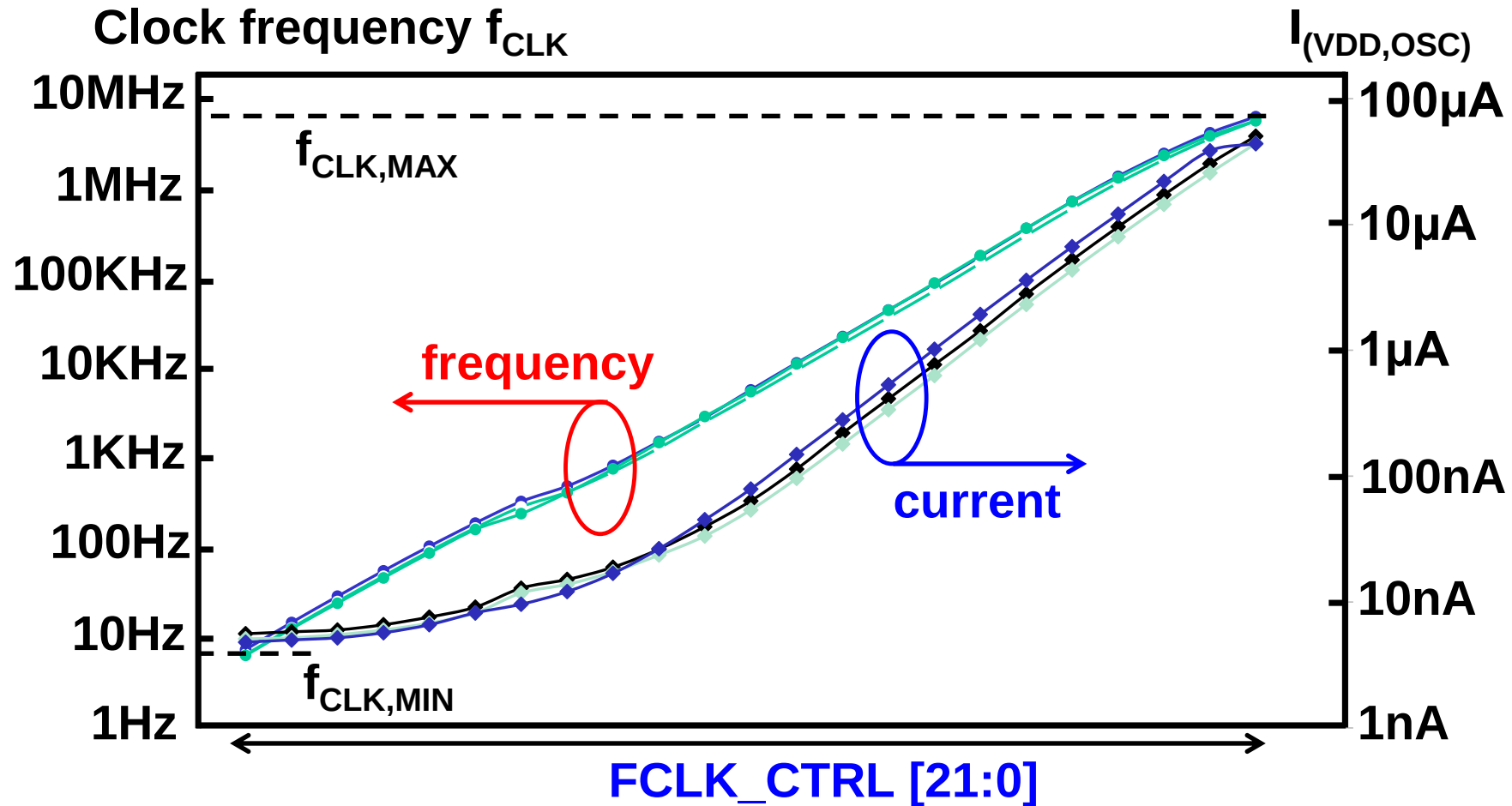


- **WAKE\_UP**: reset  $f_{CLK}$  to highest frequency ( $2^{21} f_{CLK}$ )
- Asynchronized logic can be designed to reset  $f_{CLK}$  immediately



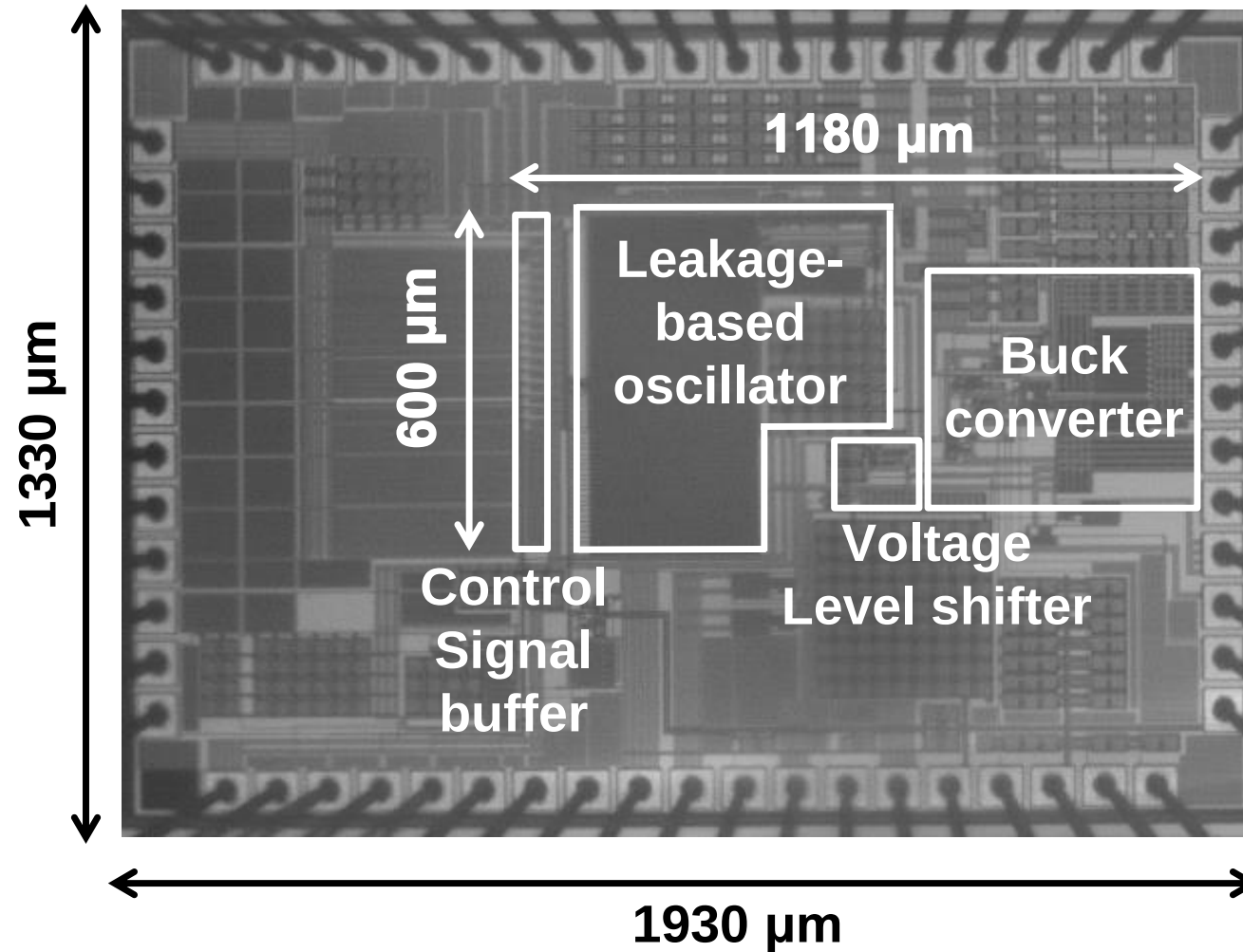
- **Power: proportional to the oscillating frequency**
- **No additional voltage reference**
- **Leakage current is designed as bias**

# Measured Oscillator Power vs. Freq.



- Measured 3 chip showing small variation on  $f_{CLK}/I_{(VDD,OSC)}$
- $f_{CLK} = 7\text{Hz} \sim 6\text{MHz}$  controlled by 22 bits thermometer code
- $P_{(VDD,OSC)} = 3.5\text{nW} \sim 32\mu\text{A}$  when  $V_{DD,OSC} = 0.6\text{V}$

# Chip Micrograph



■ 0.18μm CMOS

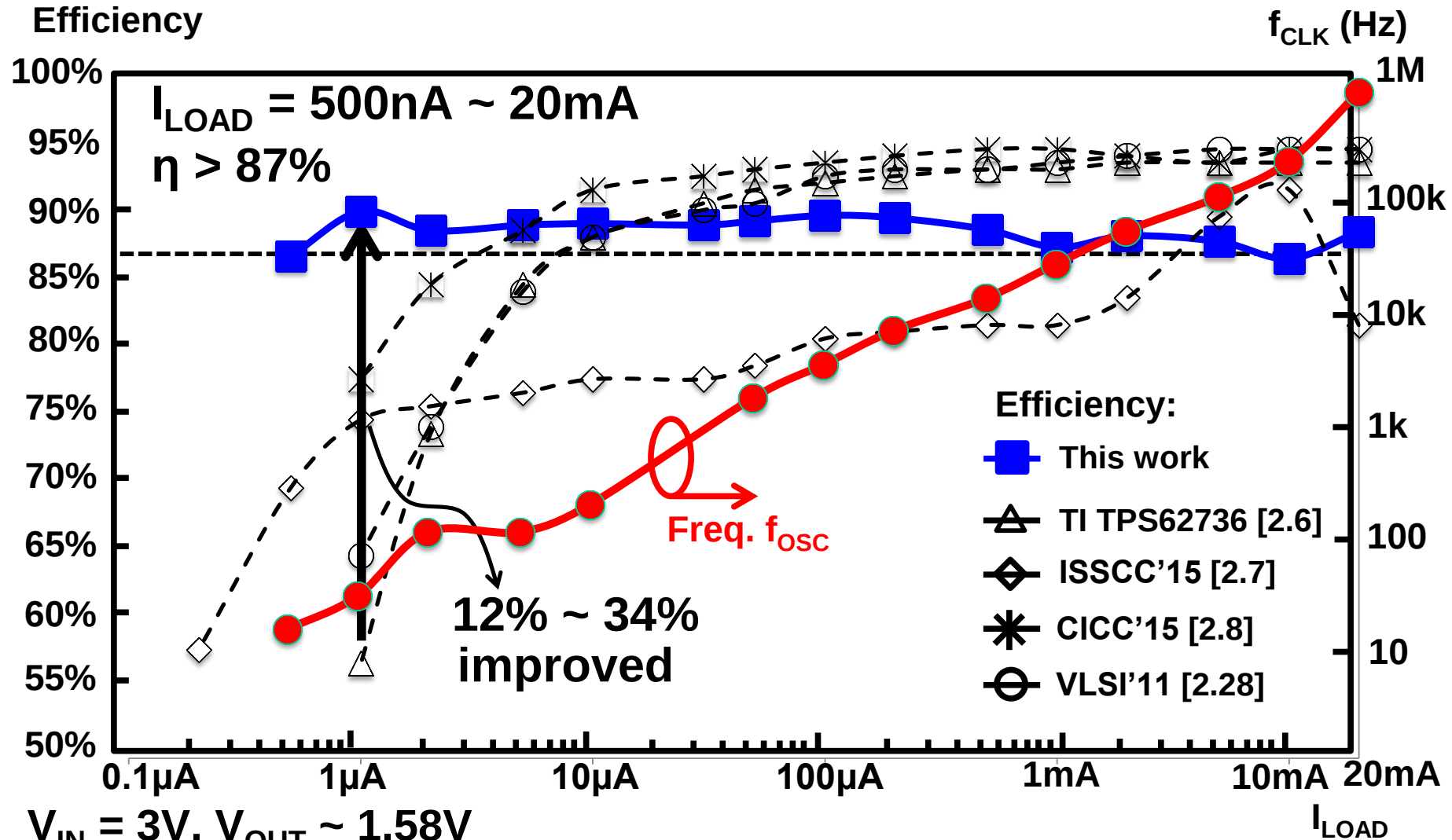
■  $V_{IN} = 2.4 - 3.3V$ ,  $V_{OUT} = 1.5 - 1.6V$

■ Active area: 0.71mm<sup>2</sup>

■ Off-chip: 4.7-μH L, 1-μF C

C.-S. Wu, et al., IEEE  
Trans. on VLSI, 2018

# Efficiency of Buck Converter



■  $\eta > 87\%$  over 500nA to 20mA for BLE application

■ 12% ~ 34% improvement is achieved @  $I_{Load} = 1\mu A$

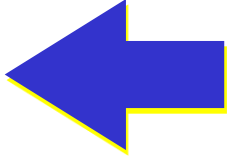
# Performance Comparison

|                            | ISSCC'15<br>[2.7]      | CICC'15<br>[2.8]      | VLSI'15<br>[2.9]    | VLSI'11<br>[2.28]      | This work                                 |
|----------------------------|------------------------|-----------------------|---------------------|------------------------|-------------------------------------------|
| Technology                 | 180nm<br>CMOS          | 350nm<br>CMOS         | 180nm<br>CMOS       | 250nm<br>CMOS          | <b>180nm<br/>CMOS</b>                     |
| Die size                   | 1.44mm <sup>2</sup>    | 2.88mm <sup>2</sup>   | 2.42mm <sup>2</sup> | 0.21mm <sup>2</sup>    | <b>0.71mm<sup>2</sup> *</b>               |
| $V_{IN}$ (V)               | 0.6/1.2                | 2.2 – 6               | 3                   | 1.2 – 2.5              | <b>2.4 – 3.3</b>                          |
| $V_{OUT}$ (V)              | 0.35 – 0.5             | 2.5                   | 1                   | 1                      | <b>1.5 – 1.6</b>                          |
| $I_{LOAD}$                 | 100nA –<br>20mA        | 1μA –<br>100mA        | 10nA –<br>1μA       | 1μA –<br>100mA         | <b>500nA –<br/>20mA</b>                   |
| Peak eff. $\eta_{PEAK}$    | 92%                    | 95%                   | 87%                 | 95.2                   | <b>90.4%</b>                              |
| $\eta$ @ $I_{LOAD}=1\mu A$ | 75%                    | 78%                   | 87%                 | 65%                    | <b>90.4%</b>                              |
| Inductor value L           | 4.7μH                  | 2.2μH                 | 47μH                | 1.5μH                  | <b>4.7μH</b>                              |
| Control methodology        | PWM,<br>PFM, and<br>AM | Hysteresis<br>control | Constant<br>on-time | Dynamic<br>on/off time | <b>Clocked<br/>hysteresis<br/>control</b> |

\* Active area

■  $\eta > 87\%$  over 500nA-20mA  $I_{Load}$  with the proposed clocked hysteresis control

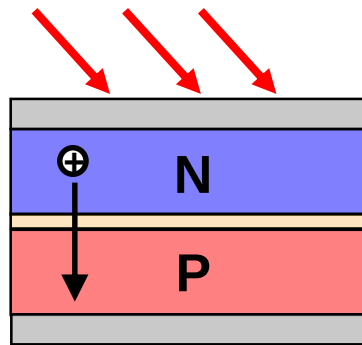
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# Energy Harvesters

## Single-cell Solar Cell

Light

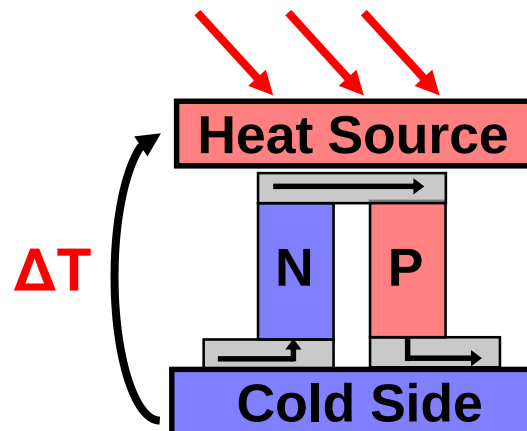


- Producing electricity from **light**
- Output : 500~600mV (Outdoor),  
**100~200mV (Dark office)**

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## Thermoelectric Generator

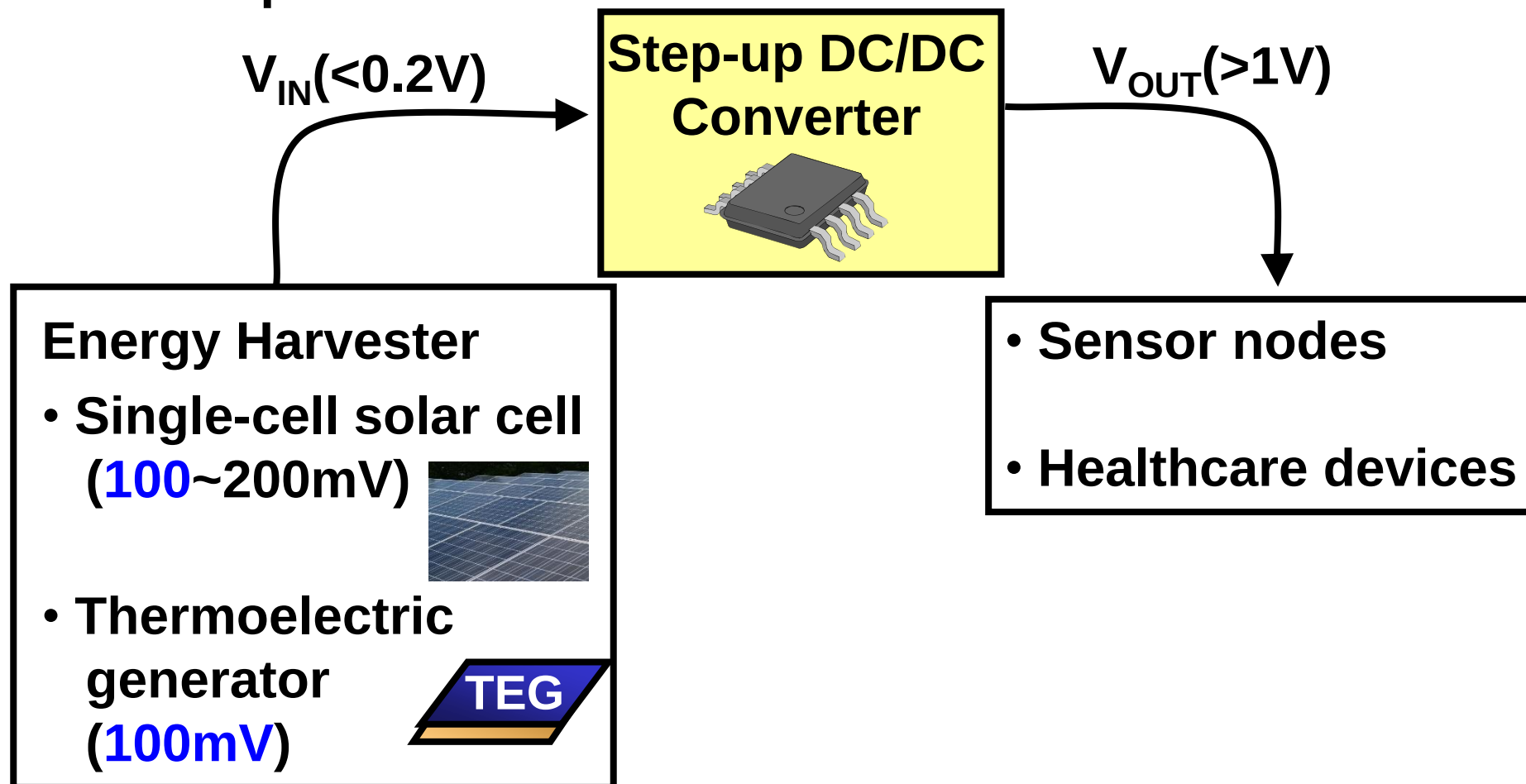
Heat



- Producing electricity from **heat**
  - Output : 10mV/K~50mV/K
- ⇒ From body heat (2K) : **100mV**

# DC/DC for Energy Harvester

**Startup voltage ( $V_{\text{Startup}}$ ):** The minimum  $V_{\text{IN}}$  that the converter starts to operate.

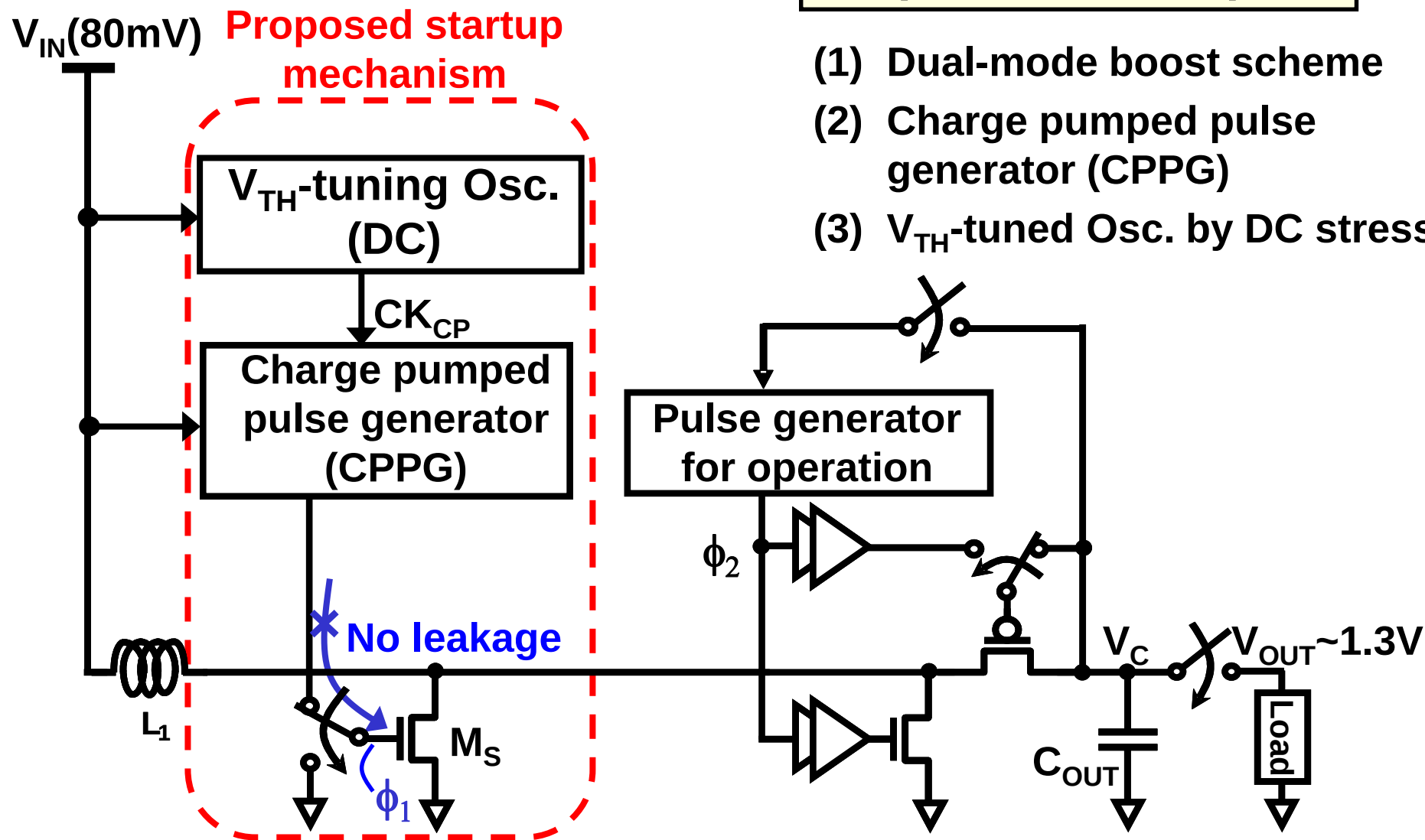


**Target startup voltage of DC/DC converter is 100mV.**

# Proposed Dual-Mode Boost

## Proposed Techniques

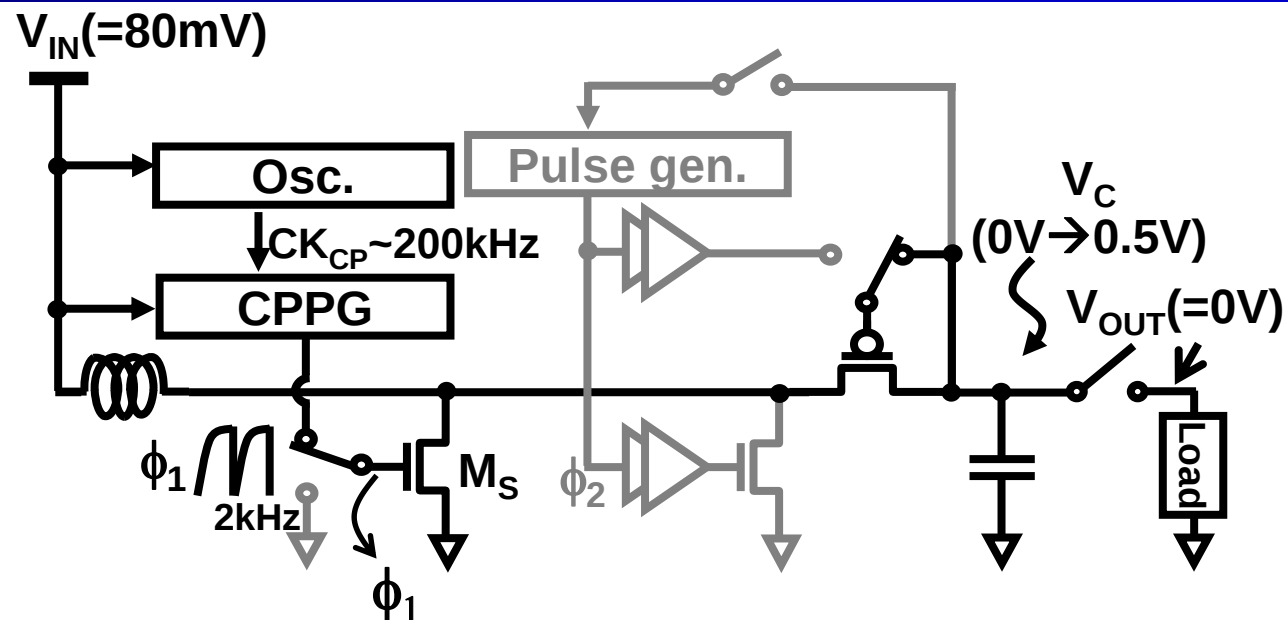
- (1) Dual-mode boost scheme
- (2) Charge pumped pulse generator (CPPG)
- (3)  $V_{TH}$ -tuned Osc. by DC stress



# Dual Modes Operation

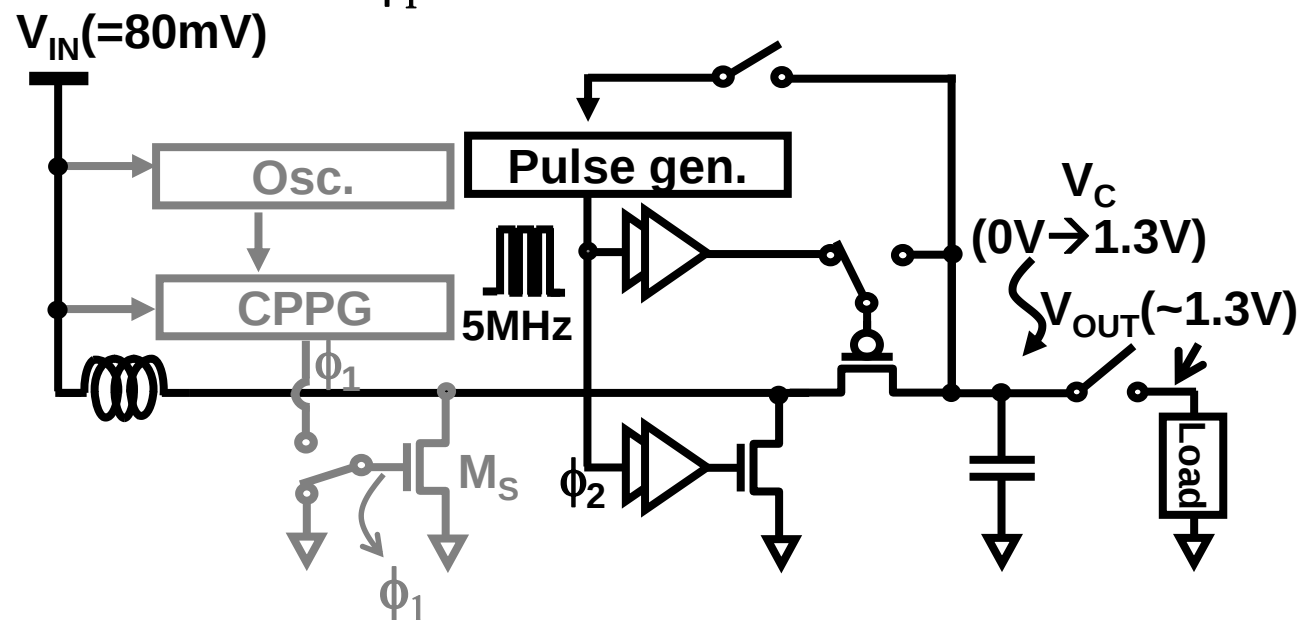
## Startup mode

The system is kick-started by CPPG.

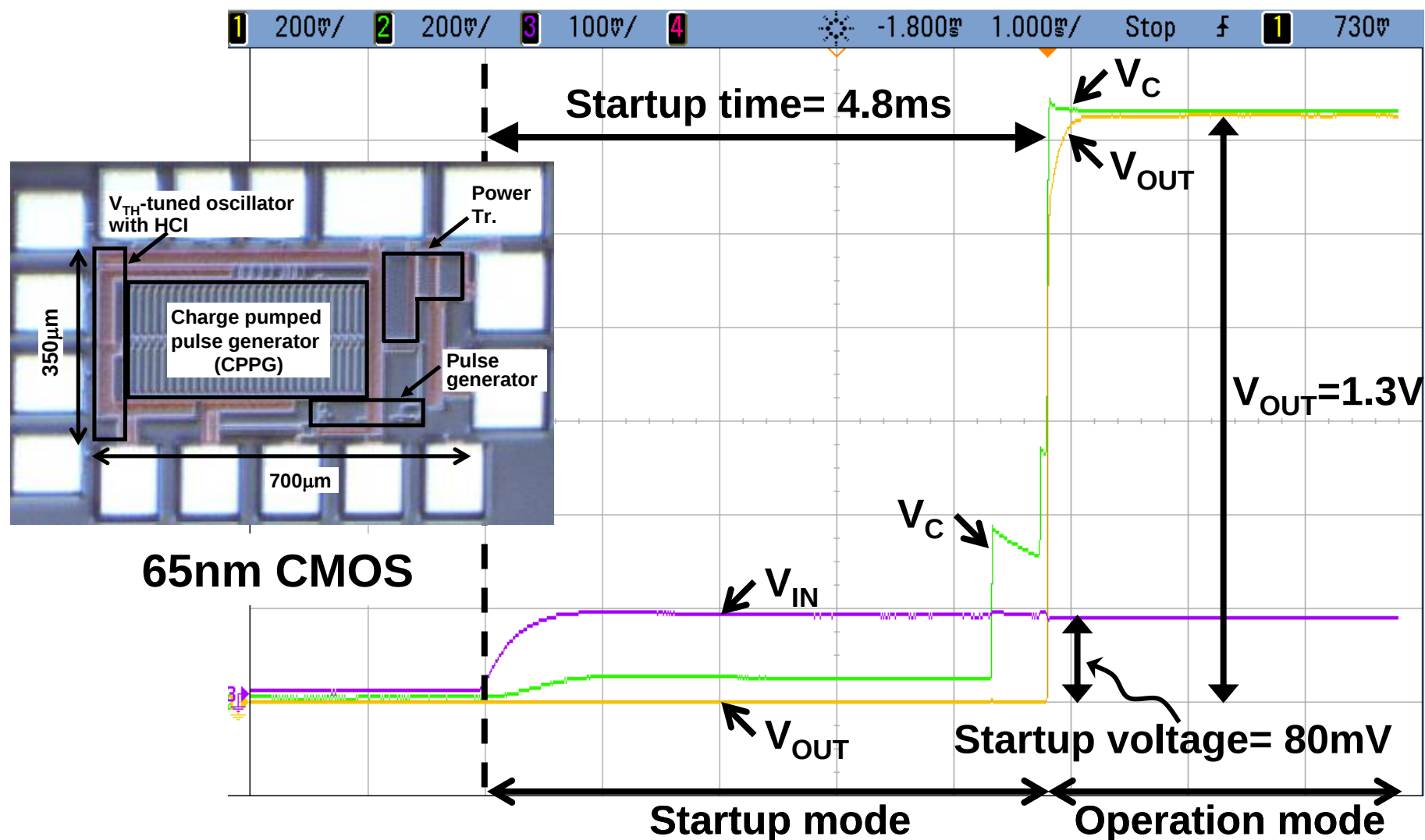


## Operation mode

The power transistors are driven by output voltage for high efficiency.



# Measured Boost Waveforms

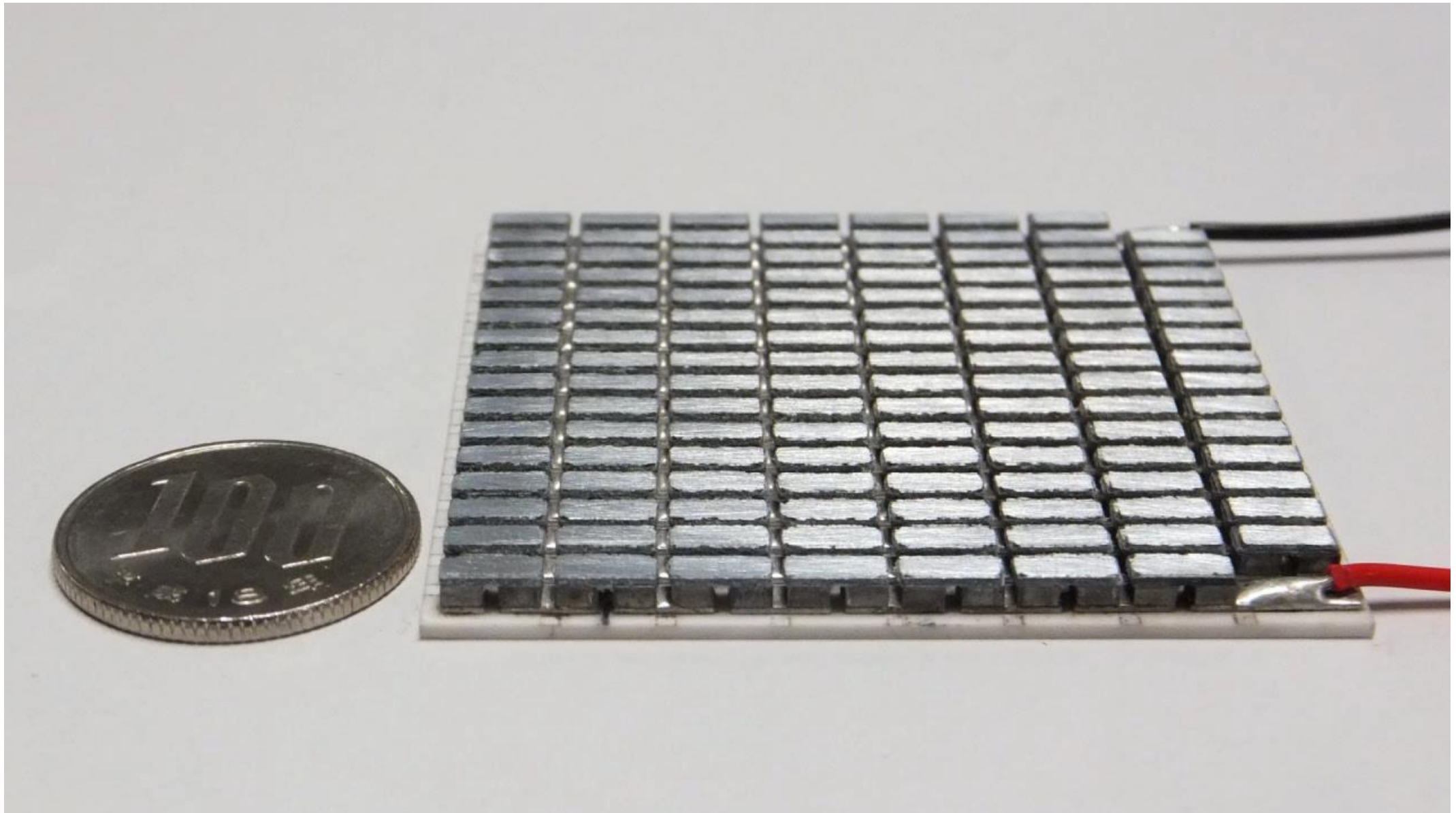


The step-up converter successfully startups from **80-mV**  $V_{IN}$  with 4.8ms startup time.

# Comparison of Startup Converter

| Ref       | Startup                      |                     |                     | Peak Efficiency               | Program time for Osc. | CMOS process |
|-----------|------------------------------|---------------------|---------------------|-------------------------------|-----------------------|--------------|
|           | <i>Mechanism</i>             | <i>Min. Voltage</i> | <i>Startup time</i> |                               |                       |              |
| [3]       | Boost with mechanical switch | 35mV                | 18ms                | 58%@<br>$V_{IN}=50\text{mV}$  | –                     | 350nm        |
| [4]       | External Voltage             | 650mV               | N/A                 | 75%@<br>$V_{IN}=100\text{mV}$ | –                     | 130nm        |
| [5]       | Charge pump                  | 95mV                | 262ms               | 72%@<br>$V_{IN}=100\text{mV}$ | 60min                 | 65nm         |
| This work | Boost with CPPG              | 80mV                | 4.8ms               | 60%@<br>$V_{IN}=80\text{mV}$  | 3min                  | 65nm         |

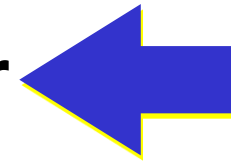
# Energy Harvesting from Thermoelectric Generator



# Outline

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- ◆ Energy-efficiency in IoT systems
- ◆ 0.45-V input buck converter
- ◆ Wide  $I_{OUT}$  buck converter
- ◆ 80-mV input boost converter
- ◆ **Switched capacitor DC-DC converter**
  - **Integration of MLCCs on die**
- ◆ Summary



# IVRs for Energy Efficient CPUs

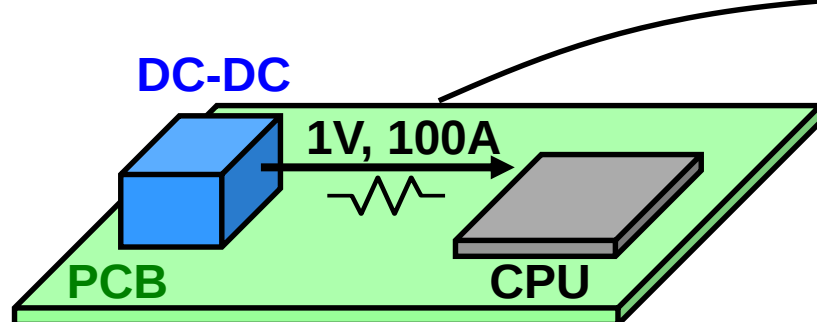
## Integrated Voltage Regulator (IVR)

### Problems in CPU

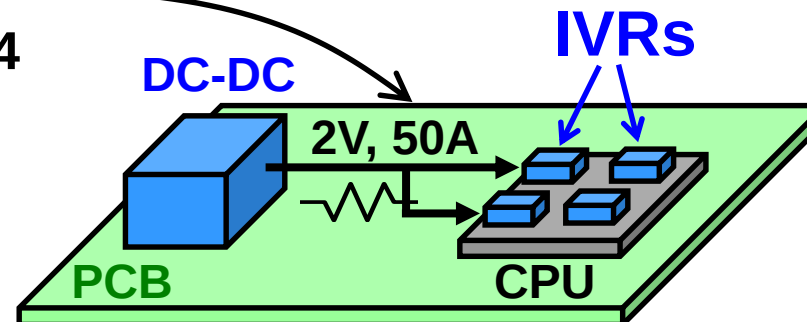
- (1) Increase of power
- (2) Reduced  $V_{DD}$   
→ Circuits are sensitive to  $V_{DD}$  noise.
- (3) Large  $I_{DD}$   
→  $R I^2$  loss on PCB increases.

### Solution by IVR

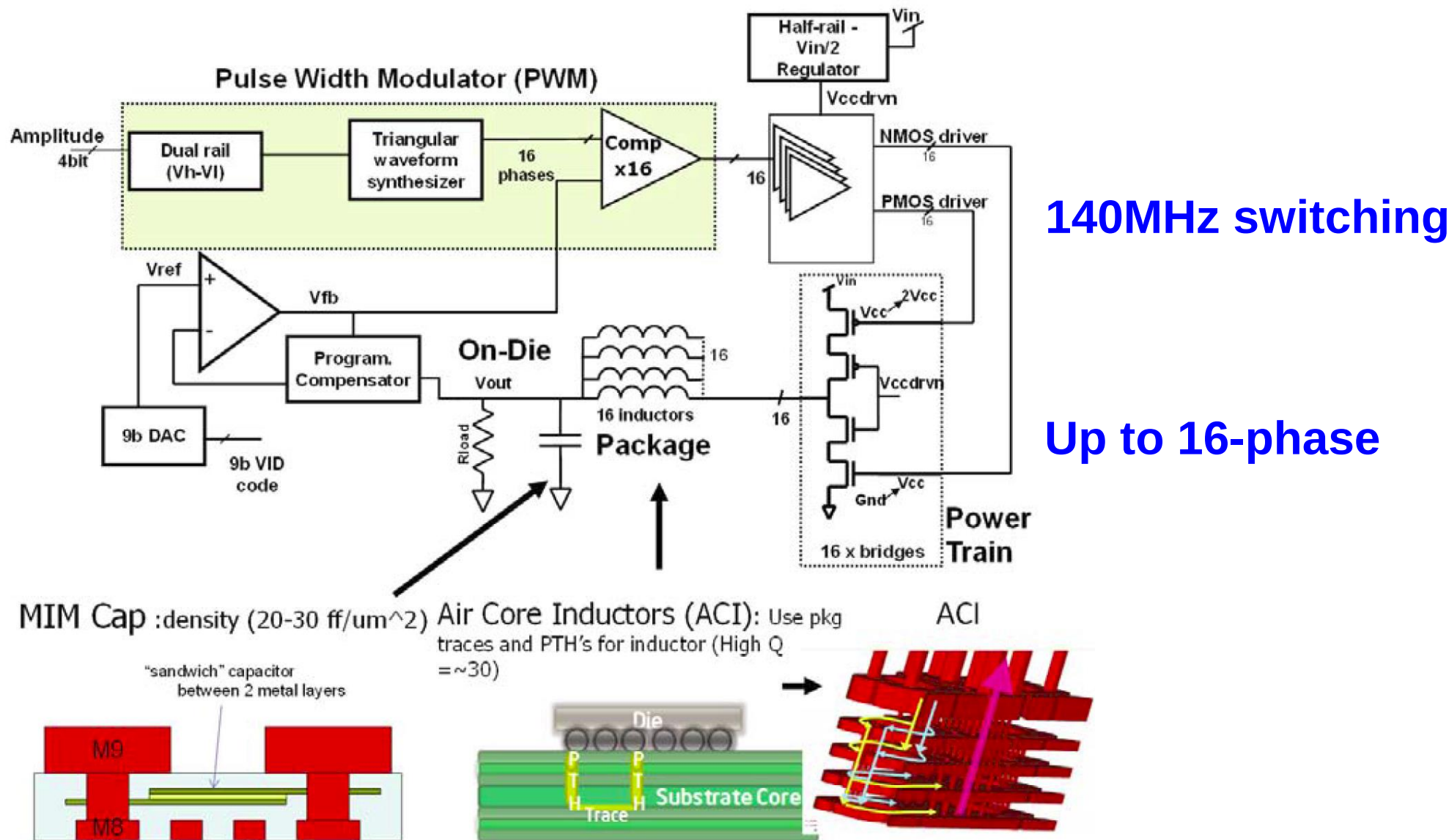
- (1) Per-core dynamic voltage scaling  
→ Low power
- (2) Reduced  $V_{DD}$  noise
- (3) Reduced  $I_{DD}$  on PCB  
→ Reduced  $R I^2$  loss



Loss: x1/4



# Integrated Buck Converter (Haswell)

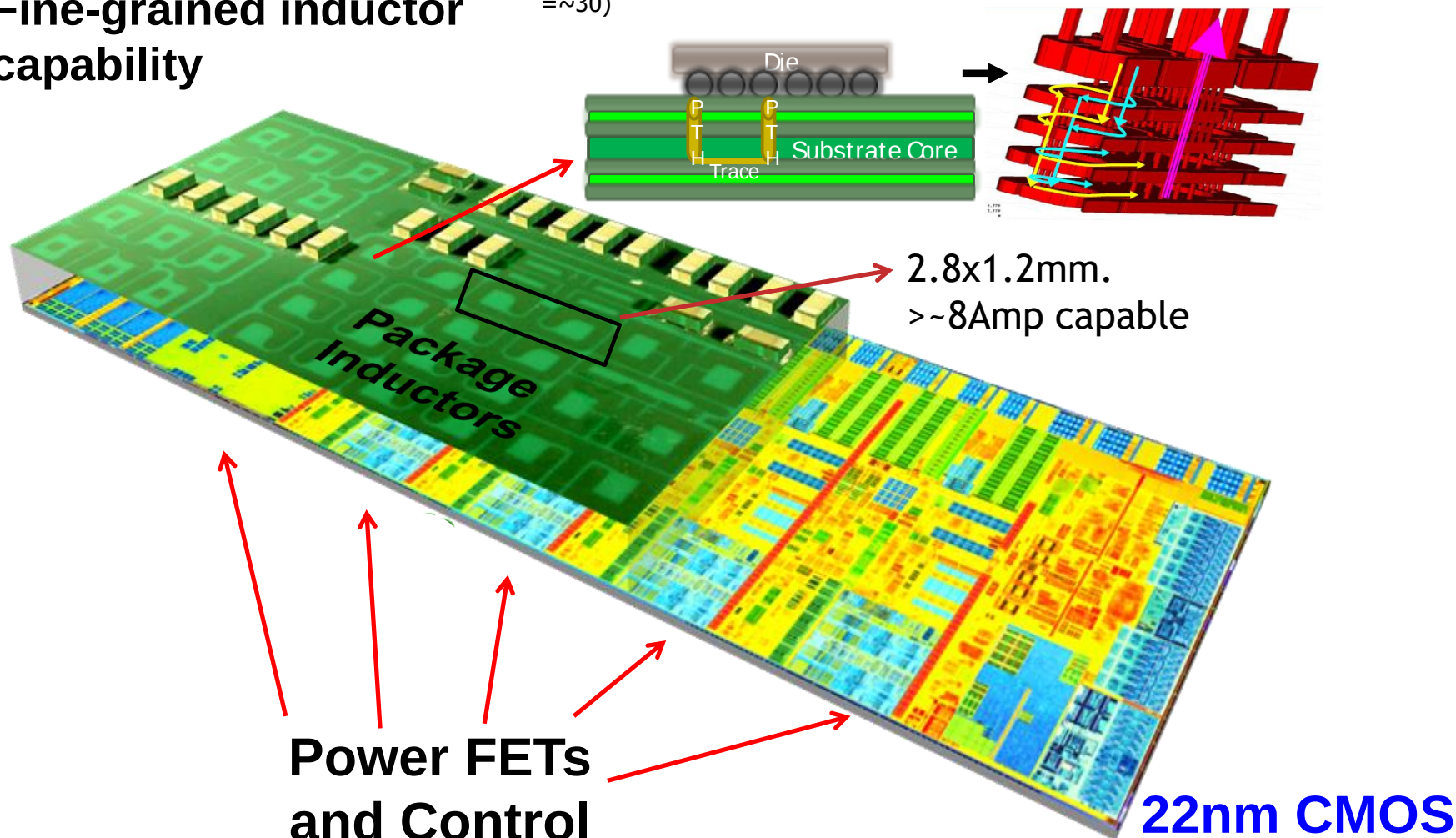


# Inductors on PCB and On-die Capacitors

**VR Cutaway View:  
Fine-grained inductor  
capability**

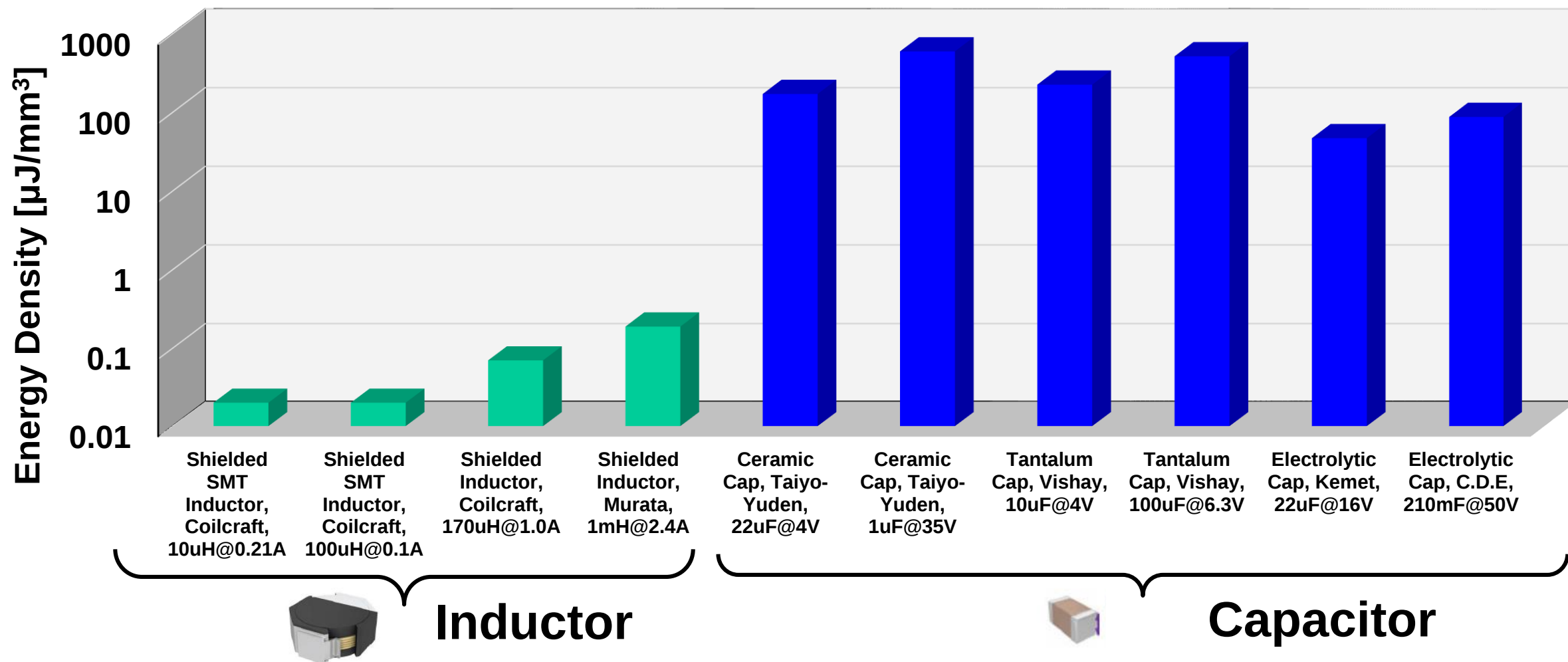
**Air Core Inductors (ACI):** Use pkg  
traces and PTH's for inductor (High Q  
 $\approx 30$ )

ACI



J. Douglas, "Fine-Grained Power Management Using Integrated DC-DC Converters," Short Course in IEEE Symposium on VLSI Circuits, 2014. (Intel)

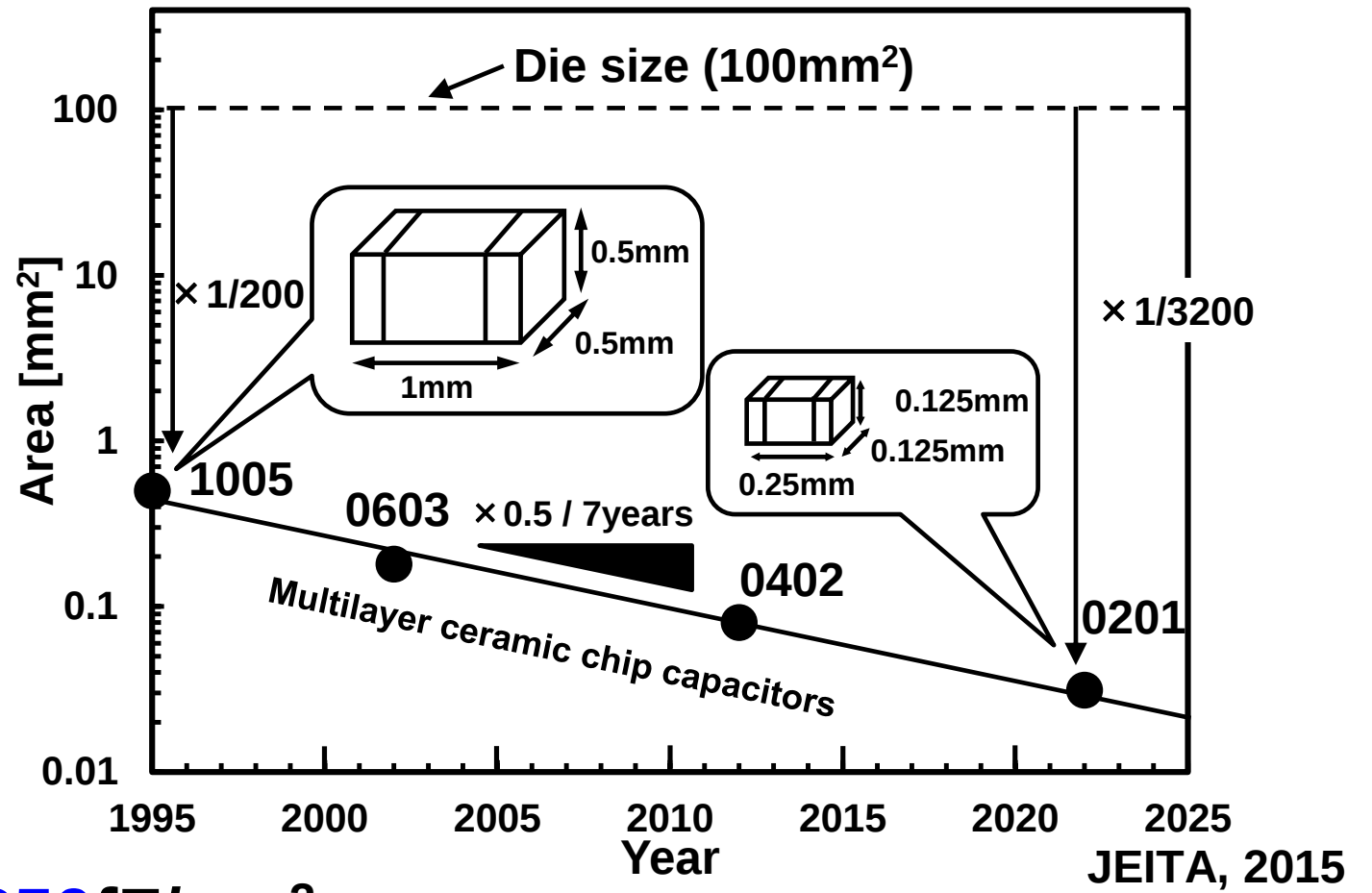
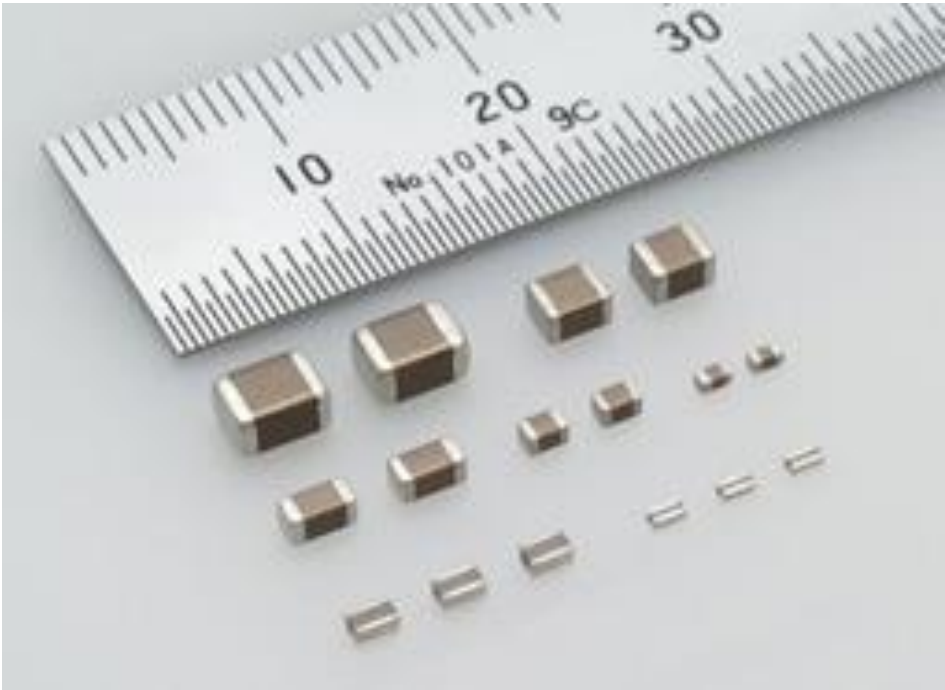
# Inductors vs. Capacitors



**High energy density of capacitors than inductors.**

# Scaling of MLCCs

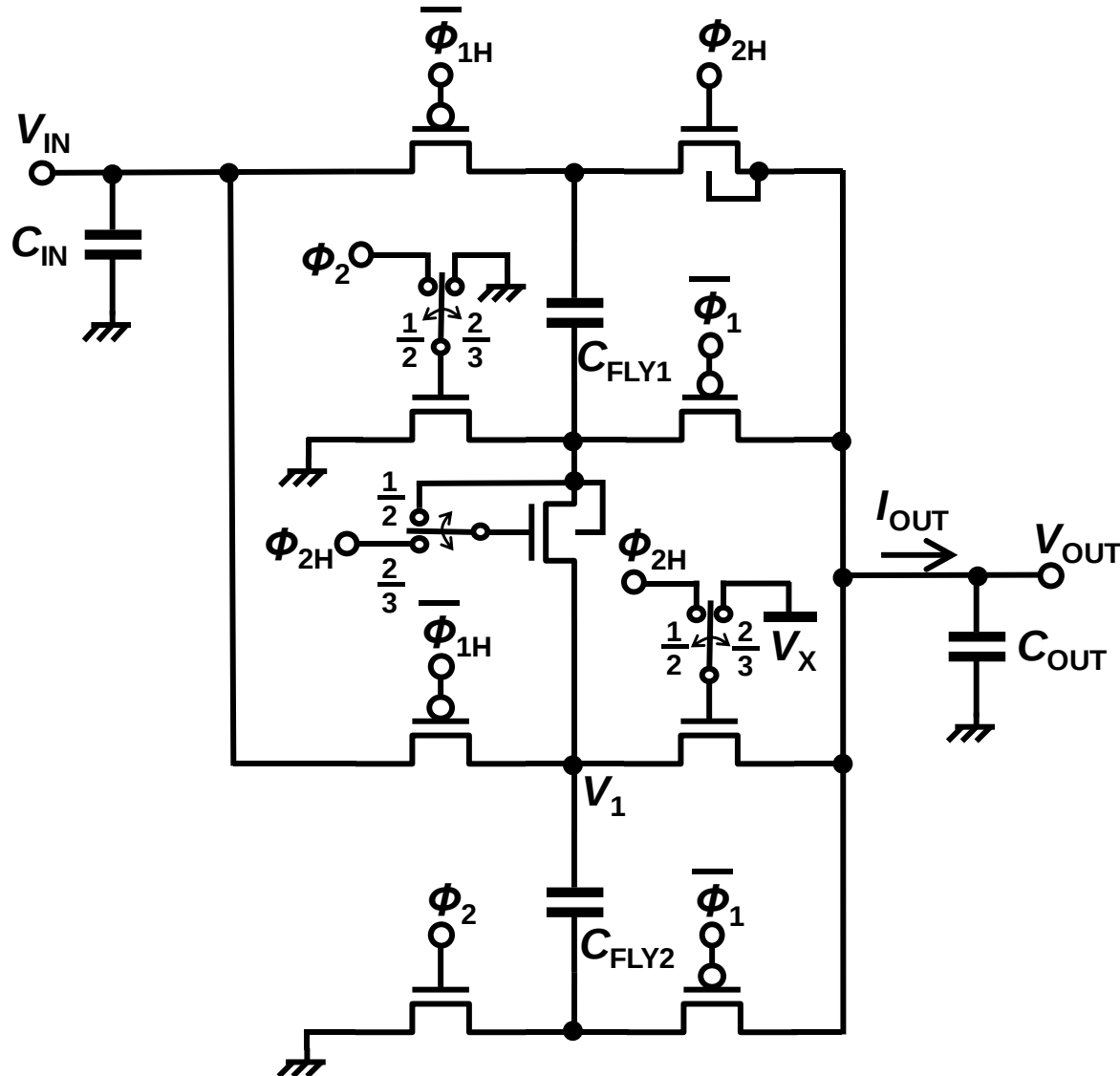
## Multi-Layered Ceramic Capacitor (MLCC)



0402 MLCC = 100nF  $\rightarrow$  1250fF/ $\mu\text{m}^2$

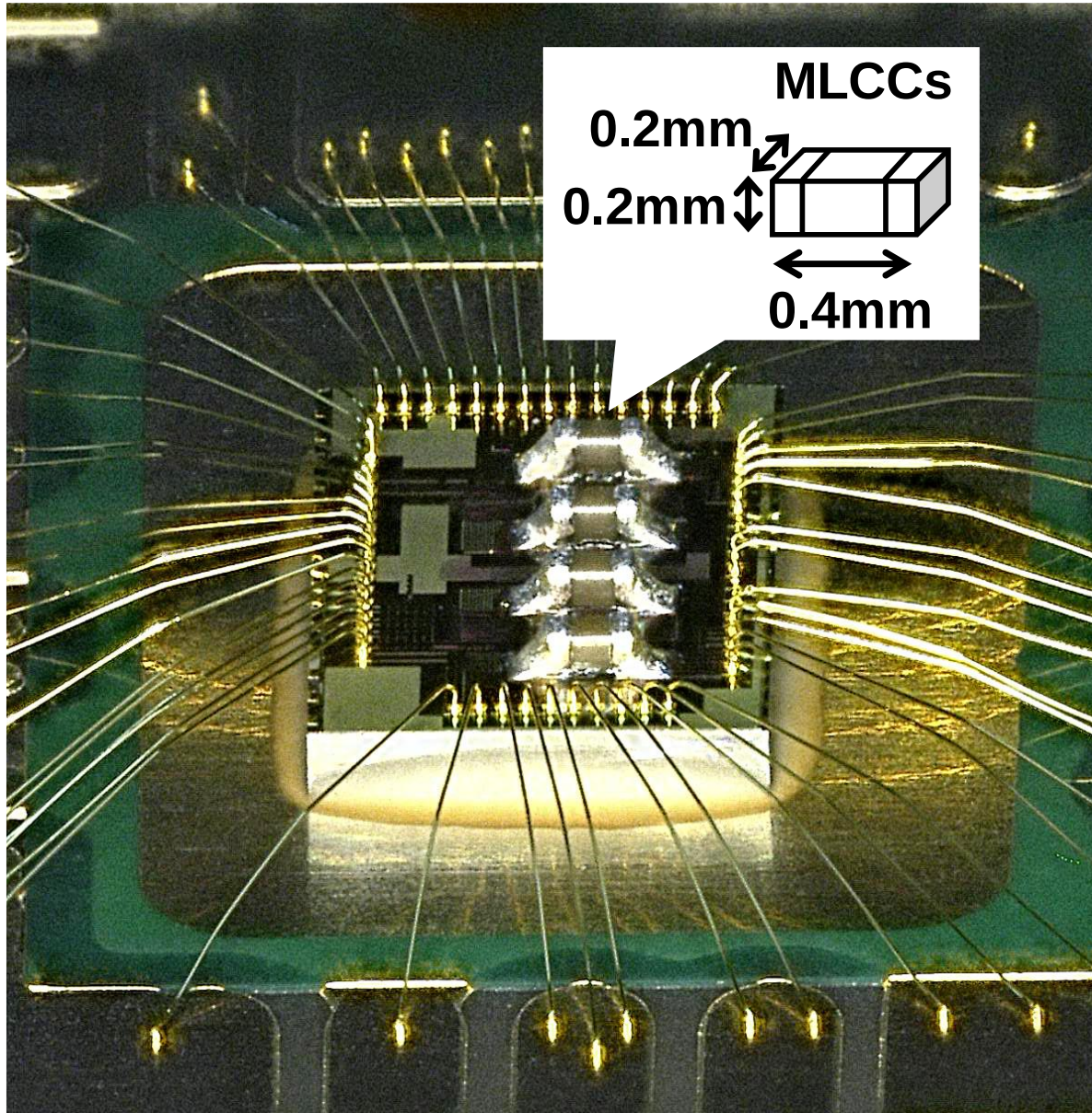
(e.g.) MIM 1-10fF/ $\mu\text{m}^2$ , MOS 10-20fF/ $\mu\text{m}^2$ , Deep Trench 200fF/ $\mu\text{m}^2$

# Switched Capacitor (SC) DC-DC Converter



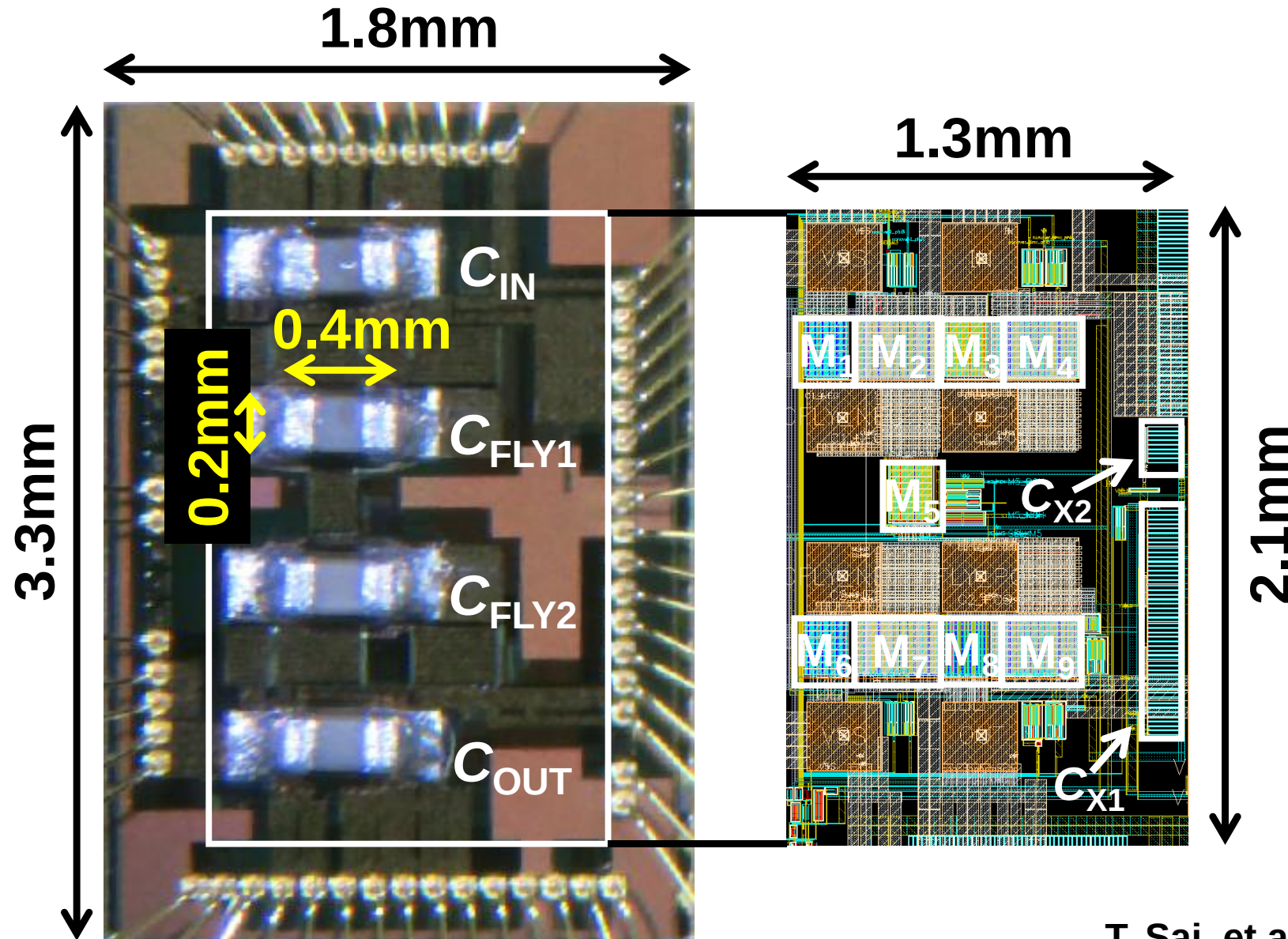
|                                                    |                     |
|----------------------------------------------------|---------------------|
| Technology                                         | 180nm bulk          |
| Conversion ratio                                   | 2/3, 1/2            |
| $V_{IN}$                                           | 2.7V                |
| $V_{OUT}$                                          | 1.1V – 1.75V        |
| $P_{OUT} @ \eta_{MAX}$                             | 171mW               |
| $\eta_{MAX}$                                       | 92.9%               |
| Die area                                           | 2.73mm <sup>2</sup> |
| Capacitors                                         | Off-chip MLCC x 4   |
| $C_{FLY}$                                          | 100nF x 2           |
| Power density (mW/mm <sup>2</sup> ) @ $\eta_{MAX}$ | 62                  |

# Fabricated SC DC-DC Converter in 180nm

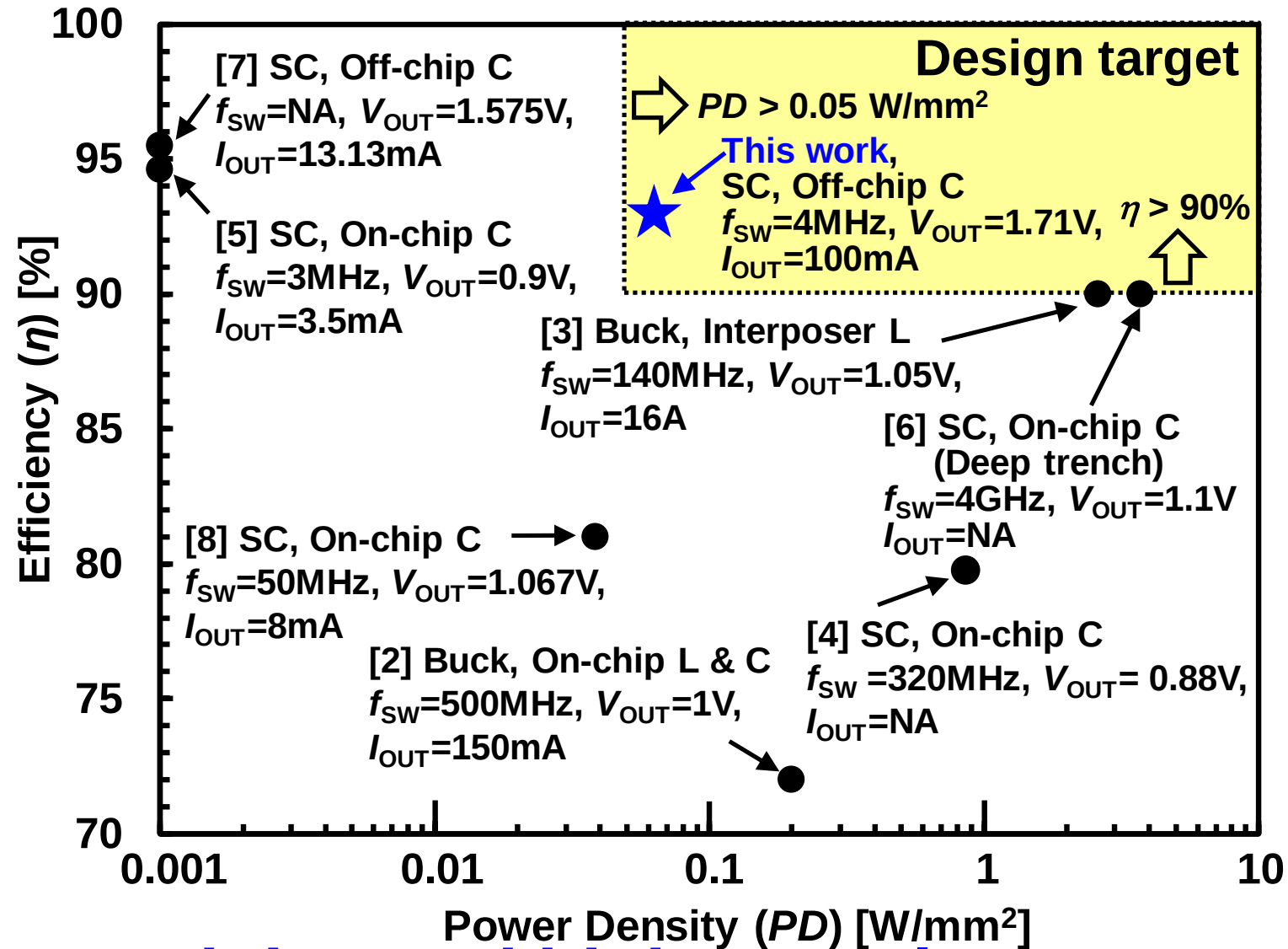


2.7-V input SC DC-DC converter  
mounting **four 100-nF 0402  
MLCCs** on 180-nm CMOS die

# Fabricated SC DC-DC Converter in 180nm



# Comparison in Step-down DC-DC Converters



**High  $\eta$  and high PD at low-cost**

# Summary

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- ◆ Integrated power management circuits for energy-efficient IoT systems
- ◆ **Gate boosting** for low  $V_{IN}$  DC-DC converters
- ◆ **Clocked** comparator for low  $I_{OUT}$  buck converter
- ◆ **Integration** of MLCCs on die for SC DC-DC converter